Digital Control in Microwave Receiver Front-End Components

by

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Abstract

In this thesis digital control techniques for two receiver front-end components i.e. the downconverter mixer and the modulator are presented. With decrease in size of CMOS-based geometries, decrease in performance and yield of analog components has become an issue. Using the digital components on a System-on-Chip to account for the shortcoming in analog circuitry and thereby developing 'self-calibrating' systems has become a reliable way to address this issue. In the telecommunications industry, this is directly correlated to lower post-fabrication testing times, quicker product development and lower overhead costs.

The first design presented is a 0.13 µm CMOS mixer with variable gain capability. A Digital Assist system was put in place to extend the 3-dB bandwidth of the system using a microcontroller. An interpolation routine was used to predict the bias voltages based on variations in frequency and desired input power. The digital-to-analog converter on the microcontroller was used to set the required bias voltages. The mixer’s bandwidth was extended from 12GHz to 15GHz using digital assist. The gain of the mixer
with the digital assist in place could be varied from 1.2-9.8dB.

The second design presented is a 5.4GHz multi-scheme modulator fabricated in 0.13 µm CMOS technology. The modulator is capable of carrying out quadrature amplitude modulation as well as phase-shift keying modulation. The modulator makes use of a novel OTA design to generate a set of orthogonal basis vectors which allows for facile mapping of the modulated data on the I-Q plane. The modulator carries out modulation in 4-PSK, 8-PSK, 4-QAM and 16-QAM modes with a maximum error vector magnitude of only 8.51%. A digital assist model to attain ubiquitous operation inside a system is also presented for this modulator.
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<th>Meaning</th>
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<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>BiST</td>
<td>Built-in Self-Test</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DA</td>
<td>Digital Assist</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EVM</td>
<td>Error Vector Magnitude</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input-Referred Third-Order Intercept Point</td>
</tr>
<tr>
<td>LNA</td>
<td>Low-Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
</tr>
<tr>
<td>LUT</td>
<td>Look-Up Table</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>NF</td>
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OTA  Operational Transconductance Amplifier
P1dB  1dB Compression Point
PA  Power Amplifier
PVT  Process-Voltage-Temperature
PWM  Pulse Width Modulation
PSK  Phase-Shift Keying (Modulation)
QAM  Quadrature Amplitude Modulation
RF  Radio-Frequency
SoC  System-on-Chip
ROM  Read-Only Memory
Chapter 1

Introduction

1.1 Overview

Wireless Telecommunications has grown to become a dominating industry in the field of analog electronics particularly with the advances made in the last few generations of wireless systems. The evolving needs in the wireless industry has led to growing demands for more complex devices with seamless connectivity and multi-faceted performance. These needs have been met with the development of heterogeneous systems that combine digital, analog and mixed-signal circuits on the same substrate.

The development of such heterogeneous systems, however, has not been without its own share of challenges. A problem that is apparent with reduction in CMOS geometries is that analog circuits tend to become quite susceptible to small variations in the process, voltage and temperature (PVT)
while the device is functioning. Digital circuits, however, are much more resilient to these variations even at reduced scales. One of the ways to correct the issue of analog circuit sensitivity is to use the digital components to detect PVT variations and calibrate the analog parameters for these small variations.

Self-calibration techniques through digital means can be used not only to correct for errors propagating through the system [9] but also to regulate the nature of circuit performance through a user interface [8]. Still in its nascent stage, Digital Control techniques of RFICs is a novel approach to curb some of the foreseeable problems of reduced transistor size. Much of the work in this thesis is devoted to exploring RF architecture with parameters that can be varied and used in conjunction with digital assist.

![Figure 1.1: A block diagram of a heterodyne transmitter](image)

Figure 1.1 shows the components in a typical heterodyne transmitter. For
undisrupted transmission of the original signal, it is desirable for the individual components in the transmitter chain to process the signal with minimal deviation from the intended output. This can be ensured by placing a Digital Assisted calibration system in place to react to any real-time deviations in the input or the output for each RF component.

1.2 Contributions

The overall contribution of this thesis is to illustrate the versatility in range of operation that can be attained in RFIC by virtue of an auxiliary digitally assisted system. Depending on the type of RF circuit, digital assist can not only be used for self-correction of the circuit performance but also to control the mode of operation of the circuit. This implies that, for a given RF implementation, the same device could be personalized for use with a myriad of different analog devices, thereby giving the device a sense of ubiquity in its operation.

- The first contribution of this thesis is a variable-gain mixer with digital assist employed to extend its operational bandwidth. Digital Assist was implemented with a PIC18F87J11 microcontroller with corresponding matlab code for consolidating the data. The operating bandwidth of the mixer was extended from 12GHz to 15GHz which equates to a 25% increase in operational range. The gain of the mixer can be varied from 1.2dB to 9.8dB.
The second contribution of this thesis is a modulator with multiple modulation scheme capability. The modulator uses a unique orthogonal vector generation scheme which allows for a large degree of flexibility in its mode of operation. The modulator carries out 4-QAM, 16-QAM, 4-PSK and 8-PSK modulation with error vector magnitude values of only 2.33\%, 6.20\%, 3.69\% and 8.51\% respectively. The modulator consumes an input power of 22dBm for each modulation scheme.

1.3 Thesis Organization

This thesis is organized as follows:

Chapter 2 gives a general introduction to Digital Assist and Self-Calibration techniques. An overall model for approaching designing digital assisted systems is explored with further discussions into some specific requirements that need to be considered. This is followed up with a review of some relevant models that have used digital assist in the past to improve the performance of some existing RF architectures.

Chapter 3 presents a variable-gain mixer with an extended operating bandwidth. Digital Control is employed on the analog chip to achieve flat gain throughout the frequency range and to extend the mixer bandwidth. The calibration algorithm used to vary the DC biases on the chip is described in detail. The chapter is closed off by presenting the measured performance of the chip with the digital assist system in place.
Chapter 4 presents a multi-scheme analog modulator that allows for phase shift keying (PSK) as well as quadrature amplitude modulation (QAM). A model for incorporating the model with a digitally assisted system for varying the modulation schemes is described. Error propagation through the system is investigated through some simple mathematical modelling techniques. The results of the performance of the modulator are presented for both modulation techniques.

Chapter 5 presents a summary of the overall thesis by briefly reviewing the prior discussions in the thesis. Some final conclusions are drawn and approaches towards future work are suggested.
Chapter 2

Literature Review

2.1 Introduction

This chapter explores some of the foundational concepts which the work in the latter chapters is based on. As much of the work in this thesis deals with the concept of digital assist applied to RF systems, some of the design considerations for digital calibration in RF circuits are discussed. Particular attention is given to the requirements necessitated by a self-calibrating structure in an embedded system. Finally, a literature review of published works employing digital assist techniques is carried out, highlighting some of the conventional approaches to error correction in different RF-type architectures.
2.2 Digital Assist System Design

With the increased reduction in transistor size, precision and control over circuit performance has become an issue. The reduction in size makes RF circuits highly sensitive to variations in process, voltage and temperature (PVT) and a greater degree of control of the circuit performance is demanded. Unlike their analogue counterparts, digital circuits do not undergo performance degradation with decrease in size. Thus, using digital circuitry to diminish the deleterious effects of reduced component size on analogue circuits is a veritable approach to this problem.

![Figure 2.1: RF Device with Self-Calibration System](image)

Figure 2.1: RF Device with Self-Calibration System

Figure 2.1 shows a generalized approach for a digital assist system design. The input reference and system output are detected using sensors and
input into the digital assist system. The digital assist system then uses a predesigned calibration routine to determine the correction that needs to be made in the RF circuit. The information is then delivered back to the RF circuit in a continuous feedback loop until the optimal operating point is reached. It is important to note that all the analog information needs to be properly conveyed to the digital assist system before re-calibration and vice-versa. Some of the salient features involved in designing the system are now considered in further detail.

2.2.1 Sensing

The input and output signals for a given RF core operate at high frequencies and cannot be directly steered to the digital core. The main point of interest in designing an on-chip sensor lies in converting the information from the RF input and output to a digitally legible format. Depending on what property needs to be calibrated in the RF-core, a corresponding analog detector can be used to sense the required feature and the information can then be passed to the digital core through an Analog-to-Digital Converter (ADC). Some existing sensors for RF-signal features are amplitude [11, 12], power and frequency detectors. A common practice in this type of sensing is to translate the RF information to a DC value. Based on the type of feature that was sensed, the RF core can be controlled by the digital core to vary the gain, compression points, distortion, noise levels etc.
2.2.2 RF Core

The most important issue in the RF Core design is flexibility i.e. the design needs to have tunable elements, preferably through voltage or current variations. One way to approach this is through identifying the parts of the circuits that are most susceptible to PVT variations. Having the aforementioned flexibility in these areas of the circuit will allow the calibration routines enough elbow room to optimize the RF-core operating parameters. DC biasing is one of the more popular approaches as this can allow for variations in transconductance, effective load, offset voltage etc. [10, 25]. AC calibration can also be carried out by using varactors and tuning knobs [4].

2.2.3 Digital Core and Feedback

The exact design of the digital core will vary depending on the nature of calibration required and the design of the RF core. It is, however, possible to take a systems-level approach and analyse the requirements for feedback using general control theory principles.

Consider the RF core to be represented by a system F and the digital core to be represented by a system G. Since the feedback loop takes in analog information through the ADCs and produces analog information, we treat G as a time-continuous system. The sensors are assumed to only contribute time-delays to the reference signal $x(t)$ and the system output $y(t)$. $d(t)$ represents a time-varying ‘calibration signal’ that is sent from the system G.
The system output is given by:

\[ y(t) = f(t) \ast [x(t) + d(t)] \]  \hspace{1cm} (2.1)

The calibration signal is given by:

\[ d(t) = g(t) \ast [y(t - \Delta t_y) + x(t - \Delta t_x)] \]  \hspace{1cm} (2.2)

Substituting Equation 2.3 in Equation 2.1, we get:

\[ y(t) = f(t) \ast [x(t) + g(t) \ast [y(t - \Delta t_y) + x(t - \Delta t_x)]] \]  \hspace{1cm} (2.3)

Taking the continuous-time fourier transform on both sides (with \( s = j\omega \)),

Figure 2.2: System Level Model of Entire System
we get:

\[
Y(s) = F(s) \left[ X(s) + G(s) \cdot \left[ e^{-s\Delta t_y} \cdot Y(s) + e^{-s\Delta t_x} \cdot X(s) \right] \right] \\
= F(s)X(s) + F(s)G(s)X(s)e^{-s\Delta t_x} + F(s)G(s)Y(s)e^{-s\Delta t_y}
\]  (2.4)

Rearranging the variables, the system transfer function (TF) is given by:

\[
\frac{Y(s)}{X(s)} = \frac{F(s) + F(s)G(s)e^{-s\Delta t_x}}{1 - F(s)G(s)e^{-s\Delta t_y}} \\
= F(s) \left[ \frac{1 + G(s)e^{-s\Delta t_x}}{1 - F(s)G(s)e^{-s\Delta t_y}} \right] \\
= \frac{F(s)}{1 + F(s) \left[ \frac{-G(s)}{F(s)} \cdot \frac{1 + F(s)e^{-s(\Delta t_y - \Delta t_x)}}{e^{-s\Delta t_x}G(s)} \right]}
\]  (2.5)

![Figure 2.3: A general feedback loop system](image)

The transfer function of a generic feedback loop (where \( \alpha \) is the TF of the main circuit and \( \beta \) is the TF of the feedback loop) is given by:

\[
\alpha_f = \frac{\alpha}{1 + \alpha\beta}
\]  (2.6)
Comparing (2.5) to (2.6), we see that the feedback for the digital assist system is given by:

$$\beta(s) = -\frac{G(s)}{F(s)} \cdot \frac{1 + F(s)e^{-s(\Delta t_y - \Delta t_x)}}{e^{-s\Delta t_x} + G(s)}$$

(2.7)

The above equation has some noteworthy implications. Firstly the entire $\beta$-value is negative which denotes that the system will form a closed negative feedback loop. This is consistent with what we are trying to achieve as negative feedback loops are used for signal correction whereas positive feedback loops are generally used to generate oscillation. Secondly, the feedback is dependent on the delay time in sensing, so this needs to be taken into consideration when designing the feedback circuit. For instance, a bistable multivibrator might be used to hold the values, so that both delay times are matched. Thirdly, the feedback has a frequency dependence which is expected since we defined $G$ and $F$ to be time-dependant systems. Finally, the feedback to the RF circuit (system $F$) is dependent on the transfer function of $F$ itself $i.e.$ the nature of feedback system (and thus the calibration algorithm) will depend on the nature of RF blocks in place.

2.2.4 Calibration Routines

The work of the calibration routine, much like that of the overall system, lies in testing, comparing, computing and correcting for optimization of the main circuit. Some of the things to be taken into consideration while devis-
ing the calibration algorithm are complexity, efficiency and execution time. In a Built-in Self-Test (BiST) system, there is a scheduled detection process in place that tests the system output at intermittent intervals. It is the calibration routine’s role to respond to PVT variations in the system and correct the RF parameters accordingly. Depending on the scope of calibration required, it is desirable to have several sub-calibration routines that are governed by one master calibration routine. This master calibration routine oversees the overall process flow and prioritizes the sub-routines based on the rate-determining routines. The role of a sub-routine generally involves carrying out a linear search of existing data on the RF core to find an optimal parameter value. Multilinear or non-linear search algorithms may also be implemented depending on the number of parameters being solved for and the interdependence between parameters.

2.3 Applications

Some existing circuits which have employed digital assist to improve their respective performances are now considered. The following circuits, in order, use digital assist to improve:

- input match in an LNA
- third order linearity in a power amplifier
- phase angle in a phase shifter
• second order linearity in a mixer

2.3.1 Digital Assist in Distortion Cancellation in a Power Amplifier

Power Amplifier (PA) design often calls for a tradeoff between power efficiency and linearity. The linearity of a PA is essentially a measure of the range that a PA can operate under without altering the contents of the signal that it is processing. Linearity enhancement through derivative superposition is a unique and efficient approach to addressing this issue. In this section, a PA with an auxiliary derivative superposition circuit is presented; the design uses digital assist to refine the performance of the derivative superposition circuit[25]. The operating range of the PA is 1-6GHz.

Distortion in RF circuits often arises from unwanted harmonics at frequencies that lie very close to the frequency of the carrier signal. Figure 2.6 shows the third-order harmonic gain \((g_{m3})\) by a transistor as a function of the transistor’s gate-to-source voltage. This general sinusoidal shape is a consistent characteristic over different transistor sizes and geometries. Distortion cancellation through derivative superposition exploits this transistor behaviour by biasing an auxiliary transistor in parallel with an amplifying transistor to cancel the third-order harmonics generated by the latter transistor.

The shape of this third-order harmonic curve is, however, incredibly sensi-
Figure 2.4: \(gm_3\) variation a transistor as a function of gate voltage (taken from [25] with permission © 2013 IEEE)

tive to the frequency and power-level of the input RF signal. Slight variations in the input signal’s frequency and power cause the optimum bias-points for cancellation to shift causing the linearity of the entire PA to decrease drastically. This design mitigates these effects by implementing a digital assist system in a feedback loop to correct the bias voltages of the PA for the changes in PVT conditions.

Figure 2.5 shows the schematic of the PA with the distortion cancellation circuit in place. Transistors \(M_1\) and \(M_2\) in the PA constitute a Darlington-style topology. \(M_3\) is used to regulate the drain-to-source voltage for \(M_1\). \(R_F\) and \(C_F\) constitute a shunt-shunt feedback network for the amplifier. Transis-
tors $M_{1A}$ and $M_{2A}$ are the auxiliary transistors that are placed in parallel with $M_1$ and $M_2$ respectively to carry out the distortion cancellation. Transistors

![Circuit Schematic of Power Amp](image)

$M_1$ and $M_2$, are biased in the saturation mode since they are the main ‘gain-producing’ pair and thus have a negative $gm_3$ value (Figure 2.4). $M_{1A}$ and $M_{2A}$ are accordingly biased in the triode/pinchoff region to have a positive $gm_3$ value to cancel out the intermodulation distortion (IMD) products produced by $M_1$ and $M_2$. The IMD tones are thus matched in magnitude and phase and cancelled through derivative superposition.

For a given input power and frequency level, each transistor has an optimal bias voltage that provides the maximum IMD cancellation. This peak
voltage has to be extremely precise and also varies considerably for different power and frequency values. A digital assist system is thus put in place to account for the bias voltages of $M_1$, $M_2$, $M_3$, $M_{1A}$ and $M_{2A}$ which are denoted by $V_{GA1}$, $V_{GA2}$, $V_{GAC}$, $V_{GA1A}$ and $V_{GA2A}$ in Figure 2.5, respectively.

The digital assist system used a calibration algorithm which used a lookup table (LUT) to find the optimal bias points for the PA. The lookup table was constructed using bias voltages for different power-levels and frequency values that would maximize the linearity i.e. the output third-order intercept ($OIP_3$) of the PA. An interpolation routine was used to derive the voltage values that were not available in the LUT. The corresponding bias voltages were then passed through an active RC low-pass filter (LPF) for digital-to-analog conversion and delivered to the PA.

Figure 2.6: Comparison of $OIP_3$ variations of PA at 3GHz before adding distortion cancellation (Baseline-PA), with the distortion cancellation circuit (DC-PA) and with the digital assist in place (DADC-PA) (taken from [25] with permission © 2013 IEEE)

Figure 2.6 shows the variation of the output third-order intercept of the
system at 3GHz over power levels from 21-25dBm. The digital assist is able to increase the PA’s OIP\textsubscript{3} from 46dBm to a constant level of 51dBm. A similar trend of overall OIP\textsubscript{3} improvement is observed over the 1-6GHz frequency range.

2.3.2 Digital Assist for controlling the input and output matching networks in an LNA

Low-Noise Amplifiers (LNAs) occupy the first element in an antenna’s receiver chain. Good input matching is desirable with the antenna to ensure isolation of the received signal from interfering signals. After amplification the signal usually is directed to a downconverting mixer, so good output match at the LNA is also needed for proper amplification and filtering at the frequency range of the carrier signal. A 2.4GHz LNA design [4] which uses digital assist to self-correct the input and output matching networks is discussed in this section.

The LNA design is based on a common-source LNA with inductive degeneration as shown in Figure 2.7. \(M_1\) is the main amplifying transistor and \(M_2\) is a simple switching transistor. At the resonant frequency \(\left(\omega_0 = \frac{1}{\sqrt{(L_g+L_s)C_{gs}}}}\right)\), the input impedance of the LNA is given by:

\[
Z_{in} = g_m \frac{L_s}{C_{gs}}
\]  \hspace{1cm} (2.8)

In Equation 2.8 \(C_{gs}\) represents the effective gate-to-source capacitance and \(g_m\)
Figure 2.7: Circuit schematic of LNA (dark) with digital control components (light) (taken from [4] with permission © 2011 IEEE)

represents the transconductance of $M_1$. $L_d$ similarly determines the peaking frequency at the output for maximum signal transfer at the output. The resonant frequency and input and output match parameters need to be consistently maintained for proper signal transfer. Changes in PVT conditions can easily lend themselves to variations in parasitics of the passive elements thereby altering the performance of the LNA.

The matching network is calibrated through digital assist by using varactor turning. Three varactors are placed in shunt with $C_{gs}$, $L_s$ and $L_d$. The capacitance of the varactor is controlled through a digitally programmable bias generator, which essentially functions as a DAC. The amplitude of the
RF signal is monitored at the input and the output of the LNA. Once a change is detected the calibration routine is initiated and each of the varactors are tuned for maximum RF amplitude. The steps are in the calibration routine (Figure 2.8) are as follows:

1. A constant feedback loop is initiated where the change in RF-amplitude is monitored

2. $C_d$ is varied for an optimal value which gives the highest RF amplitude

3. $C_g$ is varied for an optimal value

4. $C_s$ is varied for an optimal value

5. the calibration routine ends and the feedback loop is discontinued. The system goes back to monitoring the RF-in and RF-out for changes.
The digital assist stores the three optimal bias values and continues operating the LNA at those parameters until it senses a significant drop in RF-amplitude.

2.3.3 Digital Assist for Phase Shift Correction

Adaptive antennas use constructive addition of the phase angles of its signals to nullify the effects of interfering signals. It is therefore desirable to have a good range of control over the phase shift angle of the signal that is being transmitted through an antenna. In this section, a phase shifter design [6] that lends itself to digital control is described.

![Block Diagram of digitally controlled analog phase shifter](taken from [6] with permission © 1998 IEEE)

Figure 2.9: Block Diagram of digitally controlled analog phase shifter (taken from [6] with permission © 1998 IEEE)

Figure 2.9 shows the block diagram of the phase shifter which is made
up of one 90° phase shifter, two variable gain amplifiers, a summer and two DACs. The signal control through the block diagram is as follows:

1. The incoming RF signal is split into two signals of equal amplitude
2. One of the two signals is offset by 90°
3. Both signals then pass through VGAs the gains of which are controlled digitally via two on-chip DACs
4. The two signals are then summed and the desired phase shifted signal is produced at the output

The phase shifted vector $R$ at the output can be represented as (considering the amplifications of the two VGAs to be represented by $A$ and $B$ respectively):

$$R = \sqrt{A^2 + B^2} \cdot \tan^{-1} \left( \frac{B}{A} \right)$$  \hspace{1cm} (2.9)

Since the phase of the output vector is given by $\tan^{-1} \left( \frac{B}{A} \right)$, proper digital control of the respective VGA gains allows for precise variations in the phase shift of the output signal. The on-chip 6-bit DAC allows for exactly this level of precision control. Figure 2.10 shows the 3-bit priority encoder and the 3-bit R-2R ladder which make up one of the DACs. The three most significant bits are encoded by the priority encoder and the three least significant bits are encoded by R-2R ladder. Each bit value has a voltage level higher than its next lowest bit value by $0.2V$. This makes the corresponding current values vary in accordance to the word received by the DAC. The currents
from both the encoder and the ladder are added and delivered to the VGA to control its gain.

Figure 2.11 shows the phase plot of the phase-shifter’s transmission gain with each bit value set to high for one of the DACs. The other DAC was delivered a constant word value of “001000” during this measurement. The digital assist of the system allows for accurate phase-shift adjustments of more than 60°. Furthermore, the phase-shifter maintains this window within a ±100MHz tolerance around its 1GHz operating frequency.
2.3.4 Digital Assist for 2nd-order IMD calibration in a mixer

High levels of intermodulation (IMD) at the front end of direct conversion receivers degrade the overall system’s signal-to-noise ratio (SNR) quite acutely. Proper monitoring and control of second-order IMD is thus desired in direct conversion mixers. A 2.1GHz mixer with an IM2 calibration circuit [5] is presented in this chapter.

Second-order IMD components can arise in mixers due to device mismatches, duty-cycle distortions or poor isolation between ports. The input current of a mixer is given by:

\[ i_{\text{in}}(t) = g_1 v_{\text{in}}(t) + g_2 v_{\text{in}}^2(t) + g_3 v_{\text{in}}^3(t) + \ldots \quad (2.10) \]

If a two-tone signal \((v_1 \cos(\omega_1 t) + v_2 \cos(\omega_2 t))\) is introduced at the input, the
second-order intermodulation product generated is given by: \( g_2 v_1 v_2 \cos((\omega_1 - \omega_2) t) \). This design incorporates the use of an IM2 generator which takes in the RF signal of the mixer and produces and output signal \( A \cos((\omega_1 - \omega_2) t) \). The IM2 generator is designed such that the magnitude of the signal can be easily controlled and set to:

\[
A = -g_2 v_1 v_2 \tag{2.11}
\]

The beats produced by the IM2 generator are at the same beat frequencies as those at the output of the mixer. Since the IM2 coefficients \( (g_2) \) are independent of beat frequency, the IM2 generator is effective at cancelling out the distortion at the output by taking in a simple two-tone input.

![Circuit Schematic for complete calibration system](image_url)
The overall system is based on an IMT-2100 mixer (as shown in Figure 2.12). The currents generated from the IM2 generator are added with the current output of the mixed signal and the effective second-order distortion of the mixer is cancelled. Figure 2.13 shows the schematic for the IM2 generator. The IM2 generator uses a squaring circuit to generate the requisite distortion signal. The RF signal is amplified and summed at the drains of $M_1$ and $M_2$. Transistors $M_3$ to $M_{11}$ duplicate and split the IM2 correction currents. The IMD signal then goes into a scaling unit for amplitude scaling for distortion cancellation.

Figure 2.14 shows the schematic of the RF amplifiers used for scaling. The amplifiers used are in a common-source type configuration. A biasing network controls the driving DC current for both amplifiers. This driving current is controlled by a variable resistor network in the biasing network.
This variable resistor is implemented by using the parallel resistor chain as shown in Figure 2.15. Switching transistors are placed in series with the resistors allowing the calibration algorithm to control the gain. One bit-value is also reserved to select between a high/gain or low-gain mode by doubling the effective resistance.

The calibration algorithm is developed based on the variation of the IM2 over PVT changes. A calibration code ‘x’ is sent to the variable resistor network to control the IM2 magnitude produced. Because the IM2 magnitude is controlled by the resistor branch, the IM2 of a signal produced by the IM2 generator varies not just over the signal frequency but also temperature. So the IM2 magnitude is measured for frequency and temperature variations to gather a database of different word-values for x. Figures 2.16 and 2.17 show the variation in IM2 generated by the circuit for cancellation for frequency and temperature variations respectively.
The IM2 generator is thus able to generate IM2 values to more than 20dB and this is more than enough to cancel out the mixer’s maximum IM2 components at 15dB. The calibration code values allow for variations from -30 to +85°C

2.4 Conclusion

This chapter introduced an array of approaches to solving some pertinent issues in microwave circuits through digital assist techniques. An overview of digital assist design methodology was provided with a systems view of approach. Specific instances of use of digital assist in correcting for linearity improvement, phase shift correction and input network were matching were

Figure 2.15: Circuit Schematic resistor branch for resistor calibration(taken from [5] with permission © 2006 IEEE)
explored for different topologies. The discussion touched upon some of the calibration algorithms, associated analog designs and DACs used in each design.
Chapter 3

Bandwidth Extension in Variable-Gain Mixer using Digital Assist

3.1 Introduction

3.1.1 Overview

One of the veritable issues with analog downconverter mixers has been that of maintaining a flat conversion gain over the operational frequency. In this chapter, the design and realization of a digital assisted mixer with variable conversion gain, is presented. In mixers, it is desirable to have a variable conversion gain as well as a maximally flat gain over a large frequency range.
In trying to achieve this, often a tradeoff is made between the conversion gain and the 3dB bandwidth [21, 22]. A mixer with high conversion gain variability and very wideband operating range was designed by Jiangtao Xu, a former lab member; these results have been detailed in [2]. Although the mixer maintained high levels of conversion gain, the 1-dB cutoff of the conversion gain curves was reached at around 8GHz (Figure 3.2). In this chapter, a digital control technique is described that allows the existing mixer to attain a maximally flat conversion gain with a 1dB cutoff of 15GHz.

### 3.1.2 Mixer Description

As described in [2], the mixer design employs a very wideband Operational Transconductance Amplifier (OTA) in the transconductance stage with a double-balanced Gilbert-type mixing core. The gain of the mixer can be regulated by varying two input voltages: \( V_{ctl} \) and \( V_{switch} \). \( V_{switch} \) is a simple switching voltage that puts the mixer either in a high-gain (7-16 dB) or low-gain (1-9 dB) mode by switching the active load at the IF-output. \( V_{ctl} \) varies the gain of the mixer in gradual increments by varying the OTA gain at the transconductance stage.

Within its full functioning range, the gain of the mixer varies from 1-16 dB with a 3dB bandwidth of 12 GHz. The 3dB bandwidth is a measure of tolerance of how flat the gain of the mixer is. For a fixed control voltage \( (V_{ctl}) \) the mixer retains its flatness (variations of \( \pm 0.5 \) dB) out to 8 GHz and then gradually drops off by almost 4 dB within the 8-15 GHz range. The
contribution of this thesis is to significantly increase the bandwidth of this design by attaining a flat gain for the mixer at variable levels of conversion gain through digital control of the two control voltages $V_{\text{switch}}$ and $V_{\text{ctl}}$. 

Figure 3.1: Circuit Schematic of the variable conversion gain mixer (taken from [2] with permission © 2011 IEEE)
Figure 3.2: The Gain Response of the Mixer showing the effect of the switching ($V_{\text{switch}}$) and control voltages ($V_{\text{ctl}}$)

3.1.3 Approach

The key to achieving a maximally flat gain is to discretize the behaviour of the conversion gain of the mixer at different control voltages. Once the characteristic behaviour of the mixers gain is related to the two control voltages, digital control is employed to output the respective control voltages for a desired conversion gain over the 1-15 GHz range.
3.1.4 Chapter Layout

In this chapter, the main concepts of digital assist as well as the specific implementation for this project are described. The algorithm used, in particular, is covered in extensive detail. The measurement procedure, results and improvement achieved in the design by using this approach for bandwidth extension are reported.

3.2 Digital Control

3.2.1 Concept

Digital assist has been used in previous analog designs to improve linearity in amplifiers [25] and to improve the accuracy of phase shifters [6]. In this design, the high variability of the mixer gain is exploited in order to attain a maximally flat conversion gain over a large frequency spectrum. The employed system for digital control takes the desired conversion gain and frequency as inputs and outputs two control voltage values \((V_{\text{switch}}, V_{\text{ctl}})\) which are then delivered to the mixer. A microcontroller with PWM outputs was used for the digital assist implementation. The hardware and digital-to-analog conversion involved is discussed in further detail in Section 3.2.3.

Developing a digital control algorithm with the desired efficacy demands a proper understanding of the behaviour of the conversion gain of the mixer as a function of input frequency and control voltage. The switching voltage
Figure 3.3: Logic Flow Diagram for Digital Control System

\( V_{\text{switch}} \) takes a logic-level high or low and makes the mixer operate in either the high or low gain modes, respectively. It is important to note in Figure 3.2 that there is an overlapping gain-region of 7-10 dB in the two modes of operation. This is an important consideration for the digital control algorithm and is discussed later in this section. The operational range of the mixer also limits the range in which flat conversion gain can be attained. The minimum conversion gain for the maximum control voltage and the maximum conversion gain for the minimum control voltages are thus chosen to define a working window for the digital control algorithm. This working window or region of interest is shown in Figure 3.4 in the shaded area.

The first step in the digital control algorithm is choosing the mode of operation \textit{i.e.} if the mixer will be operating in the high-gain or low-gain mode. The mode of operation depends completely on the value of flat conversion gain desired. Low gain mode is picked for gain values between 1-5.9dB and high-gain mode is picked for values higher than 6dB. Once the operating mode for the mixer is picked, this value is stored as an the output voltage

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Figure 3.4: The gain region within which digital assist can theoretically flatten the gain for the mixer ($V_{\text{switch}}$). Linear interpolation is then carried out to find the exact value of the control voltage ($V_{\text{ctl}}$) for the desired gain at that frequency value.

### 3.2.2 Bilinear Interpolation

The linear interpolation part of the digital control algorithm aims to accurately predict the control voltage for a given point in frequency for a desired gain level. The control voltage values vary depending on the frequency and
desired conversion gain. The control voltage is, in a sense, a function of the frequency and desired gain. A bilinear interpolation method is thus used to estimate the value of \( V_{ctl} \) as it varies over gain and frequency. To be clear, the term ‘bilinear interpolation’ is, in a sense, a misnomer as the interpolation routine is not linear; rather, the final value is calculated as a product of two linear functions.

For the interpolation process to have a database to work with, measurements of the variance of conversion gain at different frequencies for different control voltage values were made with no digital assist added to the system. A lookup table (LUT) was then constructed and programmed into the microcontroller’s Read-Only Memory (ROM). Once the algorithm estimated the requisite \( V_{ctl} \), the value was output in the form of a PWM wave.

Some of the key moves in the bilinear interpolation algorithm are as follows:

1. The desired frequency \( (f_{in}) \) and conversion gain \( (G_{in}) \) are received as inputs

Figure 3.5: Logic Flow of Digital Control Algorithm
2. The two closest frequency values to $f_{in}$ stored in the ROM are computed $(f_1, f_2)$

3. The two closest gain values to $G_{in}$ stored in the ROM are computed $(G_1, G_2)$

4. The corresponding stored voltage values for the resultant four co-ordinates are recorded as $V_{11}$, $V_{12}$, $V_{21}$ and $V_{22}$ respectively.

5. The relative distance of $f_{in}$ from $f_1$ and $f_2$ is used to interpolate the relative voltage ($V_{1}'$) on the $G_1$ row of values
6. The last step is repeated to find the $V'_2$ value on the $G_2$ row.

7. The relative distance of $G_{in}$ from $G_1$ and $G_2$ is then used to interpolate the required $V_{ctl}$ value.

The relative distance referred to in steps 5-7 in the aforementioned list is where the linear interpolation actually takes place. It is essentially a fractional translation of the offset of the frequency and gain values to voltage values.

The $V'_1$ value in step 5 is given by (setting $\Delta V = V_{21} - V_{11}$ and $\Delta f = f_2 - f_1$):

$$V'_1 = V_{11} + \left( \frac{f_{in} - f_1}{\Delta f} \right) \Delta V$$

$$= V_{11} + \left[ \left( \frac{f_{in} - f_1}{\Delta f} \right) V_{21} - \left( \frac{f_{in} - f_1}{\Delta f} \right) V_{11} \right]$$

$$= \left[ 1 - \left( \frac{f_{in} - f_1}{\Delta f} \right) \right] V_{11} + \left( \frac{f_{in} - f_1}{\Delta f} \right) V_{21}$$

$$= \left( \frac{f_2 - f_{in}}{\Delta f} \right) V_{11} + \left( \frac{f_{in} - f_1}{\Delta f} \right) V_{21}$$

(3.1)

The $V'_2$ value is similarly derived to be:

$$V'_2 = \left( \frac{f_2 - f_{in}}{\Delta f} \right) V_{12} + \left( \frac{f_{in} - f_1}{\Delta f} \right) V_{22}$$

(3.2)

Using interpolated voltage values on the $G_1$ and $G_2$ rows ($V'_1, V'_2$) we can carry out the same fractional translation as in equation 3.1 to derive $V_{out}$.
which is the control voltage of interest for the mixer.

\[
V_{\text{out}} = \left( \frac{G_2 - G_{\text{in}}}{\Delta G} \right) V'_1 + \left( \frac{G_{\text{in}} - G_1}{\Delta G} \right) V'_2
\]

Based on the conversion gain response of the mixer in Figure 3.2, it is evident that, given a fixed \( V_{\text{ctl}} \), the conversion gain is much more constant in 1-8GHz region than in the 9-15GHz region. It is also important to note that the gain response is not well-behaved (i.e. not linear) in the higher gain regions of 10-16dB. These are two important facets that were taken into consideration while devising the digital assist algorithm.

The digital assist algorithm employs lookup tables (LUTs) to be able to interpolate between the frequency and gain values. While the linear interpolation used in the digital assist algorithm made fairly accurate predictions in the 1-8GHz region, its performance fell short in the 9-15GHz for the same set of data points in preliminary tests. While attempting to identify the issue, it was observed that part of the failure in interpolation happened because gain values stopped being flat and started degrading at different rates over frequency. This issue was resolved by measuring the gain values for the 9-15GHz region using a denser grid of data points for the lookup table. The algorithm was then modified such that the program interpolated the control voltage value from a second lookup table for the 9-15GHz region.
3.2.3 Hardware

The microcontroller used for this project was a PIC18F87J11 model developed by Microchip Technology. The controller has a reprogrammable ROM which allows for programming at the C-level using Microchip’s C-compiler, C18. The controller has five PWM output ports with a 10-bit resolution at each port. Two of these five ports were used to output the two voltages for controlling the chip ($V_{ctl}$) and ($V_{switch}$).

![Circuit schematic of the DAC used for the microcontroller output](image)

Figure 3.7: Circuit schematic of the DAC used for the microcontroller output

The PWM output from the microcontroller is a digital waveform and the sharp edges of the output pulses can produce spurious unwanted frequency components. To account for this, a pair of active low pass filters in combination with an inverting op-amp configuration (shown in 3.7) were used as
digital-to-analog converters (DACs) for the mixer input.

3.3 Results

3.3.1 Procedure

The original mixer chip was designed and fabricated in a 130nm CMOS process by Jiangtao Xu. Measurements for conversion gain, compression points and third-order intercepts were carried out using an Agilent E4446A Spectrum Analyzer and two Anritsu MG3694A Signal Generators. A Maxim 4444 buffer was used at the output stage for output matching as well as filtering out the downconverted frequency component. Three of the chip’s bias voltages were provided by external DC supplies while the remaining two were provided from the DAC outputs for the PIC18 microcontroller.

Measurements for the chip were carried out with and without the digital assist systems. The initial measurements of the mixer were carried out to assess the effectiveness of the digital assist as well as to create the lookup tables for the digital control algorithm. The frequency measurements were carried out every half of a Gigahertz for each gain curve. Since the gain values change based on the control voltage, the control voltage was varied until increments of 1dB would take place with the gain values over the bandwidth where the mixer response was the most flat (1-8 GHz region). Although this latter technique meant that not all gain values would be exactly discrete, the window between each gain curve was still wide enough for linear interpolation.
to be carried out properly. These measurements were carried out for both the high gain and low-gain modes for values applicable to the region of interest (1-10 dB). These values were then entered into the microcontroller ROM as a lookup table.

The system was then re-measured with the digital assist in place providing the control voltages for the desired gains and frequencies. The frequency and gain for each measured point was entered manually into the microcontroller’s input ports using switches on an external breadboard setup. The gain value
for a ‘desired gain’ was then measured with the microcontroller controlling the chip’s gain modes.

Both sets of measurements were carried out for an IF frequency of 100 MHz. The input RF and LO signal powers were maintained at -20dBm and 0dBm, respectively. The chip was biased with a 1.2V which is the standard for a 130nm CMOS technology. The power consumption of the chip varied between 1.8mW and 5.8mW, depending on the gain modes and control voltage value of $V_{CTL}$ set by the microcontroller.

### 3.3.2 Results

The results presented in this section outline the performance of the mixer with the digital assist in place. The graph in Figure 3.9 shows the effect of the output conversion gain of the mixer with the digital control dictating the two control voltages based on a predefined frequency. Predicted gain lines are presented within the 1.2-9.8dB window which was the chosen region of interest as depicted in Figure 3.4.

Within 1-12GHz range, the digital algorithm shows good efficacy in predicting the proper control voltages and the gain lines are flat with variations of less than or equal to 0.2dB. Within the 12-15GHz range, the flatness of the gain curves degrades with variations up to 0.6dB. Although this drop in performance is noticeable, it is not significant as the variance occurs within only a 0.6dB window. Although the graph in Figure 3.9 shows predicted gain lines at intervals of only 1dB, accurate predictions can be made up to
Figure 3.9: Measured conversion gain curves with digital control in place intervals of 0.1 dB.

The following figures of merit were taken at the edge of the frequency operating range of the mixer (15GHz). Since the gain decreases with an increase in frequency, these graphs are meant to exhibit how much the mixer’s performance is affected with the new extended bandwidth achieved through digital control.

Figure 3.10 shows the input-referred compression point (P1dB) as a func-
Figure 3.10: Variation of Input-referred P1dB as a function of conversion gain of the conversion gain from 1.5dB to 9.5dB. As the gain increases the input P1dB drops fairly consistently from -5.3dBm to -11.5dBm. The input compression point of a mixer gives us a measure of the linearity of the mixer’s behaviour. This 6.7dB drop adheres to contemporary mixer theory in that the mixer's dynamic range decreases and it becomes less linear as a higher conversion gain is demanded of it.

The variation of the input third-order intercept point (IIP₃) with the change in conversion gain is shown in Figure 3.11. The third-order inter-
Figure 3.11: Variation of Input-referred Third-Order Intercept as a function of conversion gain

ccept point is essentially a measure of a mixer’s sensitivity to signal distortion caused by undesired harmonics in the frequency spectrum. As the gain increases, the IIP3 undergoes a drop of about 6dB. Much like the linearity, the level of distortion at the mixer output also increases as the mixer operates in the higher gain regions.

Finally, the double sideband noise figure (NF) of the mixer is presented in Figure 3.12 at an input frequency of 15GHz. The double sideband noise figure
is around 10-11dB when the gain is set to 6dB or less but when the gain is set any higher, the NF increases sharply to about 14.5dB at a conversion gain of 9.5dB. As a higher gain is extracted out of the system, all the active circuit components are operating at higher levels of DC current, so this increase is not unprecedented.

A performance summary of the mixer with and without digital assist is presented in Table 3.1. The mixer's maximum gain, frequency operating range, input-compression point, input third order intercept point and noise
<table>
<thead>
<tr>
<th>Figure of Merit</th>
<th>Without Digital Assist</th>
<th>With Digital Assist</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency (GHz)</td>
<td>1-12</td>
<td>1-15</td>
</tr>
<tr>
<td>Gain Range (dB)</td>
<td>1.2-17</td>
<td>1.2-9.8</td>
</tr>
<tr>
<td>P1dB (dBm)</td>
<td>-3.7</td>
<td>-5.3</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>+8.6</td>
<td>+6.8</td>
</tr>
</tbody>
</table>

Table 3.1: Comparison of the mixer’s performance with and without digital assist figures are presented.

### 3.4 Conclusion

In this chapter, a digital assist system implemented on a variable-gain 12-GHz bandwidth mixer was presented. The goal of employing the digital assist was to extend the operational bandwidth upto 15 GHz by controlling the operating conditions of the mixer. The mixer was designed in a 130nm CMOS process by Jiangtao Xu and the digital assist was implemented using a PIC18 microcontroller and LPFs. Flat gain lines with variations of less than 0.6dB were acheived from the 1.2-9.8dB range. Although the digital assist meant a drop in the maximum gain of the mixer, the system does show the versatility of the mixer by extending its operating bandwidth.

This design could be improved in the future by implementing a frequency
detector as part of direct feedback loop between the chip and the microcontroller. This would represent a more wholistic system which would be closer to a practical implementation.
Chapter 4

Multi-Scheme Modulator with PSK and QAM Capability

4.1 Introduction

4.1.1 Overview

In the telecommunications industry, phase-shift keying (PSK) and quadrature amplitude modulation (QAM) are two common modulation formats for data transfer. Several different modulator circuits have been proposed for both formats but few modulators exist with the versatility of carrying out both modulation formats. In this chapter, an analog modulator design with dual PSK and QAM capability is presented. A 5.4GHz configurable 4-QAM and 16-QAM modulator was designed by Jiangtao Xu, a former lab member.
The results of this work are detailed in [1]. The modulator employs a novel vector-manipulation technique using variable-gain Operational Transconductance Amplifiers (OTAs). That same design is adapted for a PSK modulation scheme by exploiting the vector-manipulation technique. This results in a modulator which offers amplitude modulation up to 16-QAM and phase-shift keying modulation up to 8-PSK which can be externally controlled through the digital assist techniques discussed in previous chapters.

4.1.2 Modulator Architecture

The modulator shown in Figure 4.1 has a symmetrical structure and is composed of a pair of identical active baluns, variable-gain OTAs and switching networks. The modulator takes a differential input signal with a phase offset of 90°. The signal is then decomposed into four orthogonal basis vectors by the active baluns. Each of these signals are offset from each other by 90°. The magnitude of these vectors can be controlled by the $b_2$ and $b_3$ control voltages. These four orthogonal basis vectors are represented in Figure 4.1 by $I^+$, $I^-$, $Q^+$ and $Q^-$ respectively. The $b_0$ and $b_1$ control voltages allow the system to pick two of the four vectors (one on the $I$-plane and the other on the $Q$-plane) to pass through via the switching network. These two vectors are finally summed by a trans-impedance amplifier (TIA) to create the desired constellation point at the output. The range of variability over the $I$ and $Q$-plane vectors via the four control voltages ($b_0$, $b_1$, $b_2$, $b_3$) is what lends the modulator a high degree of flexibility in its modulation format of
Figure 4.1: Block Diagram of entire schematic of PSK modulator [REF]

operation.

4.1.3 Modulation-Format Control

Figure 4.2 shows a systems-view model for varying the modulation format of the chip. The different modulation formats are achieved by taking advantage of the modulator’s versatile vector generating architecture. A digital assist system that takes in the data to be transmitted and scales it accordingly for the modulator allows for a highly flexible modulation system. The analog data ($m_3m_2m_1m_0$ in Figure 4.2) needs to be converted to a proper digital format before the system can process it.

In the following pages, the methodology used to manipulate the generated vectors for 2-PSK, QPSK and 8-PSK modulation formats are described. The
effect of phase and amplitude mismatch on the output signal are covered in detail with corresponding mathematical analysis for each scenario. The chapter is closed off with the measurement procedure and the results of the m-PSK modulation scheme.

4.2 Vector Manipulation

Modulation, at its core, takes place by tracing out the data to be transmitted on the I-Q plane. This is done by generating four orthogonal vectors which are then combined accordingly to trace out the corresponding constellation. This design uses a variable-gain OTA to generate the I and Q vectors. An OTA is an amplifier which takes in a differential input voltage and produces an amplified output current. The transconductance of the amplifier ($g_m$)
Figure 4.3: Schematic of an Operational Transconductance Amplifier where $V_{gm}$ represents the control voltage.

determines the gain of the amplifier. The OTA used in this modulator has a variable $g_m$ value which can be controlled by a control voltage.

The data to be transmitted in the form of $b_3b_2b_1b_0$ is directed to the modulator as follows. The $b_0$ and $b_1$ voltages are used as binary switching voltages which pick the positive or negative vector on the I and Q-planes, respectively (Figure 4.2). The $b_2$ and $b_3$ voltage levels control the gain of the OTAs and thereby determine the length of the corresponding output vector on the I and Q-planes, respectively (Figure 4.2). This allows the system to trace out a constellation point anywhere within the range on the I-Q plane with the resultant output vector.

It is evident that the range of the OTA-gain variability for the basis vectors determine the highest value we can attain for an $m$-PSK modulation scheme. That is to say, the vectors produced at maximum gain need to be large enough to effectively map out the necessary constellations. To elaborate, consider the 8-PSK constellation shown in Figure 4.2. The constellation points at $22.5^\circ$ and $67.5^\circ$ are generated using a ‘small vector’ and a ‘large vector’ on the I and Q-planes: $I_{SMALL}$, $I_{LARGE}$, $Q_{SMALL}$ and $Q_{LARGE}$. A mathematical analysis is presented to calculate the ratio of the two vectors.
to determine the required gain range of the two OTAs.

If the required ratio between the large and small vectors is represented by $K$, the relationship between $Q_{\text{SMALL}}$ and $Q_{\text{LARGE}}$ is therefore derived to be:

$$Q_{\text{SMALL}} = \frac{Q_{\text{LARGE}}}{K}$$

Since the constellation set is symmetric, a similar relationship holds between $I_{\text{SMALL}}$ and $I_{\text{LARGE}}$:

$$I_{\text{SMALL}} = \frac{I_{\text{LARGE}}}{K}$$
Since the constellation point set in Figure 4.2 is an 8-PSK constellation:

\[
\angle CAB = \frac{\pi}{8}
\]

And,

\[
\angle DAB = \angle CAB + \frac{\pi}{4} = \frac{3\pi}{8}
\]

Therefore,

\[
\tan \angle CAB = \frac{BC}{AB} = \frac{Q_{\text{SMALL}}}{I_{\text{LARGE}}}
\]  \hspace{1cm} (4.1)
And,
\[ \tan \angle DAE = \frac{DE}{AE} = \frac{Q_{\text{LARGE}}}{I_{\text{SMALL}}} \]  
(4.2)

Dividing equation 4.2 by equation 4.1, we get:

\[
\frac{\tan \angle CAB}{\tan \angle CAB} = \frac{Q_{\text{SMALL}}}{I_{\text{LARGE}}} \times \frac{I_{\text{SMALL}}}{Q_{\text{LARGE}}} = \frac{Q_{\text{SMALL}}}{K \cdot I_{\text{SMALL}}} \times \frac{I_{\text{SMALL}}}{K \cdot Q_{\text{SMALL}}} = \frac{1}{K^2}
\]
(4.3)

Equation 4.4 is now re-arranged to calculate the value of \( K \):

\[
K = \sqrt{\frac{\tan \angle CAB}{\tan \angle CAB}} = \sqrt{\frac{\tan \frac{3\pi}{8}}{\tan \frac{\pi}{8}}} = 2.414
\]
(4.4)

The ratio between the \( I_1 \) and \( I_2 \) vectors needs to be 1:2.4 to achieve 8-PSK modulation. Using a similar approach, the ratios for 4-PSK (QPSK) and 16-PSK are found to be 1:1 and 1:5.03 for modulation schemes respectively.

Figure 4.6 shows the variance of the modulator’s gain as a function of the OTA’s control voltage (\( b_2 \) and \( b_3 \)). It is important to note the extent to which
the OTA gain can be manipulated. Varying the $b_2$ or $b_3$ voltage from ground to 1.2V correlates to a variance in gain of 4dB which is approximately a gain factor of 2.51. Given the range of the OTA gain, it is evident that PSK modulation can be achieved only up to 8-PSK for this chip.

![Figure 4.6: Variance of output power as a function of the OTA control voltage](image)

### 4.3 Error Propagation Analysis

High fidelity PSK modulation depends on accurate mapping of the data to the intended constellation points on the I-Q plane. Slight deviations in the system structure can, however, cause one or more of the vectors to plot out
a point that is offset from its intended co-ordinate. This offset is measured by the error vector magnitude (EVM) of the system. In this section, a basic two-part mathematical analysis is carried out to assess the contribution of this offset by the different system components. The first part considers how the EVM value of the system is swayed by offsets in amplitude and phase of the output. The second part investigates how errors in amplitude and phase contributed by some of the system components contribute to the output signal to deviate from the desired signal.

4.3.1 EVM development due to offsets at output

The EVM of a modulator is a numerical value that denotes the percentage offset of a received constellation point from the intended location. The EVM is defined as:

\[ EVM = \sqrt{\frac{P_{error}}{P_{ref}}} \]  

(4.5)

The power of the signal at the output is given by:

\[ P = \frac{V^2}{R} \]  

(4.6)

Combining these two relations, the EVM of the output constellation can be reduced to:

\[ \therefore EVM = \sqrt{\frac{\frac{V_{error}^2}{R}}{\frac{V_{ref}^2}{R}}} = \frac{|V_{error}|}{|V_{ref}|} \]  

(4.7)
EVM contribution due to Amplitude offset at output

First, consider a change in the offset of the amplitude of the output signal while the phase remains unchanged. In Figure 4.7 we define the received vector \( \alpha'_T \) superimposed on top of the desired constellation-vector \( \alpha_T \). Since we assume no phase mismatch, the geometrical interpolation to be taken into consideration is minimal. Invoking equation 4.7, we know:

\[
EVM = \frac{|V_{error}|}{|V_{ref}|}
\]

Based on our definitions in Figure 4.7, we can rewrite this as:
\[ EVM = \frac{|V_{error}|}{|V_{ref}|} = \frac{|V_{ref} - V_{received}|}{|V_{ref}|} = \frac{|\alpha_T - \alpha'_T|}{|\alpha_T|} = |1 - \frac{\alpha'_T}{\alpha_T}| \] 

(4.8)

Equation 4.7 implies that the EVM contributed to the system varies as a linear function of the amplitude offset of the received signal.

**EVM contribution due to Phase offset at output**

The effect of a phase offset at the output on the EVM value of the system is now taken into consideration. The amplitude of the received signal is assumed to be equal to that of the desired constellation as illustrated in Figure 4.8. The received vector \( V_{error} \) is represented by AB and the phase offset to the reference vector \( V_{ref} \), represented by AC, is given by \( \Delta \gamma \).

Since the amplitude of the received signal is assumed to stay constant, 
\[ AB = AC' = |V_{ref}| \]

\( V_{ERROR} \) is computed by investigating the triangle ABC:
$BC^2 = AC^2 + AB^2 - 2 \cdot AB \cdot AC \cos \Delta \gamma$

$|V_{error}^2| = |V_{ref}^2| + |V_{ref}^2| - 2 \cdot V_{ref} \cdot V_{ref} \cos \Delta \gamma$

$= 2 \cdot |V_{ref}^2| \cdot [1 - \cos \Delta \gamma]$

$= 4 \cdot |V_{ref}^2| \cdot \left[ \frac{1 - \cos \Delta \gamma}{2} \right]$

$= 4 \cdot |V_{ref}^2| \cdot \sin^2 \left( \frac{\Delta \gamma}{2} \right)$

(4.9)

Taking the square root on both sides,

$\frac{|V_{error}|}{|V_{ref}|} = 2 \sin \left( \frac{\Delta \gamma}{2} \right)$

(4.10)
Comparing Equations 4.10 and 4.7, it is derived:

$$EVM = 2|\sin \frac{\Delta \gamma}{2}|$$

(4.11)

Figure 4.9: The Error Vector Magnitude (EVM) as a function of the phase error $\Delta \gamma$

Figure 4.9 shows the variation of the EVM as $\Delta \gamma$ varies from $\pi$ to $-\pi$. 
4.4 Measurement Results

CPW probes were employed to carry out on-chip measurements. Two Filtronic 6705K tunable phase-shifters were used at the input to attain the 90° phase difference for the RF signal. It is noteworthy that although the phase difference was achieved through setting the phase-shifters at offsets of 30° and 60°, the difference in transmission loss was only 0.02 dB. Three Tektronix AFG310 function generators were used to generate the pseudorandom bit-sequence.

For an n-bit $m_n, m_{n-1}, \ldots, m_1, m_0$ signal to be modulated in Figure 4.1, QPSK modulation was attained by setting $b_0$ to $m_0$ and $b_1$ equal to $m_1$. The $b_2$ and $b_3$ voltage levels were set to a logic-level high. For 8-PSK modulation, the $m_0$ and $m_1$ bits are set to be equal to $b_0$ and $b_1$ as in QPSK. The $m_2$ bit was set equal to $b_2 = \overline{b_3}$. This direct complement was achieved by using an inverter. The voltage levels for the $b_2$ and $b_3$ bits were also stepped down using a voltage divider circuit by a factor of 0.96 to attain the required vector ratio for 8-PSK derived previously in Section 4.2.

The function generators were synchronized via the trigger-in/out ports to ensure proper transmission of the message signal. The chip was biased using a digital DC supply voltage. The digital demodulation option in an Agilent E4446A Spectrum Analyzer was used to measure the performance of the modulation. For each set of constellations a set of 100 sample constellation points were taken and the results were averaged. Each demodulation scheme
was carried out on three chips to account for any manufacturing defects. The power of the input signal in both modes was 22dBm.

The measured constellation charts and eye-diagrams of the output signals for the PSK and QAM modulation schemes are shown in Figures 4.10 and 4.11 respectively. The constellation graphs confirm that the modulator is
Figure 4.11: (a) 4-QAM constellation, (b) 16-QAM constellation, (c) 4-QAM eye diagram and (d) 16-QAM eye diagram

effective at carrying out modulation in both modulation schemes effectively. There is an even spread in the number of the paths between each constellation point which confirms that the system is proficient at modulating with non-deterministic pseudorandom data.

Table 4.1 shows the EVM of the received signal for different modulation
Table 4.1: Error Vector Magnitude developed in the respective modulation schemes.

<table>
<thead>
<tr>
<th>Modulation Scheme</th>
<th>EVM(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-PSK</td>
<td>3.69</td>
</tr>
<tr>
<td>8-PSK</td>
<td>8.51</td>
</tr>
<tr>
<td>4-QAM</td>
<td>2.33</td>
</tr>
<tr>
<td>16-QAM</td>
<td>6.20</td>
</tr>
</tbody>
</table>

The highest EVM is developed for the 8-PSK modulation while the lowest EVM is observed during 4-QAM modulation. It is important to note that the 4-PSK and 4-QAM modulation, although essentially the same modulation schemes, have slightly different EVM values. This is because the accounted to the difference in filters used for the modulator measurements during the demodulation process. The EVM value of a modulator signifies how close the modulator is able to map out the transcribed data to the desired constellation. A higher EVM value for a given modulation scheme implies that the modulator components behave more non-ideally at that modulation scheme. An extended discussion on the error contribution of the modulator components is presented in Appendix A. Overall, the modulator is able to carry out phase-shift keying and amplitude modulation with EVM values at less than 9%.
4.5 Conclusions

A novel multi-scheme modulator with an operating frequency of 5.4GHz is presented in 0.13um CMOS. The modulator is capable of modulating signals in PSK as well as AM modulation schemes. The modulator is composed of two OTAs and a switching network which allows for convenient selection and scaling of vectors on the I and Q-planes. Measurement results show accurate constellation points depicting proper modulation of the data with a maximum EVM of 8.51%.

As observed in Section 4.2, the largest achievable $m$-PSK modulation scheme by the modulator is limited by the modulator’s gain range. This architecture can be expected to support higher modulation schemes efficiently with a redesigned OTA with superior gain capabilities.
Chapter 5

Summary and Conclusions

5.1 Summary

The realization in Moore’s Law of shrinking transistor size has opened up several opportunities of integrating different areas of electrical research. Although the reduction in size offers new opportunities of ubiquitous interaction between digital, analog, mixed-signal components, it often comes at a price of reduced efficiency of the effective heterogeneous system due to PVT variations. Since the diminished performance due to reduced size is most acute in the analog parts of the device, digital components which are immune to the effects of size reduction can be used to compensate for the shortcomings of the analog parts. Such a ‘self-healing’ system [7] can thus be attained through the use of digital assisted self-calibration network. The scope of using digital control in conjunction with some existing microwave circuits was
proposed in this thesis. The downconversion mixer and modulator are both integral parts of the transceiver chain and, as such, are excellent candidates for this type of self-correction.

A variable-gain downconverter mixer designed in 0.13 \( \mu \text{m} \) with added digital control was realized. A microcontroller which took in input levels of power and frequency produced DC bias voltages to vary the gain of the mixer to decrease the 3-dB compression point over a 15GHz range. A linear interpolation algorithm developed with previously measured mixer data was used to estimate the requisite DC bias voltages. The use of digital control extended the operating bandwidth of the mixer from 12GHz to 15GHz. The digital assist system allowed for controllable variations in conversion gain from 1.2-9.8dB. At the maximum operating frequency point, the P1dB was found to vary between -5.3dBm to -11.5dBm and the IIP3 to vary between +6.8dBm to 0.78dBm for the range of conversion gains. Overall, the experiment displayed the ability of digital assist to increase the operating bandwidth of the mixer by 25%.

A 5.4GHz QAM modulator was fabricated in 0.13 \( \mu \text{m} \). The modulator used a novel OTA design to develop orthogonal vector basis for modulation. This versatility of the OTA was exploited to use the same modulator to achieve 4-PSK and 8-PSK modulation. The modulator was able to carry out PSK modulation successfully with its original carrier frequency of 5.4GHz. The EVM for the modulator was measured to be 3.69% and 8.51% for the 4-PSK and 8-PSK schemes respectively. This is within the range of the EVM
incurred for the original 4-QAM and 16-QAM schemes at 2.33% and 6.20% respectively. The input power was maintained at 22dBm for modulation in both cases. In summary, this experiment displayed the versatility of using this modulator in multiple modulation schemes with room for a digital assist system to allow for control of the modulation process by the user.

The ramifications of the performance attained by these two systems goes beyond simply demonstrating their versatile range of operation. The constant gain lines attained within the 1-15GHz range through digital assist implies that the system can be calibrated to operate anywhere within the selected window of operation solely by an external digital system. Similarly, the modulator’s scheme of operation can be dictated by a digital core that lies external to the analog architecture. The most significant takeaway is that, given a multi-faceted analog architecture, analog signals can be controlled through a digital interface. This indicates that in a more mature system, a high degree of control can be exercised over the analog domain simply by improving the software end of the digital core without touching the analog components of the system.

5.2 Future Work

Both designs have some areas that essentially act as bottlenecks that limit the performance of the system. Addressing these limiting issues and overcoming them offers the scope of increasing the performance of both designs
significantly. In general, the implementation of active feedback loops with digital control to both systems would provide more practical insight to the versatility of both designs.

Firstly, employing the aforementioned feedback loop in the mixer, the robustness of the RF components could be estimated by observing the frequency of interrupts the digital core has to make to the system for self-correction. Secondly, as observed in Section 3.1.2 the gain range used to develop the digital assist algorithm is effectively limited by the 3-dB bandwidth of the OTA used in the mixer’s transconductance stage. Using an OTA with an extended bandwidth would provide opportunities to increase the mixer’s operating bandwidth as well as the range of conversion gain.

Following from the discussion in Section 4.2 the range of OTA gain limits the PSK modulation to a maximum of 8-PSK. Improving the OTA gain in the modulator would allow for a greater ratio of the $I_{LARGE}$ and $I_{SMALL}$ vectors thereby enabling the modulator to carry out QPSK modulation. Appendix A describes the propagation of phase offsets in the constellation vectors developed through mismatches in the symmetric RF components. It follows that, in addition to controlling modulation schemes, a digital assist system could also be employed to calibrate for phase errors developed in the system.
Bibliography


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Appendix A

Error Propagation through Modulator Circuit

The offset at the output is generally caused by small inconsistencies and offsets in some of the system’s core components. Some of these components contribute to the deviation of the output signal more so than others. An analysis is conducted to assess the extent to which phase and amplitude propagates to some of the components of the system.

Figure A.1 shows a simple system level schematic depicting the path of the signal through the modulator. The system is symmetric, so the amplitude losses for each path are assumed to be the same. $\Delta \alpha_n$ represents the added amplitude loss and $\Delta \theta_n$ represent the added phase error by the corresponding system component respectively. For illustration purposes, all error propagation is calculated assuming a QPSK modulation scheme.
sinusoidal signal \( s(t) = A \cos(\omega t + \phi) \) is considered to be the input RF signal for this analysis. So each of the four basis vectors coming out of the baluns can be represented by:

\[
\begin{align*}
    s_0(t) &= \alpha_0 \alpha_1 A \cos(\omega t + \phi) \\
    s_{90}(t) &= \alpha_0 \alpha_1 A \cos(\omega t + \phi + \frac{\pi}{2}) = -\alpha_0 \alpha_1 A \sin(\omega t + \phi) \\
    s_{180}(t) &= \alpha_0 \alpha_1 A \cos(\omega t + \phi + \pi) = -\alpha_0 \alpha_1 A \cos(\omega t + \phi) \\
    s_{270}(t) &= \alpha_0 \alpha_1 A \cos(\omega t + \phi + \frac{3\pi}{2}) = \alpha_0 \alpha_1 A \sin(\omega t + \phi)
\end{align*}
\]

The modulated output signal is thus given by:

\[
y(t) = \alpha_2 \alpha_3 \alpha_4 \left[ b_0 \cdot s_0(t) + \bar{b}_0 \cdot s_{180}(t) + b_1 \cdot s_{90}(t) + \bar{b}_1 \cdot s_{270}(t) \right] \\
\quad = A \alpha_0 \alpha_1 \alpha_2 \alpha_3 \alpha_4 \left[ b_0 \cos(\omega t + \phi) - \bar{b}_0 \cos(\omega t + \phi) - b_1 \sin(\omega t + \phi) + \bar{b}_1 \sin(\omega t + \phi) \right]
\]

(A.1)
A.1 Amplitude Offset propagation

The variation of the output signal incurred by an offset caused at one of components stages is now investigated. The output signal tends to be affected in particular by the parallel components in the system i.e. the OTAs, active baluns and switching networks. For illustration purposes, we isolate the change in the amplitude of the pair of active baluns and assume the amplifications rendered by the other system components to stay constant. It will become intuitively obvious how the results derived for the baluns is also applicable to the other parallel components in the system. The difference in amplitude between the two baluns is represented by $\Delta \alpha$. The basis vectors thus become:

\[
\begin{align*}
  s_0(t) &= \alpha_0 \left( \alpha_1 - \frac{\Delta \alpha}{2} \right) A \cos(\omega t + \phi) \\
  s_{90}(t) &= \alpha_0 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) A \cos(\omega t + \phi + \frac{\pi}{2}) = -\alpha_0 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) A \sin(\omega t + \phi) \\
  s_{180}(t) &= \alpha_0 \left( \alpha_1 - \frac{\Delta \alpha}{2} \right) A \cos(\omega t + \phi + \pi) = -\alpha_0 \left( \alpha_1 - \frac{\Delta \alpha}{2} \right) A \cos(\omega t + \phi) \\
  s_{270}(t) &= \alpha_0 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) A \cos(\omega t + \phi + \frac{3\pi}{2}) = \alpha_0 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) A \sin(\omega t + \phi)
\end{align*}
\]

In Equation A.1, all the amplitude contributions from the other components are lumped into one value as $\alpha'$. Equation A.1 can thus be re-written as follows (when $y_e(t)$ represents the 'erroneous' signal at the output):
\[ y_e(t) = \alpha' \left[ b_0 \left( \alpha_1 - \frac{\Delta \alpha}{2} \right) \cos(\omega t + \phi) - \bar{b}_0 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) \cos(\omega t + \phi) \right] \\
+ \alpha' \left[ -b_1 \left( \alpha_1 + \frac{\Delta \alpha}{2} \right) \sin(\omega t + \phi) + \bar{b}_1 \left( \alpha_1 - \frac{\Delta \alpha}{2} \right) \sin(\omega t + \phi) \right] \]

(A.2)

The error offset in the received signal is given by subtracting Equation A.2 from Equation A.1:

\[ \Delta y = y(t) - y_e(t) \]
\[ = \alpha' \frac{\Delta \alpha}{2} \left[ -b_0 \cos(\omega t + \phi) + \bar{b}_0 \cos(\omega t + \phi) - b_1 \sin(\omega t + \phi) + \bar{b}_1 \sin(\omega t + \phi) \right] \]
\[ = \alpha' \frac{\Delta \alpha}{2} \left[ (\bar{b}_0 - b_0) \cos(\omega t + \phi) + (\bar{b}_1 - b_1) \sin(\omega t + \phi) \right] \]

(A.3)

Taking the magnitude of \( \Delta y \), we get,

\[ |\Delta y| = \left| \frac{\alpha' \Delta \alpha}{2} \right| \left[ (\bar{b}_0 - b_0) \cos(\omega t + \phi) + (\bar{b}_1 - b_1) \sin(\omega t + \phi) \right] \]
\[ = \frac{|\alpha' \Delta \alpha|}{2} \cdot \sqrt{1^2 + 1^2} \]
\[ = \sqrt{2} |\alpha' \Delta \alpha| \]

(A.4)

Equation A.4 implies that the offset of the output signal is directly proportional to the magnitude of the offset incurred in the parallel component in question.
A.2 Phase Offset Propagation

Similarly, the propagation of phase errors contributed by the system components are now considered. In particular, the analyses focus on the effects of the two-way 90° phase-shifter and the two 180°-split balun since these two components are highly likely to add to the phase offset of the system.

For the purposes of this part of the analysis we assume that the amplitude gains at each system component for all four signal paths is the same. In equation A.1, the attenuated amplitude term \([A\alpha_0\alpha_1\alpha_2\alpha_3\alpha_4]\) can be represented simply as \(\alpha_T\). Since the phase information of the signal is given by the \((\omega t + \phi)\) term, assuming a constant input frequency of the signal, we define:

\[\theta \triangleq \omega t + \phi\]

Equation A.1 is thus rewritten as:

\[y(\theta) = \alpha_T[b_0 \cos(\theta) - \bar{b}_0 \cos(\theta) - b_1 \sin(\theta) + \bar{b}_1 \sin(\theta)]\]  

(A.5)

\(\Delta\theta\) is defined as the phase mismatch of the signal as it comes out of the phase shifter such that the phase difference of the signal going into the second Balun is \((90^\circ + \Delta\theta)\) instead of \(90^\circ\). The basis vectors now become:

\[s_0(t) = \alpha_0\alpha_1 A \cos(\theta)\]
\[s_{90}(t) = -\alpha_0\alpha_1 A \sin(\theta + \Delta\theta)\]
\[s_{180}(t) = -\alpha_0\alpha_1 A \cos(\theta)\]
\[s_{270}(t) = \alpha_0\alpha_1 A \sin(\theta + \Delta\theta)\]
Equation A.5 now becomes:

\[ y_e(\theta) = \alpha_T[b_0 \cos(\theta) - \bar{b}_0 \cos(\theta) - b_1 \sin(\theta + \Delta \theta) + \bar{b}_1 \sin(\theta + \Delta \theta)] \]  

(A.6)

The next part of the analysis is carried out assuming a bit-value transmission of \( b_0 = b_1 = 1 \). The results for all four values are, however, summarised later in a table. Equation A.6 is thus reduced to:

\[ y_e(\theta) = \alpha_T[\cos(\theta - \sin(\theta + \Delta \theta))] \]

\[ = \alpha_T[\cos \theta - \sin \theta \cos \Delta \theta - \cos \theta \sin \Delta \theta] \]

\[ = \alpha_T[\cos \theta(1 - \sin \Delta \theta) - \sin \theta(\cos \Delta \theta)] \]

For a given bitstream value of \( b_0 = b_1 = 1 \), the error signal has a form similar to the expected signal in equation A.5: \( y(\theta) = \alpha_T[\cos \theta - \sin \theta] \)

The difference between the received and desired signal is thus given by:

\[ \Delta y = |y_e(\theta) - y(\theta)| \]

\[ = |\alpha_T[\cos(\theta - \sin \Delta \theta) - \sin \theta(1 + \cos \Delta \theta)]| \]

\[ = |\alpha_T[\cos(\theta(\sin \Delta \theta) + \sin \theta(1 + \cos \Delta \theta)]| \]  

(A.7)

Developing the rest of the truth table for all the other values of \( b_0 \) and \( b_1 \), we get:
Note that for all values of \( b_0 \) and \( b_1 \),
\[
\Delta y = |\alpha_T[\cos \theta(\sin \Delta \theta) + \sin \theta(1 + \cos \Delta \theta)]|
\]
This signifies that the offset of the output signal caused by the phase shifter
does not depend on the data being transmitted at all. The value of \( \Delta y \)
depends only on the phase error angle \( (\Delta \theta) \) and the phase angle \( (\theta) \) of the
signal being transmitted. Figure A.2 shows how the deviation of the output
signal varies from the expected constellation point as a function of the phase
error in the phase shifter.

The same phase propagation analysis is now carried out for the two ac-
tive baluns in the modulator. Assume that the first balun \( (0^\circ/180^\circ \text{ split}) \)
undergoes a phase mismatch of \( \Delta \theta_1 \) and the second balun \( (90^\circ/270^\circ \text{ split}) \)
experiences a phase mismatch of \( \Delta \theta_2 \). The original four basis vectors can
thus be represented as:
\[
s_0(t) = \alpha_0 \alpha_1 A \cos \left( \theta - \frac{\Delta \theta_1}{2} \right)
\]
\[
s_{90}(t) = -\alpha_0 \alpha_1 A \sin \left( \theta - \frac{\Delta \theta_1}{2} \right)
\]
\[
s_{180}(t) = -\alpha_0 \alpha_1 A \cos \left( \theta + \frac{\Delta \theta_1}{2} \right)
\]
\[
s_{270}(t) = \alpha_0 \alpha_1 A \sin \left( \theta + \frac{\Delta \theta_2}{2} \right)
\]
As in the last analysis a bitstream of \( b_0 = b_1 = 1 \) is assumed for the purposes

<table>
<thead>
<tr>
<th></th>
<th>( b_0 )</th>
<th>( y_c(\theta) )</th>
<th>( \Delta y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>(-\alpha_T[\cos \theta(1 - \sin \Delta \theta) - \sin \theta(\cos \Delta \theta)])</td>
<td>(</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>(\alpha_T[\cos \theta(1 + \sin \Delta \theta) + \sin \theta(\cos \Delta \theta)])</td>
<td>(</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>(-\alpha_T[\cos \theta(1 + \sin \Delta \theta) - \sin \theta(\cos \Delta \theta)])</td>
<td>(</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(\alpha_T[\cos \theta(1 - \sin \Delta \theta) - \sin \theta(\cos \Delta \theta)])</td>
<td>(</td>
</tr>
</tbody>
</table>
Figure A.2: Variation of the output signal mismatch as a function of the phase error at the phase splitter of illustration.

\[ y_e(\theta) = \alpha T \left[ \cos \left( \theta - \frac{\Delta \theta_1}{2} \right) - \sin \left( \theta + \frac{\Delta \theta_2}{2} \right) \right] \]

\[ = \alpha T \left[ \cos \theta \cos \left( \frac{\Delta \theta_1}{2} \right) + \sin \theta \sin \left( \frac{\Delta \theta_1}{2} \right) - \sin \theta \cos \left( \theta + \frac{\Delta \theta_2}{2} \right) + \cos \theta \sin \left( \theta + \frac{\Delta \theta_2}{2} \right) \right] \]

\[ = \alpha T \left[ \cos \theta \left\{ \cos \left( \frac{\Delta \theta_1}{2} \right) + \sin \left( \frac{\Delta \theta_2}{2} \right) \right\} - \sin \theta \left\{ \cos \left( \frac{\Delta \theta_2}{2} \right) - \sin \left( \frac{\Delta \theta_1}{2} \right) \right\} \right] \]
\[ \Delta y = |y(\theta) - y_e(\theta)| \]
\[ = |\alpha_T \left[ \cos \theta \left\{ 1 - \cos \left( \frac{\Delta \theta_1}{2} \right) - \sin \left( \frac{\Delta \theta_2}{2} \right) \right\} - \sin \theta \left\{ 1 - \cos \left( \frac{\Delta \theta_2}{2} \right) + \sin \left( \frac{\Delta \theta_1}{2} \right) \right\} \right]| \]

Developing the rest of the truth table for the other three bitstream combinations, we get:

<table>
<thead>
<tr>
<th>( b_1 )</th>
<th>( b_0 )</th>
<th>( \Delta y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>(</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>(</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>(</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(</td>
</tr>
</tbody>
</table>

Extrapolating from the table above, the error offset of the output signal can be generalized as follows:

\[ \Delta y = \cos \theta \left\{ 1 - \left( \cos \left( \frac{\Delta \theta_1}{2} \right) + (-1)^{b_0+1} \sin \left( \frac{\Delta \theta_2}{2} \right) \right) \right\} \]
\[ + (-1)^{b_0+b_1+1} \sin \theta \left\{ 1 - \left( \cos \left( \frac{\Delta \theta_2}{2} \right) + (-1)^{b_0+b_1+1} \sin \left( \frac{\Delta \theta_1}{2} \right) \right) \right\} \]

(A.8)

The error contributed by the baluns depends on the phase error contributed by each system as well as the bit values being transmitted in each case. The complexity of the formula insinuates that no direct correlation can be drawn between the signal offset and the dependent variables.

Although all the analysis carried out in this section dealt with a QPSK modulation scheme, the results should be similar for other modulation schemes.
as well. Mathematical modelling for higher modulation schemes may can eas-
ily be carried out using this analysis as a starting point.