ADAPTIVE RESISTANCE CONTROL SOLUTIONS IN AN
ASSISTED CODING ENVIRONMENT

By

Sarah Jane Burton

A thesis submitted to the Department of Electrical and Computer Engineering
in conformity with the requirements for the

Degree of Master of Applied Science

Queen’s University

Kingston, Ontario, Canada

March, 2016

Copyright © Sarah Jane Burton, 2016
Abstract

This thesis focuses on the implementation of a human energy harvester’s resistance control scheme for a full capacitance boost converter, low capacitance boost converter, and a voltage controlled attenuator. The boost converter control schemes utilize an adapted PFC ACMC boost converter topology with input resistance as a controlled feedback variable for the current loop, while disregarding the output voltage resistance. The electronic module’s power draw affects the applied resistance felt by the user. The prototype outputs a nominal 10W of power for the emulated 2.5Ω full load. Previous research has enabled constant resistance, threshold resistance, and variable resistance control implementations on a boost converter coded in Code Composer Studio’s C/C++ environment.

The first goal of this thesis sought to eliminate or minimize the necessary C/C++ coding required for resistive control. This was achieved through the implementation of MATLAB Simulink’s Embedded Coder’s C2000 Library coding environment, using a block diagram control scheme with integrated MATLAB coding.

Three control schemes are proposed: Ramp and Hold, Optimized Resistance, and Power Regulation control algorithms. The Ramp and Hold scheme targets the decoupling point between the motor and the input encoder. The control method increases from light to full load peaking and holding the full load condition at this decoupling point to target the energy harvester’s negative work period. The Optimized Resistance algorithm averages the user’s average voltage at light load, and then increments the resistance until this voltage begins to drop, indicating a change in the user’s kinematics. The Power Regulation control scheme programs a required average output power per step for the user, and dynamically alters the resistance felt by the user to achieve this goal.

The final boost converter had a peak efficiency DC of 93.4% for 25W input power at $V_{in}=20V$ and $R_{in}=15Ω$. The linear regulator voltage controlled attenuator acts as a simple resistive load to dissipate the entire 10W input power, using the low side MOSFET for power dissipation. The three control schemes were
implemented and tested on a boost converter with a 2200µF, 940µF, and 47µF output capacitor. Integrated improvements to the system and future work are then proposed.
Acknowledgments

I would first like to give my deepest thanks to my supervisors, Dr. Yan-Fei Liu and Dr. Qingguo Li, who have afforded me exceptional patience, liberty, guidance, and support over these past two years. Thank you, Dr. Liu for sharing your peerless knowledge in the field of electronics while demonstrating an unmatched support for the personal and technical growth of your students. Thank you Dr. Li for allowing me entrance into the exciting field of biomechanics which I had never before considered. I cannot thank them both enough for the opportunity that they have afforded me. I would like to extend this thanks to my colleagues in both labs, particularly Michael Shepertycky, whose intensive knowledge of the energy harvester and willingness to take the time to share that knowledge have been inexhaustible. To my lab mates in Dr. Liu’s lab, I continue to be impressed by your abilities, adversity, and versatility with electrical systems at home and abroad, and would like to thank you for helping with the electrical support that I have needed.

I would also like to thank my partner Brian White whose emotional and technical support have been invaluable. He has helped me troubleshoot five years of life’s pitfalls and has been a pillar of my work, someday I’ll be able to return the favour and be a valuable partner in AoE or Civ or something and we can call it even. I would also like to thank my friends who have provided critical distraction outside of work when things have been difficult, especially Clay Doggart for inspiring me with his mettle (even when he doesn’t believe it), my brother Nicholas for his keen sense of humour and vast esoteric knowledge (I’m so sorry, I glossed over a lot of those IV/EV optimization details), Veronique Tomlinson for always aiming high, and Alex Bloor for investing his time and creative genius to entertaining us table-top folk. To my friend Andrew Richardson, I promised you an acknowledgment, here’s a +1 to your SEO.

Lastly I would like to thank my parents Janet Davies and David Burton for their interest and support, both emotionally and financially. They have always supported me in my life choices and this time was no different. I would like to dedicate this thesis in memory of my grandfather George Henry Burton, who has always been proud of the work of his children and grandchildren, I regret that I could not show him this work come to fruition.
# Table of Contents

Abstract........................................................................................................................................... ii
Acknowledgments............................................................................................................................. iv
Table of Contents............................................................................................................................. v
List of Tables..................................................................................................................................... viii
List of Figures.................................................................................................................................... ix
List of Abbreviations....................................................................................................................... xiii
List of Symbols.................................................................................................................................. xv
SI Units............................................................................................................................................. xviii

Chapter 1 Introduction...................................................................................................................... 1
  1.1 Introduction............................................................................................................................... 1
  1.2 Existing Energy Harvesting Methods....................................................................................... 2
    1.2.1 Types and Power Ranges of Energy Harvesters............................................................... 2
    1.2.2 Power Electronics in Human Energy Harvesting............................................................. 6
    1.2.3 Biomechanical Considerations of HEH and an Analysis of Gait..................................... 9
    1.2.4 Prototype: Lower Limb Driven Energy Harvesting Device............................................. 11
  1.3 Research Motivation.................................................................................................................. 17
    1.3.1 User-Friendly Implementation......................................................................................... 18
    1.3.2 Flexible Resistance Control Implementations................................................................. 19
    1.3.3 Proof of Electrical Adaptability...................................................................................... 19
  1.4 Thesis Objectives and Contribution......................................................................................... 19
  1.5 Thesis Organization.................................................................................................................. 20

Chapter 2 Application and Research Adaptation......................................................................... 21
  2.1 Introduction............................................................................................................................... 21
  2.2 Boost Converter Principles of Operation............................................................................... 21
  2.3 Previous Research: Power Electronics Module with Battery Charging.............................. 29
  2.4 Adapted Boost Converter Design............................................................................................ 36
    2.4.1 Tuning and Stability........................................................................................................... 39
      2.4.1.1 PI Control Scheme....................................................................................................... 46
      2.4.1.2 Fuzzy Logic Investigation........................................................................................... 47
  2.5 Conclusion............................................................................................................................... 50

Chapter 3 Digital Control Methods............................................................................................... 51
  3.1 Introduction............................................................................................................................... 51
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.2</td>
<td>Software Selection: MATLAB Embedded Coder</td>
<td>52</td>
</tr>
<tr>
<td>3.3</td>
<td>TMS320F2808 DSP Evaluation Board</td>
<td>56</td>
</tr>
<tr>
<td>3.4</td>
<td>Digital Sensing Scheme and Sensitivity</td>
<td>56</td>
</tr>
<tr>
<td>3.5</td>
<td>Constant and Threshold Control Scheme Replication Methods</td>
<td>59</td>
</tr>
<tr>
<td>3.6</td>
<td>Experimental Test Rig</td>
<td>62</td>
</tr>
<tr>
<td>3.7</td>
<td>Experimental Results</td>
<td>65</td>
</tr>
<tr>
<td>3.7.1</td>
<td>Block Diagram Configuration</td>
<td>67</td>
</tr>
<tr>
<td>3.7.2</td>
<td>Code Composer Studio</td>
<td>71</td>
</tr>
<tr>
<td>3.7.3</td>
<td>Ideal AC Source Experimental Results</td>
<td>72</td>
</tr>
<tr>
<td>3.7.4</td>
<td>Test Rig Experimental Results</td>
<td>75</td>
</tr>
<tr>
<td>3.8</td>
<td>Conclusion</td>
<td>81</td>
</tr>
<tr>
<td>4</td>
<td>An Improved Control Method</td>
<td>82</td>
</tr>
<tr>
<td>4.1</td>
<td>Introduction</td>
<td>82</td>
</tr>
<tr>
<td>4.2</td>
<td>The Biomechanics of Negative and Positive Work</td>
<td>83</td>
</tr>
<tr>
<td>4.3</td>
<td>Mechanical Feedback: Optical Encoders</td>
<td>85</td>
</tr>
<tr>
<td>4.4</td>
<td>Proposed Control Schemes and Terminology Clarification</td>
<td>88</td>
</tr>
<tr>
<td>4.4.1</td>
<td>The Mechanical and Electrical Implications of Resistance</td>
<td>88</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Ramp and Hold Scheme</td>
<td>90</td>
</tr>
<tr>
<td>4.4.3</td>
<td>Resistance Optimization (Constant Voltage) Scheme</td>
<td>90</td>
</tr>
<tr>
<td>4.4.4</td>
<td>Power Regulation (Constant Power) Scheme</td>
<td>91</td>
</tr>
<tr>
<td>4.5</td>
<td>Experimental Results</td>
<td>92</td>
</tr>
<tr>
<td>4.5.1</td>
<td>Ramp and Hold Experimental Results</td>
<td>94</td>
</tr>
<tr>
<td>4.5.1.1</td>
<td>Encoder Decoupling Targeting</td>
<td>96</td>
</tr>
<tr>
<td>4.5.1.2</td>
<td>Encoder Reference Counting</td>
<td>98</td>
</tr>
<tr>
<td>4.5.1.3</td>
<td>Step Counting</td>
<td>101</td>
</tr>
<tr>
<td>4.5.1.4</td>
<td>Test Rig Experimental Results</td>
<td>104</td>
</tr>
<tr>
<td>4.5.2</td>
<td>Resistance Optimization (Constant Voltage) Experimental Results</td>
<td>107</td>
</tr>
<tr>
<td>4.5.3</td>
<td>Power Regulation (Constant Power) Experimental Results</td>
<td>109</td>
</tr>
<tr>
<td>4.6</td>
<td>Conclusion</td>
<td>112</td>
</tr>
<tr>
<td>5</td>
<td>Low Capacitance and Linear Regulator Adaptability</td>
<td>113</td>
</tr>
<tr>
<td>5.1</td>
<td>Introduction</td>
<td>113</td>
</tr>
<tr>
<td>5.2</td>
<td>Low Capacitance Boost Converter</td>
<td>114</td>
</tr>
<tr>
<td>5.2.1</td>
<td>Stability</td>
<td>114</td>
</tr>
<tr>
<td>5.2.2</td>
<td>Experimental Results</td>
<td>117</td>
</tr>
</tbody>
</table>
List of Tables

Table 1-1- Shoe Mounted HEHs and their average power levels………………………………………………. 3
Table 1-2 Backpack-based HEH Designs and their average Power Output………………………………………. 5
Table 2-1 Comparison between conventional PFC and $R_m$ controlled boost converter…………………….. 31
Table 2-2 Boost converter component selection……………………………………………………………….. 38
Table 2-3 Fuzzy logic implementation of a two-input membership function…………………………………….. 48
Table 3-1 Boost converter resistive divider values……………………………………………………………….. 57
Table 3-2 ADC RC filter values……………………………………………………………………………………….. 58
Table 4-1 Terminology clarification ………………………………………………………………………………………. 89
Table 4-2 Functional average step power output for an emulated step input……………………………………….. 110
Table 5-1 Effects of a low capacitance boost capacitor on a ACMC PFC converter…………………………….. 123
Table F-1 Input Encoder to boost converter/Linear Regulator inputs…………………………………………….. 159
Table F-2 BMC 2120-Pin Connections………………………………………………………………………………… 159
Table F-3 TMS320F2808 GPIO eQEP pin configuration…………………………………………………………. 160
Table F-4 TMS320F2808 GPIO ePWM pin configuration………………………………………………………….. 160
Table F-5 TMS320F2808 Underside pin connections …………………………………………………………………… 161
List of Figures

Figure 1-1 Biomechanical knee brace energy harvester.......................................................... 4
Figure 1-2 PFC boost topology and control scheme................................................................. 6
Figure 1-3 Maximum Energy Harvesting Control with MPPT Tracking for a PFC boost.............. 7
Figure 1-4 Control scheme of an EH system with SEPIC converter and battery charging [1]........ 8
Figure 1-5 Mechanical configuration of a 10W gear-driven energy harvesting backpack............ 11
Figure 1-6 Cable length velocity and power profile of a gear and pulley-based LLDEH.............. 12
Figure 1-7 3-phase simulated input waveform [45]................................................................. 13
Figure 1-8 Rectified 3-phase generator output overlaid by a calibrated AC sine wave [45]............. 14
Figure 1-9 COH 10W of a LLDEH compared to comparable devices at similar power.............. 15
Figure 1-10 TCOH of a LLDEH compared to comparable devices at similar power levels.......... 16
Figure 1-11 Kinematics of a gear driven energy harvester on ten averaged subjects................ 16
Figure 1-12 User setup configuration for a gear train lower limb driven energy harvesting device... 17
Figure 2-1 Simplified boost converter topology...................................................................... 22
Figure 2-2 Boost Converter during first power MOSFET conduction...................................... 23
Figure 2-3 Boost Converter operation during first power MOSFET off period......................... 24
Figure 2-4 Boost Converter during capacitor discharge stage.................................................. 25
Figure 2-5 Differing modes of operation for a boost converter based on the inductor current........ 25
Figure 2-6 Simplified CCM versus DCM at follow a reference current.................................... 26
Figure 2-7 Switching Waveforms of a CCM boost converter.................................................. 27
Figure 2-8 Two-stage PEM with ESC, designed for a LLDEH backpack.................................. 30
Figure 2-9 Emulated Constant $R_{in}$ control scheme for a two stage PEM............................. 32
Figure 2-10 Emulated Voltage Threshold $R_{in}$ control scheme for a two stage PEM............... 32
Figure 2-11 Emulated Variable $R_{in}$ control scheme for a two stage PEM.............................. 32
Figure 2-12 Emulated threshold input resistance for a two stage PEM...................................... 33
Figure 2-13 Emulated variable resistance for a two stage PEM.............................................. 33
Figure 2-14 Buck Charging where $P_{in}<P_{out\max}$................................................................. 34
Figure 2-15 Battery charging in CC mode with higher $P_{in}$...................................................... 35
Figure 2-16 High level power flow diagram of a two-stage PEM module................................... 35
Figure 2-17 Constant $R_{in}$ control on a calibrated test rig...................................................... 36
Figure 2-18 Boost converter components design................................................................. 39
Figure 2-19 Discretization and digital control of a PFC boost converter’s feedback path............ 42
Figure 2-20 Compensated Bode plot of a full load PFC boost converter without \( G_{adp} \) .......................... 43
Figure 2-21 Compensated Bode plot of a full load PFC boost converter with \( G_{adp} \) .......................... 44
Figure 2-22 Direct form implementation of a 2P2Z compensator ................................................. 45
Figure 2-23 Separate form implementation of a 2P2Z compensator ............................................. 46
Figure 2-24 Continuous-Time PI control with built in integral correction gain ............................... 47
Figure 2-25 Triangular membership function error input plot for a non-linear control system ........ 49
Figure 3-1 Simulink Embedded Coder code generation flowchart ............................................ 53
Figure 3-2 Resistive divider for ADC conditioning ................................................................. 57
Figure 3-3 ADC RC Filter configuration .................................................................................. 58
Figure 3-4 ADC-Update configuration in MATLAB Embedded Coder ........................................... 60
Figure 3-5 Digital PWM Control for an ACMC boost converter using the TMS320F2808 DSP ...... 61
Figure 3-6 ADC Hardware interrupt update control workflow with MATLAB’s Simulink .......... 62
Figure 3-7 Resistively damped EPOS studio 2.1 profile at full load ........................................... 63
Figure 3-8 Light loading of the ideal sinusoidal EPOS 2.1 profile with magnetics ...................... 64
Figure 3-9 DC Test 10% duty cycle 5V in inductor current emulated a light load condition ......... 65
Figure 3-10 Boost Converter 25W DC Efficiency at an input voltage of 20V ............................... 66
Figure 3-11 Uncompensated full load constant 80% duty cycle for a 10W boost converter ....... 66
Figure 3-12 Boost Converter high level Simulink control blockset workflow ............................ 67
Figure 3-13 Gain and Tuning Simulink subsystem blocksets ..................................................... 69
Figure 3-14 Simulink PWM Update subsystem block ............................................................... 70
Figure 3-15 Code Composer Studio graphing feature ............................................................... 71
Figure 3-16 Constant input resistance control for \( R_{in} = 10 \Omega \) on a boost converter ............... 73
Figure 3-17 Threshold input resistance control for \( R_{in} = 10 \Omega \) to 5\( \Omega \) on a boost converter .... 74
Figure 3-18 DC Rise time of an ACMC PFC boost converter .................................................... 75
Figure 3-19 EPOS Pulley configuration with integrated LLDEH ............................................... 76
Figure 3-20 Range of emulated resistance control for an ACMC PFC boost converter .............. 76
Figure 3-21 Full load PFC of a simulated walking profile for an ACMC PFC boost converter .... 77
Figure 3-22 Emulated 2.5\( \Omega \) (Full load) PFC control scheme for an ACMC boost converter .... 78
Figure 3-23 Emulated threshold input resistance testing for \( R_{in} = 10 \Omega \) to 3\( \Omega \) on a boost converter ...... 79
Figure 3-24 Boost converter settling time on an emulated EPOS input .................................. 80
Figure 4-1 Negative work phase of a LLDEH device during right leg swing phase ................. 83
Figure 4-2 LLDEH Device’s contribution for an optimized constant 6\( \Omega \) load ..................... 84
Figure 4-3 Waveform diagram of a bidirectional optical encoder ............................................. 85
Figure 4-4 High level eQEP encoder integration in Simulink Embedded Coder ....................... 87
Figure 4-5 Motor encoder velocity block diagram workflow in Simulink Embedded Coder .......... 87
Figure 4-6 Encoder control block diagram ................................................................. 93
Figure 4-7 Ramp Up Resistance based on targeting the LLDEH’s encoder decoupling instant .......... 94
Figure 4-8 Force contributions of a lower-limb driven energy harvesting backpack .................. 96
Figure 4-9 11Ω Constant resistance decoupling output for a scaled leg and motor encoder ........ 97
Figure 4-10 Light load decoupling output for a scaled leg and motor encoder ......................... 98
Figure 4-11 Encoder ramp count and input voltage at full load ........................................ 98
Figure 4-12 Encoder ramp count with respect to the LLDEH’s input (Leg) encoder .................. 99
Figure 4-13 Threshold implementation by encoder count .............................................. 100
Figure 4-14 Step count function, triggers on the fall of the leg encoder count ...................... 101
Figure 4-15 Ramp function based on decoupling instant averaged during normal walking ...... 102
Figure 4-16 Resistance Ramp Up output resistance selection by average decoupling instant ...... 103
Figure 4-17 Light load acclimatization, sensing and averaging, and applied resistance periods ..... 104
Figure 4-18 Experimental Ramp and Hold experimental selected output resistance ................. 105
Figure 4-19 Ramp and Hold output of a PFC dynamic emulated input resistance .................. 106
Figure 4-20 Ramp and Hold output without updated decoupling ...................................... 107
Figure 4-21 Optimized voltage control scheme given a voltage threshold ............................ 108
Figure 4-22 Average sensed power per step for increasing power levels ........................... 109
Figure 4-23 Average input power over one emulated step at high power ......................... 110
Figure 4-24 Constant Power regulation resistance control ........................................... 111
Figure 4-25 Cable force felt by the user for a functional range of emulated resistances .......... 111
Figure 5-1 Stability test of a PFC boost converter for varying output capacitances .............. 115
Figure 5-2 Output voltage capacitor impact on output voltage ripple ................................ 117
Figure 5-3 Constant emulated resistance waveforms for a 940µF output capacitor boost converter .... 117
Figure 5-4 Ramp and Hold input resistance profile on a 940µF PFC boost converter ............ 118
Figure 5-5 Ramp and Hold Actual input resistance profile on a 940µF PFC boost converter ...... 119
Figure 5-6 Constant emulated resistance waveforms for a 100µF output capacitor boost converter ... 119
Figure 5-7 Inherent light load current draw for a 100µF PFC boost converter .................... 120
Figure 5-8 Ramp and Hold input resistance profile on a 100µF PFC boost converter ............ 121
Figure 5-9 Ramp and Hold Actual input resistance profile on a 100µF PFC boost converter .... 121
Figure 5-10 Set input resistance and actual input resistance control for a 100µF boost converter .... 122
Figure 5-11 Constant emulated resistance waveforms for a 47µF output capacitor boost converter ... 122
Figure 5-12 Ramp and Hold input resistance profile on a 47µF PFC boost converter ............ 123
Figure 5-13 Set input resistance and actual input resistance control for a 100µF boost converter .... 123
Figure 5-14 Ramp and Hold Actual input resistance profile on a 100µF PFC boost converter……… 124
Figure 5-15 Size comparison for a 2200µf and 47µF output capacitor…………………………… 125
Figure 5-16 Digital PWM Control for an ACMC boost converter using the TMS320F2808 DSP … 127
Figure 5-17 Onsemi NTD6416ANT4G Typical characteristic voltage profiles……………………… 128
Figure 5-18 Full load 5V rise time of a voltage controlled attenuator with digital PI control……… 131
Figure 5-19 Light load 5V rise time of a voltage controlled attenuator with digital PI control…… 132
Figure 5-20 Light load 5V rise time of a voltage controlled attenuator with gain scheduling……… 132
Figure 5-21 Full load 5V rise time of a voltage controlled attenuator with FET linearization……… 133
Figure 5-22 Constant resistance control of a voltage controlled attenuator………………………… 134
Figure 5-23 Constant resistance control of a voltage controlled attenuator- CCS Output………… 134
Figure 5-24 Threshold resistance control of a voltage controlled attenuator- CCS Output……… 135
Figure 5-25 Constant resistance control of a VCA on an experimental test rig…………………… 136
Figure 5-26 Threshold resistance control of a VCA on an experimental test rig…………………… 136
Figure 5-27 Threshold resistance control of a VCA on an experimental test rig- CCS Output…… 137
Figure 5-28 Ramp and Hold Resistance profile for a VCA operated on a mechanical test rig……… 137
Figure 5-29 Ramp and Hold profile for a VCA operated on a mechanical test rig- CCS Output……… 138
Figure E-1 High level control diagrams……………………………………………………………… 157
Figure E-2 Gain and tuning subsystem block diagram……………………………………………… 157
Figure E-3 PWM Update subsystem…………………………………………………………………… 158
Figure E-4 Motor Encoder Speed signal conditioning subsystem, with exported motor velocity…… 158
Figure E-5 Input (leg) encoder subsystem……………………………………………………………… 159
Figure E-6 Variable resistance control schemes……………………………………………………… 160
Figure G-1 PFC Boost converter integrated with the TMS320F2808……………………………… 164
Figure G-2 Adapted Voltage Controlled Attenuator………………………………………………… 164
Figure G-3 Unpopulated PCB………………………………………………………………………… 164
Figure H-1 Altium board layout and pin connections………………………………………………… 165
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACMC</td>
<td>Average Current Mode Control</td>
</tr>
<tr>
<td>BMRL</td>
<td>Bio-Mechatronics and Robotics Laboratory</td>
</tr>
<tr>
<td>CC</td>
<td>Constant Current</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>CCS</td>
<td>Code Composer Studio</td>
</tr>
<tr>
<td>ChC</td>
<td>Charging Current</td>
</tr>
<tr>
<td>COC</td>
<td>Cost of Carry</td>
</tr>
<tr>
<td>COH</td>
<td>Cost of Harvest</td>
</tr>
<tr>
<td>COM</td>
<td>Centre of Mass</td>
</tr>
<tr>
<td>CrCM</td>
<td>Critical Conduction Mode</td>
</tr>
<tr>
<td>CSA</td>
<td>Current Sense Amplifier</td>
</tr>
<tr>
<td>DAQ</td>
<td>Data Acquisition (Unit)</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>DDHO</td>
<td>Driven Damped Harmonic Oscillator</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>EH</td>
<td>Energy Harvester</td>
</tr>
<tr>
<td>eQEP</td>
<td>Enhanced Quadrature Pulse Encoders</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>ESC</td>
<td>Energy Storage Capacitor</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input/Output (Pins)</td>
</tr>
<tr>
<td>HEH</td>
<td>Human Energy Harvesting</td>
</tr>
<tr>
<td>IDE</td>
<td>Integrated Development Environment</td>
</tr>
<tr>
<td>ISR</td>
<td>Interrupt Service Routine</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>LDO</td>
<td>Low Dropout (Regulator)</td>
</tr>
<tr>
<td>LLDEH</td>
<td>Lower Limb Driven Energy Harvester</td>
</tr>
<tr>
<td>LPB</td>
<td>Lithium Polymer Battery</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-pass filter</td>
</tr>
<tr>
<td>LR</td>
<td>Linear Regulator</td>
</tr>
<tr>
<td>MAF</td>
<td>Moving Average Filter</td>
</tr>
<tr>
<td>MCU</td>
<td>Microcontroller</td>
</tr>
<tr>
<td>MEECC</td>
<td>Maximum Energy Extraction and Charge Control Scheme</td>
</tr>
<tr>
<td>MEHC</td>
<td>Maximum Energy Harvesting Control</td>
</tr>
<tr>
<td>MPP</td>
<td>Maximum Power Point</td>
</tr>
<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PEM</td>
<td>Power Electronics Module</td>
</tr>
<tr>
<td>PEM</td>
<td>Power Electronics Module</td>
</tr>
<tr>
<td>PFC</td>
<td>Power Factor Correction</td>
</tr>
<tr>
<td>QPG</td>
<td>Queen’s Power Group</td>
</tr>
<tr>
<td>S/H</td>
<td>Sample and Hold</td>
</tr>
<tr>
<td>SARAM</td>
<td>Sequential Access and Random Access Memory</td>
</tr>
<tr>
<td>SoC</td>
<td>State of Charge</td>
</tr>
<tr>
<td>TCOH</td>
<td>Total Cost of Harvest</td>
</tr>
<tr>
<td>TI</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>VCA</td>
<td>Voltage Controlled Attenuator</td>
</tr>
<tr>
<td>VCR</td>
<td>Voltage Controlled Resistor</td>
</tr>
<tr>
<td>VVA</td>
<td>Voltage Variable Attenuator</td>
</tr>
<tr>
<td>ZOH</td>
<td>Zero-Order Hold</td>
</tr>
</tbody>
</table>
## List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$COH$</td>
<td>Cost of Harvest</td>
</tr>
<tr>
<td>$P_{met_elec}$</td>
<td>Metabolic power of electrical engagement</td>
</tr>
<tr>
<td>$P_{met_walk}$</td>
<td>Metabolic power of weighted walking</td>
</tr>
<tr>
<td>$P_{elec}$</td>
<td>Electrical power</td>
</tr>
<tr>
<td>$\eta_d$</td>
<td>Device efficiency given a defined electrical resistance</td>
</tr>
<tr>
<td>$\eta_m$</td>
<td>Peak muscle efficiency during positive work</td>
</tr>
<tr>
<td>$P_{met_nwalk}$</td>
<td>Metabolic power of normal walking</td>
</tr>
<tr>
<td>$I_L$</td>
<td>Inductor/Input Current</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Input Voltage</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance</td>
</tr>
<tr>
<td>$r_f$</td>
<td>Inductor’s parasitic winding resistance</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitance</td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>Load/Output Resistance</td>
</tr>
<tr>
<td>$r_{esr}$</td>
<td>Capacitor’s parasitic equivalent series resistance</td>
</tr>
<tr>
<td>$V_C$</td>
<td>Capacitor voltage</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty Cycle</td>
</tr>
<tr>
<td>$K_{crit}$</td>
<td>Critical inductor conduction parameter</td>
</tr>
<tr>
<td>$R_{crit}$</td>
<td>Critical load resistance</td>
</tr>
<tr>
<td>$T_{sw}$</td>
<td>Switching period</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$R_{nom}$</td>
<td>Nominal load resistance</td>
</tr>
<tr>
<td>$I_{L_max/min}$</td>
<td>Peak/minimum inductor current</td>
</tr>
<tr>
<td>$PF$</td>
<td>Power Factor</td>
</tr>
<tr>
<td>$V_{Boost}$</td>
<td>Boost (Output) voltage</td>
</tr>
</tbody>
</table>
$V_{rect}$ Rectified input voltage

$p_{avg}$ Average power

$L_{Boost}$ Boost converter inductor

$V_{rms}/I_{rms}$ Root-mean-square voltage/current

$R_{in}$ Emulated input resistance

$I_{in}$ Input current

$k_d$ Distortion factor

$k_{\theta}$ Displacement factor

$R_{sense}$ Sense resistor value

$\omega_Z$ Zero-frequency

$\omega_{RHPZ}$ Right-half-plane-zero frequency

$K_d$ Current sense and ADC gain factor

$H_C$ Zero-Order-Hold (ZOH) delay

$T_d$ Computational Delay

$SH$ Sample and Hold (S/H) delay

$G_{id}$ Open-loop power stage transfer function (control-to-output)

$G_{pBoost}$ Small-signal power stage model (For an ACMC boost converter)

$f_{clk}$ Clock frequency

$V_{ADC}$ Voltage at the ADC unit pin

$f_c$ Cut-off or roll-off frequency

$R_{select}$ Selected emulated input resistance

$R_{light}$ Light load resistance

$R_{full}$ Full load resistance

$t_{avgdecouple}$ Average decoupling period

$G_{adpvCA}$ Variable adaptive gain for the voltage controlled attenuator

$R_{DS}$ Drain to source MOSFET resistance

$R_{series}$ VCA Series resistance
\( V_{DS} \)  
Drain to source MOSFET voltage

\( V_{GS} \)  
Gate to source MOSFET voltage

\( I_{DSS} \)  
Zero gate voltage drain current

\( I_D \)  
MOSFET drain current

\( \Delta V_C \)  
Capacitor ripple voltage

\( \Delta I_L \)  
Inductor ripple current

\( F_{\text{cable}} \)  
Physical oppositional force on the user by the energy harvester’s cable

\( F_{\text{elec}} \)  
Harvester’s force contribution via electrical control methods

\( F_{\text{inertia}} \)  
Harvester’s physical inertia force overcome by the user

\( F_{\text{friction}} \)  
Harvester’s physical frictional force overcome by the user

\( F_{spring} \)  
Harvester’s physical spring force overcome by the user
SI Units

A  Amperes
F  Farads
H  Henries
h  Hours
Hz Hertz
J  Joules
m  Meters
N  Newtons
s  Seconds
V  Volts
W  Watts
Ω  Ohms

Prefixes for SI Units

p  Pico (10^{-12})
n  Nano (10^{-9})
µ  Micro (10^{-6})
m  Milli (10^{-3})
k  Kilo (10^{3})
M  Mega (10^{6})
Chapter 1
Introduction

1.1 Introduction

In recent decades, society has seen a surge in renewable energy technologies, investigated as an alternative to conventional consumable resources. These alternatives provide feasible and tested energy for a wide range of human needs from optimized large scale power generation [1-6] to military and remote applications [7-11], to lower power personal electronic devices [12-15]. These alternative technologies often rely on natural renewable resources such as solar power, wind power, and hydroelectric generation. More recently, research has developed pertaining to biomechanical energy harvesting: The generation of power harvested via regular human activity. Like conventional renewable energy sources, this energy can be used to power low-power devices or charge batteries, for uses such as in wearable medical or athletic sensors, personal cellular phones, wearable communications such as blue tooth devices, night vision goggles, flashlights, and many other applications. Bioenergy harvesting is particularly enticing as an area of research because the perpetual, small scale harvesting of energy can help to compensate the increasing battery size, weight, and charge requirements of modern society’s increasing dependence on technology [16]. However unlike conventional energy harvesting, this energy comes at the expense of a human host, and the burden on the user must be taken into deliberate consideration. Ideally, the extracted energy should be negligible compared to the host’s regular activity level (such as self-winding mechanical wrist watches like the Seiko AGS, which generates 5µW on average seemingly without burdening the user during power generation [17]).

As bioenergy harvesting methods are becoming better optimized and understood, research is now beginning to focus on other potential advantages of energy harvesting. While most energy harvesting devices expend the generated energy into a simple resistive bank, the increasing complexity and integration of power electronic loads into the system can allow for more sophisticated applications in the bioenergy harvesting
field. With information gathered from other wearable tech such as rotational encoders, load cells, heat and pressure sensors, and other smart devices, it is now possible to enable research to better understand, adapt, and exploit the relationship between energy harvesters (EHs) and the biomechanics of their hosts. With this capability, the efficiency of energy harvesters could be improved while even opening the possibility to using energy harvesters as assistive devices for rehabilitative purposes.

Section 1.1 provides an introduction to the chapter, Section 1.2 introduces existing energy harvesting research, Section 1.3 outlines the motivations of the ongoing research, Section 1.4 defines the thesis goals and objectives, and Section 1.5 describes the general organization of the subsequent chapters.

1.2 Existing Energy Harvesting Methods

Past research into human driven bioenergy harvesters focuses on extracting the greatest amount of energy from a finite mechanical source. Depending on the type of energy harvester and the power level requirements, this typically involves either determining how to extract energy from very small ranges of motion, such as using mechanical impact or load cells such as through piezoelectrics, or determining how to extract the maximum amount of energy possible from larger motions, such as through limb movement. Some research has been done into the integration of bioenergy harvesters and power electronics, though little research and applications exist beyond simply burning off or storing the energy in a battery.

Note that for the purposes of this work, the background information is extensive and imperative, as the current design iterations depend on previous existing prototypes that have been developed.

1.2.1 Types and Power Ranges of Energy Harvesters

Research can categorize Human Energy Harvesters (HEH) into two divisions: High power harvesters and low power harvesters. High power HEHs have achieved power generation as high as 18W [18], whereas their low power counterparts typically operate in the µW range [19]. A wide variety of HEHs have been designed. Often the foot is targeted as a means of non-invasive energy harvesting. The human body exerts up to 130% of their weight across their foot during heel-strike and toe-off, resulting in a potential 7W of
extractable energy [20]. However extracting the full potential of this energy is limited by the available piezoelectric and capacitive generators, as well as the potentially cumbersome nature of enclosing a foot during normal walking or jogging. Several shoe-mounted devices, their respective mechanisms, and their power outputs, are described below in Table 1-1:

**Table 1-1- Shoe Mounted HEHs and their respective average power levels**

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Average Power Generated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Piezoelectric Heel Strike [21]</td>
<td>342 ± 132mW for a 60kg average</td>
</tr>
<tr>
<td>Variable Shape Piezoelectric Cantilever Beam [22]</td>
<td>0.7W at optimal load</td>
</tr>
<tr>
<td>Sliding Magnet Electromagnetic Generator [23]</td>
<td>8.5mW</td>
</tr>
<tr>
<td>Heel Strike, Various Incorporations [20]</td>
<td>800mW Dielectric Elastomer Heel</td>
</tr>
<tr>
<td></td>
<td>700mW Hydraulic Piezoelectric Actuator</td>
</tr>
<tr>
<td></td>
<td>10mW Piezoelectric Insole</td>
</tr>
<tr>
<td>Linear Permanent Magnet Generator [24]</td>
<td>8.5mW/cm$^3$ walking</td>
</tr>
</tbody>
</table>

In order to increase the amount of power extracted, many HEHs target joint movement, such as the Biomechanical Knee Brace Energy Harvester shown below in Figure 1-1 [25].
Figure 1-1 Biomechanical Knee Brace Energy Harvester

In order to reduce the burden on the user, the knee brace has a goal of *generative braking*. Generative braking targets energy harvesting during negative joint power, which is elaborated upon in Section 1.2.3. When acting only under generative braking, the knee brace generates an average of 4.8W of power, compared to 7W of power in continuous conduction mode, which is a greater burden to the wearer and joint action. The primary drawback of joint targeted energy harvesters is that they generally assume perfectly linear motion of the joint, which is not true in practice, and can impact the biomechanics of walking and the intrusiveness of the device.

An alternative higher power HEH design is to incorporate energy harvesting into a backpack configuration. In order to reduce the cost of energy harvesting on the user, it is beneficial to have the harvester’s centre of mass near the user’s centre of mass, particularly as larger harvesters are typically heavier due to motor/generator combinations [26-27]. However, some backpack designs have been generated which still produce small amounts of energy, which are designed to be incorporated into regular backpacks as part of a diverse energy harvesting scheme, while other heftier models use linear motors or rotary-magnetic generators. A summary of some energy harvesting backpacks and their power production are summarized in Table 1-2.
Table 1-2 Backpack-based Human Energy Harvester designs and their average power output

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Average Power Generated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Piezoelectric Polymer Polyvinylidene Fluoride (PVDF) Straps [28]</td>
<td>45.6mW when loaded at 45kg</td>
</tr>
<tr>
<td>Suspended Load Linear Vertical Movement [29]</td>
<td>7.4W when loaded at 38kg</td>
</tr>
<tr>
<td>Driven Damped Harmonic Oscillator (DDHO) [30]</td>
<td>700W by mechanical testbed stimulation at 167Hz</td>
</tr>
<tr>
<td>Linear Motion Suspended Load [18]</td>
<td>18W by mechanical testbed stimulation</td>
</tr>
</tbody>
</table>

Such high powered energy harvesting devices typically aim to replace or compensate for otherwise large batteries in either daily life situations, or more feasibly for the power output, remote or military applications where the weight of carrying a battery is not viable. Some research indicates that for this condition to be achieved, high power energy harvesters (6-12W) can require upwards of 260 hours of walking to generate the equivalent power provided by a carried battery for an equivalent burden on the user [26]. This indicates that even high power energy harvesters are not an ideal replacement for batteries for short duration trips, however they do have the added benefit of harvesting from an incidental power source, where the user would be expending energy regardless of harvesting or not (particularly if the burden on the user is minimized). This research also encourages insight into how else energy harvesters may be used in novel ways aside from simply trying to garner a maximum amount of energy, such as assistive devices, or rehabilitation therapy. In order to achieve these alternative uses, prototypes must be able to adapt and control the energy harvested from the device, as opposed to simply burning it off through a resistive bank or storing it in a battery. This requires a greater level of integration and sophistication on the power electronics side to enable further research and insight. Other non-mechanical solutions to HEH include body-heat thermoelectric generators (21µW) [31], implantable biofuel cells (20.7µW) [32], and integrated
solar and thermal clothing solutions (500mW) [33] which may all be seen as potentially less invasive energy harvesting devices. It is difficult, however, to harvest large amounts of power without some degree of mechanical integration.

1.2.2 Power Electronics in Human Energy Harvesting

Of the discussed energy harvesters, the majority use a simple resistive bank to measure the power outputted by the energy harvester [22-20, 25-29, 27]. Some designs do make efforts to store the generated energy [18, 24, 34]. Of the examples cited, only one (The Driven Damped Harmonic Oscillator Design) further digitizes the power control method [30] implemented a boost-PFC topology to implement Maximum Energy Harvesting Control (MEHC) over a basic Maximum Power Point Tracking (MPPT) algorithm in order to improve the linear generator efficiency, although testing was limited to a testbed rather than an actual backpack. The simplified PFC and MEHC control scheme is shown below in Figure 1-2.
Alternately, Xingping et al. [34] use an analog boost converter to step up the voltage from a 35mW vibrational power source to a super capacitor for storage. So long as the input voltage is less than that of the storage medium, the device is able to extract energy; however, the specific energy density of a super-capacitor is low when compared to other battery storage mediums despite having a better THD (and depending on the battery type, improved power density) [35-36], and requires a large capacitance. Additionally, although super-capacitors boast lower self-discharge rates than conventional capacitors, they still do not compare to batteries over long periods of time, and the energy harvested would have to be used accordingly [37]. However, the goal of the vibrational power source is to power a sensor, and the supercapacitor is expected to be discharged regularly, so the additional complexity required for battery charging respective to the power generated would be unnecessarily complex. When compared to high power energy harvesters such as the backpack designs, it is more important to have better energy storage capabilities, thus requiring more complex electrical integration.

With this line of reasoning, Guanghui et. al [18] have presented a power electronic circuit designed for a 16W energy harvesting backpack whose output is connected to a SEPIC converter to emulate a resistive

Figure 1-3 Maximum Energy Harvesting Control by means of a Maximum Power Point Tracking algorithm for a PFC boost
load. The energy is subsequently stored in ultracapacitors where it may then be used, or stored in a battery. A SEPIC topology was chosen to eliminate the limitation of the ultracapacitor voltage on the generator voltage while still maintaining usable output power due to the buck-boost topology. The SEPIC converter used a standard PI controller with an analog comparator to ensure linear damping of the system. For this particular example, it was imperative that the backpack never be underdamped under walking conditions in order to avoid excessive displacement of the backpack, thus disregarding the electrical load requirements in favour of the user. The overall control scheme is shown in Figure 1-4.

![Control Scheme of a backpack energy harvesting system with SEPIC converter and battery charging](image)

When the battery pack (BB-2590 Bren-Tronics) is at risk of exceeding its voltage limit, the switched resistive bank is enabled to dissipate excess power in the system. Once the power falls below the threshold, the battery pack is re-enabled. The charging of the battery pack is not otherwise controlled, since the design specifications of the generator have a peak power capability that is far less than the battery pack’s maximum charging power. Unfortunately, the battery pack is very heavy at 3.3lbs, costly, and less practical for a personal wearable device. Requiring 12 continuous hours of walking for a full charge, the battery pack is oversized for the application, and the ultracapacitor energy storage bank is underused [38]. However, while this may seem impractical, there are several advantages to energy scavenging devices which harvest
negative work (the incidental work that humans expend regardless). These can include their remote-accessibility, and their low-social stigma compared to other alternative energy sources such as the aesthetic debates of solar and wind farms.

There has therefore been some research into how to maximize the energy capture of an HEH, and how to subsequently store that energy. Now, research is focusing on how to minimize the energy expended by the user, rather than how to maximize the energy produced and stored. To this end, it is important to consider what and how energy is expended by a human host, and how this changes when loaded. This metric is known as the Cost of Harvest (COH), and is integral to upcoming research in the field of HEHs.

### 1.2.3 Biomechanical Considerations of Human Energy Harvesting and an Analysis of Gait

When considering the design specifications of a HEH, there is one single metric that is absolutely imperative to the field of biomechanics, and that is the concept of a device’s Cost of Harvest (COH). COH is an indication of a harvester’s burden on a user when considered with and without loading (with a base assumed weight applied to the device, most common in backpack energy harvesters). COH is defined by Equation (1-1) [25]:

\[
COH = \frac{P_{met_{elec}} - P_{met_{walk}}}{P_{elec}}
\]  

Where \( P_{met_{elec}} \) is the metabolic power of electrical engagement, \( P_{met_{walk}} \) is the metabolic power of weighted walking, and \( P_{elec} \) is the system’s electrical power. The metabolic cost of a user is determined from the rate of oxygen consumption and carbon dioxide production, which are usually measured using an open respirometry. The COH of bioenergy harvesting devices is typically compared to a metric known as “conventional generation” data, which is defined by harvesting energy through dedicated tasks (such as peddling or typically a hand crank device) as opposed to scavenging energy incidentally. Note that conventional generation follows the COH Equation in Equation (1-2):
\[ COH_{ConventionalGeneration} = \frac{1}{\eta_d \times \eta_m} \]  (1-2)

Where \( \eta_d \) is the device efficacy at the same electrical resistance, and \( \eta_m \) is the peak muscle efficiency of a human when performing positive work (25%) [39]. This provides a standard to which all HEHs may be compared for viability.

Although the COH can be used as an indicator of viability for a HEH device, it does not consider the device’s Cost of Carry (COC), where the weight of the device is considered. Although backpack harvesters aim to reduce this metabolic COC by concentrating the weight near the user’s Centre of Mass (COM) [40], the weight cannot be neglected. However, Equation (1-1) assumes that weight is being carried regardless of whether or not energy is being harvested such as when carrying a loaded backpack. Because every watt of energy produced is generated at the user’s expense, HEH target to have as low a COH as possible, ideally such that the maximum amount of energy harvested does not exceed the negative work available [41].

With respect to bioenergy harvesters, negative work is defined as the work that the body expends in order to slow regular movement, such as during the terminal swing phase of gait when the hamstrings stop the forward swing motion of the lower leg prior to heel strike. This energy can be targeted to reduce the energy spent by a user during exertion, thereby intending to reduce a user’s COH. In this sense, HEHs have the potential to be used as an assistive device, although more sophisticated control techniques are required to this end, as described in the Thesis Objectives. However, it is difficult to determine whether or not a device is seen as biomechanically assistive by the COH alone. A device’s assistive properties are opposed by that same device’s COC during use. This relationship is complex and poorly understood in existing research, due to the uncertainty of to what degree an energy harvester causes co-contraction of a user’s muscles. This co-contraction is an oppositional force to a HEH device. In order to better understand this relationship, a more dynamic resistive profile could be used to burden the user strategically throughout the positive and negative work phases of a user’s gait while minimally impacting existing power extraction schemes. In this spirit, there is a more accurate pertinent metric that can be examined to better indicate an energy harvester’s burden on a user, known as the Total Cost of Harvest (TCOH), defined in Equation (1-3):
$$TCOH = \frac{P_{met_{elec}} - P_{met_{nwalk}}}{P_{elec}}$$  \hspace{1cm} (1-3)

Where $P_{met_{nwalk}}$ is the metabolic power for normal walking. The TCOH better defines how an energy harvester’s COC impacts the user [42, 43, 44].

This research in particular focuses on an energy harvesting backpack that has been designed by the Bio-Mechatronics and Robotics Laboratory (BMRL) operating through Queen’s Department of Mechanical Engineering. The details of the device follow in Section 1.2.4.

### 1.2.4 Prototype: Lower Limb Driven Energy Harvesting Device

A 10W lower limb driven energy harvester (LLDEH) device has been designed, implemented, and tested that utilizes a gear and pulley based backpack to harvest energy from the human walk cycle [44]. A design overview of the device is shown below in Figure 1-5:

![Mechanical configuration of a 10W gear-driven energy harvesting backpack](image)

Figure 1-5 Mechanical configuration of a 10W gear-driven energy harvesting backpack
Two input cables are spooled onto spring-connected pulleys. One end of each cable is attached to a harness on the user’s feet and extend and retract as the user walks at a constant 1.5m/s (5.4km/h, a brisk walking pace) via treadmill. The linear motion of the pulley is amplified by a 5:1 internal gear train which then drives a 3-phase permanent magnet motor. Due to the incorporation of a unidirectional clutch into the generator design, energy is only targeted for extraction during the swing phase of a user’s walk cycle (ie; during a pull). The swing phase of a human gait cycle also incorporates the negative work phase, wherein the user is expending energy to slow their limb, so the device helps to minimize the energy expended by increasing the resistance at this time. This aim of targeting the negative swing phase is coined as “generative braking”, wherein electricity is produced without requiring additional positive muscle power, as the energy is not repurposed into the system and minimal resistance is applied during the stance phase when energy must be expended to accelerate the leg forwards [27]. The stance and swing phase, cable velocity, length, and power are shown below in Figure 1-6.

![Figure 1-6 Cable length velocity and power profile of a gear and pulley based lower limb driven human energy harvester](image-url)
The device typically has a variable high frequency (upwards of 350Hz) 3-phase voltage inside of a low frequency (1-2Hz) envelope indicative of the user’s walk speed and frequency, as shown in the ideal simulation in Figure 1-7. The peak voltage is dependent on the user’s pace and the applied resistance, and varies from 0V-15V with an unloaded average peak per step around 10V at 5.4km/h (1.5m/s). Because the user’s muscular co-contractions are oppositional to the applied resistance, the generator is not an ideal voltage source, and the voltage amplitude is subject to changes when loaded.

![Figure 1-7 Vrms In-In 3-phase simulated input waveform with a 1.5Hz sinusoidal walking envelope with 300Hz inherent generator signal without leg switch interrupt](image)

When fully loaded, the rectified output of the generator is a nearly ideal half sinusoidal waveform, however light load conditions result in a “tail off” while the motor spins freely after release due to the incorporated unidirectional clutch, as shown in Figure 1-8.
During controlled walking, the input source waveform is nearly periodic, barring aberrations in the user’s walking cycle.

Currently, only constant resistances have been tested via a purely resistive load, and at the time of the previous power energy module’s (PEM) development, as described in Section 1.2.5, the mechanical system lagged the electrical system and they were never tested in conjunction with one another. The LLDEH was tested and averaged over ten young healthy male subjects (24±3 years old, 1.78 ±0.08m tall, 75.6±10.4kg) at the Human Performance Laboratory at Hotel Dieu Hospital, Kingston, ON. Each subject was tested for walking, weighted walking, and mechanical engagement (ie; using the energy harvester) following an acclimatization period for kinematics, kinetics, and energetics [44]. The range of resistances determined experimentally were 2.5Ω, 4Ω, 6Ω, 11Ω, and 19Ω were applied, where 2.5Ω is the full load case and most difficult for the user to engage the pulleys (requiring the greatest cable force), and 19Ω is the light or open-load case, where higher resistances were deemed to change the user’s metabolic cost by a negligible amount. The harvester’s COH results are documented in Figure 1-9. The device is compared to two similarly high power energy harvesters, an 18W [18] suspended load backpack, and a 7W knee brace generator [25].
The device’s COH from 19Ω to 2.5Ω ranged from 1.8±5.8 to 3.5±2.1 with a mean of 0.5±2.0 for all trials when considering the mechanical engagement’s metabolic cost and the power generated. These results indicate that the LLDEH generates 1W of electrical power for a consumed 0.5W of metabolic power (averaging all 5 different electrical load conditions), which results in a slightly lower COH than the knee mounted device (0.7) and the suspended backpack (4.8). Figure 1-9 demonstrates that the device acts as an assistive device when loaded at 19Ω and 6Ω respectively, potentially indicating a non-linear relationship between the COH and the COC, where the COH is negative. Although the metabolic variance for the 11Ω loaded case is greater than anticipated, it is within range for the indirect calorimetry measurements[29, 46], and does not affect the anticipated metabolic trend line having used a quiet standing baseline and the same methodology as previous metabolic studies of interest[47-48].

However, as previously discussed it can be deceptive to measure a device’s potentially assistive nature by COH alone. Therefore, the total cost of harvest (TCOH) of the LLDEH is shown in Figure 1-10.
Figure 1-10 Total Cost of Harvest of a 10W gear driven energy harvesting backpack (lower-limb driven energy harvester) compared to comparable devices at similar power levels (18W suspended load backpack, and 7W knee brace generator), from 2.5Ω (full load) to 19Ω (light load).

For the used range of resistance’s, the LLDEH’s TCOH ranged from 4.0±3.6 to 7.7±6.2 with a mean of 6.1±1.6, a significant improvement over the knee mounted device (13.6) and the suspended load backpack (30.7). The device’s impact on the kinematics of walking can be plotted, which is imperative as large deviations in normal walking could cause damage to the user. The kinematics of the LLDEH are shown in Figure 1-11.

Figure 1-11 Kinematics of a gear driven energy harvester on ten averaged subjects. Demonstrates a comparison of the ankle, knee, and hip angle, moment, and power respectively over 19Ω, 11Ω, 6Ω, 4Ω, and 2.5Ω trials.
The device has little impact on the joint kinematics (ankle, knee, and hip) for the 19Ω and 11Ω cases while the ankle and knee joint angle begin to deviate from normal at higher resistances (6-2.5Ω). Despite this, results indicate that the device contributes approximately 7-24% of the total negative work done by the user’s knee during mechanical engagement as the resistance felt by the user increases. A resistance of 6Ω was found to be optimal for the conducted trials resulting in the smallest COH (4.0) without significantly impacting the user’s gait [49]. The user’s required mechanical input power was also lowered from previous iterations of the prototype by reducing the three stage gear ratio of 18:1 to a single stage gear ratio of 5:1.

A photo of the device during data collection is shown in Figure 1-12.

![Diagram of user setup configuration for a gear train lower-limb driven energy harvesting device](image)

**Figure 1-12 User setup configuration for a gear train lower-limb driven energy harvesting device**

### 1.3 Research Motivation

While these efforts have been prototyped to extract and store the maximum available power from an intermittent human energy source, the motivation of the BMRL mechanical lab has shifted somewhat to better focus on reducing the EHs COH or burden on the user, potentially rendering the final system to be as an assistive device. While extracting the maximum available energy is important, it has been proven
that the power can be extracted and stored in a feasibly small PEM, and the current goals have become
three-fold:

1. User-Friendly Implementation
2. Flexible Input Resistance Control
3. Proof of Adaptive Application

1.3.1 User-Friendly Implementation

When the original PEM was developed, the mechanical system lagged the electrical prototype. Because of this, the final integration of the two-systems was minimal, and the only testing achieved on the physical device was that used by the mechanical test rig described in Section 1.2.5. The original adaptive control scheme was coded in TI’s Code Composer Studio (CCS), an integrated development environment (IDE) with an optimized C/C++ compiler. The code was predominantly managed using pre-existing Interrupt Service Routine (ISR) example code provided by Texas Instruments to control the feedback, tuning loops, and peripherals for the DSP[50], ADC [51], CPU [52], System Control Interrupts [53], High Resolution Pulse Width Modulation [54], and Enhanced Pulse Width Modulator [55]. A C/C++ environment can be very obtuse to a non-programmer, and as a development environment requires a relatively sophisticated understanding to code more complex systems without base code. Additionally, debugging in CCS can be a very counter intuitive process, as the functionality of the extraction and plotting of variables are limited, as will be further analyzed in Chapter 3. The research motivation of the Bio-Mechatronics and Robotics Laboratory will in future require a great deal of adaptation of the resistive profile of the PEM, fully exploiting the Variable \( R_{in} \) Control Scheme developed but not incorporated beyond a mapped AC-reference input resistance. This project spans several iterations of both mechanical and electrical components, and a smoother integration of the two processes that can be interpreted both by mechanical and electrical researchers alike is critical. Without this integration, the project stalls in between researchers. As such, this document intentionally aims to be transparent and comprehensive about the electrical integration as to aid future researchers that undertake this work.
1.3.2 Flexible Resistance Control Implementations

The final system aims to implement a variety of resistance control profiles to demonstrate the adaptability of the integration for future development. The demonstrated control schemes include constant resistance, threshold resistance, a Ramp and Hold function, an Optimized Resistance algorithm, and a Power Regulation control scheme. The versatility of using MATLAB Simulink’s Embedded Coder implementation allows for the fast and adaptable development of new control schemes with minimal and intuitive debugging.

1.3.3 Proof of Electrical Adaptability

The current iteration of the mechanical LLDEH has more sophisticated feedback, including an integrated encoder on the motor, and a second for the lead leg. The proposed research by the BMRL aims to use this feedback data to better understand and exploit the biomechanics of walking. As such, the Variable R_in Control scheme described in Chapter 2 was targeted to be used and developed to use data other than simply the input voltage or power metrics in order to change how and when a user’s desired resistance profile changes. This information is exploited for all variable resistance control schemes, including constant and threshold resistance applications, as a voltage threshold is impractical on a non-ideal voltage source. This thesis then further proposes to demonstrate the adaptability of these profiles on a low-capacitance boost converter, as well as on a voltage controlled attenuator, to demonstrate that the developed control scheme can be adapted to other electrical configurations.

1.4 Thesis Objectives and Contribution

The objectives of this thesis are:

1) To integrate the Variable R_in Control Scheme into a more user-friendly and adaptable format than raw CCS coding.

2) The design, development, and test several dynamic emulated resistance profiles using encoder feedback from the actual mechanical prototype.
3) To test the system for adaptability on a linear regulator and low-capacitance boost converter as a proof of concept for versatility.

1.5 Thesis Organization

Chapter 1 introduces a summary of energy harvesting, power electronics in the energy harvesting industry, as well as an overview of the existing mechanical and electrical research that has been completed on a lower-limb driven energy harvesting backpack completed by the Queen’s Bio-Mechatronics and Robotics Laboratory. Chapter 1 additionally gives a brief overview of the thesis objectives and necessary project goals of this work.

Chapter 2 reviews the principles of operation of a boost converter, the existing research done for maximum energy capture boost-buck converter with battery charging, and introduces the adapted design and tuning considerations.

Chapter 3 introduces the digital control software and hardware selection, digital considerations that extend beyond their analog implementation, as well as the resulting experimental results for the constant input resistance and threshold input resistance control schemes, having coded the device via the selected software.

Chapter 4 introduces the additional proposed variable input resistance control schemes as well as their prototyping and experimental test results. Chapter 4 also includes a description of the relevant optical encoder implementation.

Chapter 5 demonstrates the design implementation’s versatility on a low capacitance boost converter. It additionally examines the operating principles of a linear regulator, and the tuning implementation.

Chapter 6 summarizes the thesis contributions and findings and provides insight into possible future improvements and additions to this work.
Chapter 2
Application and Research Adaptation

2.1 Introduction

The research conducted for this thesis is an improvement and adaptation of a previous power energy module (PEM) prototype which focused on harvesting the maximum available energy from a human energy source developed at Queen’s University. While the previous prototype operated on the original prototype of the LLDEH, the prototype was used as a basis for this research’s development presuming by default that the user still wishes to capture all available energy, which is desirable as examined in Chapter 1. Chapter 2 examines the operating principles of a boost converter, why it is desirable for energy harvesting applications, and then documents the examined tuning methods investigated for the new adapted prototype. The additions and alterations of the previous PEM prototype are also included.

Section 2.1 provides an introduction to the Application and Research Adaptation chapter, Section 2.2 describes the principles of operation of a boost converter, Section 2.3 elaborates on relevant previous existing research within the Bio-Mechatronics and Robotics Laboratory and Queen’s Power Group for this ongoing project, Section 2.4 Introduces the new adapted power module and its tuning considerations, and Section 2.5 concludes the chapter.

2.2 Boost Converter Principles of Operation

A boost converter is a DC-DC switching converter that is widely used in power systems, characterized by an increased voltage at the output compared to the input terminal. This is achieved using an inductor at the input terminal, an energy storage capacitor in parallel with the load, and two switches. A very simplified boost converter is shown in Figure 2-1, following rectification of the 3-phase input AC signal, and without parasitics or sense resistors.
Figure 2-1 Simplified boost converter topology

When current flows through the input terminal at $V_{\text{rect}}$, it has two path choices at the drain of the control MOSFET. Which path it takes depends on the MOSFET’s on or off state, which either allows current to flow through the switch, or opens the MOSFET path, directing the current to flow through the output parallel RC bank. These on-off states can be analyzed in their equivalent circuits and define how a boost converter behaves during switching operation. The selected design uses a simple diode for the high side switch, whereas a power MOSFET is used for low-side switching and controlled by the output of a microcontroller’s (MCU) pulse width modulation unit. A square-wave pulse signal turns the power MOSFET on and off at the gate. When the square wave is high for the first time, the switch conducts and the inductor stores energy from the rectified input voltage, $V_{\text{in}}$, as seen in the simplified on state equivalent circuit in Figure 2-2 (parasitic elements are not included). Because the MOSFET has a nearly negligible on-state resistance, the power flows preferentially through it to ground instead of following the load path.
When the switch is on and conducting, the circuit dynamics are as follows [56]:

$$\frac{dI_L(t)}{dt} = \frac{1}{L} (V_{in} - I_L(t)r_f)$$  \hspace{1cm} (2-1)$$

$$\frac{dV_C(t)}{dt} = -\frac{V_{out}}{C R_{load}}$$  \hspace{1cm} (2-2)$$

Where $I_L(t)$ is the inductor voltage, $L$ is the inductance, $V_{in}$ is the input voltage, $r_f$ is the inductor’s parasitic resistance, $V_C(t)$ is the capacitor voltage, $V_{out}$ is the output voltage, $C$ is the capacitance, and $R_{load}$ is the load resistance. In this initial state, Equation (2-2) begins at zero and is not dissipating, as the capacitor has no initial charge.

When the gate signal is then driven low, the rapid increase in resistance of the system causes a back e.m.f in the inductor, which resists the sudden change in current, and which attempts to keep the current flowing at the same rate. This results in a boosted voltage at the load of $V_{in} + V_L$. The diode only allows current to flow in one direction (with a small threshold voltage drop, a Schottky diode given $V_f=490mV$ is used to minimize this effect), and allows the Capacitor to charge while in this mode of operation. This state is demonstrated in Figure 2-3.
When the switch is off, the system behaves as follows [56]:

\[
\frac{dI_L(t)}{dt} = \frac{1}{L}(V_{in} - I_L(t)r_{esr} - V_o)
\]

\[
\frac{dV_C(t)}{dt} = \frac{1}{C}(I_L(t) - \frac{V_{out}}{R_{load}})
\]

Where regardless of the switch state, the following is true:

\[
V_o(t) = r_{esr}C \cdot \frac{dV_C(t)}{dt} + V_C(t)
\]

Where \(r_{esr}\) is the parasitic resistance of the capacitor (equivalent series resistance, ESR).

When the switch again drives high and the MOSFET begins to conduct again, the inductor stores energy once more. This time, however, the capacitor holds a charge which is discharges to the load. The diode prevents the capacitor from discharging to the inductive branch and operates in reverse bias as an open switch, as shown in Figure 2-4.
In this way, the load continues to be supplied with a voltage of $V_{in} + V_L$ without discontinuity. A boost converter’s mode of operation is defined as either being in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), where each operating mode requires different control [57]. CCM and DCM are terms used to identify what is happening to the input, or inductor, current, $I_L$. In CCM, current flows continuously through the inductor during a complete switching cycle, whereas in DCM the inductor current ramps up and discharges completely to zero. If the inductor current only just discharges to zero before ramp up, the mode of operation is known as Critical Conduction Mode (CrCM), which is a specific enforcement of CCM operation. The difference is illustrated in Figure 2-5.
In a typical boost converter operation, the output voltage, $V_{in} + V_L$, is regulated, however this scheme is adapted to instead regulate the input current, thereby dynamically changing the loading felt by the user.

Generally, high power boost converters are designed to operate in CCM while lower power solutions operate in DCM. Although this application might be considered to be of a lower power, CCM allows for lower peak currents throughout the circuit, which is desirable for this particular application, and has lower losses as a result, however CCM can require large on-times compared to a DCM counterpart. Current mode boost converters are often operated in CCM. When attempting to follow an average current reference (to calculate the required electrical input resistance), it is anticipated that a simplified CCM and DCM waveform will behave as shown in Figure 2-6.

![Figure 2-6 Simplified CCM (Left) versus DCM (Right) at follow a reference current (dotted line)](image)

The inductor’s resulting current ripple is generally designed to be 20-40% of the average input current. This allows for a lower peak current, which also results in lower turn-off loses. Conversely, CCM control is worse in that its MOSFET turn on losses are worsened by the boost rectifier’s recovery losses, which is why Schottky diodes are preferred to minimize this effect [58]. The pertinent currents and voltages during CCM operation are shown in Figure 2-7 [59].
Figure 2-7 Switching Waveforms of a CCM boost Converter

It is observed that the inductor current can be divided into the MOSFET current and diode currents respectively, assuming perfect switching. The drain voltage is zero when the MOSFET is on (conducting) because the voltage at the top of the switch is being tied to ground, resulting in the inductor-only path of Figure 2-2. Assuming ideal switching without parasitics, the boost converter’s switching duty cycle \( D_{CCM_{ideal}} \) is defined by Equation (2-6) [60], where the converter sinks more current when the switch is on, and less current when it connects to the load and the switch is off.

\[
D_{CCM_{ideal}} = 1 - \frac{V_{in} \cdot \eta}{V_{out}}
\]  
(2-6)

Where \( \eta \) is the converter’s efficiency, for which a boost converter is experimentally at worst 80%. The boundary condition between CCM and DCM in a boost converter can be defined by a critical inductor value, known as the critical inductor conduction parameter, \( K_{crit} \), or can be given as the critical value of the load resistance, \( R_{crit} \), which is more intuitive for emulated load purposes [61].
\[ K_{\text{crit}} = \frac{2 \times L \times f_{\text{sw}}}{R} = \frac{R_{\text{nom}}}{R} \]  \hfill (2-7)

\[ R_{\text{crit}} = \frac{R_{\text{nom}}}{K_{\text{crit}}} \]  \hfill (2-8)

\[ R_{\text{crit}}(D) = \frac{2L}{D(1-D)^2 \times T_{\text{sw}}} \]  \hfill (2-9)

Where \( f_{\text{sw}} \) is the converter’s switching frequency, \( T_{\text{sw}} \) is the converter’s switching period, and \( R_{\text{nom}} \) is the converter’s nominal load resistance for second-order PWM converters.

The important note to take away is that depending on the system’s tuning parameters, the DCM boundary for the desired CCM converter is dependent on the selected inductance, \( L \), as well as the regulated duty cycle, \( D \), and switching period, \( T_{\text{sw}} \), where the converter is most susceptible to DCM at light loads potentially resulting in crossover distortion issues. These design factors must be considered when designing a boost converter for CCM operation, and are critical for the inductor selection, as outlined in [60].

When in CCM mode, the inductor current is modelled as in Equations (2-10) and (2-11), regardless of whether or not the switch is on or off at time \( t \):

\[ I_{L_{\text{max}}} = I_{\text{in}} + \frac{1}{2} \Delta I_{L} \]  \hfill (2-10)

\[ I_{L_{\text{min}}} = I_{\text{in}} - \frac{1}{2} \Delta I_{L} \]  \hfill (2-11)

Where \( I_{L_{\text{min}}} \) is the valley, and \( I_{L_{\text{max}}} \) is the peak, and \( \Delta I_{L} \) is the variation in the current over the switching period [62].

The designed boost converter components have been selected to operate in CCM mode, which affects the necessary tuning. Ultimately, the designed average current mode boost converter topology is operating as what is known as a Power Factor Correction (PFC) circuit.
As a variety of PFC converter, it is important to understand the concept of power factor correction, which is the ratio of average power to apparent power for an AC terminal. Power factor is an important measure of a system’s efficiency, as a system with a low power factor will draw more current than a load with a higher power factor for the same amount of usable energy, and accommodates lower component power ratings.

\[
PF = \frac{\text{Average Power}}{\text{Apparent Power}} = \frac{\text{avg}[v(t) \times i(t)]}{V_{\text{rms}} \times I_{\text{rms}}} = k_d \times k_\theta
\]  

(2-12)

Where \(V_{\text{rms}}\) is the root-mean-square voltage at the input terminal, \(I_{\text{rms}}\) is the root-mean-square current at the input terminal, \(k_d\) is a distortion factor, and \(k_\theta\) is the displacement factor. If both are in balance and equal to one, then the input current follows the shape of the input voltage perfectly, and the power usage is efficient. Compared to a buck converter, a boost converter is better suited for PFC functionality as the inductor current achieves a smaller ripple current, allowing for easier average current mode control (ACMC) [63]. In the case of the adapted variable adaptive gain PFC boost converter, the current reference to be tracked is the current value that provides the intended resistive load on the user. AMC has several advantages, one of which being that is does not require the need for slope compensation as peak and valley current control modes do, while also benefiting from excellent noise immunity and adaptability compared to buck and flyback topologies. [64].

2.3 Previous Research: Power Electronics Module with Battery Charging

Having investigated several previous control methods attuned to energy harvesting devices, previous research was conducted through Queen’s Power Group (QPG), and the BMRL lab via Queen’s Mechanical Engineering Department which sought to develop a power converter that could store the peak power generated by the HEH while maintaining a reasonably sized battery to reduce the load on the user [38]. The energy extracted from the system was determined according to the user’s desired power profile (offering more flexibility than the previously investigated methods), and the stored energy was required to remain within the charging limitations of the battery.
The original iteration of the PEM was designed to accommodate a three stage gear ratio of 18:1, which was later revised to a single stage 5:1 ratio, resulting in slight variations in the anticipated voltage ratings (From a per step peak voltage of 20-10V approximately), while providing a theoretical improved mechanical efficiency of 8.5% without impacting the device’s biomechanical profile as the constant resistances used were identical [65].

To capture and store the entirety of the energy produced from this intermittent human energy source, a two stage boost-buck power electronics module (PEM) was designed and prototyped. A load resistance was emulated by the first stage of the device by forcing the input current to follow a programmed current reference, which correlated to a required resistance in the range of 2.5Ω to 19Ω. The second stage was used to regulate the voltage and charging current of the 2000mAh Lithium Polymer Battery (LPB) pack using two cells with a nominal voltage of 7.4V holding 14.8Wh of energy storage. The original prototype for the LLDEH could generate approximately 53W at peak power for a short time, so the excess energy was stored in and released by a 2200µF Energy Storage Capacitor (ESC) placed in between the two stages so as to not waste the peak power produced. The PEM with an ESC basic design is shown below in Figure 2-8.

![Power Electronics Module Diagram](image)

Figure 2-8 Two-stage power electronics module with energy storage capacitor, designed for a lower limb driven energy harvesting backpack
The two-stage PEM operated at a switching frequency of 250kHz and was digitally controlled using a Texas Instruments (TI) C2000 TMS320F2808 Digital Signal Processor (DSP) coded in Code Composer Studio (CCS). The components of the power stage boost converter were designed to operate in continuous conduction mode (CCM), and the schematic and printed circuit board (PCB) was designed with Altium Designer 10 and debugged in-lab given the following design parameters: \( V_{in} = 0 - 35 \text{Vrms} \) with an envelope frequency changing from 0 - 2 Hz. The boost output voltage is not regulated. With the \( R_{in} \) control range, \( V_{boost} \) will change from 6V to 80V, given \( f_{sw} = 250\text{kHz} \), \( L_{boost} = 180\mu\text{H} \), \( C_{\text{Energy Storage Capacitor}} = 2200\mu\text{F} \), \( R_{sense} = 0.02 \Omega \), \( I_{in} = 0-4\text{A} \), \( P_{\text{inpeak}} = 140\text{W} \), \( P_{\text{avg}} = 15\text{ W} \).

The boost converter control scheme was modified to control the inductor current rather than regulate the output voltage, and was modified to incorporate three basic control schemes: Constant \( R_{in} \) Current Control, Variable Threshold \( R_{in} \) Control, and Dynamic \( R_{in} \) Control. The differences between a conventional PFC boost and the prototyped boost converter are outline in Table 2-1.

**Table 2-1 Comparison between conventional PFC and prototyped \( R_{in} \) controlled boost converter**

<table>
<thead>
<tr>
<th>Control Parameter</th>
<th>Conventional PFC</th>
<th>Energy Harvesting Boost Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>( V_{out} )</td>
<td>( R_{in} )</td>
</tr>
<tr>
<td>Regulated</td>
<td></td>
<td>Unregulated</td>
</tr>
<tr>
<td>Input Frequency</td>
<td>60Hz</td>
<td>1-2Hz</td>
</tr>
<tr>
<td>( \text{Seen by Source As} )</td>
<td>Emulated Resistor defined by ( V_{out} )</td>
<td>Emulated Resistor defined by User</td>
</tr>
</tbody>
</table>

The boost converter was digitally implemented using a difference equation tuned by a two-pole two-zero compensator using voltage adaptive gain designed using MATLAB’s SISO design toolbox. The compensated Bode plot including variable adaptive gain controller, achieved an increase in the bandwidth at \( V_{boost} = 10V \) from 1.06 kHz to 11.8 kHz with a phase margin of 79.3 degrees. The variable gain compensator can achieve a turn on time of 5.7 ms under the operating conditions \( V_{\text{rect}} = 5V \), \( V_{\text{boost}} = 10V \).
The differing control schemes and their control motivations are outlined in Figures 2-9 through 2-11.

Figure 2-9 Emulated Constant $R_{in}$ control scheme for a two stage PEM

Figure 2-10 Emulated Voltage Threshold $R_{in}$ control scheme for a two stage PEM

Figure 2-11 Emulated Variable $R_{in}$ control scheme for a two stage PEM

The prototyped boost stage was connected to a constant voltage 1-2Hz AC generator and the outputs for the threshold and variable input resistance schemes are demonstrated in Figure 2-12.
Similarly, the device was fed a mapped variable resistance profile to emulate, however no additional mechanical feedback was integrated. The demonstrative variable resistance profile is shown in Figure 2-13:

Using the constant $R_m$ control scheme, the boost converter’s efficiency was measured to have a peak efficiency of 93% for an emulated resistance of 40Ω.

The purpose of the subsequent buck converter stage was to minimize the energy stored in the ESC and to regulate the charging current to the lithium polymer battery pack, as to not exceed the maximum Charging Current (ChC). This was necessary to prevent the ESC voltage from maxing out, which would require
energy dumping (Via a reduction of the input power through resistive control) as to not damage the components. This would also have been counter-productive to the goal of capturing all available energy from the human energy source. To this end, the energy stored in the ESC was minimized by regulating the voltage of the capacitor to a minimum voltage of $V_{\text{boost min}}$, where the instantaneous $P_{\text{in}}$ must be less than $P_{\text{out}}$ for the buck to effectively regulate the through power, and $P_{\text{out}}$ varies with the State of Charge (SoC) of the battery pack. This control was achieved using a Maximum Energy Extraction and Charge Control Scheme (MEECC), adapting to the Li-Po battery pack’s two modes of charging: Constant Voltage (CV) and Constant Current (CC). These charging modes were controlled using a two-loop controller with both a current and a voltage loop. Unlike with solar cells, the maximum energy extraction in this context refers to the maximum energy available for any inputted user power source, as energy harvesters have a non-fixed Maximum Power Point (MPP). The control of the buck power scheme was experimentally verified given the following design parameters: $V_{\text{in}} = 6 - 80\text{V}$, $V_{\text{out}} = 5 - 8.4\text{V}$, $f_{\text{sw}} = 250\text{kHz}$, $L_{\text{Buck}} = 150\mu\text{H}$, $C_{\text{Buck}} = 90\mu\text{F}$, $R_{\text{sense}} = 0.02\ \Omega$, $I_{\text{out}} = 0 - 4\text{A}$ (limited to 2A when used with 2000mAh battery pack), $P_{\text{outpeak}}=16.8\text{W}$ $P_{\text{avg}} = 15\ \text{W}$. The same TMS320F2808 DSP that was used for the boost converter was also used for the control of the buck converter. Figure 2-14 demonstrates the buck converter charging the batteries when the generated power is less than the average output power, ($P_{\text{in}} < P_{\text{out}}$). The experimental parameters are as follows: $V_{\text{in}}=17.6\ \text{V peak}$, $f_{\text{in}}=1.85\ \text{Hz}$, $R_{\text{in}}= 24\ \Omega$, $I_{\text{in}}=0.8\ \text{A peak}$, $P_{\text{inmax}}=14\ \text{W}$, $P_{\text{inavg}}=3.2\ \text{W}$.

![Figure 2-14 Buck Charging where $P_{\text{in}} < P_{\text{out max}}$, Top: Boost converter input current, Second from top: Boost converter input voltage, Second from bottom: Battery voltage, Bottom: Battery charging current.](image-url)
Figure 2-15 demonstrates what occurs when the input power is increased and the instantaneous input power exceeds the peak output power, given an emulated resistance of 16Ω and a peak battery charging current of 2A. In this case, the battery is expected to be charging at the peak 2A ChC rate and that the ESC is being used to store the excess energy.

![Battery charging in CC mode with higher P\textsubscript{in}](image)

**Figure 2-15 Battery charging in CC mode with higher P\textsubscript{in}.** Top: Boost converter input current, Second from top: Boost converter input voltage, Second from bottom: Battery voltage, Bottom: Battery charging current.

The buck converter’s DC efficiency was measured in CC charging mode and was found to have a peak efficiency of 93.7% for an emulated input resistance of 20Ω at an input power of 18W.

The ultimate power flow of the combined boost-buck PEM can be summarized in Figure 2-16 [38].

![Power Flow Diagram](image)

**Figure 2-16 High level power flow diagram [38]**
Finally, a mechanical test rig was constructed to replicate the anticipated power profile generated, achieved by rectifying an 3-phase AC generator and coupling it with the DC motor used in the mechanical prototype, which was still under development at the time. The test rig was fed a $V_{in}=25\text{V}$ with an average $9\text{W}$ produced at $1.5\text{m/s}$ walking speed for a constant emulated input resistance. The preliminary results are shown below in Figure 2-17.

![Figure 2-17 Constant R\textsubscript{in} control on a calibrated test rig, designed to mimic the feedback and voltage profile of the energy harvester](image)

Integrated tested at the time was minimal as the mechanical prototype was not yet complete. The LLDEH has since undergone several revisions requiring some small adaptation of the original PEM.

### 2.4 Adapted Boost Converter Design

In order to achieve the desired goals outlined in Section 1.3 the two-stage PEM that was previously developed was redeveloped and adapted to better suit the current needs of the development team’s research. This section begins a presentation of the new research conducted based on the previous section’s work. Although it is important to gather the energy generated by a human walking, the BMRL has focussed new areas of research into examining how, instead of increasing the power output of the LLDEH, they can instead reduce the impact of the device on the wearer for every watt of power produced (ie; a reduction of
the COH and TCOH as defined in Equations (1-1)-(1-3)). The details of this necessary control scheme are outlined in Section 2.3. Since the original PEM, the new LLDEH now has a single stage gear ratio of 5:1 compared to the previous three stage ratio of 18:1, the reduction of which increased the mechanical efficiency of the device by 8.5% without impacting the effect on the user [65]. The BMRL made all changes to previous iterations with the constant goal of maintaining an approximate output power of 10W for consistent comparison, however the new gear train ratio now results in an average voltage peak per step of 10V, compared to closer to 20-35V pk-pk in the first prototype. In order to maintain the capability of storing all of the generated energy, the boost converter was isolated from the buck and charging stages, and the high-side MOSFET was replaced with a simple Schottky diode to simplify control for testing purposes while experiencing a minimal voltage drop at the output. The load, instead of a buck converter, was initially replaced with a 100W 20Ω heat-sunk resistor, although it was later revised to a 100Ω resistor to improve the light-load functionality, as examined in Section 3.7. The board used for testing was the second iteration of the boost converter board to improve the current sensing which was unreliable due to long signal sensing paths and poor Current Sense Amplifier (CSA) performance. The second board was also designed so that a linear regulator could be more easily integrated, and so that input and output current sensing on an oscilloscope would be easier without interrupting the load path. The final prototype also integrated the motor and leg encoders, as well as the required line receiver for the former, eliminating a 25ft cable that had been used in conjunction with an off-board ADC whose functionality can be replaced by the selected DSP.

As before, the input to the system is an intermittent human-driven power source. The generator voltage output has a variable high frequency 3-phase component around 300-350Hz, which experimental data shows is close to 320Hz at its peak. This signal is within a low frequency 1-2Hz 10-15V rectified AC wave envelope, as seen in Figure 1-6, which varies as the human subject walks at 1.5m/s (5.4km/h). The motor used is a brushless two pole-pair Maxon EC-4-Pole 3-Phase 305015 [66]. The final utilized components based on the boost converter design criterion for CCM operation [60] have again been adhered to with the
final component selection seen below in Table 2-2, with the final boost converter design weighing a total of 197g including the DSP and boost converter.

Table 2-2 Boost converter component selection

<table>
<thead>
<tr>
<th>Component</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor</td>
<td>PCV-2-184-05L</td>
<td>Coilcraft</td>
<td>180μH, 4Arms, Dc 0.092Ω</td>
</tr>
<tr>
<td>Energy Storage Capacitor</td>
<td>ECO-S1XA222BA</td>
<td>Panasonic</td>
<td>2200μF, 80V</td>
</tr>
<tr>
<td>Control MOSFET</td>
<td>NTD6416ANT4G</td>
<td>ON Semiconductor</td>
<td>100V, 17A, Rds 81mΩ</td>
</tr>
<tr>
<td>DSP</td>
<td>TMS320F2808</td>
<td>Texas Instruments</td>
<td>C2000 Standard</td>
</tr>
<tr>
<td>Rectifier/High Side Diodes</td>
<td>SSB44-E3/52T</td>
<td>Vishay Semiconductor</td>
<td>40 V, 4 A Vf=490mV</td>
</tr>
<tr>
<td>Op Amp</td>
<td>OPA2335AIDR</td>
<td>Texas Instruments</td>
<td>GBW 2 MHz</td>
</tr>
<tr>
<td>Sense Resistor</td>
<td>311-.10PCT-ND</td>
<td>Yageo</td>
<td>100mΩ Current Sense</td>
</tr>
<tr>
<td>Decoupling Capacitor</td>
<td>1276-1443-1-ND</td>
<td>Samsung</td>
<td>1µF</td>
</tr>
<tr>
<td>Driver</td>
<td>LTC4444IMS8E-5#PBF</td>
<td>Linear Technology</td>
<td>114 V Bootstrap, 1.4 Amp</td>
</tr>
</tbody>
</table>
The boost converter schematic is illustrated in Figure 2-18 with parasitic components.

![Boost Converter Schematic](image)

**Figure 2-18 Boost converter components design**

### 2.4.1 Tuning and Stability

There are a multitude of ways to tune a converter. One method is to look at the converter’s Open Loop Transfer Function to determine the inherent stability of the system, and then to design a corresponding compensator either via Bode Plot or Root Locus design which meets the required criteria. For an ACMC PFC boost, the most commonly used compensator types are the PI controller, and the 2-pole-2-zero (2P2Z) compensator. This section will analyze the particular difficulties in tuning a current-mode boost converter. Stability begins with the Open Loop Transfer Function. When in CCM the linearized open loop uncompensated power stage $G_{id}$ without parasitics can be defined by Equation (2-13):

$$
G_{id}(s) = \frac{i}{d} = \frac{2 \times V_{out}}{R_{Load} (1 - D)^2} * \frac{1 + \frac{sR_{Load}C}{2}}{1 + \frac{sl}{R_{Load} (1 - D)^2} + \frac{s^2LC}{(1 - D)^2}}
$$

(2-13) [63]
With a high frequency approximation given by:

\[
G_{id}(s) = \frac{\bar{i}}{\bar{d}} = \frac{V_{out}}{Ls + R_{Load}} \tag{2-14} [63]
\]

Where \(R_L\) is the equivalent resistance of the current path. The small signal power stage model of an average current mode boost converter, \(G_{pboost}(s)\), including parasitics, is shown in Equation (2-15) [38], which is used as the basic for the compensated Bode plot in Figure 2-8, derived from small signal modelling [67].

\[
G_{pboost}(s) = \frac{\bar{G}_d}{\bar{d}} = \frac{s.C_{boost}V_{boost}(1 + r_{esrR_{Load}}) + l_Lr_{esr}(1-D) + 2.l_L(1-D)}{s^2.L_{boost}C_{boost}(1 + r_{esrR_{Load}}) + s(L_{boost}/R_{Load} + C_{boost}(R_f(1 + r_{esrR_{Load}}) + r_{esr}(1-D)^2)) + (1-D)^2 + r_fR_{Load}} \tag{2-15}
\]

Where \(r_f\) is the inductor’s parasitic resistance, and \(r_{esr}\) is the boost capacitor’s parasitic resistance. This transfer function exhibits two poles, one ESR zero, and most importantly, one Right-Half-Plane-Zero (RHPZ) described by [68]:

\[
\omega_z = \frac{1}{r_{esr} * C} \tag{2-16}
\]

\[
\omega_{RHPZ} = \frac{R_{Load}(1-D)^2}{L} \tag{2-17}
\]

\[
f_{RHPZ} = \frac{R_{out}}{2\pi * L} \left(\frac{V_{in}}{V_{out}}\right)^2 = 3.1kHz \text{ at full load, peak voltage} \tag{2-18}
\]

Where \(\omega_z\) is the frequency of the first zero in rad/s, and \(\omega_{RHPZ}\) is similarly the frequency of the RHPZ.

The existence of the RHPZ, occurring when the boost converter is operating in CCM, and is caused by the lack of continuous current flow to the output, regardless of which model of compensation is being used [69]. While this pole provides a gain increase, it also causes a phase lag. While using current mode control does eliminate the inductor pole present in voltage control mode and eliminate the need for a compensation
ramp to remove subharmonic oscillation instability, it does not remove this RHPZ. Equations (2-17) and (2-18) demonstrate that the value of the RHPZ shifts with respect to the input voltage and loading by emulated resistance, necessitating the need for a variable adaptive gain term, where the DC gain of the system for the variable adaptive gain can be derived as:

\[
DC \text{ Gain} = \frac{2 \cdot I_L(1 - D)}{(1 - D)^2} = \frac{2 \cdot V_{\text{boost}}}{R_{\text{in}}}
\]

(2-19)

Where the system compensates linearly for the large span of input voltages to the system without adversely affecting the compensator’s bandwidth, as discussed in Section 2.3. For average current model control, control systems generally implement integral and lead lag control, however a two pole two zero compensator allows for improved control performance. This Type II compensator designed for the system can be expressed as a difference Equation:

\[
U(n) = A_1 \cdot U(n - 1) + A_2 \cdot U(n - 2) + G_{\text{adp}}(B_0 \cdot E(n) + B_1 \cdot E(n - 1) + B_2(n - 2))
\]

(2-20)

Where \(G_{\text{adp}}\) is normalized to \(V_{\text{BoostMax}} \cdot (V_{\text{Boost}})^{-1}\), or in the designed case, \(80 \cdot (V_{\text{Boost}})^{-1}\). Equation (2-20) may alternately be converted to a state space Equation, or flow chart in Simulink as necessary.

When designing a compensator for the digital domain it is important to consider the effect of the signal conditioning, Sample and Hold delays, digital delays, and conversion delays on the system. Unlike an analog control, these introduce phase margin reduction to the system that can invalidate control methods that would otherwise be functional in an analog topology [70]. The system is introduced to these delays as shown in Figure 2-19.
Figure 2-19 Discretization and Digital Control of a PFC boost converter’s feedback path

Where $K_d$ takes the ADC and current sensing gain into account, and $H_c$ takes the PWM’s Zero-Order-Hold (ZOH) Sample and Hold computation delay of $T_d/2$ into account (this is enforced within the program itself).

The Sample and Hold delay can be described by:

$$SH(s) = \frac{1 - e^{-sT_s}}{s}$$  \hspace{1cm} (2-21)

Thereby introducing an additional phase lag of $180^\circ f/f_{sw}$ where $f$ is the bandwidth where the phase is calculated. The time delay between the ADC sampling instant and the next PWM update is denoted by the $H_c$ block, where:

$$H_c = e^{-sT_d}$$  \hspace{1cm} (2-22)

Where $T_d$ is the time delay. $T_d$ is enforced by controlling how and when the PWM unit updates, so the combined plant Equation to be compensated is given by:

$$G_{pBoost}(z) = Z\left[\frac{1}{s}(1 - e^{-sT_s}).H_c(s).G_{pBoost}(s).K_d\right]$$  \hspace{1cm} (2-23)
Where the order of the final system is sensitive to changes in $T_d$. $T_d$ is maintained at a value of $T_s/2$ to result in a three-pole, two-zero system, to be compensated by a Type II two-pole two-zero compensator designed in the digital domain using MATLAB’s SISO tool. A compensated full load design tuned for a switching frequency of 250kHz, an output load of 100Ω, and an input voltage of 15V loaded at 2.5Ω using a two-pole two-zero compensator is shown below in Figure 2-20. The Figure is shown at full load over the full 15-80V boost range without the adaptive gain value, $G_{adp}$.

![Bode Diagram](image)

**Figure 2-20 Compensated Open loop Bode plot of a full load PFC boost converter without variable adaptative gain for a varying boost voltage**

The DC gain variation discussed in equation (2-19) migrates as the output voltage varies. This can affect the crossover frequency, and therefore the system stability. There is some variation in the poles and zeros of the system which experience some drift. The system should be compensated such that the crossover...
frequency bandwidth and phase margin are beyond this DC variation. The Bode diagram in Figure 2-21 demonstrates the same full load condition with the variable adaptive gain factor, $G_{adp}$ added.

![Bode Diagram](image)

**Figure 2-21** Open loop Bode plot of a full load PFC boost converter with variable adaptive gain for a varying boost voltage

Switched mode power converters often use either PI (lead-lag), two-pole-two-zero (2P2Z), or three-pole-three-zero (3P3Z) feedback compensation for their current and voltage loops. If both loops exist in the system, the faster current loop must have a higher bandwidth than the voltage loop in order for the system to have good performance. However the current loop is the more stable of the two, and can generally be compensated by a simple PI controller [71] [72]. In this case, a 2P2Z (Or, Type II compensator, aka a digital biquad filter) has the advantage of being a PI controller plus a low pass filter allows for better handling of integrator saturation, which negates any error accumulation that might be inherent for PI control. However, in its 2P2Z form, the integrator saturation is difficult to apply, so Bode plot manipulation
for a PI solution may be preferred for user accessibility. Whereas a 2P2Z compensator should be implemented using either a discrete equation form, or state-space equations, the PI controller can be easily modelled and interactively tuned without significant change to the matrices. It is relevant to note also that Simulink contains a C2000 DMC block for PI(D) control with an additional integrated Integral Accumulation Error term that can be exploited similarly, as is discussed in Chapter 3. MATLAB’s pidtool can be used for this design similarly, or Bode plot design using a pole-zero combination can be designed, so long as the open loop control to duty cycle transfer function of the system has a) A phase margin of greater than 0 degrees (At least 45, or better yet 60 or greater), and b) Compensator eigenvalues where any right half plane zeroes in the system, are above the crossover frequency as their compensation can be tedious, particularly with the shifting RHPZ resultant from a wide voltage range (while the variable adaptive gain compensates the gain, particularly for low-frequency operation, the peaks and Q value of the Bode plot can shift at light loads or low voltage conditions as seen in Figure 2-21. A 2P2Z compensator can be implemented in MATLAB either by being converted to its state-space format (using MATLAB’s ss() function from the compensator’s exported discrete transfer function), or can be implemented as a block-diagram workflow in its direct form implementation where the gain values correspond to their equivalent values in Equation (2-20), and 1/z denotes a discrete delay:

![Diagram](image)

**Figure 2-22 Direct Form implementation of a 2P2Z Compensator in the discrete domain**
Note that the components and integral saturation are fully integrated and obfuscated, which can be difficult for manually fine tuning a real-world solution. Alternately, the discrete form implementation can be selected to clarify each gain factor's influence on control. The distinctive Low Pass Filter (LPF) and PI control aspects of the system are now evident.

![Diagram of a 2P2Z compensator in the discrete domain]

**Figure 2-23** Separate form implementation of a 2P2Z compensator in the discrete domain

Integral saturation can easily be manually added in this form by tying a saturation block at the output and feeding back to the integrator block input.

### 2.4.1.1 PI Control Scheme

A PI controller with built in weighted integral saturation was selected to maximize use of the C2000 Library to be elaborated in Chapter 3. The corresponding current controller was selected to be a DMC C2000 Optimized PI controller with Integral Windup negation, as the 2P2Z performance was found to be slow with a poor bandwidth in practice, and would require active tuning by means of a Spectrum Analyzer to verify and fine tune. The final approximate PI values were tuned using MATLAB’s SISO tool Bode plot compensator design tool with Equation (2-15) for prototyping (Code available in Appendix B). It was then manually fine-tuned on the actual prototype. The final tuned values for the tuning parameters are as follows: Proportional Gain=0.0546, Integral Gain=9.89, Integral Correction Gain=2.2007.

The output saturates the duty cycle between 10-90% so that the switch is never fully on or off for an entire switching cycle. Because Simulink’s DMC fixed-point Digital PID block integrates control through a
reference and feedback respectively as inputs, leading multiplication blocks are implemented into both paths to incorporate the variable adaptive gain into the system’s error pre-emptively. In this design, the system does not control the output voltage loop, and controls only the inner current loop instead. Without an outer voltage loop, a standard feed-forward voltage gain to stabilize the outer loop’s degradation of the current loop bandwidth is not required [73]. The integral correction gain (or “anti-windup”) saturates the integral term to a maximum value to prevent unwanted error accumulation, and is integrated into a standard PI controller as follows: If the controller saturates, the system becomes unstable and could trip the user [74]. Figure 2-24 demonstrated a general continuous time PI control with windup correction. The DMC block is discretized.

![Continuous-Time PI control with built in integral correction gain](image)

**Figure 2-24 Continuous-Time PI control with built in integral correction gain**

### 2.4.1.2 Fuzzy Logic Investigation

In order to exploit the full control capabilities of the Simulink Embedded Coder control functionality outlined in Chapter 3, some initial testing was also implemented to look at non-linear control methods, specifically fuzzy logic control as a third control option. Unlike the aforementioned control schemes, fuzzy logic better models the non-linear nature of PFC correction that necessitates the variable adaptive gain term modelled in the introduction of Section 2.4.1. However due to the shifting nature of the poles and zeros at
light load compared to full load, non-linear control can help to prevent unnecessary overshoot that would otherwise be caused by the reduced gain and phase margins of these shifted eigenvalues. This is a result of the poles, the RHPZ, and magnitude of the system’s frequency response being dependent on an ever-varying duty cycle, D [75]. Unlike linear control, fuzzy logic controllers do not require a precise mathematical model, but instead rely upon user feedback and intelligence to develop the performance of the system. For fuzzy logic control, a reference input signal undergoes fuzzification, and is compared to a user-developed rule base where a deterministic outcome is determined based on the value of the input. This decision making is driven by a pre-specified rule base. The control output is then selected and mapped to the system output following defuzzification, where the output signal continues to the plant and feedback is retrieved, much with conventional linear control methods. Simulink’s Embedded Coder contains a Fuzzy Logic Toolbox that enables the user to develop and implement this rule base, and convert it into C/C++ code for the C2000 development kit. For PFC control two sets of inputs are required (the error signal, as well as the change in error from the last time, so that an appropriate reaction may be gauged without overshooting the target). A total of 25 rules are required based on these inputs to determine how the output reacts, as shown below in Table 2-3. [76]

Table 2-3 Fuzzy Logic Implementation of a two-input membership function PFC boost converter control with 25 outcomes

<table>
<thead>
<tr>
<th>ΔError</th>
<th>Error</th>
<th>NB</th>
<th>NS</th>
<th>ZO</th>
<th>PB</th>
<th>PS</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZO</td>
<td></td>
</tr>
<tr>
<td>NS</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>ZO</td>
<td>PS</td>
<td></td>
</tr>
<tr>
<td>ZO</td>
<td>NB</td>
<td>NS</td>
<td>ZO</td>
<td>PS</td>
<td>PB</td>
<td></td>
</tr>
<tr>
<td>PB</td>
<td>NS</td>
<td>ZO</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
<td></td>
</tr>
<tr>
<td>PS</td>
<td>ZO</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
<td></td>
</tr>
</tbody>
</table>
Where NB indicates a Negative Big error or change, NS is a Negative Small error or change, ZO is zero error, PS is positive small, and PB is positive big change to the control output. The predetermined ruleset is used as a guide for how drastic the change in output must be based on the input membership functions. An example membership function is shown below in Figure 2-25. Triangular over Gaussian membership functions can be used to save space on the MCU [77]. Additionally, the overlapping of the membership functions ensures that no more than four outcomes are applied at any point.

![Membership Function Editor: FuzzyController](image)

**Figure 2-25 Triangular membership function error input plot for a non-linear control system**

However, when integration was attempted, the aforementioned fuzzy logic control scheme was found to be too memory intensive for the TMS320F2808 MCU, and the program could not be loaded onto the board when incorporating more than one input membership function. This is a known and common issue with fuzzy logic control [78]. While fuzzy logic control would be advantageous to enforce certain user-friendly
rules (such as enforcing no quick changes to the resistance as to not trip the user in case of any aberrant current spikes or malfunction, or enforcing zero overshoot for resistance), it was not a suitable solution for this proposal.

2.5 Conclusion

This chapter provided an in depth explanation of the operating principles of a CCM boost converter as well as the existing two-stage PEM and control methodology, and then elaborated on the prototype changes that were adapted to suit the new research goals. The stability of the PFC boost controller was discussed and three tuning methods were presented with their advantages and disadvantages: 2P2Z compensation, PI Controller with anti-windup (integral correction saturation), and Fuzzy logic control. Suitable background information was provided to establish a basis for the replication methods, software integration, and variable resistance control schemes that will be discussed in subsequent sections.
Chapter 3
Digital Control Methods

3.1 Introduction

Due to the difficulty in transitioning the electrical research to newer mechanical prototypes, there was a keen need for a more accessible code development environment than Code Composer Studio could offer, particularly in foresight of the development team’s need to develop more complex, sophisticated emulated resistance control schemes. While determined within the code, the emulated resistance is defined as the equivalent constant physical resistance that would be felt by the user by the entirety of the electrical board, regardless of if it is a boost converter, voltage controlled attenuator, or other configuration. CCS offers a development IDE that is well suited to developing code, however which can be obtuse to understand from a non-programmer’s perspective particularly as the control scheme complexity increases. As the software integration is intended to be a “means to an end” for biomechanical research, the programming method for future work cannot be too intensive nor time consuming to yield worthwhile results, as it is not the purpose of the integrated project’s goal (which is to reduce a human energy harvester’s (HEH) cost of harvest (COH), or burden, on a wearer). Furthermore, although the Constant $R_m$, Threshold $R_m$, and Variable $R_{in}$ control schemes can be implemented relatively easily using example code provided by TI, debugging more complex control schemes can be tedious due to limited graphing and variable export functionality. An improved, simplified alternative is necessary to continue research. MATLAB Simulink’s Embedded Coder was selected for coding purposes in conjunction with TI’s C2000 TMS320F2808 Development Kit Digital Signal Processor (DSP) for prototyping in conjunction with the Altium designed boost converters and linear regulators. The selection details are outlined in this chapter.

The final implemented system allows for an incredibly versatile system which can be easily used by mechanical and electrical engineers alike for both mechanically oriented goals (such as those outlined in
this thesis for minimizing the COH and targeting decoupling), or electrical goals (such as full energy
capture, battery charging, or implementation on a multitude of systems for the implementation of additional
electrical stages).

Section 3.1 provides an overview of the Digital Control Methods chapter, Section 3.2 elaborates on the
selection of MATLAB Embedded Coder for integration, Section 3.3 evaluates the appropriateness of the
TMS320F2808 DSP for the required research objectives, Section 3.4 introduces the digital sensing scheme,
Section 3.5 provides an overview of replicating the threshold and constant resistance control schemes using
the new Embedded Coder functionality, Section 3.6 describes the experimental test rig necessary for
practical testing of the device, while Section 3.7 provides experimental results for the block diagram setup,
for Code Composer Studio debugging methods, for the ideal AC source experimentation, and some
introductory experimental test rig results. Finally, Section 3.8 provides an overview of the chapter and
contributes closing remarks.

3.2 Software Selection: MATLAB Embedded Coder

MATLAB Embedded Coder is an integrated MCU program which allows users to generate thousands of
lines of commented C/C++ code from a Simulink workflow for a variety of controllers. This functionality
offered an attractive solution to the obfuscation of coding in Code Composer Studio directly. Additionally,
the BMRL is familiar with MATLAB and Simulink as a result of utilizing external mode for data capture
through an external data acquisition unit (DAQ) with an integrated ADC. Note that the Embedded Coder
used to be known as Real-Time Workshop, however the official name was changed to Simulink Coder
officially in 2012 (Which works in conjunction with MATLAB Coder to generate .out files). The terms
are occasionally used interchangeably. The general code generation process is shown in Figure 3-1:
Figure 3-1 Simulink Embedded Coder code generation flowchart

Initially, MATLAB generates C-Code based on the Simulink model, which is subsequently translated into an MCU compatible instructions sequence, depending on the target configuration block’s configuration settings [79]. The performance of the resulting code is affected by many factors, including the arithmetic and precision [80]. For best performance and minimal precision loss, it is recommended to use fixed-point arithmetic, [80]. MATLAB contains a C2000 arithmetic block set that takes advantage of this improved precision, and should be used for arithmetic operations when possible.

When collecting the current biomechanical data, the BMRL has been using an external DAQ with real-time integration to MATLAB/Simulink v.2010 using the data export functionality to record walking trials for their subjects. MATLAB has a high-level proprietary programming language developed by
Mathworks that allows interfacing with other programming languages such as C, C++, Java, Fortran and Python [81],[82]. Simulink is Mathwork’s graphical programming environment used for modelling using block diagrams and customizable block libraries. While it can be used for purely simulation based projects, Simulink also incorporates the “Simulink Real-Time” integration, which allows programs to be run and controlled from a desktop environment and monitored in Simulink. However, MATLAB has a more applicable, powerful functionality known as MATLAB Embedded Coder, which can take a Simulink model block diagram, and convert it to C/C++ code that may then be run on an embedded processor without in-depth knowledge of CCS’s programming environment [83]. Simulink’s Embedded Coder has gone through several iterations over time, with varying functionalities. MATLAB Embedded Coder and MATLAB Coder (a pre-requisite for the former) were previously included and supported up to MATLAB v.2012a and b, however functionality was dropped in 2013 and later reinstated as optional toolkits (Requiring a MATLAB license, Embedded Coder license, and MATLAB Coder license). While the MATLAB license could be acquired at student pricing, the additional two toolkits were not a part of Queen’s’ Student pricing toolkits, and this research was developed in MATLAB 2012a as a result. A full license has recently become available through Queen’s, and should be integrated into future developments for improved control and monitoring. Should further investments into this research be made, the 2015 version could be purchased and integrated, although the current Simulink models being used by the BMRL use MATLAB v.2010b, with 2014 being used for simulation on the lab computers. The integration from 2010/2012 is analogous with small changes documented within Appendix B. The only detriment to this version is that Real Time Workshop (enabling live viewing from within “Scope” blocks of Simulink) was discontinued in 2012 and reinstated in 2013 with the optional packages. This means that some simple debugging for variable viewing is required in CCS, however it is minimal compared to the debugging required to code in CCS. The necessary steps are also outlined in this document to that end. Additionally, while the control scheme can be coded and controlled through Embedded Coder, the lab is free to monitor and report variables using a simple Arduino setup as they have been, should that simplify the consistency of their results.
The Arduino was initially considered as an alternative to the F2808, but was ultimately not viable for a boost converter topology. The reasons are two-fold. Arguably, the TMS320F2808 is over-spec’d for the requirements of a simple boost converter [65], however keeping this converter has some critical advantages. The Arduino Mega2560 can only achieve a maximum switching frequency of 62.5kHz when the time prescaler is set to a time base of 1 and a corresponding cycle length of 256, where the maximum achievable frequency is given by Equation (2-1) [84]:

$$f_{\text{CLKMax}} = \frac{f_{\text{CLKArduino}}}{{\text{Prescale Division}}} = \frac{16\,MHz}{256} = 62.5\,KHz$$

(3-1)

This clock frequency is only available on certain pins adhering to Timer0 in fast PWM mode. While this is sufficient for many Arduino projects, switching converters require a high switching frequency generally >100kHz in order to reduce the required size and impact of the magnetic components (inductive and capacitive), whose parasitics and size are proportional to the switching frequency. Conversely, a higher switching frequency worsens switching losses and can be exacerbated by poor ringing, if poorly designed or dampened. Secondly, the Arduino is also limited in its capabilities when it comes to decoding. Currently, the BMRL uses a dedicated ADC board to decode the signals generated by their motor and cable encoders to determine the motor velocity, which is then outputted to MATLAB/Simulink. The TMS320F2808 has two enhanced Quadrature Pulse Encoders (eQEP) on board, one of which may at present be dedicated to the motor encoder, and the second to the cable encoder, as outlined in Chapter 4. This replaces the off board DAQ currently being used by the BMRL. However, both the Arduino and C2000 platforms are compatible with MATLAB’s Embedded Coder integration as necessary. Additionally, although the switching frequency is too low for a switching converter, the Arduino could potentially be used for a linear regulator where the low side MOSFET is instead fed a continuous variable bias voltage as outlined in Chapter 5, though the encoder decoding issue remains.
3.3 TMS320F2808 DSP Evaluation Board

When considering a platform for digital control, a user has the choice between a microcontroller (MCU) or a digital signal processor (DSP). For more complex control, a DSP offers greater flexibility, speed, and memory than an MCU, though at a higher cost. Texas Instruments developed three families of TMS320 DSPs for digital control, the TMS320C6000™, TMS320C5000™, and the TMS320C2000™. The latter of which includes the TMS320F2808, which is of interest in this research and belongs to a smaller subset of DSPs under the TMS320C28x generation. The board used was part of the TMS320F2808 Experimenter’s Kit [70], which includes the controlCARD, a breadboard development area with 3V and 5V LC decoupled supply, JTAG connectors, and on-board USB JTAG Emulation that eliminates the need for an emulator. The control card itself has 2 ADC units with 16 3.3V 12-bit inputs, clamping diode protection on the ADC inputs, and built-in anti-aliasing filters, which may be run as two parallel simultaneous 8-pin ADCs, or one sequential 16-pin module. Unlike an MCU, the F2808 is a fast 100MHz Fixed-point processor with 64Kx16 Flash memory, and 18Kx16 Sequential Access and Random Access Memory (SARAM). The TMS320F2808 also has up to 16 PWM outputs, and/or 6 (High Resolution) HRPWM outputs. The unit also has two integrated eQEP (Enhanced Quadrature Pulse Encoder) units, 128KB of flash memory, and 36KB of RAM. Although it may be considered overpowered for a simple PFC application, the versatility of the board allows for the more complex development and feedback integration required for improved biometric feedback.

3.4 Digital Sensing Scheme and Sensitivity

The analog pins of the TMS320F2808 have an input range from 0-3V for the board’s 12-bit ADC with built-in anti-aliasing filtering and Sample and Hold (S/H). There are 16 ADC channels on two ADC units, A and B, which may be converted simultaneously or in parallel depending on user needs at a maximum conversion rate of 80ns for the 25MHz ADC clock. Because the pins are not 5V sensitive, the system must be careful to have sufficiently high resistive dividers at the input and output, where R1-R4 have been selected as noted in Table 3-1, pertaining to Figure 3-2.
Table 3-1 Boost converter resistive divider values

<table>
<thead>
<tr>
<th>Resistor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>100k</td>
</tr>
<tr>
<td>$R_2$</td>
<td>10k</td>
</tr>
<tr>
<td>$R_3$</td>
<td>340k</td>
</tr>
<tr>
<td>$R_4$</td>
<td>10k</td>
</tr>
</tbody>
</table>

With the resistive divider configuration shown in Figure 3-2:

Figure 3-2 Resistive divider for ADC conditioning

The digital value seen on the ADC can be described by Equation (3-2), when the input is between 0 and 3V, where the ADC converts to 0 below 0V, and maxes out at 3V above that threshold. Voltages upwards of 5V or higher may damage the ADC unit, so the encoder logic signals must be voltage divided accordingly, as described in Chapter 4, including any encoder signals to the General Purpose Input/Output (GPIO) Pins[85].

\[
Digital\ Value = \frac{2^{12} \times Input\ Analog\ Voltage - ADCLO}{3} \tag{3-2}
\]
ADCLO is grounded in normal operation. This means that the smallest change that the ADC is capable of measuring is described in Equation (3-3):

\[
\Delta V_{\text{ADC Min}} = \frac{V_{\text{high}} - V_{\text{low}}}{\text{Register}} = \frac{3}{4096} = 0.73 \text{mV} \tag{3-3}
\]

The 12-bit ADC provides a sufficiently high resolution above the recommended 8-bit resolution for a low current harmonic RMS value for an input current reference signal by IEC 61000-3-2 Class A requirements, and a >99.9% PF reference voltage signal [86]. As with the previous iteration, the revised board uses Average Current Mode Control (ACMC) for the PFC circuit. A surface mount RC filter right on the ADC pins that removes switching noise and additional interference, in order to better sense the input voltage and currents. This filter must not eliminate the 350Hz component of the input signal or it will be neglected.

The F2808 already has incorporated high frequency antialiasing filters, although these can be pole-compensated with a PI or 2P2Z compensator if necessary. The implemented RC values of the control values are shown below in Table 3-2 and Figure 3-3.

**Table 3-2 ADC RC Filter Values**

<table>
<thead>
<tr>
<th>Sense Voltage</th>
<th>Filter Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin, Vo, lin</td>
<td>R</td>
<td>221Ω</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>1μF</td>
</tr>
</tbody>
</table>

With the RC filter configuration shown in Figure 3-3:

![Figure 3-3 ADC RC filter configuration](image)
Where the cut-off frequency of a simple RC filter is defined in Equation (3-4):

$$f_c = \frac{1}{2\pi RC}$$  \hspace{1cm} (3-4)

When using digital control methods for PFC converters, one must take into consideration several factors that do not influence their equivalent analog counterparts. The first of which being the introduced S/H delay of the converter. This delay results in a phase lag, which increases at the crossover frequency as the bandwidth increases [63]. The current control loop (which is the only one enforced for this particular control scheme) has a wider bandwidth than its analogous voltage counterpart in a conventional boost converter, and is susceptible to computational delay. As such, these delays must be carefully considered when compensating in the digital domain, which may otherwise be alleviated by reducing the current loop’s bandwidth as described in Chapter 2, or by increasing the switching frequency. A switching frequency of 250kHz is selected with an ADC read frequency of 125kHz, which is greater than 10x the current bandwidth (which is in the range of 8-11kHz), and well above the recommended 8 bit voltage resolution by Equation thanks to the 12 bit ADC implementation (3-5):

$$\frac{f_{clk}}{f_{sw}} > 2^8$$  \hspace{1cm} (3-5)

### 3.5 Constant and Threshold Control Scheme Replication Methods

Once the software and hardware have been selected, the original constant emulated and threshold input resistance control schemes can then be replicated via Embedded Coder. In order to enforce average current mode control (thus eliminating the need for slope compensation), the sampling and update timing of the device must be considered. This is also critical for accurate tuning of the device, as the gain and phase margin suffer when the delay, $T_d$, becomes greater than the sampling frequency when the system attempts to calculate and update the PWM signal within a single switching cycle. [70]. Additionally, the inductor current’s average value is sampled either by the input filter, or midway through a switching cycle as to
avoid the signal reading irregularities that can occur at the beginning or end of the inductor’s current slope. In order to achieve this control scheme, a hardware interrupt regulates the timing of the sampling and calculations. This is the primary driving factor for the PFC circuitry to ensure that the reference signal is followed.

In order to configure the device setup, you must include a Target Preference block that affiliates the correct DSP for the appropriate code generation. The system is triggered as a subsystem by means of a hardware interrupt. Within this subsystem, all sample times must be inherited or equivalent to the switching frequency at 250kHz. This is unfortunately more memory intensive than sampling at lower frequencies, although cycles can be skipped within the subsystem to a half or third of this rate via the PWM and ADC blocks.

Figure 3-4 ADC-Update configuration in MATLAB Embedded Coder

The pace of sampling and mathematical workflow calculations are governed by the ePWM module, which switches at a constant 250kHz with the clock counting up for 200 cycles and down for a symmetrical 200 cycles, triggering at the apex. This halved UP/DOWN clock cycle count is compared to the output of the
PI or 2P2Z controller to generate the switching signal at the switch as a gate voltage. The general control hierarchy is shown in Figure 3-5:

![Control Hierarchy Diagram]

**Figure 3-5 Digital PWM Control for an ACMC boost converter using the TMS320F2808 DSP**

The ADC has its own gain and is followed by a sample and hold delay. A ZOH and computational delay precedes the PWM update. Figure 3-6 demonstrates the triggered ADC update scheme block workflow.
3.6 Experimental Test Rig

Experimental testing was largely conducted in two ways: Firstly, using a constant AC voltage course to emulate an ideal rectified sinusoid for stability and PFC testing. However the ideal AC source does not incorporate the encoder data that is integral to the more sophisticated variable control schemes introduced in Chapter 4. Therefore, a second experimental test rig was configured using EPOS, a digital positioning module developed by Maxon Motors. Using the text software EPOS Studio 2.1, the control system can be loaded with a torque profile that matches user trials, or which emulated a simple non-ideal voltage profile that reacts dynamically to loading similar to a human host. This “ideal, but practical” 1-2Hz walking cycle is periodic without discontinuities, asymmetrical irregularities, or the varying pk-pk amplitude of a natural gait, while still encapsulating the relevant encoder data necessary for feedback. The EPOS was loaded with one such ideal sinusoidal profile for extensive testing of the motor/generator combination such that the system’s inherent ~300Hz signal could be analyzed, as well as interpreting the non-ideal non-voltage source...
nature of a user’s force profile, compared to using an AC generator. When fully loaded, the motor cable velocity and leg cable velocity follow each other very closely, resulting in minimal trailing off of the voltage profile, as demonstrated in Figure 3-7. This feedback control method is used for all subsequent testing as an “ideal” case where the system retaliates when loaded gradually or suddenly, representing a more true reaction than a simple power supply otherwise would.

When configured for a simple constant 2.5Ω full load scenario, the results of the EPOS Studio sinusoid configured mechanical rig are shown in Figure 3-7:

![Figure 3-7 Simulated fully damped (2.5Ω) ideal sine function using EPOS studio 2.1 connected to the motor pulley configuration. Resistive load only, no magnetic components](image)

Figure 3-7 was demonstrated on a purely resistive load. Note that a sufficiently damped system emulated a near ideal symmetrical sine wave without the motor encoder freewheeling. The system can similarly be loaded with an uncontrolled boost converter to emulate the lightest possible load (without switching to sink the current). With no control on the boost converter (the low side switch is left off), the light load minimum current draw is as follows:
Figure 3-8 Light loading (100Ω with magnetic components and no switching) of the ideal sinusoidal EPOS 2.1 profile.

The input voltage no longer drops to zero as the motor encoder free-spins when released by the leg pulley, displaying that the system has an inherent minimum current draw without switching. As elaborated in Chapter 5, this is proportional to the magnetics in the system, and can affect the control resolution at light loads.
3.7 Experimental Results

Using the design component selection outlined in Chapter 2, a boost converter prototype was designed in Altium 10, fabricated, populated in the lab, and tested. The system was initially tested for a constant duty cycle. The results at light load are shown in Figure 3-9 given the following parameters: $V_{\text{rect}}=5\text{V}$, $V_{\text{Boost}}=5.27\text{V}$, $f_{\text{sw}}=250\text{kHz}$, $R_{\text{in}}=19\Omega$:

![Figure 3-9 DC Test 10\% duty cycle 5V in inductor current emulated a light load condition (R=19\Omega)](image)

The 19Ω case occurs for a Duty Cycle of 10\%, so a limitation on the duty cycle of 5-10\% to a maximum of 90\% is appropriate to maintain light load without turning the switch entirely on or off for any one switching period. Figure 3-9 demonstrates the minimal switching noise and ringing in the system, as well as the negligible output ripple at light load. The converter operates in CCM at light load and low voltage conditions, but is still susceptible to the generator’s inherent 350Hz ripple while it regulates if the current ripple zeroes. The converter’s DC 25W efficiency is recorded and found to have a peak efficiency of 93.4\% following the diode bridge at 15Ω and $V_{\text{in}}=20\text{V}$, as shown in Figure 3-10.
Figure 3-10 Boost Converter 25W DC Efficiency at an input voltage of 20V

There are several non-idealities of the EPOS system that can also be demonstrated prior to PFC implementation. An EPOS profile is fed a steady full load duty cycle (uncontrolled) with the boost converter to demonstrate the non-ideal properties of the emulated voltage profile, as seen in Figure 3-11, given a peak $V_{\text{rect}}=10V$, Duty Cycle=80%.

Figure 3-11 Uncompensated full load constant 80% duty cycle for a 10W boost converter
As expected, the resulting current draw does not closely follow the input voltage without PFC. Additionally, despite being at full load, the current is peaking only at around 2A for a 4A maximum system. This is because as a non-ideal voltage source, the voltage instead falls in response to the heavy loading and peaks at 5.1V instead of the programmed 10V periodic signal. Additionally, the voltage experiences a falling trailing end, in part due to the loading of the magnetics which must discharge the 2200µF capacitor, and the unidirectional motor which free-spins once released from the leg pulley. As seen in Figure 3-7, a fully loaded resistive system experiences no voltage tail, however the adapted system experiences the limitation that it can only control the system when affecting the leg encoder (i.e.; the human control parameter). It is demonstrated how the PFC control affects this voltage dissipation in both boost converters and linear regulators in Chapters 4 and 5 respectively. Without control, the system only draws the current that it can while the user adds power into the system producing current from the generator, i.e.; during the swing phase. This can be improved in the boost converter, and eliminated with a linear regulator, which mimics a simple resistive load.

3.7.1 Block Diagram Configuration

Within the subsystem trigged in Figure 3-6 are additional Simulink blocksets and subsystems that monitor V\textsubscript{in}, I\textsubscript{in}, and V\textsubscript{out}, while exporting the tuned output to the C2000 ePWM control block to control the boost converter’s control MOSFET. The relevant ADC-PWM Subset blocks are shown below in Figure 3-12:

![Figure 3-12 Boost Converter high level Simulink control blockset workflow](image-url)
The function() block is inherent to the hardware interrupt control described in Section 3.5. The ADC block is configured to control the two ADC units in sequential mode, and is triggered to inherit the sampling rate set by the PWM_Update subsystem (Although this triggers at a frequency of 250kHz, it can be selected to skip cycles to conserve power, as 125kHz is sufficient for the system update rate). The control variables are fed into another subsystem block which controls signal conditioning and the tuned controller, while also implementing the selected resistive control scheme. The output of the Gain and Tuning block is saturated to prevent component damage prior to updating the ePWM unit. The details of the Gain and Tuning Subsystem block are shown in Figure 3-13.
Figure 3.13 Gain and Tuning Simulink Subsystem for boost converter and linear regulator implementation
System inputs and outputs are highlighted in red. Gray blocks indicate signal conditioning and calibrate the input signal from the input voltage, input current, and output voltage. These have been additionally calibrated as detailed in Section 3.7.2. Light blue blocks indicate global variable allocation, which allows for simple debugging in Code Composer Studio when necessary, as a means of monitoring variables. Yellow blocks indicate the control system, incorporating the boost converter’s variable adaptive gain, $G_{\text{adp}}$, while green blocks are optional development blocks that can be used for a variety of flexible control schemes. Unlike when conventional code is generated in CCS directly, changing the applied control scheme is fast, easy, and intuitive in block diagram form. The constant, threshold, or variable resistance profiles are simply selected and fed in as a resistance reference as required, while MATLAB code blocks can be used to easily incorporate testing or safety thresholds, or more sophisticated control. Orange ‘Go To’ blocks feed in information from other blocks within the same program, or within the same subsystem, and are occasionally used to limit the number of crossing lines for clarity. Note that most mathematical operations utilize the IQMath library’s IQN blocksets, which are optimized for use with C2000 DSPs and use floating-point numbers.

Next, the PWM update subsystem is shown in Figure 3-14:
For precision, the ePWM block is set to ramp up in clock cycles as opposed to percentages, as detailed in Figure 3-4. For a switching frequency of 250kHz, and a 100MHZ clock, each period has a duration of 400 cycles, 200 of which count up, and 200 of which count down on the reference comparative ramp within the ePWM block. Due to the fact that the maximum value is 200, the input signal, which is the output of the tuning block, is multiplied by 2 to achieve the appropriate control range. A constant duty cycle can alternately be fed into the ePWM block for testing.

Blocks which are pertinent to the expanded range of variable resistance control are detailed in Chapter 4.

### 3.7.2 Code Composer Studio

While the bulk blockset in Simulink accounts for the ADC and resistive divider gain values, CCS can be used for rudimentary debugging and graphing techniques in order to better calibrate the system. However, unlike an integrated Processor-in-the-Loop (PIL) feedback, CCS suffers from some graphing limitations that must be considered during calibration, and results should be confirmed by oscilloscope for accuracy. Appendix D describes the methodology for adding global variables to the Simulink project, which can be accessed in CCS, graphed, and exported as required. Similarly, Appendix C details how to graph two variables simultaneously to achieve a common time base. A preliminary “pull test” is shown in Figure 3-15 to demonstrate an example CCS output, recording the range of input voltages over three pulls, calibrated with an adaptive gain value in MATLAB.

![Code Composer Studio graphing feature, demonstrating the input voltage over three leg pulley extensions](image)
One of the primary limitations of debugging in Code Composer Studio is the sampling rate for the graphing and visualization tools. With the goal of having minimal or no code modification after compilation by the Embedded Coder programmer, the user is ideally ideally limited from using printf() or similar functions for debugging, and instead use the (dual) graph feature. The inherent sampling rate of the program is limited to 1Hz, and must be manually overwritten [88] [89], due to an imposed limitations on the system’s refresh rate (otherwise limited to a value of 100ms in CCS V4.1 and later) to maintain stability within the program. Alternately, code could be modified to include a printf() statement after variables update, or to include a graph refresh function triggered on a breakpoint, or the signal could be tapped and monitored externally using more familiar methods. Ultimately, it would be an improved system to be able to visualize, export, and debug the Embedded Coder Expressions within MATLAB itself, using the external mode functionality and Simulink scope blocks in MATLAB versions 2013 and later, which could be investigated following this research.

Using this debugging functionality in Code Composer Studio, the sensed voltages can be monitored to within ±0.03% of their experimental value measured on an oscilloscope, while the current experiences a little more noise due to the low current sense resistor value, CSA, and filtering, and is monitored within ±0.2% of the unfiltered response by means of a current probe. The reference programmed resistance (\(V_{in}/I_{in}\) then subtracted from a reference current) therefore has a combined error of ±0.43% on the reference current fed to the PI controller due to measurement discrepancies.

### 3.7.3 Ideal AC Source Experimental Results

The tuned boost converter can be tested on an ideal AC voltage source run at a frequency of 1.5Hz and 10V to mimic an ideal walking profile. There are however several key differences between the actual system and the ideal AC source. Firstly, the ideal AC source does not experience a voltage drop when loaded, as the available power is unlimited within the limitations of the power supply. This is not true for a human host who slows in response to loading, as discussed in the introduction of Section 3.7. Additionally, an ideal
AC source does not contain the inherent variable 0-350Hz signal of the LLDEH’s generator, for which the system must be fine-tuned. Some potential discrepancies in tuning accuracy are expected to this end, as the ideal AC voltage source is very low frequency, as well as the actual output ripple of the device (not the ripple of the switching converter, but that which is subject to the rectified high frequency 350Hz signal). Figure 3-16 demonstrates the constant input resistance PFC control scheme applied according to the block diagram detailed in Section 3.7.1, given $R_{in}=10\Omega$, $V_{rect}=15V$.

![Figure 3-16 Constant input resistance control for $R_{in}=10\Omega$ for an ACMC PFC boost converter coded in Embedded Coder](image)

The PFC control accurately tracks the shape and duration of the input voltage. There is a small crossover delay at start-up that could be improved despite the variable adaptive gain factor. This should not be affected by a slew rate issue, as $G_{adp}$ updates as frequently as the ADC due to how all triggered subsystems must have inherited sampling rates. The delay of 13ms is undesirable as the available power is only accessible for 200-400ms for each walk cycle. This likely indicates an experimental phase lag in the system which could either be improved by real-time tuning using a Spectrum Analyzer, or by incorporating PIL tuning in further research iterations. This is a result of a reduced bandwidth at low output voltages and light
loads which was found to be exacerbated under DC conditions, which is improved by the incorporation of \( G_{\text{adp}} \). However, some delay is still anticipated due to the voltage drop over the diode rectifier bridge as well as the boost diode (all Schottky to minimize this affect). Additionally, a phase lag in the control at the outset emulates a lower than intended emulated resistance, which allows the user to pull more easily at the outset, which is desirable, so long as the resulting overshoot is still within acceptable parameters. Generally a threshold is applied at low voltages to ease the load on the user regardless. Figure 3-17 demonstrates the threshold resistance control while \( R_{\text{in}} \) increases from 10\( \Omega \) to 5\( \Omega \).

![Figure 3-17 Threshold input resistance control for \( R_{\text{in}}=10\Omega \) to 5\( \Omega \) for an ACMC PFC boost converter coded in Embedded Coder](image)

Unlike in a non-ideal system, the threshold testing for an ideal AC voltage source can be set to trigger on an input voltage. On a real human-driven system, however, the resulting drop in voltage caused by suddenly loading the user would cause a resistive chatter as the user struggles to exceed the programmed voltage threshold. Hysteresis can be applied to minimize this chatter, although a more constant reference would be better, as discussed in Section 3.7.4. The boost converter was found to have a DC rise time of 3.2ms in response to sudden loading, as shown in Figure 3-18.
Figure 3-18 shows some low frequency instability, which again could be improved with PIL tuning.

3.7.4 Test Rig Experimental Results

The boost converter was then attached to the EPOS Studio emulated sinusoidal profile for testing with a non-ideal voltage source (Though a real user profile could easily instead be implemented and used). The voltage profile is attached then a driving motor (A Maxon Motor which is being used as a generator, although the terms can be used interchangeably as the motor itself is referred to as the “Maxon Motor”) that pulls and retracts the cable of the LLDEH, which incorporates the actual 3-phase motor generator combination, as shown in Figure 3-19. The test setup is demonstrated with the original 25ft line receiver boost signal cabling, line receiver board, external DAQ and a constant resistance board. All systems were moved on-board for the final prototype, and take the place of the attached electrical loading board.
Figure 3-19 EPOS Pulley configuration with integrated LLDEH

The constant resistances of interest are tested and were recorded in CCS for accuracy, using the variable gain compensation with the results shown Figure 3-20.

![Figure 3-20 Range of emulated resistance control for an ACMC PFC boost converter](image)

The boost converter controls the desired input resistance best at high load conditions, with some control degradation at low voltage light loads. The PI controller effectively removes the steady state error to within
a 5% ripple. Overshoot over the voltage variation is negligible due to the fast 125kHz update rate, however overshoot upwards of 12% at full load can occur at start-up, which does affect the beginning of each step as the magnetic components of the system discharge entirely between each leg pull. Resistive control is also poor at low voltages due to recording difficulties (as the inherent 300Hz ripple zeroes, even though the system is tuned to CCM), as well as the calculation of very low voltages and very low currents (decimal values) reading as higher resistances at very lower powers. The full voltage control range is demonstrated in Figure 3-21.

![Figure 3-21](image)

**Figure 3-21 Full load PFC of a simulated walking profile for an ACMC PFC boost converter**

As anticipated, the converter loses some control once the swing phase ends and the motor encoder begins to freewheel as the magnetic components dissipate, as discussed in the introduction of Section 3.7. The converter can only ideally regulate the input current while the user actively injects power into the system. Any ideal delay in control is still subject to the diode voltage drop, however, and the start-up and slow charging limitations of an electrolytic filter capacitor. The full load oscilloscope regulation for the EPOS 2.1 emulated sinusoidal profile is shown in Figure 3-22.
Figure 3-22 Emulated 2.5Ω (Full load) PFC control scheme for an ACMC boost converter

Given a boost converter with a 100Ω load the system has better control at light load as the system can avoid DCM operation (expanding the potential range from 2.5Ω-100Ω), but the magnetic components drain more slowly as the output resistance impedes the voltage held in the capacitor, resulting in the voltage drain tail seen above in Figure 3-22. As a result of this the power factor (ratio of real/apparent power where the real power is the mean of the multiple of the signals, and the apparent power is the multiple of the rms of current and voltage respectively) is 0.98, and the THD was measured to be 18%. Even at a constant duty cycle, the voltage trailing occurs due to the circuit’s capacitance after the boost converter loses the real power draw, however compared to the unregulated case (such as in Figure 3-11), the applied PFC control scheme extends the controlled voltage range and minimizes the trailing voltage for the available range. This is again a function of the non-ideality of the voltage source. The available working power is not 100% of the available voltage as the pulley withdraws control of the system. The final populated board weighs 197g, eliminating 25m of cabling and external boards for the PC6s and line receiver.
A threshold emulated resistance scheme is then programmed using the block configuration from Section 3.7.1. Note that this threshold uses encoder ramp data rather than a voltage threshold to avoid chatter. Figure 3-23 demonstrates this control scheme:

![Graph](image)

Figure 3-23 Emulated threshold input resistance testing for $R_{in}$=10Ω to 3Ω for an ACMC PFC boost converter

Because the power source is a non-ideal voltage source, it is difficult in practice to implement thresholds based on the input voltage. As the load increases, the voltage drops, causing “chatter” at the threshold which demonstrates as quick switching between the full and light load values. To instead demonstrate threshold control on the practical emulated user, the system can instead take advantage of the leg encoder, which is configured to set a ramp count while a “pull” occurs (Full functionality described in Chapter 4). Because the input and output voltage do not necessarily reach zero during operation, particularly at light loads due to the motor encoder freewheeling, the system should not use a voltage for a ramp count, whereas the leg encoder always zeroes as the user pulls and retracts the cable. This ramp function only approximately reaches the decoupling of the two encoder signals, and does not cover the entirety of the
pull, so the threshold is asymmetrical in nature to demonstrate functionality. The voltage drops in response to sudden increased loading, and that the controller responds quickly and with minimal overshoot. In reality, it is generally impractical to use thresholding in this manner as it could trip the user, although it can be used to enforce light loads below certain voltages as to make swing initiation easier. At light load, the inherent light loading from Figure 3-8 is present. Figure 3-24 demonstrates the current increase response to loading.

![Graph showing settling time from 40% load to 80% load on an emulated EPOS 2.1 sinusoidal periodic 10V input](image)

Figure 3-24 Settling time from 40% load to 80% load on an emulated EPOS 2.1 sinusoidal periodic 10V input

The system settles quickly within 7ms when the load is doubled from 40 to 80% of full load. Note the inherent ~300-350Hz rectified input ripple with minimal distortion due to input filtering. In practical experimentation, there is no longer the current spike of the ideal AC load, indicating a high gain at low (nearly DC) frequencies, likely due to the integrator component.
3.8 Conclusion

Chapter 3 has introduced MATLAB Simulink’s Embedded coder as a solution to the development hurdles that this project has encountered in the past. This chapter discussed how Embedded Coder could be used in conjunction with TI’s C2000 TMS320F2808 DSP and why the board was selected, and analyzed the digital control considerations that further justify the use of this board. The control and ADC trigger updating were also discussed for PFC, and the Simulink block diagram workflow was demonstrated. Chapter 3 also introduced two testing methods by which to gauge the ACMC boost converter: An ideal sinusoidal AC voltage source, and a more realistic EPOS Studio 2.1 sinusoidal voltage driver which uses the actual motor/generator combination integrating the necessary motor and leg encoders. The chapter then concluded with a demonstration of experimental results on both test systems for the constant voltage and constant threshold control schemes.
Chapter 4
An Improved Control Method

4.1 Introduction

Chapter 4 introduces a variety of new control schemes that elaborate on the idea of a “variable input resistance”. As discussed in Chapter 1, the benefits of more sophisticated control schemes are dual: Firstly, changing when and how the user feels certain resistances while walking could help researchers to better understand the impact of Energy Harvesting devices on the kinematics (and muscular co-contraction) of the host. Secondly, dynamic resistance control can more accurately target the negative work phase wherein the system aims to harvest energy. Doing so would mean that the energy harvester is doing work on behalf of the wearer of the device, where they would otherwise need to expend energy in order to slow their limbs. This could mean using an energy harvester as an assistive device, rather than simply for harvesting purposes, expanding its potential research applications. Chapter 4 introduces three new control schemes that enable and interact with the user’s biomechanics by means of two optical encoders: one on the user’s leg which follows the pull and retraction of the cable, and a second on the motor which spins unidirectional in response to the LLDEHs 5:1 input gear train. The three control methods are proposed, implemented, and experimental waveforms are demonstrated using the EPOS Studio 2.1 sinusoidal voltage profile, which simultaneously mimics realistic loading of the device, while allowing for an ideal symmetrical input waveform, and incorporates the highly essential motor and leg encoders. This chapter introduces a Ramp and Hold control Scheme, a Resistance Optimization control scheme, and a Power Regulation control scheme.

Section 4.1 provides an overview of the Improved Control Methods chapter, Section 4.2 defines the necessary information on the biomechanics of negative and positive work in human energy harvesting, Section 4.3 introduces the addition of mechanical encoders to the control scheme and their operating principles, Section 4.4 outlines the three primary proposed control schemes (Ramp and Hold, Resistance
Optimization, and Power Regulation), Section 4.5 provides experimental results for each control scheme, and Section 4.6 concludes the chapter.

4.2 The Biomechanics of Negative and Positive Work

As discussed in Chapter 1, it is desirable to target the negative work phase of the LLDEH device’s power generation, wherein the user is expending energy in order to slow their limb. Increasing the physical resistance at this time allows for the greatest energy capture while also impeding limb movement in a targeted fashion to reduce the overall TCOH. Figure 4-1 demonstrates this targeted period, K4, with the harvester’s knee power during one walk cycle.

![Figure 4-1 Negative work phase of a LLDEH device during right leg swing phase](image)

When the current LLDEH’s device is set at the optimized constant 6Ω load resistance, the harvester’s contribution to the negative work phase is shown in Figure 4-2, shown as the black dotted-dashed power line, compared to the human user’s contribution in dashed-red:
The velocity graph demonstrates the input (leg encoder) velocity, as well as the motor encoder velocity. The point at which they separate is known as the *decoupling point* or *decoupling instant*, and gives an indication of the point at which the electrical contribution to the force felt by the user can no longer be controlled by the electrical system. Although the leg decelerates during the negative work phase, the velocity of the cable profile is not identical to that of the knee power, which is why decoupling does not begin as soon as the negative work phase initiates. The control scheme aims to aid the user prior to decoupling, and then dissipate the free-spinning voltage as quickly as possible afterwards. Currently, the energy harvester is capable of harvesting the black dotted line (The cable constant resistance line in B) in the power figure of Figure 4-2. The goal of resistive profiling would be to actively adapt the resistance felt by the user until the red (dashed-knee power expended by the user) and black (dotted and dashed-energy harvested by the harvester) overlap entirely. Previously, the “dummy” resistive profiles that can be fed to the boost converter are simply mapped from a sinusoid waveform, or other generic shape. However it is desirable to integrate a more sophisticated profile using the biometric feedback provided by such devices.
as encoders, load cells, and motion capture as applicable. To this end, the motor contains an embedded 3 channel ML encoder with an integrated Line Driver. The details of the encoder implementation are in Section 4.3.

4.3 Mechanical Feedback: Optical Encoders

Biometric data is compiled by use of two optical rotary encoders, one on the motor, which uses a unidirectional clutch that freewheels once released by the second encoder, a leg encoder that strictly follows the pull and retract motion of the leg. Each encoder outputs three signals: An index signal, which indicates a full optical rotation, and two channels, A and B. One channel is the clock signal, which generates 2000 counts/revolution and is used as a speed reference, and a second, Up/Down signal that indicates a pull or retraction. While the leg encoder experiences both a pull and retraction velocity, the motor encoder spins in only one direction and therefore only registers up counts. An example count for a leg encoder output is shown in Figure 4-3:

![Waveform diagram of a bidirectional optical encoder with an Index reference, X4 clock configuration, and UP/DN signal](image-url)

Figure 4-3 Waveform diagram of a bidirectional optical encoder with an Index reference, X4 clock configuration, and UP/DN signal
When set in X4 mode, the CLK signal generates a pulse train of four pulses per encoder click. In a bidirectional encoder, the decoded signal counts up and down, and can be differentiated to determine the velocity of the motor, such as with the input (leg) encoder. The unidirectional motor encoder will only produce UP counts, and care must be taken to avoid rollover within the program. The differentiated result will provide the speed of the encoder, and will be positive only when compared to the leg encoder. To avoid overflow for the motor encoder, and is set to reset on the first Index event to a positive bias with a maximum allowable position counter value of $2^{32}$ (4,294,967,295). For the average experimental motor encoder count per step, with an average of one step per second with alternating legs, it would take 6 hours of continuous walking to roll over the internal count value, well over the 10 minute trial duration required. Because of the configuration and equal pull and retraction of the leg cable, the input encoder count will always zero each step, and is not at risk of rolling over.

The motor encoder outputs 3 signals with their complements: Channel A, Channel B, and an Index. These signals must then be decoded by an AM26LS32ACDR Differential Line Receiver that has been integrated into the PCB layout to minimize additional cabling, and therefore the critical system weight. The leg encoder comparatively uses a US Digital E2 Optical Encoder, and a PC6-C-X-X Optical decoder to decode the quadrature output of the incremental shaft encoder for directional up/down counting. The PC6 has also now been integrated into the board to save on space and weight, whereas previously 25ft of cable and a signal booster were required with the standalone PC6 unit, which then were fed into an external DAQ for analysis in MATLAB. This system has now been circumvented and can be achieved on-board. The PC6 is configured to operate in X4 mode, resulting in 2000 clocks/rev.

The TMS320F2808 contains two Enhanced Quadrature Encoder Pulse (eQEP) units to be fed the Channel A, Channel B, and Index values from the PC6 and motor’s Line Receiver respectively. This configuration does not use the Strobe value [90]. The current configuration has an Index signal, and Up/Down (CHA) count signal, and a Clock (CHB) signal. Simulink’s C2000 Blockset contains an eQEP block that has been
configured in Direction-Count Mode at 1x Resolution triggered on the signal’s rising edge. The QEP signal is updated on every ADC signal as with the entire rest of the system at 125kHz, providing sufficient resolution for the encoder count. One eQEP block must be used for each encoder integrated. The position latch counter may also be included for optional debugging. The relevant high level encoder blocks are shown in Figure 4-4, and are integrated at the same level as the ADC blockset in Figure 3-12.

Figure 4-4 High level eQEP encoder integration in Simulink Embedded Coder

The eQEP blocks (one for the input/leg encoder and one for the motor encoder) are fed into subsystems to decode and control the outputted count information. The motor encoder speed block diagram workflow is shown in Figure 4-5, with the position latch data disregarded as optional for testing:

Figure 4-5 Motor Encoder Velocity block diagram workflow in Simulink Embedded Coder
The same colour conventions introduced in Section 3.7.1 apply. The UP counts of the motor encoder are discretely differentiated to determine the velocity and are filtered through a low pass decimation filter with a 0.4πrad/sample roll-off. A calibrated gain value is compared to the legacy Simulink system for accuracy, and the final velocity is outputted to a ‘Go To’ block to be used in the leg encoder subsystem which contains the control schemes. The leg encoder is filtered similarly.

4.4 Proposed Control Schemes and Terminology Clarification

This section defines the term resistance as it applies to both the mechanical difficulty and the electrical loading, and introduces the proposed control schemes and their respective control algorithms and principles of operation.

4.4.1 The Mechanical and Electrical Implications of Resistance

Before the proposed control schemes are introduced, it is critical to clarify the “resistance” terminology used in this section and alluded to in other chapters, as well as a couple additional terms. When speaking mechanically, “resistance” is the difficulty felt by the user. A high resistance makes it more difficult for the user to mechanically engage the system, and a low resistance means that it is easier for the user to engage the pulley. However, the electrical resistance, ie; the emulated resistance programmed by the DSP, is inversely proportional to this difficulty. A full load condition corresponds to a 2.5Ω emulated resistance. This low emulated resistance means that current can flow more readily through the board, resulting in a high current draw and a high power draw from the motor. This is the most difficult setting selected experimentally for the user. A light load condition corresponds to an emulated load resistance of 19Ω (or upwards of approximately 100Ω if the MOSFET is entirely open or running at a limited 10% duty cycle). This high emulated load resistance opposes current flow and draws very little power from the user, and is the easiest setting for the user. We can also clarify the motor and the leg encoder terminology to avoid confusion. The difficulty settings and terminology are clarified in Table 4-1.
### Table 4-1 Terminology clarification for electrical load versus mechanical difficulty and other terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Light Load</strong></td>
<td><em>An emulated experimental</em> 19Ω or 100Ω load. The easiest setting for the user to engage the LLDEH.*</td>
</tr>
<tr>
<td><strong>Full Load</strong></td>
<td><em>An emulated 2.5Ω resistance, corresponds to a high duty cycle at the MOSFET gate. The most difficult setting for mechanical engagement.</em></td>
</tr>
<tr>
<td><strong>Emulated Resistance</strong> or <strong>Input Resistance</strong></td>
<td><em>The target resistance reference of the electrical load. Emulates between 2.5-100Ω. Corresponds to</em> $V_{in}/I_{in}$ <em>of the electrical system where a high</em> $I_{in}$ <em>requires a large power draw from the user and is more mechanically difficult.</em></td>
</tr>
<tr>
<td><strong>Set Resistance</strong> or <strong>Programmed Resistance</strong></td>
<td><em>The emulated resistance value. Used when referring to the reference signal exported from one of the proposed control schemes within the coded control algorithms.</em></td>
</tr>
<tr>
<td><strong>Leg Encoder</strong> or <strong>Input Encoder</strong></td>
<td><em>The encoder attached to the leg pulley for velocity measurement. Bi-directional, the velocity can be both positive and negative depending on if the pulley is being drawn or retracted.</em></td>
</tr>
<tr>
<td><strong>Motor Encoder</strong></td>
<td><em>The encoder attached to the motor for velocity measurement. Unidirectional, it only ever spins in a “positive” direction, and is accelerated by the leg encoder during pulley extension. While the Maxon Motor is being used as a generator, the term “Motor” is often used in the publication for the power generating system and the motor encoder, as the device in question is an adapted “EC-4 pole Maxon Motor”.</em></td>
</tr>
</tbody>
</table>

Any unadorned instances of the term “resistance” within figures are clarified by their respective vertical axes labels when applicable.

With this clarification in mind, three dynamic control schemes are proposed that utilize the integrated encoder feedback: Ramp and Hold, Resistance Optimization, and Power Regulation. Control is handled through the Leg Encoder Subsystem block within the Simulink file. Descriptions of the three proposed control schemes are as follows:
4.4.2 Ramp and Hold Scheme

The goal of the ramp up function is a scheme which targets the decoupling point between the leg and motor encoders, thus indicating the end of the positive work period wherein the user is actively engaging their muscles for forward movement. After this period, the resistance should be maintained optimally high in order to target the desired negative work phase. The Ramp and Hold control scheme aims to harvest the maximum amount of energy during the negative work phase without suddenly burdening the user during swing phase initiation.

1. Allows the user to acclimatise for a period at light load (ex: ten or thirty steps). During this period, step counting begins as a measure of the acclimatization period, and for decoupling period averaging purposes. The step count is triggered on the falling edge of the leg encoder ramp count.
2. Measures the decoupling rate for three steps and averages the result, still at light load.
3. Takes an inputted range of resistances (ie; 19Ω to 2.5Ω), and decrements the programmed input resistance from the low physical resistance values to the high physical resistance value over a pull period, using the averaged decoupling rate as a range.
4. Hold the high physical resistance value until the cable is fully retracted to ensure maximum power extraction over the negative power period. Then returns to light load so that the user is minimally burdened at the beginning of the next step.
5. Continue to measure and average decoupling rate using a moving average filter for every 3 steps. This captures any major changes in gait length, as felt by the user (ie; pace changes, which affect the cable pull length, and therefore the decoupling rate).

4.4.3 Resistance Optimization (Constant Voltage) Scheme

The goal of the Optimized Resistance function is to indirectly minimize the effect of energy harvesting on the user’s kinematics, while extracting an optimal amount of energy for that particular user. When a user’s
walking is under duress, the average voltage over a step is reduced, as anticipated from a non-ideal voltage source. The user is allowed to walk freely until acclimatized, and then the applied input resistance of the boost converter or linear regulator is increased until an average voltage drop is sensed. The input resistance is then reduced until the average voltage at light load is still approximately maintained. This targets an optimal resistance with minimal joint impact for a particular user.

1. The user is provided an acclimatization period (ex: 10 to 30 steps), while step counting begins.
2. A three step-averaging is applied the same as in the ramp up case, only targeting the average output voltage over a given step. Peak voltage may also be targeted.
3. The input resistance is increased at a linear rate per step until an average voltage drop is detected.
4. Voltage averaging continues, with the input resistance reacting dynamically as the user speeds or slows to maintain new averages.

The limitation of this profile is that the user is expected to walk at an approximately constant rate once the optimal average voltage value is found. It continues to react dynamically, to aid the user as they speed up and slow down, though this can be disabled, and only the initial average voltage targeted for the duration of testing.

4.4.4 Power Regulation (Constant Power) Scheme

This control scheme targets maintaining a constant average power output. Similar to the voltage control, it averages the output power over each step and then dynamically alters the input resistance after an acclimatization period to maintain an average input power. Unlike with the voltage profile, this does not ensure that the resistance becomes “easier” if the user is under duress, but will maximize the input resistance to a maximum of 2.5Ω if the required output power is not being met.

1. Provide the user with a light load acclimatization period, while step counting begins
2. Increase the resistance felt by the user, by increasing the load from light load at 19Ω to full load at 2.5Ω, the most difficult setting. The physical difficulty is gradually increased by a
maximum change of no more than 1Ω per step, as to not jar the user, until the manually inputted average power output requirement is met.

3. Dynamically alter the input resistance to maintain that power level.

4.5 Experimental Results

Each profile was setup within the same program and can be selected by controlling the output of the leg encoder block. The block diagram workflow is shown in Figure 4-6, following the colour conventions outlined in Section 3.7.1.
Figure 4.6 Encoder control block diagram
After the leg encoder signal is conditioned by the gray blocks, three control schemes are offered in the yellow blocks: Ramp Up (Top), Optimized Voltage (Middle), and Power Regulation (Bottom). Each actively reads the encoder data and is programmed to perform a different task. Ultimately each block selects a resistance to be used as a reference in the Gain and Tuning subsystem from Section 3.7.1. The “G” ‘Go To’ block is used to select which output should be used as a reference, and is currently connected to the Optimized voltage scheme. It is easy and fast to change which control profile is selected. The full control schemes for each subsystem and their MATLAB function blocks are shown in Appendix E.

4.5.1 Ramp and Hold Experimental Results

The ramp function is then used in the Ramp Up control scheme, which uses the average decoupling period to ramp up the input resistance felt by the user by the decreasing the emulated load resistor from 19Ω to 2.5Ω. This control scheme targets the decoupling instant between the input (leg) encoder and the motor encoder, as shown in Figure 4-7.

![Figure 4-7 Ramp-Up Resistance based on targeting the LLDEH’s encoder decoupling instant](image-url)
Targeting this decoupling point is a matter of identifying when the leg velocity begins to slow, while the motor continues to free-spin unhindered. This is indicative of the negative work phase of power generation. The electrical system’s Ramp and Hold algorithm seeks to aid the user in slowing their limb’s forward movement prior to decoupling, and hold the full load value to dissipate the energy contributed by the motor’s free-spinning as quickly as possible. However, while the electrical system can extend the range of the decoupling point at full load, it does not contribute to the physical system beyond this point. This is because the cable force felt by the user is defined by Equation 4-1:

\[ F_{cable} = F_{elec} + F_{inertia} + F_{friction} + F_{spring} \] (4-1)

Where \( F_{cable} \) is the force experienced by the user by the cable, \( F_{elec} \) is the force contributed by the electrical loading of the energy harvester control scheme, \( F_{inertia} \) is the physical inertia that must be overcome by the user during swing initiation, \( F_{friction} \) is the frictional forces of the energy harvester, and \( F_{spring} \) is the opposition of the pulley springs within the mechanical system, where the latter three forces are inherent to the biomechanical system and only the electrical force is controlled and strategically applied. Once decoupling occurs, \( F_{elec} \) becomes zero, though the system still sees the power dissipation from the free-spinning motor which does not affect the force felt by the user. Prior to decoupling, the system ramps up the resistance in a controlled manner to help slow the user’s limb, though this ramp would be better optimized in future research. The resistance is held high to quickly dissipate the free-spinning power of the motor as usable energy, as opposed to allowing it to be dampened by the frictional forces and be wasted as heat. Figure 4-8 demonstrates the system’s force contributions during the swing phase based on a simulated model:
Figure 4-8 Cable force contributions during swing phase of a lower-limb driven energy harvesting backpack design

The inherent mechanical forces are inevitable, though the system aims to minimize the electrical contribution to the force in opposition to the user in swing initiation, adding electrical resistance gradually. Figure 4-8 demonstrates how the electrical contribution to the force drops after decoupling.

4.5.1.1 Encoder Decoupling Targeting

Decoupling occurs earlier during light load conditions, where the input voltage does not necessarily fall to zero. This indicates that the motor encoder is freewheeling and continues to generate a voltage, even though
the user has stopped putting power into the system. The leg encoder output is inverted with respect to the motor encoder, and must be inverted to detect decoupling as well as amplified to match the gear ratio of the motor encoder. Trials were run on both the boost PFC and the legacy Simulink DAQ in order to calibrate the system’s encoder output velocities. A constant $R_m=11\Omega$ case is demonstrated in Figure 4-9, following signal conditioning and gain calibration.

![Graph](image.png)

**Figure 4-9 11Ω Constant resistance decoupling output for a scaled leg and motor encoder given a 5:1 gear ratio**

Note that while the leg encoder velocity outputs both positive and negative results, the motor encoder remains positive due to the unidirectional clutch. The worst-case light load case is then emulated and reported in CCS and is shown in Figure 4-10:
The leg and motor encoder follow each other closely prior to decoupling.

### 4.5.1.2 Encoder Reference Counting

In order to provide a reliable reference by which the system can measure decoupling, a ramp count is introduced that accumulates so long as the leg encoder velocity is positive (i.e., during a pull). Decoupling will always occur during this period, and the accumulation of the ramp ensures that the decoupling instant is absolute and will not have a chatter/noisy output. The ramp up function is demonstrated in Figure 4-11.

![Figure 4-11 Leg Encoder Ramp Count Signal with Respect to the Input Voltage at full load (2.5Ω), debugged in Code Composer Studio](image-url)

**Figure 4-11 Light load decoupling output for a scaled leg and motor encoder given a 5:1 gear ratio**

![Figure 4-10 Light load decoupling output for a scaled leg and motor encoder given a 5:1 gear ratio](image-url)
Although the input voltage is zeroing, the ramp ends prematurely before this occurs. This is because the input voltage does not necessarily reduce to zero, particularly at light-load conditions. The ramp function targets the motor encoder count instead, and is guaranteed to contain the decoupling period information that is required, before the ramp ends.

In order to achieve the directional output of the eQEP block, the signal is biased (to prevent noise wraparound at start-up), fed through an FIR decimation filter, is discretely differentiated, saturated, and calibrated with a gain block to match existing Simulink encoder readings recorded simultaneously with old methods. The FIR decimation (A low pass filter with a normalized roll-off at 0.4πrad/sample (72º/sample)) is necessary to smooth the signal sufficiently for a clean count, however it introduces a delay into the signal which can affect the sampling rate. A second unfiltered response is therefore included that is used exclusively for the average decoupling rate, which is then applied to the filtered response to avoid zero-crossing chatter. Note that the encoder count ends when the tailing voltage of the motor encoder begins to dissipate, indicating the control period of the leg encoder. The filtered leg encoder with the corresponding ramp up function is shown in Figure 4-12.

Figure 4-12 Encoder Ramp Count with respect to the LLDEH’s input (Leg) encoder
The ramp lasts for the entire duration of the leg encoder count while the velocity remains positive. Decoupling is experimentally tested at both light and full loads and an appropriate threshold is selected which falls within 2% of the actual decoupling sample while being 3.57x the highest observed error for the decoupling rate.

Unlike with using the input voltage as a reference, this encoder count can also be used as a threshold reference for either a threshold input resistance selection, or for error management. An example threshold resistance application is shown in Figure 4-13. A threshold is set midway through the average path length for which the emulated load resistance is reduced to 2.5Ω based on the encoder count ramp, and then is returned to light load. The encoder ramp count is absolute, thus eliminating the chatter from a voltage triggered threshold.

Figure 4-13 Threshold implementation by encoder count. The selected resistance varies between 10Ω and 4Ω based on the encoder ramp count.

The resistance selection is absolute as the encoder ramp does not fall until the leg encoder velocity reverses.
4.5.1.3 Step Counting

In order to correctly apply the proposed control schemes from Section 4.4, the system must be able to count the steps taken to apply both a moving average filter, to average the step power, and to average the voltage. As a user’s kinematics change when loaded, calibrated values at light load may change later on due to differing loading, or exhaustion. The system must be able to react dynamically to these conditions. In order to count steps, the system uses the absolute falling edge of the encoder count function prior to incrementing the step variable. An appropriate threshold is set to avoid false triggers. Some initial step counting is demonstrated in Figure 4-14.

![Figure 4-14 Step count function, triggers on the fall of the leg encoder count](image)

This control scheme means that for a measured $n$ number of steps, the control scheme will not be updated until the $p+1^{\text{st}}$ step after a control scheme is triggered by a step count. The step count function is used to average the decoupling instant (the separation point between the leg and motor encoder velocities), for the first $p$ number of steps. Although the EPOS Studio profile provides a nearly ideal sinusoid mimicking a human walking at a constant pace, there will be variations in the decoupling rate. As a user slows or is
loaded, their gait length decreases, decreasing the cable velocity proportionally. Slight variations in the decoupling rate of the programmed profile exist during normal walking even when provided an ideal sinusoidal profile and are shown in Figure 4-15.

![Graph showing decoupling rate](image)

**Figure 4-15** Ramp function based on decoupling instant averaged during normal periodic walking

Using this decoupling instant, the average decoupling rate for the last three steps is used as a reference to ramp the resistance fed to the PFC boost controller from light load to full load, and to hold it there until the step ends, ensuring that the full load condition is maintained for the entirety of the negative work phase. This resistive ramp is demonstrated in Figure 4-16.
In this configuration, the emulated load resistance is $19\Omega$ (a light load scenario- easiest for the user to engage the pulley), when the encoder ramp is low, indicating that the user is actively accelerating their leg during swing initiation; i.e.; the beginning of the positive work period. As the average decoupling instant approaches, the system *decreases* the emulated resistance to $2.5\Omega$ thereby *increasing* the resistance felt by the user, approaching a $2.5\Omega$ full load condition at decoupling. This full load persists during the subsequent negative work period. The ramp function’s gradual resistive increase gradually applies the load rather than tripping the user with a step increase in the applied resistance felt by the user, in order to target the terminal swing phase at full load.

The resistive ramp ends before the encoder count ramp does, as anticipated, as decoupling occurs prior to the end of the leg encoder’s positive velocity cycle. The Ramp and Hold function as defined in Section 4.4 is set to remain at light load for ten steps, measure the average decoupling rate for the next ten steps, and then dynamically apply the Ramp and Hold function for all subsequent steps while updating the average decoupling instant. The duration of this acclimatization period, sending and averaging period, and applied resistance period could be adapted to any appropriate duration. The selected resistance is adapted according to Equation (4-2):
\[ R_{select} = R_{light} = \left( \frac{n_{encoder}(R_{light} - R_{full})}{t_{avgdecouple}} \right) \]  \hspace{1cm} (4-2)

Where \( R_{select} \) is the emulated resistor value applied to the PFC boost for any given update cycle, \( R_{light} \) is the programmed light load resistance value, \( R_{full} \) is the programmed full load resistance value, \( n_{encoder} \) is the current reference count of the encoder ramp, and \( t_{avgdecouple} \) is the average decoupling range given by the moving average filter. The applied control scheme is shown in Figure 4-17.

![Figure 4-17 Example Light load acclimatization period, Sensing and averaging period, and applied resistance period](image)

**Figure 4-17 Example Light load acclimatization period, Sensing and averaging period, and applied resistance period**

Three different programmed sensing periods are shown: Acclimatization, sensing, and resistance application.

**4.5.1.4 Test Rig Experimental Results**

The system is configured for a Ramp and Hold Resistance profile, and loaded onto the TMS320F2808. Figure 4-18 demonstrates the CCS debugging sensed actual resistance, as well as the selected resistance applied to the PFC boost converter.
The controller tracks the resistance to within 2% of the desired value experimentally from an emulated 15Ω-2.5Ω, but loses control at the combination of light load and light voltage below 15Ω (where DCM at very low voltages causes sensing spikes). This is later improved in the low capacitance and linear regulator solutions described in Chapters 5, but is nonetheless aided by the scheduled gain introduced by the variable adaptive gain term within CCS. Because the ramp ends at full load, and because decoupling is delayed at full load, the system extends the control range during this period. During a leg withdrawal, the converter loses control, but will achieve a full load resistance if the mechanical system is capable of providing it. Note that the resistive spike at the outset of the control is due to zeroing of the inherent 350Hz input signal, and is a low power distortion. The oscilloscope output of the Ramp and Hold method is shown in Figure 4-19.
Figure 4-19 Ramp and Hold output of a PFC dynamic emulated input resistance control algorithm applied to a PFC boost converter, with increasing load resistance from 19Ω to 2.5Ω

Because of the extended decoupling range, the ramp and hold circuit only just reaches the maximum value prior to the loss of precise control as the cable withdraws. If necessary, the system can instead average the light load acclimatization period, and apply this decoupling average without actively updating the average with a Moving Average Filter (MAF). The results are shown in Figure 4-20.
Figure 4-20 Ramp and Hold output of a PFC dynamic emulated input resistance control algorithm applied to a PFC boost converter, with increasing load resistance from 19Ω to 2.5Ω without dynamic decoupling rate update

Now the full load case is held as long as possible after the ramp function ends once the system reaches the light load decoupling value. The power available to be controlled will be controlled for as long as the converter is capable of doing so during power input.

4.5.2 Resistance Optimization (Constant Voltage) Experimental Results

The system can also work to maintain a target voltage. In this case, the system is sensing if the user is burdened based on the peak voltage drop when the gait slows, indicating that the resistance needs to be “let up”. When the user has recovered, they may speed up and regain the peak power production. An unburdened user generates the highest voltage when not loaded. Basically, the controller ramps up $R_{in}$ as much as possible for the user while they still maintain a minimum voltage. Otherwise the light load case is maintained to facilitate unburdened walking. The system is tuned at a light load to that particular user’s average voltage, and then that value is fed back into the control algorithm to attempt to maintain that voltage while gradually increasing the resistance felt by the user. The goal is to minimize the impact of the harvester on the kinematics of the user and determine an optimal resistance that does not unduly burden walking.
When a user’s kinematics are affected, their walk slows, reducing their step length, and the output voltage of the generator. The control algorithm may either be configured to utilize the average step voltage or the peak step voltage, though the average encoder velocity could easily be substituted. The bulk of the control scheme is identical to that of the Ramp and Hold function developed, however the input voltage is now the control variable instead of the decoupling instant. This control scheme still uses an acclimatization period and an averaging period prior to applying a ramping resistance. A MAF is used over every three steps to determine the changes in the user’s kinematics, though the average voltage is not updated, because the system wants to maintain the light load condition. The resistor value difficulty is gradually incremented by a unit increment with each step as to not trip the user. Alternately, a voltage can be selected that the user seeks to maintain. Figure 4-21 demonstrates the control algorithm when given a set 5V input voltage to maintain. The resistance fed to the PFC increases until the voltage reaches the desired level (emulating the user having slowed to maintain speed given a set available power), and then toggles the resistance surrounding that voltage to maintain the output. The optimal resistance for an input voltage of 5V is approximately 9Ω.

![Figure 4-21 Optimized voltage control scheme given a voltage threshold for a dynamic resistance control of a PFC boost converter](image)
4.5.3 Power Regulation (Constant Power) Experimental Results

The system can also adopt a control scheme similar to the Optimized Resistance scheme described above in Section 4.5.2, only now to maintain a set power level required to be generated from the user. This offers more of a challenge, as if that power level is not met, the user will face an incrementing resistance (upwards of the full load $2.5\Omega$), until it is achieved. Such a control scheme could be used to average the power of the device, or for resistance training in practical application similar to an elliptical. Again, the control scheme remains similar to the Ramp and Hold and Optimized Resistance control schemes, but with the input voltage and current being used as reference variables. The algorithm again enforces an acclimatization period, an averaging period, and an applied resistance period where the resistance increments by a unit similar to the Optimized Resistance case. A power level is programmed which the user must aim to achieve. The user’s power can be accumulated and averaged over the step duration as shown in Figure 4-22.

![Figure 4-22 Average sensed power per step for increasing power levels](image)

The power level sensing is calibrated by means of the equivalent oscilloscope output and is set to a threshold power level by which sufficient power is captured for an accurate measurement. Taken at full load on the oscilloscope, $P_m$ after PFC is shown in Figure 4-23:
Average step power outputs, approximate, for the given sinusoidal input. A FIFO MAF buffer is used to average the last three steps. The system is tested using the EPOS Studio sinusoidal input 10V profile for the entire functional loading range, and the results are demonstrated in Table 4-2.

Table 4-2 Functional Average step power output for a 10V emulated sinusoidal step input simulated in EPOS Studio 2.1

<table>
<thead>
<tr>
<th>Resistance [Ω]</th>
<th>Average Step Power Output [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>8.6</td>
</tr>
<tr>
<td>4</td>
<td>6.2</td>
</tr>
<tr>
<td>6</td>
<td>4.3</td>
</tr>
<tr>
<td>11</td>
<td>2.5</td>
</tr>
<tr>
<td>19</td>
<td>1.5</td>
</tr>
<tr>
<td>Open (100)</td>
<td>1.1</td>
</tr>
</tbody>
</table>

Figure 4-23 Average input power over one emulated step at high power
The performance of the applied control algorithm, when fed an average 5W of power to maintain, in demonstrated in Figure 4-24.

**Figure 4-24 Constant Power Regulation resistance control for an emulated 10V sinusoidal step profile on a PFC boost converter**

Much like in the Optimized Resistance case, the set resistance value fed to the PFC boost converter control scheme ramps up until the average output power is met, and then toggles around that value so long as it is maintained. For both the Resistance Optimization and Power Regulation control schemes, the resistance increment is set to a unit one. This corresponds to a maximum force difference between steps (From a near full load from 3 to 4Ω) of approximately 5N, where the differential between the load resistances becomes smaller and smaller at lighter loads, as demonstrated in Figure 4-25.

**Figure 4-25 Cable force felt by the user for a functional range of emulated resistances**
The system could easily be adapted to reduce this unit increment to within an acceptable force range at close-to-full loads as necessary. The initial force spike is caused by the inherent physical contribution to the cable force (i.e.; the user overcoming the inertia, friction, and spring of the mechanical system), while the levelling out of the profile demonstrates the electrical contribution of the load. From open load to the minimum loading, we notice a minimum required force to generate electrical power.

4.6 Conclusion

Chapter 4 has introduced three new control schemes that may be enforced as dynamic input resistance algorithms. All three use the motor encoder and leg encoder data for a combination of averaging, step counting, or as a reference value. The first is a Ramp and Hold function which linearly ramps the resistance felt by the user every step up from light to full load, reaching full resistance at the decoupling point between the motor and leg encoder. The second control scheme is the Optimized Resistance algorithm which averages the average or peak input voltage for a user at light load, and then increases the resistance until that voltage drops, indicating a change in the kinematics of the user. This targets an optimum harvesting resistance prior to affecting the biomechanics of the user. The final control algorithm is a Power Regulation control scheme, which demands a set programmed average input power from the user and then increases or decreases the applied resistance within an acceptable loading range until that power is met. Each control scheme has been demonstrated for the PFC boost converter, and the differences between each have been detailed. The most pertinent block diagram Simulink workflows have been shown. The Ramp and Hold control scheme aims to target a full load resistance at the decoupling point with a gradual ramp up as to not trip the user. The Optimized Resistance control scheme targets the highest resistive difficulty (closest to full load) that a user is capable of walking at without affecting the kinematics of their gait. Finally, the Power Regulation Algorithm seeks to maintain a minimum or average power over each step and dynamically alter the emulated resistance to this end.
Chapter 5
Low Capacitance and Linear Regulator Adaptability

5.1 Introduction

The previous chapters have prototyped a 10W PFC boost converter as well as five input resistance control profiles. As detailed in Chapter 2, the selected boost converter utilized a 2200µF output capacitor. The goal of this component selection was to have sufficient capacity to store the peak power produced by the LLDEH device without sacrificing any of the available power to a resistive bank. However there is a benefit to demonstrating the versatility of the proposed Simulink integration scheme on a multitude of electrical devices. Specifically, an adaptable system can further interpret and diversify the research goals.

Initially a boost converter is a good choice for a power converter because it offers a simple PFC scheme that can enable battery charging, or which boosts the voltage for any additional power stages which is efficient in the electrical domain. The worst case scenario for required capacitance occurs when the output power draw (from any subsequent stages, such as available power accommodation for battery charging) is low and the peak input power is high, where the 2200µF capacitor was selected for an optimal 80V rated output at a 12.8W output power. As the current prototype is intended as a docking stage for versatile adaptation, the power is still tied to a resistive 100Ω load, but there is some flexibility in the output capacitance selected, so long as the sacrificed parameters are in adherence to the research objectives. For instance, as an electrolytic capacitor’s capacitance increases, so does the physical size of the capacitor, generally speaking. If the research aims to control an input voltage profile while also minimizing the weight and volume of the system to reduce a user’s loading (referring to the concept of COC introduced in Chapter 1), then reducing the output capacitance offers some benefits. As seen in Section 3.7, the output voltage ripple is negligible compared to the inherent rectified 350Hz ripple, and the system additionally does not control the output voltage of the converter, so the resulting ripple voltage resulting from a decreased capacitance is not detrimental to the research goals. A variety of output capacitance tests have been
implemented to verify the impact of lower output capacitances on the system which decrease the physical loading of the system, where absolute power capture is not necessarily the goal. Similarly, if the research objectives are reduced to simply controlling the input resistance profile based on biometric feedback, then a simple voltage controlled attenuator (VCA) linear regulator (LR) control scheme is also an alternative solution, which acts as a dynamic resistive bank. Chapter 5 introduces, prototypes, and tests three low-capacitance boost converters (at 940µF, 100µF, and 47µF respectively), as well as a VCA LR by controlling the low-side MOSFET with a variable continuous gate voltage. Experimental results are demonstrated for each system and an overview of a VCA’s operating principles is provided.

Section 5.1 provides an overview of the Low Capacitance and Linear Regulator Adaptability chapter, Section 5.2 discusses the adaptation of the system on a low output capacitance boost converter system and motivations to do so, as well as experimental results, Section 5.3 introduces the operating principles and experimental results of the three proposed control schemes on a voltage controlled attenuator, and Section 5.4 concludes the chapter.

5.2 Low Capacitance Boost Converter

This section analyzes the stability, and experimental testing of a reduced capacitance PFC boost converter solution, using output capacitances of 940µF, 100µF, and 47µF. The advantages and disadvantages of reducing the output filter capacitance are discussed as well.

5.2.1 Stability

As introduced in Section 2.4.1, the stability of the converter’s compensated power stage is dependent on the magnetic components in the system, so it is imperative to consider how a change in the capacitance of the boost capacitor can affect the tuning. Figure 5-1 demonstrates in increasing capacitance from 0 to 2200µF in 200µF increments on the uncompensated open loop Bode:
Figure 5-1 Stability test of a PFC boost converter for varying output capacitances

The flat, blue line indicates a system with zero capacitance. Such a system can be difficult to stabilize, and in this case the roll-off is only due to the inductive and parasitics of the system. The system does require some capacitance to operate as a boost converter. As the output capacitance increases, the open loop Bode plot’s peak values migrate to lower frequencies, converging as the output capacitance approaches $2200\mu$F. As evident from Equation (2-14) in Chapter 2, regardless of the system’s capacitance, the high frequency response of the system remains linear with overlap for all capacitive systems, indicating that the bandwidth and phase margins are relatively independent of the selected output capacitance. Although the system may experience some loss of gain or phase margin with reduced capacitance [91], the system may require some manual fine tuning, but wild variations between varying output capacitances are not anticipated. For a simplified boost converter, the output (capacitor’s) voltage ripple and the inductor’s voltage ripple are defined by Equations (5-1) and (5-2) respectively:
\[
\Delta V_c = \frac{I_{\text{out max}} T_{\text{sw}} D}{C} \quad (5-1)
\]
\[
\Delta I_L = \frac{V_{\text{in max}} T_{\text{sw}} D}{L} \quad (5-2)
\]

Where the capacitor’s ESR adds an additional:

\[
\Delta V_{\text{ESR}} = ESR \left( \frac{I_{\text{out max}}}{1 - D} + \frac{\Delta I_L}{2} \right) \quad (5-3)
\]

The peak inductor current (the input current) is crucial for the current rating of the switching devices and to avoid saturation, while the output capacitor’s voltage rating must be sufficient for the peak output voltage, otherwise the system components may be damaged during operation. As iterated in Table 2-2, the initial designed utilized a 2200\(\mu\)F 80V capacitor rated for 120\% of the peak input power (a 50W system), with a control MOSFET rated for 100V and 17A of input current, and a 180\(\mu\)H inductor rated for 4A rms. The initial design experienced a worst case scenario peak output voltage of 60V with a 280mA inductor ripple and a 1.2mV output voltage ripple. Equations (5-1) and (5-2) indicate that this voltage ripple for the same power rating is anticipated to increase inversely to the output capacitance, which for the inductor at the same power rating and inductance remains the same, while for a minimum standard value 47\(\mu\)F capacitance has an output voltage ripple of 55mV, only 0.07\% of the rated voltage (assuming a comparable ESR between capacitances). Therefore minimizing this output capacitance will not drastically affect the voltage ratings for the output voltage, nor the current ratings for the limited availability input power. A range of 940\(\mu\)F, 100\(\mu\)F, and 47\(\mu\)F output capacitance values are selected to demonstrate the effects of minimizing the capacitor value. Figure 5-2 demonstrates the effect of the capacitance on the output voltage ripple.
5.2.2 Experimental Results

First, two 470µF capacitors are connected in parallel in place of the 2200µF value. The system is fed with an emulated full load constant resistance profile. The results are shown in Figure 5-3. The system is tested using the EPOS Studio 2.1 position controller’s sinusoidal emulated walking profile.

![Figure 5-3](image-url)

**Figure 5-3** Constant emulated resistance waveforms for a 940µF output capacitor boost converter. $V_{\text{out}}$ (Top) $I_{\text{in}}$ (Middle), $V_{\text{in}}$ (Bottom).
As anticipated, the device tuning continues to accurately control the inductor current and the input voltage and current waveforms follow each other closely. The output voltage is noisier than in the 2200µF case as the filtering is now less than half as aggressive. The 940µF boost capacitor can equivalently be fed the Ramp and Hold profile (the most complex of the three profiles introduced in Chapter 4), with the outputs plotted in Figure 5-4.

Figure 5-4 Ramp and Hold input resistance profile on a 940µF PFC boost converter. V_{out} (Top), I_{in} (Middle), V_{in} (Bottom).

Figure 5-5 demonstrates the operational range of the device drawn from the oscilloscope (taken using the MATH function of V_{in}/I_{in}) output of the same Ramp and Hold profile:
Figure 5-5 Ramp and Hold Actual input resistance profile on a 940µF PFC boost converter

The low capacitance boost converter is still capable of maintaining an accurate voltage ramp over the desired 19-2.5Ω control range without sacrificing light load control without excessive voltage or current spikes, despite the halved output filter. The output capacitance is further minimized to see the effect of a 100µF output filter capacitance, as demonstrated in Figure 5-6.

Figure 5-6 Constant emulated resistance waveforms for a 100µF output capacitor boost converter. $V_{out}$ (Top), $I_{in}$ (Middle), $V_{in}$ (Bottom).
As with before, the output voltage noise continues to increase as the capacitance decreases, as well as the average output voltage while the power dissipates through the load rather than be stored in the capacitor more readily. As the capacitance decreases, the trailing edge of the boost converter’s input voltage at full load (noted first in Section 3.7.4 due to the system magnetic components), better emulates the resistive profile of Figure 3-7 as the voltage differential between the input and output voltages decreases. Due to the operating condition that $V_{\text{out}}$ must be greater than $V_{\text{in}}$ for the converter to operate, it is anticipated that the system have improved control at low voltage light load conditions as the capacitance decreases so long as the output ripple does not exceed this condition, which it should not. This is a result of the increasing output voltage as the capacitor stores less energy over the step’s duration, instead of dumping it through the load. However, this effect is mitigated by the fact that the inherent 350Hz ripple may cause the converter to enter discontinuous mode at lower voltages, for which tuning is more difficult, even though the inductor voltage ripple itself is not sufficient to do so. Indeed, the light load idle current draw ripple is greater than that of the 2200µF case as demonstrated in Figure 5-7.

Figure 5-7 Inherent light load current draw for a 100µF PFC boost converter. $V_{\text{out}}$ (Top), $I_{\text{in}}$ (Middle), $V_{\text{in}}$ (Bottom).
The 100µF system is demonstrated with the Ramp and Hold function and shown in Figure 5-8.

Figure 5-8 Ramp and Hold input resistance profile on a 100µF PFC boost converter. $V_{\text{out}}$ (Top), $I_{\text{in}}$ (Middle), $V_{\text{in}}$ (Bottom).

Where the actual input resistance is shown in Figure 5-9.

Figure 5-9 Ramp and Hold Actual input resistance profile on a 100µF PFC boost converter

Some control is now lost at light loads due to the inherent current draw. However because the voltage and current aren’t held up by the capacitor, the system holds greater control over the minimized voltage tail and reach 2.5Ω more tightly near decoupling. There is a trade-off between capacitance, capturing all of the available energy, control at light loads, and accurate control near decoupling that can be optimized. Some
of the light load information is lost to the truncated 0-25Ω MATH function ceiling to improve readability. The system has improved control near decoupling as shown in the CCS output in Figure 5-10, where the set input resistor value and the actual experimental emulated input resistance follow each other very closely until decoupling, although there may be some poor control between the ramp up between 15-19Ω.

![Graph showing set input resistance and actual input resistance control for a 100µF boost converter](image)

**Figure 5-10** Set input resistance and actual input resistance control for a 100µF boost converter

The output capacitance is halved once more to see the extreme effects of this minimization at a reasonable worst-case scenario, substituting a 47µF capacitance as the output filter. The full load results are shown in Figure 5-11.

![Graph showing constant emulated resistance waveforms for a 47µF output capacitor boost converter](image)

**Figure 5-11** Constant emulated resistance waveforms for a 47µF output capacitor boost converter
Again the output voltage is noisier than the higher capacitance cases, though there is a point of diminishing return due to duty cycle limitations and the inverse relationship of the voltage and current ripples and their respective magnetic components. Because of the minimal capacitance, the output voltage is nearly in phase with the input voltage and current after PFC. The Ramp Up function is tested on the 47µF prototype and shown in Figure 5-12.

![Figure 5-12 Ramp and Hold input resistance profile on a 47µF PFC boost converter](image)

Much like with the 100µF case, control is tight near decoupling, but weakened at loads lighter than 15Ω, as is evident in Figure 5-13.

![Figure 5-13 Set input resistance and actual input resistance control for a 47µF boost converter](image)
The results are confirmed by oscilloscope readings shown in Figure 5-14. Note that despite being halved from the 100µF prototype, the light load control does not worsen beyond the 15Ω limitation. This is a result of the inherent current draw of the system with low output capacitance, and experiences diminishing return.

![Graph showing emulated resistance profile](image)

**Figure 5-14 Ramp and Hold Actual input resistance profile on a 47µF PFC boost converter**

Once the most complex control scheme has been verified to work, the Ramp and Hold integrated encoder function, and that the tuning of the low capacitance boost converters PFC the system function are sufficient, it is clear that the output capacitance can be lowered without impacting the converter functionality. Furthermore, while the 940µF solution does not theoretically capture the peak power generated by the LLDEH, the newer LLDEH prototype has a reduced input voltage of 10V for the lower 5:1 gear ratio given a 10W system, and typically operates at an output voltage of approximately 50-55V at full load, meaning that >80% of the energy is being captured during operation under these standard conditions. The differences between the high capacitance boost converter and low capacitance boost converter (worst case) are outlined below in Table 5-1.
Table 5-1 Effects of a Low Capacitance Boost Capacitor on an ACMC PFC converter

<table>
<thead>
<tr>
<th>Variable Parameter</th>
<th>2200µF Boost Capacitor</th>
<th>47µF Boost Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Worst Case $\Delta V_{out}$</td>
<td>1.2mV</td>
<td>55mV</td>
</tr>
<tr>
<td>Light load control</td>
<td>Accurate to 19Ω</td>
<td>Accurate to 15Ω</td>
</tr>
<tr>
<td>Full load control at decoupling</td>
<td>Fair</td>
<td>Excellent</td>
</tr>
<tr>
<td>Additional Advantages</td>
<td>Full energy capture</td>
<td>Reduced size and weight</td>
</tr>
</tbody>
</table>

If the researcher is not necessarily concerned about capturing and conditioning the full energy of the user walk cycle and wishes to improve the decoupling resistance, they could therefore compromise with a 940µF capacitor, which is capable of storing 80% of the nominal input power given the same 65V output boost voltage for which the 2200µF system could store 120%. The 2200µF to 47µF reduction in the output capacitance reduces the weight of the capacitor from 22g to 2g for 1/7th of the same volume occupied on the board, while changing the boost converter to a linear regulator from a boost converter reduced the Board and DSP weight from 197g to 133g, a reduction of 32% of the weight. This is a 10% reduction in the weight of the boost converter and DSP combination, not including the elimination of the PC6 and encoder cabling that was previously necessary as well. The electrolytic capacitors are shown below in Figure 5-15.

![Electrolytic Capacitors Comparison](image.png)

Figure 5-15 Output capacitor maximum reduction from 2200µF (Right) to 47µF (Left), size comparison
5.3 Linear Regulator: Voltage Controlled Attenuator

One final alternative to using a boost converter is to implement a simple variable resistive load, which can still be controlled digitally to implement the proposed control schemes. This can be achieved by means of a configuration known as a linear regulator (LR); or more specifically, a voltage controlled attenuator (VCA) (also known as a voltage controlled resistor (VCR)). This section examines the operating principles, design, and experimentation of this alternative, and its applicable uses with the designed control algorithms.

5.3.1 Principles of Operation

Generically, a linear regulator is typically used to control and output a constant voltage when needed regardless of power conversion loss. In this case the system can adapt the control feedback similarly to as was done with the PFC boost controller in order to maintain a constant, threshold, or variable resistance instead. The adaptation to the digital control scheme is minimal and requires only calibration for the input variables (\( V_{in} \), \( I_{in} \), and \( V_{out} \)), while the encoder feedback functions may remain the same. The system must be returned and stabilized for the VCA as the lack of magnetic components changes the system’s open loop Bode plot and power stage entirely. The PCB prototype has been designed to be easily manipulated from a boost converter to a VCA as necessary. Some minor modifications must be made to the PCB, while the pin connections on the TMS320F2808 remain unchanged. The power dissipation of the MOSFET results in heat loss, so it can be beneficial to use a through-hole device instead of a surface mount MOSFET.

Unlike with a switching converter, the VCA feeds the control MOSFET a continuous voltage signal instead of a square wave signal. The signal from the DSP is fed through a unity buffer amplifier to limit the power draw of the MOSFET, and then sent to the voltage doubler to achieve the necessary gate voltage range of the NTD6416ANT4G, the selected control MOSFET of the device. The general control configuration is outlined in Figure 5-16.
Figure 5-16 Digital PWM Control for an ACMC boost converter using the TMS320F2808 DSP

Now the system operates the control gate (transistor) as a variable resistance instead of a modulated digital pulse train, thus controlling the current flow to the load by controlling an emulated drain to source resistance $R_{DS}$. The NMOS is operated in the ohmic region instead of the active region, as a voltage controlled resistor (VCR), which occurs before the transistor’s breakdown voltage where the resistance of the transistor is minimized [92] [93] [94]. In the ohmic region where $V_{GS} - V_{GS(0ff)} < V_{DS}$, the current through the drain follows Equation (5-4):

$$I_D = \frac{2I_{DSS}}{V_{GSOff}} \left( V_{GS} - V_{GS(0ff)} \right)V_{DS} - \frac{V_{DS}^2}{2}$$  \hspace{1cm} (5-4)
Where $I_D$ is the drain current, $I_{DSS}$ is the zero gate voltage drain current, $V_{GS}$ is the gate to source voltage, and $V_{DS}$ is the drain to source voltage of the FET. The equivalent resistance of the transistor is given by:

$$R_{DS} = \frac{V_{DS}}{I_D} \quad (5-5)$$

Where for the NTD6416ANT4G the characteristic gate-source voltage and drain source equivalent resistance curves are shown in Figure 5-17 from the ON Semi(conductor) [95].

![Figure 1. On-Region Characteristics](image1)

![Figure 2. Transfer Characteristics](image2)

![Figure 3. On-Region versus Gate Voltage](image3)

**Figure 5-17 Onsemi NTD6416ANT4G Typical characteristic voltage profiles**

NMOS pass devices are improved over their PMOS counterparts in that they offer a low $V_{ds}$, a lower $R_{ds,on}$, lower output impedances, and lower capacitances than their PMOS counterparts. However NMOS devices require that their bias voltage is greater than $V_{out}$, requiring a charge pump for operation. For this NFET,
the minimum drain to source breakdown voltage is 100V, so the system is well within limits to use $V_{gs}$ to control the current flow. The threshold voltage is a minimum 2-4V, with a reasonable control range of 3-6V so the system requires a charge pump to meet this range, to operate approximately linearly (Without entering breakdown where the MOSFET operates as a fully closed switch, as done with the boost converter).

Based on the configuration provided in Figure 5-15, the output voltage is a simple resistive divider defined as:

$$\frac{V_{out}}{V_{in}} = \frac{R_{DS}}{R_{DS} + R_{series}}$$

(5-6)

Where $R_{series}$ is given a constant value from 1-2.5Ω to limit the maximum load case. The MOSFET is configured as a common source to ground the source terminal. The TMS320F2808 does not have an on-board DAC, so the program still uses a PWM configuration to output a continuous variable voltage to the FET’s gate, however the square wave is a digital signal which must be converted to an analog value to control the ohmic region of the transistor, using a simple RC filter with a 2kHz corner frequency [96].

Some adaptations are made to the board to adapt it to a linear regulator configuration. R8 and D7 are opened to eliminate the voltage doubler/driver circuit, and short R36 to close the unity buffer op amp circuit, isolating the driver circuit to avoid interference from the driver circuit and its passive elements. The inductor and boost diode are removed and the input is shorted to the positive terminal of the capacitor. The capacitor is replaced with a low resistance (the minimum load resistance for full load), in this case a 1 or 2.5Ω 60W current sense resistor which meets the power needs. The digital 5V signal from the DSP is filtered through a simple RC filter with a cut-off frequency of 2kHz and is tied to the 5V unity buffer to isolate the signal. The output is then escalated to 10V by the charge pump to reach the necessary operation range of approximately 4-6V before the resistance of the transistor becomes negligible. Finally, the original 5/10V voltage doubler signal is disconnected to allow the analog voltage signal to be doubled rather than the 5V signal fed directly from the DSP.
According to Equation (5-6), the transfer function is a simple gain factor, which can be difficult to stabilize without a crossover frequency. A ceramic 2µF capacitor can be added over the output load resistors to add an integrator to the system to boost the low frequency gain. Because the pin connections on the DSP remain unchanged for easy selection between the boost converter and the VCA, the RC and anti-aliasing filters on the ADC pins remain to remove any noise from the system. While the \( V_{in} \), \( I_{in} \), and \( V_{out} \) resistive dividers are identical to those used in the boost case, a separate Simulink file was generated for the VCR to recalibrate the gain values in CCS. Additionally, the variable adaptive gain value \( G_{ad} \) no longer applies to the VCA. Instead, an adaptive gain value that regulates the constant gain value from Equation (5-6) is implemented adhering to:

\[
G_{ad_{VCA}} = \frac{R_{select}}{R_{full}}
\]  

(5-7)

Which normalizes the PI control of the selected gain value at any point during regulation. Again, the gain and phase margins of the device must be considered. The loop gain is the voltage’s magnitude gain as the signal travels through the circuit and digital loop. The phase margin is the signal’s experienced phase differential as it travels through the loop, where ideal negative feedback is out of phase with the source by 180 degrees. Combining these two attributes gives us the device’s phase margin, which is the signal’s difference in degrees from the total phase shift of the feedback signal and -180 degrees (the ideal negative feedback value) where the loop gain crosses 0dB (ie; unity gain on the open loop compensated or uncompensated Bode plot). For stability purposes, a minimum 20 degrees is necessary, though in practice a goal of 45-60 or higher is common due to introduced phase lag in non-ideal systems. Any poles in a system cause a -20db/dec decrease from their roll-off frequency, whereas poles cause a +20db/dec increase (ie; phase shifts of -90 degrees and +90 degrees respectively, with the pole or zeros frequency corresponding to the midpoint 45 degree phase shift). A VCA does benefit from a capacitor at the output for some bandwidth reduction and to provide some positive phase shift to the system for stability purposes. [97] [98] [99] [100] [101].
A PI controller with integral corrective gain was again tuned in MATLAB’s SISO tool and was adjusted experimentally to a proportional gain of 0.28, an integral gain of 3.82, and an integral windup gain of 1. The duty cycle from the DSP was limited from 45 to 90% to maintain a minimum resistance to prevent turn-off. Unlike the boost converter, a 10% duty cycle is insufficient to maintain a minimum turn on voltage for the FET because it is no longer alternating between 0V and a saturated 10V signal.

5.3.2 Experimental Results

The linear regulator was tested on a DC source for its rise time performance, as well as on an ideal voltage AC source, and on the LLDEH with the EPOS studio configured sinusoidal input profile to test the Ramp and Hold voltage profile. Because the encoder control profiles remain unchanged, it is sufficient to demonstrate that the converter works on one (the most complex Ramp and Hold) control scheme in order to demonstrate the integrated functionality of the device.

5.3.2.1 Ideal AC Source Experimental Results

The full load 5V rise time of the device is tested and demonstrated in Figure 5-18.

Figure 5-18 Full load 5V rise time of a voltage controlled attenuator with digital PI control
The controller achieves a 90% rise time of 10.5ms for the tuned PI parameters with no overshoot. At light load, the converter performs considerably worse, as seen in Figure 5-19:

![Graph](image1)

**Figure 5-19** Light load 5V rise time of a voltage controlled attenuator with digital PI control

At light loads, the converter rise time falls to 25ms, over doubled. When the adaptive gain from Equation (5-7) is added, the performance is considerably improved at light loads as shown in Figure 5-20:

![Graph](image2)

**Figure 5-20** Light load 5V rise time of a voltage controlled attenuator with digital PI control with gain scheduling
With the adaptive gain, the light load rise time falls to 9.51ms, again within acceptable parameters. Some instability at steady state is also noted. This is a result of the non-ideal linear response of the MOSFET. The system can be linearized by connecting a large (750k) resistor from the source of the FET to the gate, and a second equivalent resistor between the DSP boosted gate signal and the gate itself. The linearized full load response is shown in Figure 5-21 [93].

![Figure 5-21 Full load 5V rise time of a voltage controlled attenuator with FET linearization](image)

The rise time of the full load case improves to 4.6ms while the rise time of the light load case improves the 1.4ms, and the noise in the system is significantly reduced. Unfortunately, this configuration doubles the necessary gate voltage to drive the MOSFET, and limits the final full load resistance to approximately 3Ω due to the limitation of using the charge boosted 3V DSP pin supply, so the testing is non-linearized, and worst at full loads.

The VCA is loaded with a full load constant resistance profile, and the results are shown in Figure 5-22.
Figure 5-22 Constant resistance full load control of a voltage controlled attenuator

Because the control system emulates a resistive load, the voltage and current are in phase with one another. The system quickly and accurately emulates the full load case over the full voltage range. Because the linearization range cannot be met, the system experience non-linearity resulting in the noise seen in Figure 5-22. An alternate MOSFET with a VCA or LDO specific functionality could be substituted in future in order to resolve this issue, while remaining within the feasible operating range of the DSP’s available voltage source, as the NTD6416ANT4G is not optimized to this end. Nonetheless, the reference emulated resistance is closely tracked for the full duration of mechanical engagement, barring the voltage drop over the bridge diodes, and is shown at full load in Figure 5-23:

Figure 5-23 Constant resistance full load control of a voltage controlled attenuator- CCS Output
A threshold resistance is introduced trigged on a voltage threshold and responds quickly and accurately to the 15V input voltage, shown in Figure 5-24:

**Figure 5-24 Threshold resistance full load control of a voltage controlled attenuator- CCS Output**

The system is capable of tracking the desired input resistance more closely than the boost converter alternatives, however is less versatile for subsequent electrical stages. The selected system should to the desired future research goals, be they mechanical or electrical in nature.

### 5.3.2.2 Test Rig Experimental Results

The VCA is then tested on the experimental test rig using the EPOS Studio sinusoidal input profile. At full load, the system behaves as shown in Figure 5-25:
Figure 5-25 Constant resistance full load control of a VCA on an experimental test rig

Similarly, a threshold resistance can be applied to the mechanical test rig, as shown in Figure 5-26:

Figure 5-26 Threshold resistance full load control of a VCA on an experimental test rig

Like with the boost converter, the threshold is triggered on an encoder count to prevent voltage chatter.

Also as before, the non-ideal voltage source properties of the mechanical test rig are shown which experiences a voltage drop when suddenly loaded. The CCS output of the threshold resistance case is demonstrated in Figure 5-27.
Because of the simplified control scheme, the Voltage Controlled Attenuator follows the selected input resistance accurately and closely for the full duration of operation. When the Ramp and Hold resistive profile is applied, the resulting profile is shown in Figure 5-28.
The set resistance versus the measured actual resistance from the CCS output is shown in Figure 5-29. The set resistance is closely followed for the entire range of operation including at light load and close to decoupling. Some resolution is still lost to the system’s rectifying diode bridge.

![Figure 5-29 Ramp and Hold profile for a VCA operated on a mechanical test rig-CCS Output](image)

While the control is accurate for a VCA over the entire desired resistive load range, there are two major drawbacks to using a VCA over a boost converter. The first is that the energy is simply burned off rather than conditioned to be utilized, which is undesirable from an electrical standpoint. However if the goal is simply to control the resistive profile, this is fine. The second drawback of a VCA is that operating the MOSFET as a variable resistor dissipates a very large amount of power over the FET, which can affect the required power and heat limitations of the system. It may be necessary to introduce a heat sink or cooling fan to the system over an extended operating period, particularly when operating at full loads. The selected series resistor and MOSFET are rated for 60W and 71W respectively with maximum operating temperatures of 150ºC and 175ºC.

5.4 Conclusion
Chapter 5 has introduced two alternative electrical solutions to the initial PFC boost converter design. The first consideration was in response to decreasing the output capacitor in order to reduce the volume and weight of the system to help reduce the board’s COC. This solution improved control near decoupling in
the Ramp and Hold resistive profile, but would decrease control at light loads potentially limiting the system to a 15Ω light load at start-up if the applied output capacitance was too low (in the 100µF and 47µF cases), where an appropriate compromise would be the 940µF solution, which captures 80% of the peak input power at a boost voltage of 65V. This solution is a valid compromise to improve control within the system if the research does not prioritize capturing all available energy within the system, as it allows the magnetics to drain more quickly near decoupling once control has been released by the leg encoder. The stability of the system for varying output capacitances and voltage ratings was also discussed. Alternately, a voltage controlled attenuator solution was proposed, built, and tested. The VCA offered exceptional control over the entire resistive range when tested on both the ideal AC voltage source as well as on the mechanical rig, however it simply dissipates the power in the system and may require higher component ratings to function. The control schemes presented in Chapter 4 all function with either the high capacitance boost converter, the low capacitance boost converter, and the voltage controlled attenuator, and the exact control implementation should be selected based on the research goals and priorities required. These alternate solutions demonstrate the versatility of the applied control schemes for a variety of applications beyond the LLDEH.
Chapter 6
Conclusion and Future Work

6.1 Conclusions
The thesis objective of this research was to provide a variable resistance control scheme to load a mechanical Lower Limb Driven Energy Harvester. In total, five control schemes were applied and tested: A constant input resistance control scheme, a threshold resistance control scheme, and three control algorithms that incorporated biometric feedback data from the LLDEH. Each control scheme utilizes the input encoder to set an absolute reference ramp that is used to apply thresholds or to determine the separation point between the input (leg) and motor encoders of the LLDEH known as the decoupling instant. Each variable resistance algorithm allows the user to acclimatize to the device at a light load for a set period, and then triggers an averaging period where either the average decoupling rate, peak/average voltage, or average power are measured. Once the data collection period ends, the control algorithms then implements one of three variable resistance control outputs to determine the resistance fed to a digitally PI controlled boost converter or voltage controlled attenuator linear regulator.

The first variable control algorithm implements a Ramp and Hold resistance, which determines the average decoupling rate at light load, and then linearly increases the resistance from light load to full load at that decoupling instant, holding there until the next step begins. Either the average decoupling rate set at light load can be held, or a MAF was developed as an alternative option which would continuously update the average decoupling rate and adjust the ramp function accordingly. The second variable resistance control algorithm averages either the average step voltage, or the average peak voltage over the measurement period, taken at light load. This light load value is used as a reference voltage for which unaffected kinematics was assumed. The resistance of the electrical conditioning system is then gradually increased until a change in voltage was sensed, indicating an optimal difficulty for which the user’s walking was not burdened. This is known as the Optimal Resistance control algorithm. A programmed target voltage can also be set. Similar to in the Ramp and Hold case, a MAF continually updates the peak voltage, or adheres to the light load voltage as a reference. The third variable resistance control algorithm programs a set power
level which the user should strive to maintain. After an acclimatization period, the resistance felt by the user is gradually increased in an attempt to generate this power level, within an acceptable emulated resistance range. This means that a user who is walking slowly will face more resistance than one in stride, in an attempt to maintain power. The threshold resistance applies a selected resistance based on either an input voltage (susceptible to chatter on the non-ideal voltage source mechanical test rig), or based on the absolute encoder count ramp.

One major focus of this research was to minimize the necessary coding for the selected TMS320F2808 DSP, which would otherwise be coded directly in Code Composer Studio’s C/C++ environment. Coding and implementing complex control schemes in this environment is difficult and unintuitive. While multiple researchers need to be able to quickly and intuitively adapt the input resistive profiles, a better solution was required. MATLAB’s Simulink Embedded Coder was selected as a coding environment, which allows users to generate C/C++ code for MCUs and DSPs without in-depth coding knowledge, generating the .out files from workflow diagrams. Embedded coder uses an optimized fixed-point C2000 toolbox which enables the addition of eQEP, ADC, ePWM blocks, and the like. Thousands of lines of code can be easily and dynamically adapted between trials without significant effort. The digital considerations of code implementation and delays are also discussed. The resulting control scheme is exceptionally versatile and adaptable.

Each of the aforementioned resistive profiles were generated and calibrated in Simulink, compiled, and loaded into Code Composer Studio for debugging without the need to manipulate the base code. Each profile was loaded onto the TMS320F2808 DSP and was tested on five prototyped boards: A high capacitance PFC boost converter (2200µF output capacitor), three low capacitance PFC boost converters (940 µF, 100µF, and 47µF output capacitors respectively), and a voltage controlled attenuator. The stability of all systems are discussed, and tuned with a digital optimized PI controllers with anti-windup integral correction gain. A 2P2Z stability solution is also discussed, as is fuzzy logic control, though the PI solution is selected for its transparency and functionality. The multiple solutions are presented to demonstrate the
functionality and versatility of the developed coding solution. The solutions are tested with an ideal AC voltages source, as well as with a mechanical test rig configured with a more “ideal” sinusoidal input voltage that mimics the loading effects of the prototypes on an actual user during normal walking.

This thesis was written with the intent that the prototyped system could be reasonably understood by those without an electrical background, so that it might be easily utilized by mechanical researchers as well. The final system is highly adaptable for both mechanical and electrical research goals in the future, and aptly enables easier integration for a variety of control schemes, as well as improving the transferability of the research for interdisciplinary projects.

Section 6.1 provides an overview of the Conclusion chapter, Section 6.2 provides an overview of the thesis’ conclusions based on the provided research, and Section 6.3 provides recommendations for future adaptation to the system and the newly enabled direction of the project as a whole.

6.2 Summary
Chapter 1 introduces the goals of energy harvesting, common energy harvesters at both high and low power levels, and the state of research of electronics in the energy harvesting field. An analysis of the biomechanics of walking was also included, highlighting the concepts of the swing and stance phases of the gait cycle, positive and negative work, and how loading can affect users during this period. The concepts of Total Cost of Harvest and Cost of Carry are introduced along with their significance in the field. Variable resistive control is introduced as a proposed method of better understanding the effects of human energy harvesters on the kinematics and muscular-co-contractions of the host. The mechanics of the Bio-Mechatronics and Robotics Laboratory’s Lower Limb Driven Energy Harvester Device are presented, and three variable resistance control schemes are proposed.

Chapter 2 introduces the current state of research of the adaptive resistance control within Queen’s Power Group, introducing the adapted PFC boost converted with controlled input resistance. The initial high capacitance boost converter was designed with the goal of capturing all available input power from the
Human Energy Harvester, and to use it to charge two 2000mAh batteries following a two-stage boost-buck PEM conditioning. This thesis refocuses that goal to allow for a more flexible control scheme to be implemented by isolating the boost converter component (which is desired for its versatility in the electrical domain) and prototyping it for use with the developed Simulink code. For clarity, the principles of operation of a boost converter are discussed. The adaptations to the original boost converter design are presented. Three stability tuning methods are introduced and analyzed: a 2P2Z solution, a PI controller, and fuzzy logic control. The PI solution is selected for its experimental performance, and intuitive implementation for fine tuning.

Chapter 3 introduces the digital control considerations such as digital delays introduced that can affect the system stability, the software selection reasoning, the hardware selection reasoning, and the digital sensing scheme implemented. The most important MATLAB Simulink block diagram implementations are demonstrated to give an overview of the final workflow of the introduced control algorithms. The Code Composer Studio debugging setup is also introduced and its limitations are discussed. The replicated PFC boost converter’s experimental results are demonstrated using the prototyped Simulink Code and PCB demonstrating the constant input resistance and threshold input resistance control schemes on an ideal AC voltage source, as well as on the experimental test rig, driven by a calibrated sinusoidal input profile using EPOS Studio 2.1 to pull the input (leg) encoder of the real LLDEH, thus providing the actual 3 phase signal data and encoder outputs at approximately 1.5m/s (5.4km/h).

Chapter 4 introduces the proposed variable resistance control algorithms. Their potential impact on the positive/negative work cycle of a human are discussed. The operating principles of the motor and leg encoder are presented, as well as the effect of the motor encoder’s unidirectional clutch on the resulting output counts. The relevant Simulink block diagram signal conditioning is shown. The three variable resistance control schemes are proposed: Ramp and Hold, Optimized Resistance (Voltage Control), and Power Regulation modes. Experimental results on the high capacitance PFC boost converter are
demonstrated for each profile. Each of the control schemes are coded using feedback data within Simulink as well as MATLAB function blocks, which use MATLAB’s proprietary coding language.

Chapter 5 introduces alternative versatile electrical solutions that may be used in conjunction with the coded resistive profiles. First, three low capacitance PFC boost converters are tested, and their stability analyzed. These three lower-output capacitance alternatives (at 940 µF, 100µF, and 47µF) are good solutions to reduce the volume and weight of the final board in an effort to reduce the COC of the 197g device, and also have some effect on the control range of the device. If it is sufficient to capture 80% of the maximum input power for a 65V boost voltage, then the 940µF device provides a better compromise trade-off for improved full load control during decoupling. For the 10W input, the device is still capable of capturing all available power on the new mechanical device given an average unloaded 10V input voltage. A voltage controlled attenuator is also introduced as a potential solution. Its operating principles are presented, a prototype adapted from the boost converter PCB, and it is experimentally tested on an ideal AC source as well as the test rig for the Ramp and Hold profile to demonstrate its feasibility. The advantages and disadvantages of these alternative solutions are analyzed.

The thesis achieves its goals of minimizing the necessary coding, prototyping an electrical solution to the need for a variable controlled input resistance, and providing several variable resistance control schemes to complement the constant and threshold resistance profiles of the previous prototype.

Chapter 6 summarizes and concludes the previous chapters, and presents future recommendations for the state of research.

6.3 Future Work and Recommendations
The future recommendations for this work are as follows:

- A later version of Simulink can now be implemented as discussed in Chapter 3 to improve the adaptability and software support of the system, as well as bug-reduction.
• A newer version of Simulink embedded Coder can be used to implement Processor-in-the-loop tuning to refine the light load and low voltage operation of the PFC boost converter, either instating a 2P2Z or 3P3Z solution that would target coding delays not immediately evident from a Bode plot compensation.

• The Schottky diode bridge could be replaced with a bridgeless solution for rectification to improve the efficiency of the system by reducing the voltage drop prior to resistance control. This would expand the available control range while increasing the power available for capture.

• An analog switch could be implemented to alternate the left leg and right leg encoder inputs and their data parsed digitally. Currently only one leg encoder is integrated, and the TMS320F2808 is limited to two eQEP modules on board.

• Newer versions of MATLAB can implement real time data monitoring to replace the CCS graph debugging, which suffers from serious graphing limitations.

• Circuitry for a pulse switch has been included on the board for a sync signal, and can be implemented for improved data export testing.
References


Appendices

Appendix A: PI Tuning Code for a small-signal PFC current-mode boost converter

%The small signal model of a boost converter
Ts=4e-6; %8e-6; %Switch at 250kHz, sample at 125
Td=Ts/2; %Enforced within the hardware interrupt
Kd=10*7.45323*0.000732421875;
fclock=100e6; %100MHz clock

Vin=15;
Vboost=80;
Rin=2.5;
Il=Vin/Rin;
L=180e-6;
Cboost=2200e-6;
%Vboost=9;
D=1-(Vin/Vboost);
Do=1-D;
%Changing D changes the system gain, but not the poles and zeroes locations
R=100;
%gain=0.09; 1/Vomax 1; %2*Vboost/(Rl*Do*Do); %DC Gain, what we need to compensate
Gdps=80/Vboost;
Res=(1/Ts)/fclock; %Resolution
rc=0.059; 0.09; 0.059;
rl=0.092;

%TF coefficients take the form (as^2 +bs+c)/(ds^2+es+f)
a=Cboost*(Vboost*(1+(rc/R))+(Il*rc*Do));
b=2*Do*Il;

c=L*Cboost*(1+(rc/R));
d=(L/R)+(Cboost*(rl*(1+(rc/R))+(rc*Do*Do)));
e=(Do*Do)+(rl/R);

%G=tf([Vboost*Cboost/(Do*Do) 2*Vboost/(R*Do*Do)],[L*Cboost/(Do*Do) L/(R*Do*Do) 1],'inputdelay',Td);
G=tf([a b],[c d e],'inputdelay',Td);

sysd=c2d(G,Ts,'zoh');
%Control bandwidth is sufficiently low to use a simple discretization method
sysd2=c2d(B,Ts,'zoh');
pidtool(sysd,'PI')

%NOTES
%Only the frequency range below half of fswitch is of a concern due to
%aliasing reduction techniques
%TF of the LPF is ignored, consequently
%Phase margin must be 45° at a minimum (60 is usually robust)
%Bandwidth should be 8-10kHz
Appendix B: MATLAB and Code Composer Studio Configuration

This guide is configured for MATLAB version R2012A and CCS v5. It is possible to use as far back as CCS v3.3 (with more functionality, in actuality, this guide requires the combination of Code Composer Studio and MATLAB to build and run a project). You might need to also install Eclipse as an intermediate IDE, if you do, use the download for C/C++ specifically. (https://eclipse.org/downloads/) If your version of MATLAB is too new (2015?), you might encounter difficulties at the xmakefilesetup stage; however integration will vary slightly with better support in new versions. Note that the Experimenter kit has a built in JTAG debugger, so don’t worry about that (for more information, you can see the somewhat informative “Getting Started” Texas Instruments channel video titled “F2808 and F28335 Experimenter Kit Quick Start Video” on YouTube. This board is a C2000 board that docks an F2808 MCU (Those are the relevant numbers for you) (http://www.ti.com/tool/tmdsdock2808 ).

Overall, this tutorial is based on the following instructional video with some variation: titled “Simulink code generation form MATLAB for TI C2000 processors- Hello world using CCS v4/v5” on the MATLAB YouTube channel with additional documentation here: http://www.mathworks.com/MATLABcentral/answers/25472-ccs-5-1-integration-when-and-how

Code Composer Studio:

You may install from the provider C2000 Experimenter’s Kit CD or you can use the free installation online (either way, it’s the same free install). Download here: http://www.ti.com/tool/ccstudio

1. **Configure the Target Configuration**: Have the dip switch on the board slipped to “USB”, and connect it to the computer. In CCS, select View>Target Configurations. In your Projects window, under the “User Defined” folder, you will see a file called “New Target Configuration…” Double Click to open the general settings. Set up as follows:
   a. **Connection**: Texas Instrument XDS100v1 USB Emulator
   b. **Board or Device**: F2808 Experimenter Kit (Or similar wording, as opposed to the full microcontroller name)
   c. Save the Configuration and Verify the connection. A pop-up will run some tests and confirm the integrity of the board. If it throws you errors, then it will not acknowledge the board.
   Right click on “New Target Configuration” (instead of a double click this time) and select “Launch Selected Configuration” to begin the debugger. In the Debug panel, right click on the board and select “Connect Target”. You may have warnings, that’s okay. It should let you open up the Disassembly window which will show you some low level code. This will show you that you’re at least connected (If you can right click and “Disconnect” instead of “Connect Target”, this will also confirm the connection). Note the Play and pause and stop buttons in the debugger window. Stop will close the debugger.

2. **Configure MATLAB**: input the command >> xmakefilesetup which will open a configuration window.
   Here you will be telling MATLAB where to find all of the necessary compilers to make CCS code from MATLAB flowcharts.
   a. **Template**: gmake
   b. **Configuration**: ticcs_C2000_ccsv4 (will work for v5)
   c. Either go to the “Tool Directories” tab, or if it doesn’t exist, click “Apply” and it should open additional directory requirements. You need to redirect to where your CCS installation is. For me, the path locations were as follows:
      i. **CCS installation**: C:\ti\ccsv5\n      ii. **Code Generation Tools**: C:\ti\ccsv5\tools\compiler\c2000_6.1.3\n      iii. **DSP/BIOS Installation**: C:\ti\bios_5_42_01_09\n   d. Once you’ve applied the settings, you should have the option to click “New…” which will let you create a clone of the settings. You can save this clone, but it will be limited in what you can now edit. Click OK to close these settings.
   e. Input >> checkEnvSetup(’css’,’f2808’,’check’) Which will run tests on the setup we just ran. You’ll likely get a bunch of errors, since we don’t have the right system variables.
f. **Install some junk:** TI has peripheral and flash software available on its website that you will need for the system variables. Follow this link [http://www.ti.com/product/TMS320F2808/toolssoftware](http://www.ti.com/product/TMS320F2808/toolssoftware) and download the files:

- “C28x, C2801x C/C++ Header Files and Peripheral Examples” ([SPRC191](#)) [Software]
- “TMS320F280x Flash APIs” ([SPRC193](#)) [Development Tools]

There are other CCS examples and goodies if you want them, but you’ll need those two to configure CCS/MATLAB. Let them install as they will. For the flash files download, use the V302 install instead of the V100.

h. **Setup System Variables:** In Windows navigator, navigate to your system properties (for me, I right click on “This PC”>Properties in the file directory, then select “Advanced System Properties > Environment Variables”). Add the following and their paths (yours will likely be very similar, since the installers have default paths.

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>(My) Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS_INSTALL_DIR</td>
<td>c:\ti\bios_5_42_01_09</td>
</tr>
<tr>
<td>(if the below BIOS names don’t work)</td>
<td></td>
</tr>
<tr>
<td>CCS_DSPBIOS_INSTALLDIR</td>
<td>c:\ti\bios_5_42_01_09</td>
</tr>
<tr>
<td>CCSV5_DSPBIOS_INSTALLER</td>
<td>c:\ti\bios_5_42_01_09</td>
</tr>
<tr>
<td>DSP280x_INSTALLDIR</td>
<td>c:\tidcs\c28\DSP280x\v170</td>
</tr>
<tr>
<td>FLASH_2808_API_INSTALLDIR</td>
<td>c:\tidcs\c28\Flash28_API\Flash2808_API_V302</td>
</tr>
</tbody>
</table>

Restart MATLAB and rerun the `>>checkEnvSetup…` command to verify that it’s not having trouble with any more variable paths.

i. **Prepare a Simulink File:** To test the setup, run a simple blinking light test.

   i. **Open Simulink:** Follow the library path `Embedded Coder > Embedded Targets >` (Then open a new file using the top left paper symbol) then drag and drop the Target Preferences icon into a new Simulink model.

   ii. In the target configuration window:

   1. **IDE/Tool Chain:** Texas Instruments Code Composer Studio v4
   2. **Board:** C2000 Custom (we’re not using an eZdsp board)
   3. **Processor:** F2808

   iii. Again, in the Simulink library browser, follow `Embedded Coder > Embedded Targets > Processors` and drag and drop a Digital Output block to the model.

   iv. Double click the Digital Output block and scroll down to the GPIO (General Purpose Input Output) block containing GPIO34. This output controls LD3, a small red LED light on the docked F2808. Select GPIO34 and set it to toggle.

   v. In the Simulink Library Browser, follow `Source> Constant` and drag a constant block into the model. (The default value of “1” is good for a high here). Double click on the constant, and under the (you can set the output data type to uint16 if you like) “Main” tab, set a sample time of 0.5, to switch the light every 0.5 seconds. Connect it to the GPIO input of the digital output block.

   vi. Select the “Incremental Build” button in the model window. If everything is configured properly, MATLAB will build the project, output a .out file in the current folder path, and toss you a cmd window with some specs (mine had one warning error which did not affect the build). Ensure that your current folder is accurate or it won’t save properly. I had to double check my `>>makefilesetup` paths once before it would build properly, so that might be your problem if it doesn’t.

   3. Run the .out file from CCS:

   a. With the board/target still connected (debugging mode) go Run > Load> Load program and locate your .out MATLAB file.

   b. Press the green run arrow to run the code. The third LED on the board should be flashing on and off if everything was setup correctly.
To run the project in MATLAB as an external device, you will need to configure the target in the configuration parameters (Ctrl-E)

Some additional useful links:

**TI RTDX and Host Communications documentation**

**RTDX implementation paper**

**MATLAB RTDX real time tutorial**
http://www.mathworks.com/help/supportpkg/texasinstrumentsc2000/ug/rmvd_MATLABlink__41b9c9ebe815b462be8ce1a2511f2131.html

**Matlab rtdx support**
http://www.mathworks.com/help/supportpkg/texasinstrumentsc2000/ug/rmvd_MATLABlink__4059725d7c9f60db299ca6e6a19ec222.html

**Rtdx tutorial**
https://engineering.purdue.edu/~ece495/Power_Electronics_Lab/exp2.pdf

**Rapid c2000 prototyping paper**

**C2000 modelling paper**
http://etd.fcla.edu/CF/CFE0000477/Klee_Andrew_S_200505_MA.pdf

**Epwn configuration**
https://engineering.purdue.edu/~dionysis/EE452/Lab5/Lab5.pdf
Appendix C: CCS Dual Time Graph

In CCS Once the board is connected and a program loaded

1. Open the variables in the “Expressions” View under the DWork folder, these are the project’s named variables
2. Tools>Graph>Dual Time
3. In the pop up configuration, set the Acquisition Buffer to 1, Display Data Size to 2000 and the display data point to 32 bit floating point (If you do not, it will not accept the doubles and will show gibberish)
4. Stack the graphs to better visualize. Both record and stop simultaneously
5. Change the y axes to decimal
6. In graph properties, there is a spot for Start Address A and Start Address B, these are the variables of interest. In the expressions view, there is an address listed for each variable, such as: 0x0000828C@Data. Find the two variables of interest and input ex: 0x0000828C. Note that when you make changes to the Simulink file, these may change/update, so recheck after each new file load.

To export Graph Data:

1. Once you have on the graph the desired data for debugging, right click, then Data>Export All. A dual time graph will plot the sample, and both columns of data into the same file with the same time base.
2. You must have a comma separated excel file to write to. On this computer it is ExportDataTest.csv on the desktop. You can then open and resave the data into another file as necessary.
Appendix D: Global Variables

For the variables to update reliably in CCS debugging, function variables were declared to have a global scope within their respective MATLAB functions. This requires several steps to complete so that they become accessible within CCS in the DWork Expressions folder.

1. The variable must be declared and named as global in a function block
2. Go to Tools> Edit Data/Ports
3. Add>Data
4. The name of the added data must match the name of the global variable precisely
5. Change the scope to Data Store Memory
6. Next, you must have a Data Store Memory Block to allocate the space for the variable within the C code. This can be replicated from one of the existed blocks or through the library browser. The variable can be within a subsystem, but the data store memory block has to be within or above the subsystem’s hierarchy for the space to be allocated properly. Within the block, the Data store name must match the variable precisely, as must the data type (I typically use double for debugging if sufficient, to save on space). MATLAB will throw a compilation error if any of these steps are improperly followed.
7. In CCS, in the expressions pane, add expression from the Filename_DWork folder to view global variables.
Appendix E: Additional Block Configuration and Diagrams

Figure E-1 High level control diagrams including gain and tuning block, ADC sensing, eQEP modules, controller output saturation, and PWM updating subsystem. The f() block is the hardware trigger interrupt controlled by the ePWM update block.

Figure E-2 Gain and tuning subsystem block diagram. Gray blocks indicate signal conditioning and gain factors, blue blocks are global variable declarations, yellow blocks are control and tuning blocks and MATLAB functions, green blocks are optional development blocks, red blocks are subsystem input and output blocks, and orange blocks are Go To blocks that clarify, import, and export signals from with or outside of a subsystem.
Figure E-3  PWM Update subsystem, configured for a 400 clock cycle period (250kHz for a 100MHz DSP) with optional constant duty cycle block.

Figure E-4 Motor Encoder Speed signal conditioning subsystem, with exported motor velocity
Figure E-5 Input (leg) encoder subsystem with signal conditioning, and 3 variable resistance control schemes. The motor encoder is imported for decoupling sensing. Includes the Ramp and Hold function, Optimized Resistance, and Power Regulation control algorithms within their respective subsystems.
Figure E-6 Variable resistance control schemes within their respective subsystems. Ramp and Hold (top), Optimized Resistance (middle) and Power Regulation (bottom). Control uses memory blocks to hold past values. The output of each system is the selected resistance to be sent to the converter controller tuning as a reference.
Appendix F: Pin Connections and Integration

Table F-1 Input Encoder to boost converter/Linear Regulator inputs (confirm cable isn’t reversed on the encoder itself)

<table>
<thead>
<tr>
<th>Wire Colour</th>
<th>Variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>GND</td>
</tr>
<tr>
<td>Green</td>
<td>INDEX</td>
</tr>
<tr>
<td>White</td>
<td>CHA (UP/DN)</td>
</tr>
<tr>
<td>Red</td>
<td>+5V</td>
</tr>
<tr>
<td>Brown</td>
<td>CHB (CLOCK)</td>
</tr>
</tbody>
</table>

Table F-2 BMC 2120-Pin Connections

<table>
<thead>
<tr>
<th>LLDEH Encoder</th>
<th>DAC Counter</th>
<th>Wire Colour</th>
<th>Variable</th>
<th>DAC Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motor</td>
<td>Counter 0</td>
<td>Orange</td>
<td>VCC</td>
<td>5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Yellow</td>
<td>CHA (CLK)</td>
<td>PFJ8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blue</td>
<td>CHB (UP/DN)</td>
<td>P0.6</td>
</tr>
<tr>
<td>Input (Leg)</td>
<td>Counter 1</td>
<td>Red</td>
<td>VCC</td>
<td>5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Brown</td>
<td>CHB (CLK)</td>
<td>PFJ3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>White</td>
<td>CHA (UP/DN)</td>
<td>P0.7</td>
</tr>
</tbody>
</table>
Table F-3 TMS320F2808 GPIO eQEP Pin Configuration

<table>
<thead>
<tr>
<th>GPIO Pin</th>
<th>ePWM input</th>
<th>Variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>eQEP1A</td>
<td>CLK</td>
</tr>
<tr>
<td>21</td>
<td>eQEP1B</td>
<td>UP/DN</td>
</tr>
<tr>
<td>22</td>
<td>eQEP1S</td>
<td>STROBE(NC)</td>
</tr>
<tr>
<td>23</td>
<td>eQEP1I</td>
<td>INDEX</td>
</tr>
<tr>
<td>24</td>
<td>eQEP2A</td>
<td>CLK</td>
</tr>
<tr>
<td>25</td>
<td>eQEP2B</td>
<td>UP/DN</td>
</tr>
<tr>
<td>26</td>
<td>eQEP2I</td>
<td>INDEX</td>
</tr>
<tr>
<td>27</td>
<td>eQEP2S</td>
<td>STROBE(NC)</td>
</tr>
</tbody>
</table>

Table F-4 TMS320F2808 GPIO ePWM Pin Configuration

<table>
<thead>
<tr>
<th>GPIO Pin</th>
<th>Variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ePWM1A (PWM high side signal)</td>
</tr>
<tr>
<td>1</td>
<td>ePWM1B</td>
</tr>
<tr>
<td>2</td>
<td>ePWM2A (PWM control signal)</td>
</tr>
<tr>
<td>3</td>
<td>ePWM2B</td>
</tr>
</tbody>
</table>
Linear Regulator pin configuration differs slightly as detailed in Chapter 5, where the 5/10V is disconnected and routed on PCB.

<table>
<thead>
<tr>
<th>PCB Side</th>
<th>GPIO Pin</th>
<th>PCB Side (con’t)</th>
<th>GPIO Pin (Con’t)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>5V/10V</td>
<td>5V</td>
<td>FREE</td>
</tr>
<tr>
<td>FREE</td>
<td>FREE</td>
<td>FREE</td>
<td>FREE</td>
</tr>
<tr>
<td>FREE</td>
<td>FREE</td>
<td>FREE</td>
<td>FREE</td>
</tr>
<tr>
<td>3IND</td>
<td>FREE</td>
<td>FREE</td>
<td>FREE</td>
</tr>
<tr>
<td>3UPDN</td>
<td>PWM2</td>
<td>2 (ePWM2A)</td>
<td>FREE</td>
</tr>
<tr>
<td>3CLK</td>
<td>PWM1</td>
<td>0 (ePWM1A)</td>
<td>FREE</td>
</tr>
<tr>
<td>1IND</td>
<td>23 (eQEP1I)</td>
<td>3V3</td>
<td>3V3</td>
</tr>
<tr>
<td>1UPDN</td>
<td>21 (eQEP1B-UPDN)</td>
<td>NC</td>
<td>FREE</td>
</tr>
<tr>
<td>1CLK</td>
<td>20 (eQEP1A-CLK)</td>
<td>FREE</td>
<td>FREE</td>
</tr>
<tr>
<td>PUSH</td>
<td>16</td>
<td>FREE</td>
<td>FREE</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>1O- (IIN)</td>
<td>GND</td>
</tr>
<tr>
<td>FREE</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>5V</td>
<td>5V</td>
<td>IO+ (ADC B3)</td>
<td>ADC B3 (Through RC Filter)</td>
</tr>
<tr>
<td>FREE</td>
<td>5V</td>
<td>5V</td>
<td>5V</td>
</tr>
<tr>
<td>2IND</td>
<td>26 (eQEP2I)</td>
<td>LDO</td>
<td>6</td>
</tr>
<tr>
<td>NC</td>
<td>25 (eQEP2B-UPDN)</td>
<td>IIN</td>
<td>ADC B2 (Through RC Filter)</td>
</tr>
<tr>
<td>2UPDN</td>
<td>24 (eQEP2A-CLK)</td>
<td>VOUT</td>
<td>ADC B1 (Through RC Filter)</td>
</tr>
<tr>
<td>2CLK</td>
<td>VIN</td>
<td>ADC B0 (Through RC Filter)</td>
<td></td>
</tr>
<tr>
<td>FREE</td>
<td></td>
<td>FREE</td>
<td>FREE</td>
</tr>
</tbody>
</table>
Appendix G PCB Layout and Fabrication

Figure G-1 PFC Boost converter integrated with the TMS320F2808 with leg encoder and motor encoder connected

Figure G-2 Adapted Voltage Controlled Attenuator

Figure G-3 Unpopulated PCB for either boost converter or VCA development
Appendix H: Altium Board Layout and Pin Connections