ADVANCED CONTROL TECHNOLOGIES FOR VOLTAGE REGULATORS OF NEXT-GENERATION MICROPROCESSORS TO ACHIEVE FAST DYNAMIC RESPONSE PERFORMANCE

by

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Abstract

With the development of computing technology, the demand for next-generation voltage regulators (VRs) to power the modern microprocessors is rising. The next-generation VRs should be more compact and perform with faster dynamic response under increasingly large load transients.

Charge balance control concept has been introduced to achieve much lower output voltage deviations and shorter settling time than linear mode controllers. However, the existing implementations of charge balance controllers are too complicated to be widely used in practical VR applications. Therefore, to improve the transient response of a VR in a practical manner, five novel ideas are presented in this thesis.

The first contribution is a novel voltage sensing based digital “charge balance controller”. The control method utilizes the concept of capacitor charge balance to achieve a near-optimal transient response for Buck converters undergoing transients. Unlike previous work, the proposed controller does NOT require 1) current sensor or advanced analog-to-digital converter (ADC) for time detection/implementation; 2) nominal output inductor or capacitor value to calculate the algorithm; 3) complex calculations such as divisions and/or square roots.

Second, for a generally designed Buck converter, the equivalent ESR of output capacitance can be significant, yielding difficulty for implementing the previous charge balance controllers. In order to extend the charge balance concept to a general Buck converter, a novel digital controller is presented. Without sacrificing the robustness of the voltage sensing based scheme, this digital controller can estimate the necessary design parameters by using proposed curve fitting methodology. By this means, the ESR impact on output voltage is compensated.
The third contribution is an analog implementation of the aforementioned voltage sensing based charge balance controller. This ready-for-integration analog controller also offers AVP extension to power the modern processors.

The fourth contribution is a practical control strategy to achieve significantly improved unloading response performance. This control strategy is capable of controlling a 12V-1.5V Buck converter and an auxiliary circuit. The auxiliary circuit is controlled by peak current mode method (for a predictable number of auxiliary switching) in boundary conduction mode for overshoot and switching loss reductions, while the analog charge balance controller minimizes the settling time of the Buck converter. Based on the proposed strategy, the trends to suppress the voltage overshoot and to reduce the power loss compromise with each other to a practical design solution.

The final contribution is a simplified new linear mode control scheme to meet the industrial load transient test requirements for two-phase VRs (laptop application). This linear mode controller consists of two independent loops for regulating the two-phase VR output voltage and the auxiliary current, separately. Above all, this control scheme is capable of addressing the Multiple Consecutive Load Transients (MCLT) issue in the existing charge balance controllers.
To My Dear Father and Mother
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### List of Symbols

- **$A$**  
  Slope of sliding line

- **$A_1$-$A_4$**  
  Capacitor charge/discharge region during specified time interval (time interval varies depending on chapter/section)

- **$A_{\text{charge}}$**  
  Capacitor charge region (x may be null, 1 or 2)

- **$A_{\text{discharge}}$**  
  Capacitor discharge region (x may be null, 1 or 2)

- **$C_{\text{IL,sens}}$**  
  Capacitor used in inductor current sensor circuit

- **$C_o$**  
  Output capacitor of Buck converter

- **$d$**  
  Duty cycle of Buck converter PWM signal

- **$d_{\text{aux}}$**  
  Duty cycle of auxiliary switching circuit

- **$D_{\text{aux}}$**  
  Schottky diode of auxiliary circuit

- **$ESL$**  
  Nominal value of the output capacitor’s equivalent series inductance

- **$ESR$**  
  Nominal value of the output capacitor’s equivalent series resistance

- **$f_{Io}$**  
  Frequency at which the load current varies

- **$f_{sw}$**  
  Steady-state switching frequency of Buck converter

- **$G_{\text{aux}}$**  
  The gain of the difference amplifier used for auxiliary current sensing

- **$k_{ic}$**  
  Gain of analog capacitor current sensor

- **$i_{\text{aux}}$**  
  Instantaneous auxiliary current

- **$I_{\text{aux_avg}}$**  
  Average auxiliary current

- **$I_{\text{aux_peak}}$**  
  Peak auxiliary current

- **$I_{\text{aux pk-pk}}$**  
  Peak-peak current ripple of auxiliary inductor

- **$i_{c, \text{avg,sw}}$**  
  Average capacitor current over steady-state switching period

- **$I_{c, pk-pk}$**  
  Steady-state capacitor current ripple

- **$I_{D_{\text{aux(avg)}}}$**  
  Average current of auxiliary diode

- **$i_C$**  
  Instantaneous capacitor current
\( i_{C_{\text{avg,sw}}} \) \hspace{1cm} \text{Average capacitor current over a switching cycle}

\( i_L \) \hspace{1cm} \text{Instantaneous inductor current}

\( i_{L,AD} \) \hspace{1cm} \text{Inductor current sensing signal used by analog-digital converter}

\( I_{L0} \) \hspace{1cm} \text{Inductor current at time \( t_0 \)}

\( I_{L_{\text{aux(rms)}}} \) \hspace{1cm} \text{RMS current of auxiliary inductor current}

\( I_{L_{\text{peak}}} \) \hspace{1cm} \text{Calculated peak inductor current following a load transient}

\( i_o \) \hspace{1cm} \text{Instantaneous load current}

\( \Delta I_o \) \hspace{1cm} \text{Load current transient magnitude}

\( \Delta I_{o_{\text{max}}} \) \hspace{1cm} \text{Maximum expected load current transient magnitude}

\( I_{o1} \) \hspace{1cm} \text{Load current before load transient}

\( I_{o2} \) \hspace{1cm} \text{Load current after load transient}

\( I_{\text{off}} \) \hspace{1cm} \text{Instantaneous auxiliary current when \( Q_{\text{aux}} \) is turned off}

\( I_{\text{on}} \) \hspace{1cm} \text{Instantaneous auxiliary current when \( Q_{\text{aux}} \) is turned on}

\( I_{Q_{\text{aux(rms)}}} \) \hspace{1cm} \text{RMS current of auxiliary MOSFET}

\( L_{\text{aux}} \) \hspace{1cm} \text{Inductor used in auxiliary circuit}

\( L_o \) \hspace{1cm} \text{Output inductor of Buck converter}

\( m_1 \) \hspace{1cm} \text{Rising inductor slew rate}

\( m_2 \) \hspace{1cm} \text{Falling inductor slew rate}

\( m_c \) \hspace{1cm} \text{Falling slew rate of the artificial ramp}

\( N \) \hspace{1cm} \text{Number of Buck converter phases}

\( P_{\text{con}} \) \hspace{1cm} \text{Total conduction loss of auxiliary circuit}

\( P_{\text{con \_D_{aux}}} \) \hspace{1cm} \text{Conduction loss of auxiliary diode}

\( P_{\text{con \_L_{aux}}} \) \hspace{1cm} \text{Conduction loss of auxiliary inductor}

\( P_{\text{con \_Q_{aux}}} \) \hspace{1cm} \text{Conduction loss of auxiliary MOSFET}

\( P_{\text{Gate}} \) \hspace{1cm} \text{Gate loss of auxiliary MOSFET}
$P_{sw/Gate}$ Total switching and gate loss of auxiliary circuit

$P_{sw,Q_{aux}}$ Switching loss of auxiliary MOSFET

$Q_1$ Control (upper) MOSFET of Buck converter

$Q_2$ Synchronous (lower) MOSFET of Buck converter

$Q_{aux}$ MOSFET of auxiliary circuit

$R_{1_AD}$ Resistor used in voltage error sensing circuit

$R_{2_AD}$ Resistor used in voltage error sensing circuit

$R_{idLsens}$ Resistor used to set the gain of inductor current sensor

$R_{2iLsens}$ Resistor used to set the gain of inductor current sensor

$R_{AD\_ref}$ Resistor used in voltage error sensing circuit

$R_{droop}$ Load-line regulation parameter equal to desired converter output impedance

$R_{ds(on)}$ On-resistance of MOSFET

$R_{ds\_on\_aux}$ On-resistance of auxiliary MOSFET

$R_I$ Output inductor winding resistance

$R_{L\_aux}$ Auxiliary inductor winding resistance

$R_o$ Load resistance

$R_{sens}$ Current sense resistor for auxiliary circuit

$R_{Vref}$ Resistor used in error voltage sensor circuit

$t_a$ Beginning of the transient period

$t_b$ End of the transient period

$t_{max}$ Time instant of maximum output voltage

$t_{min}$ Time instant of minimum output voltage

$T_0$ Time interval $t_0-t_1$

$T_1$ Time interval $t_1-t_2$

$T_2$ Time interval $t_2-t_3$
$t_0$-$t_3$ Time instants following load transient (definition variable depending on chapter)

$T_{AD\_del}$ Analog-digital converter delay

$T_{aux\_off}$ Off-time of peak-current mode, constant off-time controller (used for auxiliary circuit switching)

$T_{delay\_line}$ Total delay of entire delay line

$T_{del\_hys}$ Hysteretic comparator delay

$T_f$ Sampling frequency for curve fitting

$T_{fall}$ Typical fall time of auxiliary MOSFET

$T_{off\_sw}$ Off-period of Buck converter’s switching cycle

$T_{rise}$ Typical rise time of auxiliary MOSFET

$t_{samp}$ Time instant at which $v_{ic\_aux\_est}$ is sampled for transient magnitude estimation

$T_{samp}$ Sampling period used for load transient magnitude estimation

$t_{samp\_1}$ Beginning of sampling period

$t_{samp\_2}$ End of sampling period

$T_{set}$ Settling time

$T_{set\_pos}$ Calculated settling time for a loading step transient

$T_{set\_neg}$ Calculated settling time for a negative load step transient

$T_{sw}$ Steady-state switching period

$V_{AD\_ref}$ Voltage reference used by analog/digital converter

$v_{aux}$ Voltage proportional to auxiliary current, used for current sensing

$v_{aux\_peak}$ Voltage value used for peak current-mode, constant off time controller of auxiliary circuit

$v_c$ Capacitor voltage (neglecting equivalent series resistance and equivalent series inductance)

$v_{con}$ Linear compensator control voltage/command

$v_r$ Reference voltage
\[ v_{ramp} \] Ramp voltage
\[ V_{cc} \] Analog device rail voltage
\[ V_{\text{diode}} \] Forward voltage drop of auxiliary diode
\[ v_{\text{err}} \] Linear compensator error voltage
\[ v_{\text{err,AD}} \] Output voltage error signal used by analog-digital converter
\[ V_{\text{ESR}} \] Voltage drop caused by output capacitor \( ESR \)
\[ V_{\text{hys}} \] Comparator hysteresis voltage
\[ v_{ic} \] Output voltage of capacitor current sensor
\[ v_{ic,\text{est}} \] Output voltage of capacitor current estimator used in Chapter 4
\[ V_{\text{in}} \] Nominal input voltage of Buck converter
\[ v_{\text{max,\text{sen}}} \] Sensed maximum voltage
\[ v_{\text{min,\text{sen}}} \] Sensed minimum voltage
\[ v_{o} \] Instantaneous output voltage of Buck converter
\[ V_{o,\text{pk-pk}} \] Peak-to-peak output voltage ripple in steady-state
\[ V_{o} \] Nominal output voltage of Buck converter
\[ V_{o1} \] Steady-state voltage before load transient
\[ V_{o2} \] Steady-state voltage after load transient
\[ v_{o,\text{pk-pk}} \] Peak-peak ripple of output voltage during steady-state
\[ \Delta v_{o,\text{neg}} \] Maximum calculated output voltage deviation following a negative load step transient
\[ \Delta v_{o,\text{pos}} \] Maximum calculated output voltage deviation following a loading step transient
\[ \Delta v_{o,\text{samp}} \] Output voltage difference over sampling period
\[ v_{\text{phase}} \] Phase voltage of Buck converter
\[ V_{pp} \] Peak-peak voltage
\[ V_{\text{ref}} \] Reference voltage
\[ V_{SW_{ESR,\text{neg}}} \] Real switching point voltage considering ESR impact under negative transient
$V_{SW_{ESR\_pos}}$ Real switching point voltage considering ESR impact under loading transient

$V_{SW_{sen\_neg}}$ Calculated switching point voltage based on sensed maximum voltage under negative transient

$V_{SW_{sen\_pos}}$ Calculated switching point voltage based on sensed minimum voltage under loading transient

**Abbreviations**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>APF</td>
<td>All-Pass Filter</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>AVP</td>
<td>Adaptive Voltage Positioning</td>
</tr>
<tr>
<td>BCM</td>
<td>Boundary Conduction Mode</td>
</tr>
<tr>
<td>CAC</td>
<td>Controlled Auxiliary Current</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>COT</td>
<td>Constant Off-Time</td>
</tr>
<tr>
<td>CPLD</td>
<td>Complex Programmable Logic Device</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>DPWM</td>
<td>Digital Pulse Width Modulation</td>
</tr>
<tr>
<td>EA</td>
<td>Error Amplifier</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent Series Inductance</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>LCO</td>
<td>Limit Cycle Oscillation</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LUT</td>
<td>Look-up Table</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Silicon Field Effect Transistor</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>MUX</td>
<td>Multiplexor</td>
</tr>
<tr>
<td>OPAMP</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>PCM</td>
<td>Peak Current Mode</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>USSM</td>
<td>Unified Small Signal Model</td>
</tr>
<tr>
<td>VR</td>
<td>Voltage Regulator</td>
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</tbody>
</table>

**Prefixes for SI Units**

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>Pico ($10^{-12}$)</td>
</tr>
<tr>
<td>n</td>
<td>Nano ($10^{-9}$)</td>
</tr>
<tr>
<td>u</td>
<td>Micro ($10^{-6}$)</td>
</tr>
<tr>
<td>m</td>
<td>Milli ($10^{-3}$)</td>
</tr>
<tr>
<td>k</td>
<td>Kilo ($10^3$)</td>
</tr>
<tr>
<td>M</td>
<td>Mega ($10^6$)</td>
</tr>
</tbody>
</table>

**SI Units**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Amperes</td>
</tr>
<tr>
<td>C</td>
<td>Coulombs</td>
</tr>
<tr>
<td>F</td>
<td>Farads</td>
</tr>
<tr>
<td>H</td>
<td>Henries</td>
</tr>
<tr>
<td>Hz</td>
<td>Hertz</td>
</tr>
<tr>
<td>s</td>
<td>seconds</td>
</tr>
<tr>
<td>V</td>
<td>Volts</td>
</tr>
<tr>
<td>W</td>
<td>Watts</td>
</tr>
<tr>
<td>°</td>
<td>Degrees</td>
</tr>
<tr>
<td>Ω</td>
<td>Ohms</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 Introduction

For the last half century, electrical engineers have been building integrated digital devices at an exponentially-increasing level of transistor density. This trend was first observed by G. E. Moore in 1965 in his famous article “Cramming more Components onto Integrated Circuits”. [1] Since then, this trend has been known as “Moore’s Law” shown in Figure 1.1. As Moore predicted, digital devices have become exponentially denser as transistor sizes have become exponentially smaller through various advances in fabrication processes. Whether Moore can be credited as a visionary or whether it was merely the prediction itself that drove the semiconductor industry to reach such levels is a matter for academic debate; however, there is no doubt that the adherence to Moore’s Law is one of the most significant driving forces to the advancement of the field of power electronics.

The field of power electronics can be defined as the development of devices that convert one type of power to another. There are four types of power conversion: AC-AC, DC-AC, AC-DC and DC-DC. The former two types of conversion (AC-AC, DC-AC) serve mainly in power distribution and electric machine applications while the latter two types of conversion (AC-DC, DC-DC) serve mainly the electronics industry. As it is typically DC-DC converters that directly power the aforementioned digital integrated circuits, it is their progress that is most tightly linked to the advancement of transistor density.
As transistors become smaller and faster, the power consumption and power transition rate of digital devices also increases. These two factors are the contributing forces behind the need to continuously re-design and re-analyze DC-DC converters. This chapter will provide a brief outline of a typical DC-DC conversion application and the challenges associated with such applications. Primarily, this chapter will outline the requirement for power converters capable of reacting quickly to a rapid change in load power consumption, which is the main motivation of this thesis. Project objectives and thesis organization will then be presented.

1.2 Brief Overview of Synchronous Buck Converters and their Load Transient Response

As modern digital devices are capable of operating at increasingly lower voltages (≤1V), it has become standard to convert higher system rail voltages to low voltages at close proximity to
the load. This allows for lower conduction loss through the system rails since currents will be significantly lower than the device load current. Thus, DC-DC “step-down” converters are required for this application. As implied, step-down converters convert a higher DC voltage to a lower DC voltage.

For microprocessor applications (either central processing units (CPU) or graphic processing units (GPU)), these converters are often referred to as a voltage regulator (VR). VRs are responsible for converting a DC voltage (typically 12V) provided by an AC-DC rectifier (often referred to as the “silver box”) to a much lower DC voltage (typically 0.8V-1.5V) to supply the microprocessor. While there exists a large variety of DC-DC converters that could perform such a task, the synchronous Buck converter is usually employed due to its relative simplicity and low cost. The synchronous Buck converter can exist as a single phase, or as multiple inter-leaving phases. Figure 1.2 illustrates a multi-phase synchronous Buck converter.

Figure 1.2  Multi-phase synchronous Buck converter
A single-phase synchronous Buck converter consists of a pair of switches, (the control switch \( Q_1 \) and the synchronous switch \( Q_2 \)), an output inductor \( L_o \) and an output capacitor (or bank of capacitors) \( C_o \). The control switch is cycled at a fixed frequency \( f_{sw} \) and a duty cycle \( d \) while the synchronous switch is cycled with a duty cycle \( 1-d \). This produces a pulse train with a peak-peak magnitude of \( V_{in} \) and an average voltage of \( V_{in} \cdot d \) at the phase node \( v_{phase} \). This voltage is filtered by the output inductor and capacitor in order to output a DC voltage with a very small superimposed ripple.

In order to handle larger load currents, multiple Buck branches may be required. The multi-phase synchronous Buck converter has multiple branches of switches and inductors connected in parallel. Each leg of the multi-phase Buck converter is operated with a phase difference of \( 360^\circ/N \) (where \( N \) is the number of phases). This type of “interleaving” reduces the output voltage ripple and input current ripple.

For modern microprocessor devices, these converters must be capable of providing a tightly regulated low voltage with extremely high and dynamic load currents. For example, Intel’s recent VRM 11.0 specification [2] for its Xeon processor (see Figure 1.3), specifies that the VR must be able to supply continuous load currents of 130A and peak load currents of 150A at output voltages ranging from 0.83125V to 1.6V. Load current transitions as much as 100A with a slew rate of 1200A/\( \mu \)s may occur at the microprocessor socket [2].
Tight restrictions on the output voltage deviation are present during such load transients. For example, if a microprocessor were to suddenly change its supply requirements from 125A to 25A, the output voltage is allowed to increase by no more than 150mV, depending on the processor type [2]. In Figure 1.4, an industrial 3-phase voltage regulator for CPU (AMD Athlon 64/X2) in a motherboard is shown and 13 bulky capacitors (10 * 820 μF + 3 * 330 μF) are required to meet the output voltage regulation requirement but occupy a large board area.

---

2 This figure is from online source at [http://www.intel.com](http://www.intel.com)
Figure 1.4 The board features a 3-phase voltage regulator for a processor with 10 x 820 μF and 3 x 330 μF output capacitors.\(^3\)

The requirements to supply a highly dynamic current with a tightly regulated voltage tend to oppose each other. Significant output voltage variations occur during large load transients for a Buck converter. Figure 1.5 illustrates the response of a typical single-phase Buck converter to the load current rapidly stepping from a low load current to a high load current.

\[\text{Load current } i_o, \quad \text{Capacitor current integral}, \quad \text{Inductor current } i_L, \quad \text{Nominal reference voltage } V_{\text{ref}}, \quad \text{Output voltage } v_o\]

\(^3\) This figure is from the online sources at [http://www.ixbtlabs.com](http://www.ixbtlabs.com)
As shown, the inductor current’s inability to vary at the speed of the load current causes the output capacitor to provide the necessary current to supply the load. This, in turn, will cause the output voltage to vary from its designed nominal voltage due to the capacitor discharging. Conversely, a fast “step-down” load transient would result in a voltage overshoot caused by capacitor charging.

As will be discussed, it is the main motivation of this thesis to minimize the magnitude and duration of an output voltage deviation (to the nominal reference voltage) caused by rapid load transients.

### 1.3 Motivation of Thesis

As mentioned, the primary motivation of this thesis is to minimize the magnitude and duration of output voltage deviations due to the CPU load transients. However, it is an important goal to achieve this in a practical and relatively inexpensive manner. The load transient response of a Buck converter can be improved by modifying the following parameters of the converter:

1. Decrease the output inductor value: This will allow the inductor current to slew toward the new load current at an increased rate, thereby decreasing the time that the capacitor is required to charge/discharge, thus decreasing the magnitude and duration of the voltage deviation. However, decreasing the inductor value will increase the steady-state inductor ripple current, increasing the switching loss of the MOSFET and also increasing the steady-state output voltage ripple. [3]

2. Increase the output capacitor value: The voltage of a larger capacitor will vary less for a fixed amount of capacitor charge/discharge. However, output capacitors make up the most expensive component of a VR. Increasing the number of capacitors will drive up the cost and size of the VR. [3]
3. Increasing the switching frequency: This will increase the speed at which the converter can react to a load transient; however, this process will increase the switching loss, and thus, decrease the efficiency of the converter. [3]

Thus, it is noted that there is no “free” method to improve the transient response of a Buck converter. Therefore, it is the motivation of this thesis to improve the transient response of a Buck converter through controller improvements or small modifications to the Buck converter topology, which possess fewer drawbacks than the methods presented above.

1.3.1 Design Digital Controller which Incorporates Near-Optimal Control, Unloading Transient Improvement and Load-Line Regulation

While analog control has long been the staple for Buck converter applications, digital control offers many advantages such as:

1. Robustness: not susceptible to compensator tolerances
2. Re-programmability: easy to modify control law
3. Noise immunity: digital calculations are not susceptible to noise

In addition, digital control allows for the implementation of promising new technologies such as:

1. Parameter identification and controller auto-tuning [4]-[8]: the ability for a controller to identify a Buck converter’s parameters and adjust the control law accordingly,
2. On-the-fly efficiency improvements [9]-[12]: the ability for a controller to monitor efficiency and optimize control parameters,
3. System-level communication [13]: the ability of converters to interact with each other and modify behavior to optimize system-level performance.
Such advantages provide the motivation for Chapter 3 and Chapter 4 to design non-linear digital controllers, capable of nearly optimizing the transient response of a Buck converter.

In addition, the controller will be designed such that it can be implemented with load-line regulation (also known as adaptive voltage positioning (AVP)). Load-line regulation involves outputting a lower voltage at higher load currents. Load-line regulation is a requirement for many modern converter applications as it improves power consumption and the system’s overall transient performance.

In correspondence to previous objectives, the goal is to design the digital controller without the need for large digital two-dimensional look-up tables (LUTs). Thus, the control law will be designed with simple mathematical functions such as addition, subtraction and coefficient multiplication. Also, the requirement of current sensor will be removed for design simplicity and low cost. From the algorithm points of view, 1) the algorithm will be suitable for low-ESR (Equivalent Series Resistance) designed Buck converter and parameter-insensitive to the output filter parameter variations; 2) to extend the charge balance concept to generally designed Buck converters, an output voltage curve fitting methodology will be developed to compensate the ESR impact.

The proposed digital schemes will be suitable for DSP implementation, so that the customers can apply the proposed technologies immediately to their products.

1.3.2 Improve Transient Response to Near-Optimal Levels through Low-Cost Analog Control Scheme

A significant limiting factor to the transient response of a Buck converter is its controller’s inability to react quickly and intelligently to load current transients. Typically, feedback controllers with linear compensators have been used as a “tried-and-true” method to control Buck converters. The design of such controllers often involves tradeoffs between reaction speed (which
dictates the resulting voltage deviation) and settling time. However, for Buck converter applications, it is often necessary to optimize both.

Therefore, as will be presented in Chapter 5, significant research has been performed investigating non-linear controllers with the ultimate goal of improving the transient response (voltage deviation magnitude and duration) of a Buck converter to its physically-optimal levels.

The main drawback of such previously-proposed solutions is that they often possess complex mathematical operations (e.g. multiplication/division/square-root) in their control laws requiring expensive, slow analog multiplier/divider. Since the main motivation of improving the Buck converter’s control is to provide a relatively inexpensive method of improving its transient response, such complex methods do not serve this need.

Thus, the main objective of the work presented in Chapter 5 is to develop an analog controller capable of improving a Buck converter’s transient performance to its near-physical limits without the need for complex circuitry. It is the objective to develop a controller requiring only simple mathematical functions (such as addition, subtraction, amplification) using only standard analog circuits such as operational amplifiers (OPAMPS), comparators, and analog switches. Compared to the DSP charge balance controller, the analog implementation will significantly reduce the operating power consumption and it can be integrated to an analog controller IC in the industry.

1.3.3 Improve Unloading Response of a Buck Converter through a Small Topology Modification

As the transient performance of a Buck converter is pushed to its physical limits by the controller presented in Chapter 3, an interesting phenomenon occurs. The voltage deviation magnitude and settling time is significantly larger for an unloading transient (high load current to low load current) than it is for a loading transient (low load current to high load current). Referring to Figure 1.5, this imbalance is caused by the fact that, for a Buck converter with a very
small conversion ratio (e.g. 12V → 1.5V), the rising slew rate of the inductor current is much
taller than the falling slew rate of the inductor current. Therefore, when an unloading transient
occurs, it takes significantly longer for the inductor current to slew to the new load current than it
does when a loading transient occurs.

This is a cause for concern when designing a Buck converter since the output filter (output
inductor and capacitor) design must be based on the required voltage regulation criteria and the
worst case load transient conditions. Therefore, improving the loading transient will not result in
fewer output capacitors unless the unloading transient can be improved beyond the Buck
converter’s natural physical ability.

As will be discussed in Chapter 2, previously-proposed solutions have been presented to
improve unloading transients. However, many solutions involve auxiliary switching circuits with
unregulated currents and switching frequencies. Such unregulated auxiliary circuits may result in
potentially-damaging thermal conditions.

Thus, the main objective in Chapter 6 is to design an auxiliary current, (and related auxiliary
controller), to improve the unloading transient of a Buck converter. The objective is to ensure that
the circuit conducts a regulated current, and switches at a constant frequency for a controlled
duration dependent on load transient conditions. As will be demonstrated, a significant reduction
in output capacitor requirements can be realized through the addition of a small auxiliary circuit.
Thus, the proposed topology improvement meets the objective of improving a Buck converter’s
transient performance while not significantly increasing cost.

1.4 Thesis Organization

This thesis consists of seven chapters. Chapter 1 provides an introduction to the challenges
pertaining to improving the transient performance of Buck converter applications. Chapter 2
provides a critical overview of previously-proposed control methods and topology modifications
to improve the transient performance of a Buck converter. Chapter 3 introduces an output voltage sensing based digital charge balance controller, which is capable of optimizing the Buck converters without relying on the knowledge of design parameters. Chapter 4 discusses an enhanced charge balance controller. Based on proposed curve fitting methodology, the ESR impact can be compensated, so that this algorithm can be applied for large ESR designed Buck converters without sacrificing the robustness. Both of the algorithms proposed in Chapter 3 and 4 can be extended to adaptive voltage positioning (AVP) applications. In addition, the current sensorless AVP technique is outlined in Chapter 4. In Chapter 5, a novel analog implementation of charge balance controller is presented, resulting in low cost, low power consumption, and easy integration of the controller. Chapter 6 introduces a boundary conductive mode (BCM) peak current controlled auxiliary circuit for further improving the unloading transient performance. As a result, the output voltage overshoot can be significantly reduced, and the power loss of the auxiliary circuit is decreased. Furthermore, a simplified linear mode controller is proposed to address the “Multiple Consecutive Load Transients” issue and meet the requirements of fast load transient test. Chapter 7 presents a summary of the work presented and some recommendations for improvements and future work. All the following chapters will first present the high-level concept of operation, followed by any necessary mathematical proofs, followed by dedicated implementation and operation descriptions, and then followed by simulation and experimental verification.
Chapter 2

Classical and Modern Control Schemes on Buck Converters

2.1 Introduction

This chapter will provide a review of previously-presented literatures pertaining to methods of improving the transient response of high-current, low-voltage DC-DC converters. Section 2.2 will provide a brief overview of typical analog linear controllers and their common drawbacks. To analyze their dynamic performance, a unified small signal model is built to explain the distortion rejection capabilities of different disturbances. Section 2.3 will provide an overview of analog non-linear control solutions, including most popular ripple based regulators, such as hysteretic controller, $V^2$ controllers, and RPM controller. Also the small signal analysis has been conducted to demonstrate the benefits of this controller and the limitations. In Section 2.4, performance enhancement of digital control technologies on power electronics is outlined from the aspect of dynamic response improvements. Many state-of-art digital control concepts are introduced. Section 2.4.3 will also examine previously-proposed, so-called charge balance controller (a.k.a. minimum time controllers). Section 2.5 will examine a sample of previously-proposed topology modifications to the Buck converter to improve its transient response. Section 2.6 outlines the existing control schemes for the topology modification. Section 2.7 is the conclusion of this chapter.

2.2 Classical Linear Controllers and Modeling

This section will provide a brief overview of classical linear controllers and outline their fundamental transient response drawbacks. For example, the most straight-forward linear controller will be presented, the voltage mode controller.
While linear voltage mode control (also known as direct duty cycle control) is certainly not the most effective control method (in terms of dynamic response), it is arguably the most popular control method. A large sample of Buck converter controllers available from semiconductor companies (such as ON Semiconductor, Intersil, Texas Instruments and Maxim) utilizes linear voltage mode control. Its popularity is mainly due to the simplicity and intuitiveness of the design procedures to any engineer who is moderately versed in linear control theory.

A simplified block diagram of a voltage mode control feedback loop is shown in Figure 2.1.

As shown, the output voltage is subtracted from the reference voltage and passed through a linear compensator. The transfer function of the compensator is designed using traditional continuous control techniques (such as Bode plot analysis). There are two general types of voltage mode compensators: a) Type II compensator, which consists of two poles and one zero (shown in Figure 2.2(a)), b) Type III compensator, which consists of three poles and two zeros (shown in Figure 2.2(b)).
The decision to use a Type II or Type III compensator depends on the degree of freedom required to design a stable system. The transfer functions for a Type II and Type III compensator are expressed in (2.1) and (2.2) respectively.

\[
\frac{v_{\text{con}}(s)}{v_{\text{err}}(s)} = R_1 C_1 \left( s + \frac{1}{R_2 C_2} \right) \left( s + \frac{C_1 + C_2}{R_2 C_1 C_2} \right) (2-1)
\]

\[
\frac{v_{\text{con}}(s)}{v_{\text{err}}(s)} = \frac{R_1 + R_3}{R_1 C_1 R_3} \left( s + \frac{1}{R_2 C_2} \right) \left( s + \frac{1}{(R_1 + R_3) C_3} \right) \left( s + \frac{C_1 + C_2}{R_2 C_1 C_2} \right) \left( s + \frac{1}{R_3 C_3} \right) (2-2)
\]

The yielding control voltage \( v_{\text{con}} \) is compared with a saw tooth waveform in order to produce a constant-frequency, pulse width modulated output.

Figure 2.3 illustrates an example of a linearly controlled Buck converter undergoing a step-up load transient.
First, it is shown in Figure 2.3, that following the load current step, the controller cannot immediately react (and turn on the control switch) due to its constant-frequency synchronous operation. The controller must wait until the succeeding clock pulse before the control switch is turned on again. Furthermore, due to the finite bandwidth of the linear compensator, it is shown that the control voltage $v_{\text{con}}$ cannot increase at a sufficient rate. The compensator bandwidth is designed to be a fraction of the switching frequency ($1/3-1/5$) for the purpose of noise attenuation and system stability. These two factors combined cause the capacitor discharge integral (shaded area in Figure 2.3) to be much larger than the ideal case (shown as a dashed line in Figure 2.3).

Since the bandwidth of the compensator is designed related to the switching frequency, an obvious solution to improve the above drawbacks would be to simply increase the switching frequency of the converter; however, due to the frequency-dependant losses of a Buck converter (MOSFET gate loss, switching loss, inductor core loss), this would significantly harm the efficiency of the converter.
There exist many other types of linear controllers commonly used, such as peak current-mode control and average current-mode. These control schemes control the PWM of a Buck converter using output voltage and inductor current feedback information, as shown in Figure 2.4.

![Figure 2.4 Linear current-mode control: (a) Peak current-mode, (b) Average current-mode](image)

These controllers do possess advantages over the voltage-mode controller such as faster reaction to input voltage changes. And in the case of peak current-mode control, simplified compensation is implemented without error amplifier (EA)

To demonstrate the transient performance for different control methods, mathematical modeling is a helpful tool. Small signal model is a widely used modeling technique to analyze power converter systems, based on which the power converter can be linearly modeled and the compensator can be designed using continuous time method, like Bode plots and other sophisticated linear system methods [15][16][17].

The unified small signal model (USSM) structure is shown in the Figure 2.5 and four instantaneous feedback information sources may be available to drive and change the duty ratio $d$, which are the perturbations of input voltage $v_{in}$, control command voltage $v_{con}$ (from your error amplifier), inductor current $i_L$ and output voltage $v_o$. All the negative signs at the summator indicate that the negative instantaneous feedbacks will drive the duty ratio $d$ inversely, (for example, the increasing $v_{in}$ will lower the duty ratio) and $v_{con}$ represents the outer loop compensator control command/inner loop control reference in dual loop control. However, if any
transfer gain represents a negative value, it will result in a positive feedback, causing instable loop.

\[ d \]

\[ F_m \]

\[ F_g \]

\[ F_v \]

\[ F_L \]

\[ v_g \]

\[ v_c \]

\[ v_o \]

\[ i_L \]

Figure 2.5 Unified small signal model architecture

For voltage mode control, when we substitute the transfer gain results into the USSM structure, it is noted that since only one control loop is involved, no instantaneous feedback gains are available except the PWM modulator gain \( F_m = \frac{1}{V_m} \). That’s the reason that voltage mode control has no rejection capability of disturbance from output voltage, load current and input voltage.

In order to regulate the duty cycle of the converter, the only way is to wait for the variation of controller output command \( v_{con} \), but the control command has been filtered and slowed down by the linear mode compensator, such as Type II or Type III compensator.

Similarly, the same USSM can be applied to the peak current mode controller for performance analysis.
According to the Figure 2.6 above, we can derive the following equation, where $m_c$ is the slope of the artificial ramp, while, $m_1$ and $m_2$ are the rising and falling slopes of inductor current.

$$i_L + m_1 \frac{dT_s}{2} = v_{con} - m_c dT_s \quad (2-3)$$

So the instantaneous duty cycle can be expressed as

$$d = \frac{(v_{con} - i_L)}{\frac{m_1 T_s}{2} + m_c T_s} = \frac{(v_{con} - i_L)}{nM_1 T_s} \quad (2-4)$$

Where,

$$n = 1 + \frac{2M_c}{M_1} \quad (2-5)$$

We can get the small signal model by substituting dc component and small signal ac perturbation to the equation (2.4).

$$D + d = \frac{\left(\hat{V}_c + \hat{v}_c\right) - \left(\hat{I}_L - \hat{i}_L\right)}{\left(M_1 + m_1\right) T_s + M_c T_s} \quad (2-6)$$

Then the dc solution of the duty ratio $D$ can be derived as:
\[ D = \frac{2}{nM_1T_s} (V_{con} - I_L) \]  \hspace{1cm} (2-7)

Similarly, the small signal ac solution is solved by using the following equation:

\[
\dot{d} = \frac{2}{nM_1T_s} \left( \dot{v}_{con} - \dot{i}_L \right) - \frac{D}{nM_1} \hat{m}_1 
\]  \hspace{1cm} (2-8)

For a Buck converter, in the above equations, \( m_1 = \frac{v_{in} - v_o}{L_o} \), \( M_1 = \frac{Dv_o}{D_L} \), and \( \hat{m}_1 = \frac{v_{in} - v_o}{L_o} \). And for simplification, it is assumed the inductor sensor gain is unity. So the simplified ac solution can be written as (2.9) based on the aforementioned relationships and definitions.

\[
\dot{d} = K_{sRD} \left( \dot{v}_{con} - \dot{i}_L \right) - \frac{D^2}{nD} v_{in} + \frac{D^2}{nD} v_o 
\]  \hspace{1cm} (2-9)

Recall the USSM structure in Figure 2.5 and we can plug in the transfer gains to the unified small signal model, where \( K_s = \frac{2L_o}{R T_s} \), \( F_v = -\frac{D}{K_s R} \), \( F_i = 1 \), \( F_g = \frac{D}{K_s R} \), and \( F_m = \frac{K_s R D}{nD v_o} \).

All the instantaneous feedbacks are available in the peak current mode control but the negative \( F_v \) makes the peak current mode control suffer from the slow external voltage loop. Chaos phenomenon for peak current mode controlled Buck converter could happen by this positive feedback [14].

Although current mode controllers can provide better dynamic performance than voltage mode controllers, they still suffer from the slow reaction illustrated in Figure 2.3 due to their synchronous switching properties and the compensator’s speed limitations.

Ideally, a controller would react asynchronously and turn the control switch on for at least the duration required for the inductor current to equal the new load current. Therefore, considerable research has been performed investigating non-linear asynchronous controllers. And the most
popular analog nonlinear controllers are ripple based regulators, which will be reviewed in the next section.

2.3 Ripple based Regulators [18]

2.3.1 Hysteretic Voltage Mode Controllers

Hysteretic voltage-mode control is clearly the simplest and most intuitive control method available. The concept is simple: when the output voltage is too low, set the PWM signal high; when the output voltage is too high, set the PWM signal low. The controller is analogous to a simple thermostat. A block diagram is illustrated in Figure 2.7. Since the controller does not use a compensation network, the converter is able to react quickly to a transient event making it seem like an ideal candidate for voltage regulator modules. However, a critical drawback of the voltage-mode hysteretic controller is its reliance on the converter’s output capacitor parasitics.

![Figure 2.7 Hysteretic voltage-mode controller](image)

Although the hysteretic controller is essentially free from large-scale instability, the practical limitation is the large sensitivity of the switching frequency to the capacitor parasitics and hysteretic delays. The switching frequency of a hysteretic voltage-mode controller under CCM is expressed in (2.10).
ESR equals the output capacitor’s equivalent series resistance. ESL represents the output capacitor’s equivalent series inductance. $T_{\text{del, hys}}$ represents the hysteretic comparator delay and $V_{\text{hys}}$ represents the hysteretic band voltage. It is observed in (2.10) that the converter’s ESR and hysteretic band voltage $V_{\text{hys}}$ have a drastic effect on the converter’s switching frequency. Therefore, if ESR, or ESL are varying over time and/or thermal conditions, the switching frequency will change significantly. In addition, due to the small steady-state output voltage ripple for low-ESR converters, the extremely small band can be dominated by switching noise (rather than the natural output voltage ripple), which will cause instability. These factors alone make the controller impractical for low ESR converters.

On the other hand, when the controlled converter is operating under DCM, the switching frequency will be proportional to the load current level; therefore, a good efficiency is maintained at light load condition. However, the dc output voltage regulation performance is poorly influenced by the load current level. The dc output voltage drops with the decreasing load current.

2.3.2 Combined Linear and Non-Linear Control - V$^2$ Controllers and Modeling

In order to benefit from the fast reaction exhibited by hysteretic voltage-mode control while still keeping beneficial features such as fixed steady-state switching and zero steady-state error, a combined linear and non-linear controller is presented in [19].

While not a pure hysteretic controller (as it does not use a hysteretic comparator), the V$^2$ controller is worth mentioning as it behaves similar to a hysteretic controller. The V$^2$ controller has drawn substantial interest due to its simplistic nature and excellent dynamic response. Like linear voltage-mode control, the controller constructs a control voltage that is produced by a
compensator. However, unlike linear voltage mode control, the control voltage is modulated by the triangular waveform of the output voltage itself. The controller is illustrated in Figure 2.8.

![Figure 2.8](image)

Figure 2.8 Original $V^2$ converter concept without enhancement

![Figure 2.9](image)

Figure 2.9 $V^2$ control without artificial ramp

We can analyze the dynamic characteristics of the $V^2$ controller by using the aforementioned unified small signal model. According to the output voltage ripple $v_o$ and the compensator output voltage $v_{con}$ in Figure 2.9 above, we can derive the following equation in (2.11).

$$\frac{1}{2} m_1 d T_s = v_{con} - v_o$$  \hspace{1cm} (2-11)

Similarly, we can calculate the small signal model by substituting dc and ac signal to the equation (2.11).
\[ D = \frac{2}{M_1T_s} (V_{con} - V_o) \]  

(2-12)

\[ \hat{d} = K_sRD \left( \frac{\hat{V}_{con} - \hat{V}_o}{ESR} \right) - \frac{D^2}{D'V_o} \dot{V}_{in} - \frac{D^2}{D'V_o} \dot{V}_o \]  

(2-13)

Similar to the peak current mode control, to break the maximum operating duty cycle constraints at 50\%, an artificial ramp is added to the V^2 control scheme shown in Figure 2.10 and Figure 2.11.
According to the geometrical relationship of the ripples above, we can write the following equation (2.14).

\[
\frac{1}{2} m_i d T_s = v_{\text{con}} - v_o - m_i d T_s \tag{2-14}
\]

The small signal model can be derived by substituting dc and ac information to the equation in (2.15).

\[
d = K_{RD} \frac{v_{\text{con}} - v_o}{n D V_o} - \frac{D^2}{n D V_o} v_{\text{in}} - \frac{D^2}{n D V_o} v_o \tag{2-15}
\]

where,

\[
n = 1 + \frac{2 M_c}{M_1} \tag{2-16}
\]

Recall the USSM structure and we can plug the transfer gain expressions into the unified small signal model in Figure 2.5.

where \( F_v = \frac{K_{RD}}{n D V_o ESR} + \frac{D^2}{n D V_o}, \) \( F_i = 0, \) \( F_g = \frac{K_{RD}}{n D V_o ESR}, \) and \( F_m = \frac{D^2}{n D V_o}. \)

The instantaneous feedback signal of inductor current is still not available in \( V^2 \) control; Positive \( F_v \) provides the fast response for the output voltage distortion, therefore, the \( V^2 \) control can achieve fast output voltage regulation. However, the transfer gain \( F_i \) between \( i_L \) and \( d \) is zero, which means the inductor current or the load current is out of direct control. The controller cannot response immediately for load current transient until the output voltage deviation occurs. In the meanwhile, as previously discussed, \( V^2 \) controller is not suitable for voltage regulation of low \( ESR \) designed converters (such as low voltage VRs using ceramic capacitors for the output dc capacitor bank), when the output voltage ripple is not in phase with the inductor current. One straightforward solution is to introduce the inductor current information in the feedback loop on
top of the capacitor output voltage ripple shown in Figure 2.12. This scheme is commonly referred to as “enhanced V² control”[19]. In the analysis below, the inductor sensing gain is $R_s$.

![Enhanced V² controller with inductor current feedback to improve performance of load current transient](image)

Figure 2.12  Enhanced V² controller with inductor current feedback to improve performance of load current transient

![Enhanced V² control with artificial ramp](image)

Figure 2.13  Enhanced V² control with artificial ramp

According to the Figure 2.13 above, we can write the following equation (2.17), geometrically.

$$\frac{1}{2} m_1 dT_s = v_{con} - \left( v_o + i_z R_s \right) - m_2 dT_s \quad (2-17)$$

We can get the small signal model by substituting dc and ac signal to the equation (2.18).
\[ d = \frac{K_{RD}}{nD'V_o} \left( \frac{\hat{v}_{\text{con}} - \hat{v}_o - R_s \hat{i}_L}{nD'V_o} - \frac{D^2}{nD'V_o} \hat{v}_{\text{in}} - \frac{D^2}{nD'V_o} \hat{v}_o \right) \]  

(2-18)

Where,

\[ n = 1 + \frac{2M_e}{M_i} \]  

(2-19)

With the compensation ramp the duty ratio constraint does not exist anymore. The inductor current \( i_L \) in the internal loop contributes piece-wise linear voltage ripple to the output voltage \( v_o \) and the resulted voltage \((v_o + i_L R_s)\) will be compared with the compensator control voltage command \( v_{\text{con}} \).

Recall the control structure in Figure 2.5. We can build the unified small signal model for enhanced \( V^2 \) controller using (2.18), where, \( F_v = \frac{K_{RD}}{nD'V_o \cdot \text{ESR}} + \frac{D^2}{nD'V_o} \), \( F_i = \frac{K_{RD} - R_s}{nD'V_o} \), and \( F_g = \frac{D^2}{nD'V_o} \), and \( F_m = \frac{K_{RD}}{nD'V_o \cdot \text{ESR}} \)

The instantaneous feedback signal of inductor current is available in enhanced \( V^2 \) control; Positive \( F_v \), \( F_i \), and \( F_g \) provide the fast response for the output voltage and inductor current distortions, so that the enhanced \( V^2 \) control can achieve ultra-fast response.

In conclusion, the dynamic performance of voltage mode, current mode, \( V^2 \) and enhanced \( V^2 \) is listed in Table 2-1. The positive direct transfer gains indicate that the capabilities of suppressing the disturbances from the noise sources \((v_{\text{in}}, v_o \text{ and } i_L)\). On the contrary, as previously discussed, the negative gain will cause a positive feedback loop which may create stability issue. It is worth noting that with ripple based regulators the fast transient response is always achieved for input voltage \( v_{\text{in}} \).
Table 2-1: Gains of the unified small signal model of different controllers

<table>
<thead>
<tr>
<th></th>
<th>Voltage Mode</th>
<th>Current Mode</th>
<th>( V^2 ) Control</th>
<th>Enhanced ( V^2 ) Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>( F_v )</td>
<td>0</td>
<td>( F_v = -\frac{D}{K_s R} )</td>
<td>( F_v = \frac{K_s R D}{nD'V_o \cdot ESR} + \frac{D^2}{nD'V_o} )</td>
<td>( F_v = \frac{K_s R D}{nD'V_o \cdot ESR} + \frac{D^2}{nD'V_o} )</td>
</tr>
<tr>
<td>( F_i )</td>
<td>0</td>
<td>( F_i = 1 )</td>
<td>0</td>
<td>( F_i = \frac{K_s R D \cdot R_s}{nD'V_o} )</td>
</tr>
<tr>
<td>( F_g )</td>
<td>0</td>
<td>( F_g = -\frac{D}{K_s R} )</td>
<td>( F_g = \frac{K R D}{nD'V_o \cdot ESR} )</td>
<td>( F_g = \frac{D^2}{nD'V_o} )</td>
</tr>
<tr>
<td>( F_m )</td>
<td>( F_m = \frac{1}{V_m} )</td>
<td>( F_m = \frac{K_s R D}{nD'V_o} )</td>
<td>( F_m = \frac{D^2}{nD'V_o} )</td>
<td>( F_m = \frac{K_s R D}{nD'V_o \cdot ESR} )</td>
</tr>
</tbody>
</table>

And the comparative rating of different controllers is tabulated in Table 2-2, where “0”, “√”, and “×” represent the dynamic performance of “neutral”, “positive” and “negative”, respectively.

Table 2-2 Comparison and rating of different controllers

<table>
<thead>
<tr>
<th></th>
<th>Voltage Mode</th>
<th>Current Mode</th>
<th>( V^2 ) Control</th>
<th>Enhanced ( V^2 ) Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_{in} )</td>
<td>0</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>( i_L )</td>
<td>0</td>
<td>√</td>
<td>0</td>
<td>√</td>
</tr>
<tr>
<td>( v_o )</td>
<td>0</td>
<td>×</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td><strong>Overall</strong></td>
<td>0</td>
<td>√</td>
<td>√√</td>
<td>√√√</td>
</tr>
</tbody>
</table>

2.3.3 RPM Controller

“Ramp Pulse Modulation,” or RPM, is a combined dc regulation and transient response improvement technique for voltage regulators. Compared with constant-on-time control [18][20], RPM uses the same dual-function (error and ripple) amplifier as shown in Figure 2.14, but it is modified for improved unloading transient response.
RPM controller is capable of adaptively controlling the turn-on time during the unloading transients. This is achieved by comparing the ramp voltage with the compensator output $V_{con}$ as the threshold for the comparator that terminates the timing ramp. The illustration is shown in Figure 2.15.
Besides the advantages of fast transient performance and improved efficiency at light load condition, it is found that the RPM controller has another merit to avoid beat frequency oscillation. The beat frequency oscillation is usually caused by the constant frequency pulse width modulator (PWM) and the frequency of load current step transients.
Figure 2.16 shows the simplified waveforms of PWM. $V_{\text{ramp}}$ is the ramp voltage, $d$ is the duty cycles, $I_L$ is the inductor current and $V_O$ is the output voltage. The control voltage ($V_C$) fluctuates with the load current step frequency ($f_{Io}$) since the compensation loop attenuation at $f_{Io}$ is normally small to increase the transient response speed of VR. Output voltage disturbance from the load current is shown at the control output command. The control output command intersects the ramp with the switching frequency ($f_s$) to generate the duty cycles. The two frequency components in PWM ($f_{Io}$ and $f_s$) introduce the beat frequency component in the duty cycles and this beat frequency component is shown in the inductor current and the output voltage. If the load current step frequency ($f_{Io}$) is close to the switching frequency ($f_s$), the beat frequency component is in low frequency and it cannot be filtered out by the output inductor and the capacitors. This beat frequency component is also fed back to the modulator through the compensator presenting in the closed loop system.

Several solutions have been presented to solve this problem by applying the filter concepts, such as tuning notch filter at the beat frequency or reducing the gain of Type III compensator at beat frequency. However, both solutions suffer from the double-edged sword effects, that is, slowing down the desired transient response performance. On the contrary, due to the variable switching frequency operation at different load conditions, the RPM controller can inherently fix this problem [21].

As recently summarized in [18], hysteretic regulator, $V^2$ controller and RPM controller can be categorized as ripple regulators, which share some common features such as fast response performance to transient perturbations. However, on the other hand all of them suffer from one or more of the following drawbacks:
1. Variable operating switching frequency: The poorly defined switching frequency has a strong dependency on the parasitics of the output capacitors, propagation delays, input and output voltage and load current;

2. Poor noise immunity or jittery behavior: The noise generated from electromagnetic interference (EMI) or another converter on the same circuit board will lead to jittery issue due to the small amplitude of the PWM ramp;

3. Limited dc regulation performance: Propagation delays, ESL and ESR of the output capacitors will degrade the dc output regulation accuracy;

4. Fast-scale/Subharmonic instability: Some ripple regulators suffer from subharmonic oscillation, if the time constant (ESR \cdot C_o) is smaller than a certain fraction of the set on-time, off-time or clock period.

5. Application/topology limitations: The ripple based regulator can only be used to control the converters with output inductor, such as Buck converters, Cuk converters and Zeta converters. However, the practicality for Cuk and Zeta converters has not yet been verified through experimental results.

In order to minimize both the output voltage deviation and the settling time of a Buck converter, digital control technologies have been investigated, as summarized in the following section.

2.4 Dynamic Performance Enhancement with Digital Control Technology

Digital control is well-suited for the development of adaptive tuning and hybrid linear/nonlinear controllers, which enhance the dynamic performance of dc-dc converters significantly. In this section, the recent research on the digital system identification, digital autotuning and capacitor charge balance controller will be discussed.
2.4.1 Digital System Identification Controller

One advanced application area for digital control on Dc-Dc converter is system identification. System Identification is a crucial function block for autotuning, adaptive control, etc, to achieve the desired plug-and-play capability. One nonparametric method to identify the converter system model is correlation analysis, which has been found to be feasible for digital implementation [22][23]. Under the assumption that, in steady state, for small-signal disturbances, a power converter can be modeled as a linear time-invariant discrete-time system, the sampled system can be described by

$$y(n) = \sum_{k=1}^{\infty} h(k) u(n-k) + v(n)$$

(2-20)

where $y(n)$ is the sampled output signal; $u(n)$ is the input digital control signal; $h(k)$ is the discrete-time system impulse response; and $v(n)$ represents disturbances, including switching noise, measurement error, quantization noise, etc.

The cross-correlation of the input control signal and the output signal is

$$R_{uy}(m) = \sum_{n=1}^{\infty} u(n)y(n+m) = \sum_{n=1}^{\infty} h(n)R_{uu}(m-n) + R_{uv}(m)$$

(2-21)

where is $R_{uu}(m)$ the auto-correlation of the input signal $u(n)$. Now, if the input control signal is selected to be the white noise, then we will benefit from the following characteristics:

$$\begin{cases} R_{uu}(m) = \delta(m) \\ R_{uv}(m) = 0 \end{cases}$$

(2-22)

In other words, the auto-correlation of the input is an ideal delta function and the cross-correlation of the white noise input with disturbances is ideally zero. Under the conditions of (2.22), the cross-correlation of (2.21) can be reduced to
\[ R_{xy}(m) = h(m) \] (2.23)

Therefore, the digital controller presented in [22] applies the cross-correlation of the input and output signal to estimate the frequency response of the converter, Dc-Dc forward converter [3][17] in this case. The digitalized input signal pseudo random binary signal (PRBS) is analogue to the white noise in analog system, which can be generated by using shift register. And the calculated cross-correlation will be transformed by using Discrete Fourier Transform in (2.24).

\[ R_{xy}(m) \xrightarrow{DFT} H(j\omega) \] (2.24)

But for a single period PRBS sequence, the high frequency responses obtained by the identification method are significantly corrupted by noise. So a multiperiod pseudo random binary signal (PRBS) is injected as the input signal and the cross-correlation is averaged to suppress noise at the high frequency in the Bode plots (frequency response). An experimental digitally controlled forward converter with an FPGA-based controller is used to demonstrate accurate and effective identification of the converter control-to-output response.

![Figure 2.17 Forward converter with input filter and digital controller block diagram.](image)
In [23], another method is proposed to reduce the noise at high frequency in the Bode plots. Before injected into the converter loop during steady-state, the single PRBS is pre-emphasized by a high pass digital filter block to enhance the high frequency components. The sampled output voltage will pass through the De-emphasis block to cancel out the pre-emphasis effects. Experimental results are provided for four different PWM dc–dc converters, including a synchronous buck with two different filter capacitors, a boost operating in continuous conduction mode (CCM), and a boost operating in discontinuous conduction mode (DCM).

![Complete system identification process with preemphasis, deemphasis and spectral smoothing technique](image)

### 2.4.2 Autotuning

“Autotuning” is an exclusively digital tool that has tremendous marketing potential. The idea of a “plug-and-play” controller that can automatically identify and control a converter has attracted interest from both industry and academia. Typically, analog inductor current measurement has only been as accurate as the model of the converter. Inductor current measurement is often necessary for over-current protection, multiphase current balancing, and load-line regulation. A popular analog current measurement method is to add a parallel $RC$ branch across the output inductor and measure the voltage across the capacitor of the parallel branch. For correct current measurement, the time constant of the $RC$ branch should be equal to the time constant of the inductor and its parasitic dc resistance (DCR). However, inductor
tolerances along with varying thermal conditions that cause varying DCR present challenges to precise inductor current measurement.

Figure 2.19  Digital tuning of an analog RC inductor current sensor

In [24], a controller is presented that automatically tunes an analog RC current measurement sensor by use of a digital potentiometer (see Figure 2.19). It accomplishes this by simply observing the output voltage slope of a load-line regulated converter, following a large-load transient. As shown in Figure 2.20, when the RC filter is properly tuned to the inductor RL constant, the output voltage response is relatively flat when the load current is known to be flat. If the magnitude of the output voltage slope is greater than a specified threshold, the RC constant is adjusted.
Figure 2.20  Autotuning effect on a buck converter with load-line regulation

By use of digital control, it is also possible to predict the converter parameters $L_o$, $C_o$, $ESR$, etc., and automatically calculate control coefficients based on bandwidth and phase margin requirements. This is accomplished in [25]–[29] by injecting a specified frequency into the control loop or by adding/amplifying a nonlinearity that causes the output voltage to oscillate. In [25], the DPWM resolution is intentionally degraded for a short period such that the coarse DPWM resolution will lead to controlled (limit cycle oscillation) LCO. In order to amplify the LCO effect, the digital compensator is temporarily replaced with a PI configuration. By measuring the frequency of the resultant LCO, information related to the converter resonant frequency and output capacitance can be calculated. By measuring the amplitude of the resultant LCO, it is also possible to estimate the Q-factor of the converter (and thus, the load resistance/current). The information is used to design a proper PID by extracting appropriate parameters from LUTs (provided that the load current remains relatively constant).
In [26] and [27], autotuning is accomplished by introducing a nonlinear relay into the control loop, as shown in Figure 2.21. The relay essentially acts as a 1-bit quantizer, causing LCO at the output. When $G_c(z)$ is adjusted to an integrator (causing a $90^\circ$ phase lag in the loop), the output voltage will oscillate at the resonant frequency of the converter. This frequency is measured and stored. This allows for the proper placement of the first zero of a PID compensator. The new PID controller is passed through a low-pass filter to force the desired phase margin at the desired crossover frequency. The second zero is then iteratively placed until the output oscillates at the crossover frequency. After the two zeroes are placed, the compensator gain is set by using the desired bandwidth, zero placement, and an asymptotic Bode plot estimation. The relay function is disabled after the tuning process is completed, allowing for normal loop operation. The advantage of the aforementioned method is that only the frequency of the output voltage oscillation is required to be measured; the amplitude is not required, allowing for more robust operation.
The above-mentioned autotuning algorithms [25]-[28] induce a relatively large voltage oscillation at the output of the converter for a short period of time in order to tune the controller. However, the autotuning algorithm presented in [29] follows a different approach, as illustrated in Figure 2.22. The system operates by continuously injecting a varying frequency square wave $V_z$ into the DPWM input signal $V_x$. The DPWM input signal and the digital compensator output signal $V_y$ are passed through a bandpass filter (bandpass equal to the injected frequency) and measured by the digital stability monitor. The injected frequency is adjusted until the magnitude of the two measured filtered signals are equal (indicating the crossover frequency $f_c$). By comparing the zero-crossover points of the two signals $V_y$ and $V_x$, the phase margin $\phi_m$ of the system can also be calculated. The measured crossover frequency and phase margin are subtracted from the desired crossover frequency and phase margin to produce crossover frequency and phase margin errors ($f_{c,\text{err}}$ and $\phi_{m,\text{err}}$, respectively). A relatively low-bandwidth multi-input–multi-output (MIMO) controller continuously adjusts the controller’s coefficients in an attempt to minimize the $f_{c,\text{err}}$ and $\phi_{m,\text{err}}$. 

Figure 2.22  Autotuning based on continuous phase margin measurement
2.4.3 Minimum Time Control/Charge Balance Control

Minimum time controllers have been presented under many different aliases, such as “time optimal control”, “optimal control”[30], “continuous time control”[34] and “charge balance control”[31][32]. In this thesis, the concept will be referred to as “charge balance control” since the concept involves “balancing” capacitor charge integral regions over the transient period, as will be discussed in Chapter 3, Chapter 4 and 5.

For example, in [32], referring to Figure 2.23, the inductor current and output voltage deviation is sampled twice following the load transient. The information is used to estimate the new load current and to determine the optimal switching periods $T_{up}$ and $T_{down}$ through a set of equations presented in (2.25)-(2.26).

![Diagram](image)

**Figure 2.23** Charge balance controller response to a fast load current change

\[
I_{o2} = \frac{1}{2} \cdot (i_{L1} + i_{La}) - \frac{C_o \cdot (v_{oa} - v_{o1}) - C_o \cdot (i_{La} - i_{L1})}{T_{la}}
\]  

\[ (2.25) \]
\[ T_{up} = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2} \cdot \frac{V_{in} - V_o}{V_o}}} \quad T_{down} = T_{up} \cdot \frac{V_{in} - V_o}{V_o} \]  

(2-26)

Where \( A_0, A_1, A_3 \) are the capacitor charge integral areas that can be geometrically calculated using the estimated load current \( I_o \). As demonstrated, complex mathematical operations such as multiplication, division and square root are required to calculate the switching intervals.

As shown in [32], the controller reacts to the load transient at the next switching cycle. One drawback of non-linear digital controllers (that rely on the ADC to detect load transients) is the inherently delayed response due to the sampling delay. This typically results in larger than necessary voltage deviations, following a load transient. Such delays are not as prevalent in analog non-linear controllers such as voltage-mode hysteretic control. Thus, recent non-linear digital controllers have begun to adopt analog load transient detection or the use of asynchronous ADCs. For example, with the use of asynchronous ADCs, it is possible to detect the load transient with delays comparable to fully-analog controllers.

Based on the successful digital implementation [32], in Figure 2.25, implementation with analog circuit is illustrated. It is noted that this is the first analog implementation of a digital charge balance control algorithm.
In this analog implementation, the time instant \( t_1 \) is determined using a capacitor current sensor (by carefully matching the output capacitance \( C_o \) and \( ESR \)) to sense the capacitor current zero-crossing time instant. In order to represent the charge balance concept for deciding \( t_2 \), in lieu of directly calculating the capacitor charge integral \( A_{\text{discharge}} \) or \( A_{\text{charge}} \), the inductor current slew-rate is referred to as the integrand of a double integration function. And this operation can be simply implemented by OPAMP based circuitry shown in Figure 2.25. At the input end, different dc voltage levels serve as the scaled inductor current slew rate and are selected at the Analog Multiplexer with control signal posStep. To reset the integration, analog switches are used as the feedback resistors of the OPAMPs. And the double integration output \( v_{int2} \) will recover to the initially reset value \( Vcc/2 \), by this means, another critical time instant \( t_2 \) can be detected.
Figure 2.25  OPAMP implementation of double integrator

As shown in Figure 2.26, an asynchronous analog-to-digital controller can also be used to determine the voltage valley point (both magnitude and time instant). The controller proposed in [34] uses this information to calculate the optimal switching time instant. While in [35]-[37], the information is used to calculate the output voltage level at which the controller should alter its switching state. An advantage of the controller presented in [35]-[36] is that the inductor and capacitor values are not required; however, it is assumed that the ESR of the capacitor is negligible. If this is not the case, the capacitor and ESR values would be required in order to compensate.
While asynchronous sampling can be used for charge balance control, there are two potential drawbacks. In order to function correctly, the ADC acquisition delay must be extremely low and the timing resolution of the controller (its system clock) must be very fine. Furthermore, as shown Figure 2.26, the output voltage valley point is always detected after it occurs. In low duty cycle conversion applications (i.e. 12V → 1V), there is the potential that the valley point may be detected after the necessary optimal switching time instant.

The above nonlinear controllers can be extended to multiphase operation [39] and [40]. In [39], rather than minimum recovery time, it compromises the aim only at achieving the minimum voltage deviations. Further, a smooth controller transition is realized by inserting specified ON/OFF sequences right after the capacitor current undergoes zero-crossover, shown in Figure 2.27. However, under unloading step transient, the improvement is minor because the conventional linear mode compensator is still well-suited for regulating the low output ratio converters with sub-optimal voltage overshoot.
In [40], a current mode digital CBC controller is presented for multiphase Buck converters, which takes advantage of peak current control on the phase inductors to achieve minimum recovery time. During transients shown in Figure 2.28, new steady-state current information can be collected at the voltage valley/peak point and the digital peak current reference can be calculated and set based on CBC principles. However, both of the methods [39][40] are still limited for low ESR Buck converters and sensitive for passive components’ value. Also, the controllers will not work as well for example, if an unloading step occurs before the valley point resulted from a previous loading current step is approached.
Figure 2.28 The key waveforms of a single-phase power stage during a light-to-heavy load transient. Top: output voltage; Bottom: the inductor current.

In [41], a digital controller is presented which can achieve smooth transition after large load transients. The output voltage is filtered by matching the output capacitance and ESR to generate the ideal capacitor voltage $v_c$. And the upper and lower thresholds ($v_c^+$ and $v_c^-$) are set to immunize the detection noise and improve stability performance (see Figure 2.29). The output voltage compares with $v_c$ to detect the extreme points, shown in Figure 2.30. The transient mode is activated as soon as a significant load change occurs and is detected by the proposed detector. In the case of a loading step transient, after the first extreme point is detected, the on time of the main switch is extended by $DT_{sw}/2$, to obtain an optimum-deviation response, where $T_{sw}$ is the switching period and $D$ is the steady-state duty-cycle. For a uploading transient, extended off-time $(1-D)T_{sw}/2$ is inserted for optimum-deviation response. However, similar to the controller in [39], the overshoot performance is not improved much by using this controller. Also, filter mismatching may affect the performance of time detection and the controller, resulting from the output capacitance and ESR variations. And a well-designed linear controller should contribute to the smooth transition.
2.4.4 Oversampled Digital Controller

An oversampled digital controller based on successive load-change estimation is presented in [42] for low power dc-dc switched-mode converters with a fast response and reduced switching loss. As shown in Figure 2.31, the main principle of the oversampled controller is illustrated.
Under a large load transient, the digital controller quadruples the steady-state sampling frequency of PID controller to $4f_{sw}$. Using the first voltage sample $v_n$, the PID controller calculates the duty-cycle $d_n$. The successive three oversampled voltage samples are applied for calculation of duty-cycle deviations $\Delta d_{n+1}$, $\Delta d_{n+2}$ and $\Delta d_{n+3}$, equivalently increasing the switching frequency and PID controller operating frequency. However, the efficiency of the dc-dc converter suffers from the increased switching frequency under transients. Compromising the fast dynamic performance and the efficiency, the proposed scheme shown in Figure 2.32, glues $\Delta d_{n+1}$ and $\Delta d_{n+2}$ as one control command and $\Delta d_{n+3}$ is counted to the next control command with $d_{n+1}$. So the switching frequency is reduced to $2f_{sw}$ instead from $4f_{sw}$.

Figure 2.31 The operation of the oversampled digital controller during transient with multiple control actions based on successive load-change estimation
2.5 Topology Modifications to Improve the Transient Response of a Buck Converter

Many topology modifications to the Buck converter have been proposed to enable the converter to yield transient responses beyond the physical capability of the conventional Buck VR. In particular, these topology modifications are useful for unloading transients since they tend to exhibit larger voltage deviations and settling times than loading transients of equal magnitude.

Ideally, the steady-state duty cycle would be close to 50% in order to achieve a symmetrical transient response to loading and unloading current changes. One solution is to use two Buck converters in series in order to increase the duty cycle of the second stage. For example, the first stage could convert the voltage $12\text{VDC} \rightarrow 5\text{VDC}$ and the second stage could convert $5\text{VDC} \rightarrow 1.5\text{VDC}$. Therefore, the second stage’s steady-state duty cycle would be increased from 12.5% to 30% yielding a much more symmetric transient response. This also allows for the use of a smaller inductor for a fixed inductor current ripple value.
This concept is studied extensively in [43][44]. Three obvious drawbacks of this method are an increase in cost, an increase in physical size and a decrease in efficiency. However, it is argued in [44], that if a relatively low switching frequency is used in the first stage, so that the overall efficiency would not suffer. Additionally, the intermediate dc bus voltage can be adaptively controlled to further optimize the efficiency of the two-stage VR. But it increases the controller complexity for adding extra control loop to the first stage for Adaptive Bus Voltage Positioning (ABVP)[45][46]. And the reference voltage for controlling intermediate dc bus requires load current information to carry out adaptive voltage positioning technique. In the meantime, a bus voltage feed forward is needs to adjust the ramp peak of the second stage. In the small signal analysis, it demonstrates that the bandwidth of the first stage needs to be limited and carefully designed to ensure the stability of the entire system.

Numerous topology modifications have been proposed to increase the negative slew rate of the output inductor during a step down load transient event. In [50] a topology modification is presented (as shown in Figure 2.33) which effectively reverses the input voltage of the converter during an unloading transient, significantly increasing the negative slew rate of the output inductor. This topology modification requires a switch in series with the main power train which will result in extra switching and conduction losses.
In [51], a tapped inductor configuration is presented which extends the steady-state duty cycle and increases the negative slew rate of the inductor current. As shown in Figure 2.34, an auxiliary snubber circuit is typically required to mitigate the high voltage stress imposed on the synchronous MOSFET.

In [52], a “stepping” transformer is utilized in lieu of an output inductor, as shown in Figure 2.35. During load current transients, the inductor is essentially short-circuited and the current slew rate is limited only by the leakage inductor of the transformer. For example, during step-up transient, Q3 turns on to clamp the voltage across the output inductor (magnetizing inductance of
the stepping transformer), so that the slew rate of the output inductor current will be determined by the leakage inductance and the voltage across the leakage inductance. However, the MOSFET $Q_3$ will turn off depending on the output voltage level to track the load current.

![Diagram of the stepping transformer](image)

**Figure 2.35** "Stepping" transformer in lieu of output inductor to improve transient response

It is shown that by increasing the slew rate of the output inductor, the unloading transient performance of the system can be improved; however, many topology modifications have been proposed which do not change the inductor current slew rate, but rather divert a portion of the inductor current from reaching the output capacitors.

In [53], an auxiliary circuit is presented which operates by disconnecting the output node of the main inductor and routing it to the converter input during an unloading transient, as shown in Figure 2.36. The proposed improvement is referred to as inductor current “steering”. This method also requires an additional switch in series with the power train, resulting in higher switching and conduction losses.
A converter (which may act as a Buck or an anti-parallel boost) is connected in parallel with the Buck converter, as shown in [54] to recover excess current to the input during step-down load transients. The circuit also provides a low-impedance auxiliary path for step-up load transients as well. The auxiliary circuit is controlled using a differentiator in an attempt to instantaneously track the capacitor current. The circuit is illustrated in Figure 2.37.

In [55], a linear active clamp is added across the output capacitor in order to divert the excess inductor current to ground following an unloading transient. This is illustrated in Figure 2.38.
Figure 2.38  Active clamp to improve transient response during load transient

Alternatively, the amount of charge absorbed by the capacitor can be reduced by transferring excess current from the output inductor of the Buck converter to the converter’s input through the operation of the proposed controlled auxiliary current (CAC). As will be shown, a large reduction in output voltage overshoot can be realized by the addition of a small inductor, MOSFET and diode.

The auxiliary current can be modeled as a controlled current source drawing current from the output of the Buck converter and transferring it to the input of the Buck converter. Figure 2.39a) shows the model of the proposed method. Figure 2.39b) shows one possible implementation of the auxiliary current, used in this thesis.
An alternate implementation would involve using a second MOSFET (in lieu of $D_{aux}$) for synchronous rectification. As observed, the auxiliary circuit resembles a small Boost converter connected in anti-parallel with the Buck converter. The auxiliary current is only active during unloading transients; thus, it has no effect on the converter’s efficiency when the converter is operating in steady-state. In addition, since the auxiliary current is only active for a small percentage of the total operating duration, electromagnetic interference (EMI) effects will be short lived and will not significantly affect the frequency spectrum.

2.6 Existing Control Schemes for the Controlled Auxiliary Current (CAC)

Based on the CAC topology, several control schemes have been presented in [47][48][56] to regulate the current of CAC, resulting in significantly reduced voltage overshoot of VR under unloading condition. The principles of three different control schemes are illustrated in Figure 2.40 with the information of load current $i_{o1}$ and $i_{o2}$, inductor current $i_L$, auxiliary current $i_{aux}$, output voltage $v_o$ and reference voltage $V_{ref}$. For comparison, the CBC controlled output voltage overshoot is also shown in Figure 2.40 without the help of CAC.
Figure 2.40 Operating principles of control schemes on CAC to reduce the overshoot under unloading transients and comparative waveforms of inductor current $i_L$ and output voltage $v_o$.

And a simulation is conducted for comparing the performance of the existing CAC controllers and the waveforms are ideal in the sense of low auxiliary current ripples. $L_o=1\mu$H, $L_{aux}=100\text{nH}$, $I_{aux\_pk-pk}=1\text{A}$, $C_o=200\mu\text{F}$, $L_{o1}=10\text{A}$, $L_{o2}=0\text{A}$. And the implementations and main drawbacks of the control schemes are discussed in the Sections 2.6.1-2.6.3.
2.6.1 Constant off Average Current Mode (COACM) Control Scheme

In [47][48], a controlled auxiliary current (CAC) in Figure 2.39 is presented to improve the transient response of a Buck converter. The duration of activation of the auxiliary current is regulated. The proposed circuit has the following advantages:

1) predictable behavior allowing for simplified design; 2) inherent over-current protection; 3) low peak current to average current ratio allowing for use of smaller components.

![Diagram showing Inductor current $i_L$, $I_{aux\_peak}$, $I_{aux\_avg}$, Off-time $T_{aux\_off}$, and Load current.](image-url)
In addition, the proposed auxiliary controller estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lower magnitude.

However, this controller is not suitable for multiphase buck converters due to the high switching frequency of the auxiliary circuit, for example, in order to maintain the average value of the auxiliary current for a two phase VR with 360nH per phase output inductance, the switching frequency of the auxiliary switch will be reaching above 5MHz, resulting in highly increased switching losses, gate drive losses and auxiliary MOSFET driver cost. Also, the controller design is relatively complex with constant $T_{aux\_off}$ delay time injection, load current estimation, and filtered current sensing. Above all, because of the low initial auxiliary current peak, the overshoot of this control scheme is not optimal/near-optimal, even though the current level is adjustable.

### 2.6.2 Current Tracking (CT) Control Scheme

The controller presented in [56], using linear mode controller to regulate a similar CAC with synchronous rectifier and independent auxiliary output capacitors (see Figure 2.43).

![Figure 2.43](image)

**Figure 2.43** The implementation of the low-voltage transient processor (LVTP)
The controller diagram is shown in Figure 2.44, during transients, the auxiliary controller will emulate the inductor current information as the auxiliary current reference. As a result, the VR with the proposed CAC or called low-voltage transient processor (LVTP) in the paper is essentially a multivariable system, where it is necessary to control two outputs, $v_{caux}$ and $v_o$, with two inputs, the duty ratios of the primary and auxiliary converter. And the output voltage of LVTP $V_{caux}$ is adjustable depending on the load current level, which is normally different from the main VR output voltage $v_o$. $K_v(s)$ is the transfer function of the VR output voltage filter, while $K_{v_a}(s)$ is the transfer function of the auxiliary voltage controller. And the auxiliary current reference will consist of the information paths of $v_o$ and $v_{err,aux}$ through $K_i$ and $K_{va}$. The current of the auxiliary circuit will track the reference $i_{ref}$ with the help of the inner loop controller $G_{ii}$. The transfer function between LVTP voltage and current is represented as $G_{iv}(s)$.

![Control loop for the LVTP under independent linear control.](image)

Figure 2.44  Control loop for the LVTP under independent linear control.

Small signal analysis is required to design the LVTP controller, considering the input impedance of the LVTP as a shunt impedance of the main VR in Figure 2.45.
Figure 2.45 Input impedance of the LVTP.

The advantages of this proposed scheme are 1) linear control operation against the unpredictable load transients; 2) flexible auxiliary output voltage to optimize the overall efficiency; 3) fully analog implementation, enabling and facilitating the analog IC fabrication.

From the simulation results shown in Figure 2.41, it demonstrates that this control law can achieve a lower voltage overshoot compared to the COACM method proposed in the last section. However, to apply this technique in non-AVP application, it requires a current reference transition at pre-calculated moment, which makes the scheme hybrid and more complicated. Otherwise, the output voltage will undergo a ringing back or recover in a longer time after the auxiliary circuit is deactivated. Also the switching frequency of the CAC is also approaching about 3MHz [56], resulting in the same limitations as COACM method.

2.6.3 Enhanced Current Tracking (ECT) Control Scheme

To achieve the optimal control solution for the CAC, the enhanced current tracking scheme is capable of reducing the output voltage overshoot as well as the settling time to the physically optimal level. Given that the equivalent falling slew rate of the auxiliary inductor current is high enough to ignore the time $t_{aux(ECT)_{off}}$, the current tracking can be activated when the output voltage recovering to the $V_{ref}$. However, obviously, the disadvantage is the large peak current, which
results in the requirement of large die MOSFET and specifically designed inductor with high saturation current capability. The high switching frequency is also a drawback of ECT method.

2.7 Conclusions

Although, linear voltage-mode controllers are the tried-and-true choice for Buck converters, it is demonstrated that due to their synchronous switching action and finite bandwidth, there is plenty of room for improvement in their transient response.

Thus, numerous non-linear controllers have been proposed to break these bandwidth limitations. In general, these non-linear controllers do not possess desirable features such as zero steady-state error and fixed switching frequency. Furthermore, it was presented that non-linear controllers such as V^2 and hysteretic voltage-mode control rely heavily on large output capacitor ESR values in order to operate effectively. Without such large ESR values, these controllers tend to “over-compensate” for a load current transient by saturating the Buck converter’s PWM cycle for an extended period. Although enhanced V^2 controller can fix the low ESR limitation, accurate current sensor to collect inductor current to the loop is required, increasing implementation cost and complicating the compensator design.

In order to solve the above drawbacks, charge balance control (CBC) methods with different implementation formats have been proposed which also employ a linear controller during steady-state conditions. While such works have shown that these controllers can minimize settling times (following a load transient), they suffer from at least one of the following drawbacks: 1) exceedingly complex algorithms, 2) slow reaction time due to sampling delay; 3) requiring both \( L_o \) and/or \( C_o \) information 4) not extendable to large ESR designed Buck converters and/or 6) high controller power consumption. In addition, many of these controllers do not present extensions for adaptive voltage positioning.
In order to solve the above drawbacks, a output voltage sensing based digital charge balance controller is presented in Chapter 3 which does not require complex calculations and accurate current sensors. It is capable of reacting very fast to a load transient (asynchronous to the switching period) and does not require both of the nominal output inductor and capacitor value to operate. With simple modification, this digital controller can be applied to adaptive voltage positioning (AVP) applications. Theoretically, the proposed algorithm is also capable of controlling the VR under ultrafast and large input voltages step transients.

In chapter 4, a digital controller is presented based on proposed output voltage curve fitting methodology, which helps to extend the charge balance control concept to general Buck converters, even those with large ESR. Estimation can be made based on three output voltage samples during load transients, and this estimation is used for time detection and load step value calculation. Also, without sacrificing previously achieved robustness, optimal response performance of generally designed Buck converter has been achieved using this controller.

In chapter 5, an analog version of this controller is presented which possesses all the above-mentioned advantages and facilities the circuit integration of IC controller in the industry. To reduce the high implementation cost and power consumption caused by the fast ADC for time detection, a new analog extreme voltage detector is presented. Furthermore, lower controller operating power consumption is achieved in this analog implementation.

In chapters 3-5, it is demonstrated that although charge balance control can push the transient performance of a Buck converter to its physical limits, the unloading transient is still poor (due to the relatively slow negative slew rate of the inductor current). In order to attempt to rectify this problem, a controlled auxiliary current for the Buck converter has been proposed to improve its transient response.
An auxiliary circuit and a practical controlled auxiliary current controller are presented in Chapter 6 which transfers a tightly controlled current from the output of the Buck converter to its input during an unloading transient. The auxiliary current switches at a reduced frequency in boundary conduction mode (BCM) and provides a higher initial peak auxiliary current to decrease the overshoot following an unloading transient. The circuit operates in parallel to the Buck converter and is only activated during unloading transients. Therefore, unlike some previously-proposed solutions, it has less effect on the converter’s efficiency due to the reduced switching frequency. More importantly, the number of auxiliary switching cycles are predictable based on the ratio of main and auxiliary inductance, resulting in improved reliability and design simplicity. At the end of this chapter, a simplified linear mode controller is presented to address the Multiple Consecutive Load Transients issue and meet the requirements of load transient test for a two-phase VR in laptop applications.
Chapter 3

A Robust Voltage Sensing Based Digital Capacitor Charge Balance Control Algorithm

3.1 Introduction

With the revolution of integration technology, it is possible to fabricate powerful microprocessors with more and more transistors on chip, resulting in higher load demand. On the other hand, to maintain/reduce the overall power consumption of the microprocessor, the output voltage level keeps dropping. As a result, the requirements of voltage regulator (VR) for powering next-generation microprocessor are more and more stringent, that is, low output overshoot/undershoot and short settling time under increasingly large load transients. So it becomes more and more difficult to meet the transient requirements using conventional linear mode controllers such as voltage and current mode controllers of which the design is normally made with the help of small signal model analysis. Due to the undesired voltage deviations, a large volume of output capacitance is often used which occupies a big board area with linear mode controllers. To break the bandwidth barrier for faster transient response, couples of analog controllers and digital control algorithms have been introduced previously to achieve this objective [57]-[60]. As one of the practical optimal control candidates, the capacitor charge balance concept was first introduced and implemented digitally in [32] for achieving minimum voltage variations and settling time. Generally speaking, compared to analog controller, digital counterpart offers many advantages such as re-programmability, reliability, noise immunity, low sensitivity to ageing and environmental factors and simplicity of complex arithmetic [49]. Particularly, for VR application, digital controller provides some unique advantages compared to analog VR controller:
1. Digital controller can help to reduce the entire footprint of the VR, since the number of required external components, such as resistors and capacitors, as well as OPAMPs and comparators, is reduced by the digital functions/codes.

2. More importantly, the digital controller can shorten the developing time for a new VR controller, and normally a successful version of VR controller IC product may take 10-12 times modifications before final release. Also, it means that the total expense for the VR controller development can be significantly reduced.

3. Some nonlinear functions may not be easy to be implemented by using analog devices. One example is the system identification function to achieve robust and dynamic control. Also, the power up sequence is another good application for digital control [49].

Furthermore, the CBC concept can be easily implemented using digital signal processing devices, such as DSP and FPGA, so extensive work has been conducted in designing digital CBC controllers that further improves robustness [33][35][36], practical performance [37][38] and simplicity of the control system [38][49]. However, all the previous schemes are not able to address at least one of the following limitations:

1. Complex real-time calculation is embedded in the algorithm, like division and square root [32][34] which requires high speed digital control devices for working out operations in a limited time interval;

2. Current sensing information is needed to implement the proposed scheme for estimation, adding more cost to the controller and/or sacrificing the accuracy [32][33][40];

3. Algorithm requires the knowledge of design parameters of passive components (output capacitance $C_o$ and inductance $L_o$) in the switched mode power supply to
perform the charge balance concept, limiting the practicality of the previous schemes [32]-[34][38][40];

4. It is difficult to apply adaptive voltage positioning (AVP) or load line regulation using proposed schemes for powering modern processors such as Intel modules [32]-[34][39]-[41];

5. A fast or asynchronous analog to digital converter (ADC) [34]-[37] or certain type of active current sensor/detector [33][38] is required to detect the capacitor current zero-crossing time instant, resulting in high cost and bad reliability of the overall system.

To derive the charge balance equations, the previous research work has always selected the capacitor charge and discharge integrals associated with the inductor and load current as the starting point [35][36]. But in this chapter, a new output voltage curve analysis based derivation is discussed to provide a possibility for achieving parameter-independent control strategy under different transients. When a well-designed and regulated Buck converter has negligibly low ESR in the output capacitor, the proposed algorithm is parameter-independent and robust, which can be extended for AVP applications with simple modifications [2].

The chapter is organized as follows. In Section 3.2, the basis of charge balance concept will be reviewed. In Section 3.3, mathematical derivations of the proposed algorithm are discussed and the method to detect the critical time instants for the proposed digital charge balance controller is presented. The principles of the proposed optimal control algorithm for load step transients are outlined in Section 3.4. In Section 3.5, the extensions of the proposed scheme for adaptive voltage positioning and ultrafast input voltage step transients are presented. In Section 3.6, the implementation and design guidelines are provided for the proposed the mixed-signal control system and extreme voltage detector. Calculations and analysis are conducted to estimate the charge balance controller performance, such as output voltage deviations, settling time and
estimation error in Section 3.7. Finally, the simulations and experimental results are demonstrated in Section 3.8 to validate the proposed control algorithm. The conclusion is made in Section 3.9

3.2 Basis of Charge Balance Control Concept

The principle of capacitor charge balance has been used extensively for the purpose of steady-state modeling and analysis of DC-DC converters. For reference, Figure 3.1 shows a synchronous Buck converter, which is a general topology for VR application.

![Figure 3.1 Synchronous Buck converter](image)

As the principle of capacitor charge balance presents, in steady-state, the average value of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output voltage to be identical at the beginning and the end of a switching cycle. Equation (3.1) represents the principle of capacitor charge balance for a Buck converter under steady state.

\[
V_c \left[ (N+1)T_{sw} \right] - V_c \left( NT_{sw} \right) = \frac{1}{C_o} \int_{c_{,avg\_sw}} i_c(t) \, dt = 0 \quad (3.1)
\]

In (3.1), \( V_c \) represents the capacitor voltage (neglecting ESR and ESL), \( i_{c,\_avg\_sw} \) is the capacitor current over the steady-state switching period, \( C_o \) represents the output capacitor value and \( T_{sw} \) is the switching period of the converter. By recognizing that the integral period of (3.1) may be extended over the total transient time of a DC-DC converter, equation (3.2) is developed.
\[ v_c(t_b) - v_c(t_a) = \frac{1}{C_o} i_{c_{avg\_trans}} = 0 \rightarrow \frac{1}{t_b - t_a} \int_{t_a}^{t_b} i_c(t) \, dt = 0 \]  \hspace{1cm} (3-2)

In (3.2), time instant \( t_a \) represents the beginning of the transient period and time instant \( t_b \) represents the end of the transient interval. \( i_{c_{avg\_trans}} \) equals the average capacitor current over the transient period. Equation (3.2) indicates that as long as the integral of the capacitor current equals zero over the duration of the transient interval (i.e. the charge removed from the capacitor equals the charge delivered to the capacitor), the output voltage at the end of the transient will be equal to the voltage at the beginning of the transient. Thus, if at \( t_b \), the inductor current \( i_L \) equals the load current and (3.2) has been satisfied, i.e, the output voltage will have returned to its reference voltage and, therefore, the converter has recovered from the transient event.

Thus, the goal of the proposed controller is to drive the Buck converter such that the inductor current and the output voltage return to their respective steady-state values simultaneously at \( t_b \).

Charge balance principle is a practical solution for achieving minimal settling time [32][33] in Figure 3.2. For all the CBC based controllers [32]-[41], the time instants \( t_1 \) (capacitor current undergoing zero-crossing) and \( t_2 \) (PWM changing ON/OFF state) are very important to arrange the desired ON/OFF control actions, accordingly. Output voltage information is a must for voltage mode controller (during steady-state operation), so output voltage sensing based charge balance concept is a simple, practical and cost effective implementation. In this chapter, a practical extreme voltage detector is present to find \( t_1 \) and then to sample the maximum/minimum output voltage at this time instant. And in place of calculating interval \( T_2 \) [32]-[34], the time information \( t_2 \) is mapped to the switching point voltage (SPV) \( V_{SW} \), which provides voltage sensing based parameter-independent formula set under load transient cases. Also an extension can be made for AVP application based on this SPV information. The operations of the proposed controller to minimize the output deviations are discussed in the Section 3.4.
3.3 Basic Idea of Voltage Sensing Based Charge Balance Control

3.3.1 Charge Balance Principles for a Buck Converter Undergoing an Unloading Transient

The CBC controller is designed for applications in which the load current slew rate is significantly larger than the inductor current slew rate, which is normally the case when fast response is needed. Therefore, in this analysis, it is assumed that the load current steps instantaneously from $I_{o1}$ to $I_{o2}$ and that the controller is able to react to the step with negligible delay. It is also assumed that the load current remains constant for the duration of the transient period. For the computer CPU VRs, sufficiently large output capacitance is required to suppress the output voltage deviation. And also for the low voltage rating, often, the paralleled ceramic output capacitors could provide very low $ESR (<1m\Omega)$. So in the following discussion, an ideal dc-dc Buck converter model is examined. And the starting time $t_0$ is set to be 0 in the analysis for simplification in Figure 3.2.

![Diagram showing capacitor charge integral areas during an unloading step change](image)

Figure 3.2 Capacitor charge integral areas during an unloading step change
Step 1: Time Interval $T_1 (t_0 \leq t < t_1)$ for an Unloading Step

For unloading step change, during the time period $t_0$-$t_1$, capacitor current $i_c$ can be approximated as a linear function in (3.3), where $m_2$ is the falling slew rate of the inductor current, $V_o$ is the output voltage and $L_o$ is the output inductance.

$$i_c(t)\bigg|_{t_0-t_1} = -m_2(t-t_1) = -\frac{V_o}{L_o}(t-t_1)$$

(3-3)

As an alternative approach for solving differential equations, the capacitor/output voltage $v_o$ can be approximated with a parabola based on its current $i_c$ in the equation (3.4).

$$v_o(t) = V_{ref} + \frac{1}{C_o} \int_0^t i_c\,dt = V_{ref} + \frac{m_2}{2C_o}t_1^2 - \frac{m_2}{2C_o}(t-t_1)^2$$

(3-4)

The capacitor charge area $A_{charge}$ can be calculated in (3.5), where $I_{o2}$ is the new steady-state load current level and $i_L$ is the inductor current.

$$A_{charge} = A_1 = \int_0^1 (i_L - I_{o2})\,dt$$

(3-5)

It is assumed, in the analysis, that $m_1$ is constant over the transient period, so the integrand in (3.5) can be expressed in (3.6).

$$i_L - I_{o2} = \int_0^t m_2\,dt$$

(3-6)

Therefore, by combing (3.5) and (3.6), the total charge area $A_{charge}$ can be expressed in (3.7).

$$A_{charge} = A_1 = m_2 \int_0^1 \int_0^t dt\,dt$$

(3-7)

Step 2: Time Interval $T_2 (t_1 \leq t < t_2)$ for Unloading Step

When the inductor current $i_L$ reaches the new steady-state load current $I_{o2}$ at $t_1$, the output voltage $v_o$ will occur its peak value, $V_{max}$. Similarly, the capacitor current $i_c$ can be expressed in
(3.8), and the instantaneous output voltage \( v_o \) will be able to be computed in (3.9) based on the voltage \( V_{\text{max}} \), \( t_1 \).

\[
i_c (t) \big|_{t_1}^{t_2} = -m_2 (t - t_1) = -\frac{V_o}{L_o} (t - t_1) \tag{3-8}
\]

\[
v_o (t) = V_{\text{max}} + \frac{1}{C_o} \int_{t_1}^{t} i_c \, dt = V_{\text{max}} - \frac{m_2}{2C_o} (t - t_1)^2 \tag{3-9}
\]

The part \( A_2 \) of discharge area \( A_{\text{discharge}} \) can be calculated in (3.10).

\[
A_2 = \int_{t_1}^{t_2} (i_L - I_{o2}) \, dt = \int_{t_1}^{t_2} m_2 \, dt \, dt \tag{3-10}
\]

**Step 3: Balancing Capacitor Charge Regions** \( A_{\text{discharge}} \) and \( A_{\text{charge}} \), \( T_3 \) \((t_2 \leq t \leq t_3)\)

According to (3.9), the output voltage at \( t_2 \), called switching point voltage (SPV, \( V_{\text{sw}} \)) in this chapter, is expressed in (3.11).

\[
V_{\text{SW}} = V_{\text{max}} - \frac{m_2}{2C_o} T_2^2 \tag{3-11}
\]

Referring to the rising slope of the inductor current \( m_1 \) in this interval, the capacitor current can be written as (3.12) and the time intervals \( T_2 \) and \( T_3 \) will follow the relationship expressed in (3.13).

\[
i_c (t) \big|_{t_2}^{t_3} = m_1 (t - t_3) = \frac{V_m - V_o}{L_o} (t - t_3) \tag{3-12}
\]

\[
\frac{T_2}{T_3} = \frac{m_1}{m_2} = \frac{V_m - V_o}{V_o} \tag{3-13}
\]

The instantaneous output voltage \( v_o \) can be calculated in (3.14) based on the capacitor current \( i_c \) information in (3.12).
\[ v_o(t) = V_{SW} + \frac{1}{C_o} \int_{t_2}^{t} i_c(t) \, dt \]  

(3-14)

So the SPV voltage \( V_{SW} \) can be calculated using (3.15), where the symbol \( T_{sw} \) represents the switching period and the \( V_{ref} \) is for the output voltage reference.

\[
V_{SW} = \frac{1}{2C_o} m_1 \left[ T_3^2 - \left( \frac{1}{2} DT_{sw} \right)^2 \right] + V_{ref}
\]

(3-15)

Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a high frequency (>100kHz) and narrow duty ratio (12 V-1.5 V), the item \((1/2DT_{sw})^2\) can be neglected in the equation (3.15) and simplified in equation (3-16).

\[
V_{SW} = \frac{1}{2C_o} m_1 T_3^2 + V_{ref}
\]

(3-16)

Therefore, the voltage \( V_{SW} \) can be expressed as (3-17) by substituting the equation (3.11) into (3.15). After that, the \( V_{SW} \) can be solved by moving \( V_{SW} \) terms on both sides of the equation (3-17) to one side. The intermediate result is shown in the equation (3-18). After substitute equation (3-13) into (3-18) and make a simplification, the final equation for calculating \( V_{SW} \) is expressed in (3-19).

\[
V_{SW} = \frac{m_2}{m_1} \frac{m_2}{2C_o} T_3^2 + V_{ref} = \frac{m_2}{m_1} \left( V_{max} - V_{SW} \right) + V_{ref}
\]

(3-17)

\[
V_{SW} = \frac{m_2}{m_1} V_{max} + V_{ref}
\]

(3-18)

\[
V_{SW} = \frac{m_2}{1 + \frac{m_2}{m_1}} V_{ref}
\]

(3-19)
In the equation (3-19), only coefficient multiplications and additions are required based on the steady-state duty cycle $D$ and voltage information $V_{\text{max}}$ and $V_{\text{ref}}$. Therefore, SPV can be simply calculated by DSP in about 10 system cycles. It is also worth noting that the control algorithm does not require the inductor and capacitor information, so the robustness of the proposed digital controller is significantly enhanced.

However, to implement the equation (3-19), the peak voltage information $V_{\text{max}}$ is required. Therefore, an analog extreme voltage detector is developed in this chapter to locate the voltage peak at time instant $t_1$, which is discussed through details in the next section.

Based on (3.13), another discharge area $A_3$ can be calculated in (3.16).

$$A_3 = \frac{m_2}{m_1} \int_{t_1}^{t_2} (i_L - I_{a2}) dt = \int \int \frac{m_2^2}{m_1} dt dt $$ \hspace{1cm} (3-20)

Therefore, the charge balance principle is achieved in (3.17)-(3.20), and the output voltage recovers to the reference voltage $V_{\text{ref}}$.

$$A_{\text{charge}} = A_{\text{discharge}} \hspace{1cm} (3-21)$$

$$A_1 = A_2 + A_3 \hspace{1cm} (3-22)$$

$$\int \int_{0}^{t_1} m_z dt dt = \int \int_{t_1}^{t_2} m_z dt dt + \int \int_{t_1}^{t_2} m_2^2 \frac{m_1}{m_1} dt dt \hspace{1cm} (3-23)$$

$$(V_{\text{in}} - V_{o}) \cdot \int \int_{0}^{t_1} dt dt = V_{\text{in}} \cdot \int \int_{t_1}^{t_2} dt dt \hspace{1cm} (3-24)$$
3.3.2 An Analog Extreme Voltage Detector for Locating the Voltage Peak/Valley at $t_1$

Because of the current sensor mismatching [33], cost and accuracy issue [34][35][36], a practical extreme voltage detector is used in this chapter to detect $t_1$ and above all, to locate the peak voltage information $V_{\text{max}}/V_{\text{min}}$ for sampling. In Figure 3.3, as an instance, during unloading step transient, the output voltage overshoot is delayed with a period of time $t_{\text{delay}}$, and represented as $v_{o,\text{delay}}$. This delay can be equalized with first-order OPAMP circuit based on Padé Approximation (3.22). Then, the voltages $v_o$ and $v_{o,\text{delay}}$ will be fed to the input ports of the output comparator. And at a certain voltage error $v_{\text{err}}$, the comparator output signal begins rising to this upper limit, such that time instant $t_1$ can be responded by an external interrupt of DSP. And the inserted delay time $t_{\text{delay}}$ can be compensated to a certain acceptable degree, with the help of the lead time (provided by ESR) and comparator hysteresis configuration (which can adjust the $v_{\text{err}}$ band in Figure 3.3).

Figure 3.3 Illustration of the proposed analog extreme voltage detector under unloading step transient case for $t_1$ detection and $V_{\text{max}}$ sensing
In Figure 3.4, an adjustable delay circuit is synthesized based on the Padé approximation (3.22).

\[
\frac{v_{o\_delay}}{v_o} = e^{-\tau s} \approx \frac{1 - \frac{\tau s}{2}}{1 + \frac{\tau s}{2}} = \frac{1 - R_f C_T s}{1 + R_f C_T s} \tag{3-25}
\]

In this circuit, the delay time constant \( \tau \) can be adjusted by the product of \( R_f \) and \( C_T \) (i.e. \( \tau = 2R_f C_T \)). And the inverting section is added to the output end to implement two-fold functions: 1) inverting the delayed signal and 2) tuning the output voltage offset level. The output comparator is connected with a hysteresis configuration and the one with latched output function is more preferred for blanking steady-state comparison “noise”, such as TL3016 (Texas Instruments Company) [61]. Also, in the experiments, the aforementioned delay can be also compensated by using a trim resistor as the feedback resistor \( R_{k2}' \) to tune the delayed voltage \( v_{o\_delay} \) offset level such that the crossover of the two voltage waveforms (\( v_o \) and \( v_{o\_delay} \), Figure 3.5) will appear at right \( t_1 \).

![Figure 3.4](image_url)  
**Figure 3.4** Hardware implementation of the detector based on the adjustable delay circuit
3.3.3 Regarding Assumptions Involving \( m_1 \) and \( m_2 \)

It is noted that \( m_1 \) and \( m_2 \) will not remain constant in actuality during a load transient due to the varying output voltage. This simplification was made in order to allow for a practical implementation of a charge balance controller. For this reason, it is claimed that the controller can only yield a “near-optimal” transient response. However, the simplification does not degrade the performance significantly due to the following reasons:

i) for a low duty ratio Buck (e.g. 12V-1.5V), the undershoot (due to a loading step transient) will be much smaller than the overshoot (due to an unloading step transient). Thus, for a properly designed Buck, the output voltage deviation during a loading transition would be very small.

ii) for an unloading transition, the output voltage can vary up to 100mV, which is close to 10% of the steady-state voltage of 1.5V. However, since the SPV is determined by the \( D \) and \((1-D)\) in (3-19), for example, a single phase 12V-1.5V Buck converter with 1μH output inductance and 200μF output capacitance, under 10A step-down load transient the overshoot will be about...
0.2V, and the exact SPV $V_{SW}$ is 1.528V considering varying duty cycle, however, using constant duty ratio $D$, the calculated $V_{SW}$ is 1.525V, causing a very small error of 3mV.

### 3.3.4 Charge Balance Equation for a Buck Converter Undergoing a Loading Step Transient

A similar analysis as was performed in Section 3.3.1 can be carried out for a loading step transient based on Figure 3.6.

![Figure 3.6 Capacitor charge integral areas during a loading step transient](image)

During the time intervals $t_0$-$t_2$ and $t_2$-$t_3$, the capacitor current can be expressed as a linear function in (3.23) and (3.24), respectively.

\[
\begin{align*}
   i_c(t)\big|_{t_0-t_2} &= m_1(t-t_1) \\
   i_c(t)\big|_{t_2-t_3} &= -m_2(t-t_3)
\end{align*}
\]
So the voltage $V_{SW}$ can be calculated using (3.25), where the symbol $T_{sw}$ represents the sampling period and the $V_{ref}$ is the output voltage reference, while the equation (3.26) provides the formula for voltage $V_{\text{min}}$.

$$V_{SW} = V_{ref} - \frac{1}{2C_o} m_2 \left[ T_3^2 - \left( \frac{1}{2} D'T_{sw} \right)^2 \right]$$

$$V_{\text{min}} = V_{SW} - \frac{1}{2C_o} m_1 T_2^2$$  \hspace{1cm} (3-28)  \hspace{1cm} (3-29)

Similarly, the item $(1/2D'T_{sw})2$ can be ignored in the equation (3.25). Therefore, the voltage $V_{SW}$ can be derived as (3.27), where $m_1/m_2 = (V_{in}/V_o)/V_o = T_3/T_2$. According to the voltage $V_{SW}$, we can change the main switch state from on-state to off-state at $t_2$. By combining (3.25) and (3.26), the SPV can be expressed in (3.27), in which neither inductor nor capacitor value is explicit.

$$V_{SW} = V_{ref} + \frac{m_2}{m_1} (V_{\text{max}} - V_{SW}) = DV_{ref} + (1 - D)V_{\text{min}}$$  \hspace{1cm} (3-30)

And the charge balance condition can be verified in (3.28)-(3.31). The discharge area is represented as $A_{\text{discharge}}$, while $A_{\text{charge}}$ represents the charge area which consists of $A_2$ and $A_3$.

$$A_{\text{discharge}} = A_{\text{charge}}$$  \hspace{1cm} (3-31)

$$A_1 = A_2 + A_3$$  \hspace{1cm} (3-32)

$$\int_{0}^{t} m_1 dt dt = \int_{0}^{t_2} m_1 dt dt + \int_{t_2}^{t_3} m_1^2 dt dt$$  \hspace{1cm} (3-33)

$$V_o \cdot \int_{0}^{t} dt dt = V_{in} \cdot \int_{t}^{t_2} dt dt$$  \hspace{1cm} (3-34)
3.4 Operations of the Voltage Sensing Based CBC Scheme

3.4.1 Operations of the Proposed Digital CBC Controller to Minimize the Output Overshoot

As previously discussed, following the load current step transient, the proposed CBC controller will firstly sample the maximum/minimum output voltage at $t_1$ and convert this information into SPV $V_{SW}$ to detect $t_2$. The main procedures of the control scheme under unloading step (in CCM mode with synchronous rectifier, SR, see Figure 3.1) are listed with reference to Figure 3.7:

1. Assuming that a load current transient happens at the time point $t_0$, triggering the optimal controller, immediately. And the voltage mode digital PID controller will be disconnected from the feedback loop with registered controller output, while the proposed voltage sensing based CBC controller will set the PWM output to low (OFF);
2. After a short period of delay for blanking the load transition noise such that the output voltage switching ringing will not degrade the performance of the extreme voltage detector, the extreme voltage detector will be activated for detecting $t_1$ (see Figure 3.3).

3. When the certified output signal edge (rising edge, shown in Figure 3.3) of the voltage detector happens at $t_1$, the output voltage peak $V_{\text{max}}$ will be sampled and registered;

4. According to the voltage peak $V_{\text{max}}$, the SPV $V_{SW}$ can be calculated using simple calculation of the proposed algorithm in (3-19). The PWM will be reset to high (ON) when the output voltage reduces to $V_{SW}$ at $t_2$;

5. At $t_3$ (by sensing $v_o=V_{\text{ref}}$), the output voltage recovers to the desired voltage $V_{\text{ref}}$, and the conventional PID controller is reactivated for output voltage regulation again.

### 3.4.2 Operations of the Proposed Digital CBC Controller to Minimize the Output Undershoot

The charge balance principles are also applicable for minimizing the output undershoot undergoing loading step transients.

1. Similarly, it is assumed that a load current transient happens at the time point $t_0$, triggering the optimal controller, immediately. And the voltage mode PID controller will be disconnected from the feedback loop with frozen controller output, while the proposed CBC controller will set the PWM output to high (ON);

2. After a short period of delay for blanking the load transition noise, the extreme voltage detector will be activated for detecting $t_1$;
3. When the certified output signal edge (falling edge) of the voltage detector happens at \( t_1 \), the output voltage peak \( V_{\text{min}} \) will be sampled and registered;

4. According to the voltage peak \( V_{\text{min}} \), the SPV \( V_{\text{SW}} \) can be calculated using proposed digital function in (3.27);

5. The PWM will be reset to low (OFF) when the sampled output voltage reduces to \( V_{\text{SW}} \) at \( t_2 \);

6. At \( t_3 \) (by sensing \( v_o=V_{\text{ref}} \)), the output voltage recovers to the desired voltage \( V_{\text{ref}} \), and the conventional digital PID controller is reactivated for output voltage regulation again.

Figure 3.8 Typical waveforms of voltage regulator using the proposed CBC controller under loading step transients
3.5 Extensions of the Voltage Sensing Based CBC Controller

In addition to the application of optimizing the load step transients discussed in the previous sections, the proposed controller can be simply extended for adaptive voltage positioning technique with small modifications but inductor current sensing is required for load line regulation. Furthermore, the proposed algorithm is possible to solve the large and ultrafast input voltage transients, although this circumstance may not normally happen in the real applications.

3.5.1 Adaptive Voltage Positioning/Load Line Regulation Extension

Adaptive voltage positioning (a.k.a. Load-line regulation) has increasingly become a requirement in many Buck converter applications, for example, Intel’s CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter as well as decreasing power consumption of the load device.

The proposed voltage sensing based CBC controller can be applied to AVP operation with only minor modifications, such as adding inductor current sensing and one more ADC channel to the DSP. In this section, the analysis will be conducted and the implementation modification will be discussed in the Section3.6.2.

It is observed in Figure 3.9, for AVP application, the difference of operation is in the interval $t_1-t_3$. At time instant $t_3$, instead of recovering the output voltage to $V_{ref}$, the AVP controller maintains the new steady-state output voltage depending on the load line at $V_{ref}-\Delta I_o \cdot R_{droop}$.

Similarly, the switching point voltage $V_{sw}$ can be calculated in (3.32) by referring the parabolic curve during $t_1-t_2$ in (3.9).

$$V_{sw} = V_{max} - \frac{m_2}{2C_o} T_o^2$$

(3-35)
Considering the new adaptive voltage positioning level, the switching point voltage $V_{SW}$ can also be expressed during $t_2-t_3$. And, as previously discussed, the term $(1/2DT)^2$ can be ignored in (3.33) when the Buck converter is operated at high switching frequency and narrow output duty ratio.

$$V_{SW} = \frac{1}{2C} m_1 \left[ T_s^2 - \left( \frac{1}{2} DT_s \right)^2 \right] + \left( V_{ref} - R_{droop} \cdot \Delta I_o \right)$$  \hspace{1cm} (3-36)

By substituting (3.32) into (3.33), the switching point voltage $V_{SW}$ can be calculated in (3.34).

$$V_{SW} = DV_{max} + (1-D) \left( V_{ref} - R_{droop} \cdot \Delta I_o \right)$$  \hspace{1cm} (3-37)

From the equation (3.34), it is noted that, compared with (3-19), we can simply replace the voltage $V_{ref}$ with the new load line voltage at $V_{ref} \cdot \Delta I_o \cdot R_{droop}$. In the same way, the switching point voltage under loading step transient is able to be expressed in (3.35).

$$V_{SW} = D \left( V_{ref} - R_{droop} \cdot \Delta I_o \right) + (1-D)V_{min}$$  \hspace{1cm} (3-38)
Figure 3.9  Inductor current and capacitor voltage waveforms for AVP applications under unloading step change case ($R_{droop}$: droop resistance)

The hardware modification for AVP operation is minor, as shown in Figure 3.12. The inductor current sensor is required to feed the load line information $\Delta I_o$ to the ADC and DSP to implement the equations (3.34) and (3.35).

3.5.2 Ultrafast Input Voltage Transients

The two-switching-cycle compensation algorithm proposed in [31] has several drawbacks, such as, losing its applicability under the ultra-fast/large input voltage change scenarios ($\geq 2.5$ V) and requiring accurate design component value ($L_o$ and $C_o$) and current sensing information to calculate the formulas to control the converter.
Figure 3.10 Calculated duty ratio values under different input voltage step changes using (1) and (2) (X-axis: input voltage step change $\Delta v_{in}$; Y-axis: duty ratio) (a) $v_{in}=5V$, $v_{in1}=v_{in0}+\Delta v_{in}$; (b) $v_{in}=7.5V$, $v_{in1}=v_{in0}-\Delta v_{in}$.

In the simulation, it illustrates that the equations in (3.36) and (3.37) cannot be implemented physically by the digital controller, when the step down input voltage larger than 2V happens in one switching cycle, since the duty ratio $d_1$ and $d_2$ calculated from the equations (3.36) and (3.37) are complex numbers. Also the duty ratio $d_1$ will be less than zero while the input voltage step up change is larger than around 2.5V per switching cycle, which needs some modifications discussed in [31].

$$d_1 = \frac{1}{2} \left[ (1+k) - \sqrt{(1+k)^2 + \frac{4L}{v_{in1}T_s} \cdot \left( i_{L1} - 2i_o + i_{L\_end} - \frac{1}{2} k^2 v_{in1} T_s + \frac{A_o}{T_s} \right) } \right]$$ (3-39)

$$d_2 = k - d_1$$ (3-40)

The proposed voltage sensing CBC can be also applied to the ultra-fast/large transient cases, without depending on any knowledge of output filter parameters or current sensing information.

The input voltage transient slew rate is often limited by the input filter, which in fact weakens the practicability and advantage of the CBC controller for improving input voltage transient...
cases. However, it is definitely a unique feature for the proposed algorithm to solve both of the transient cases from input and output sides without adding algorithm complexity. Similarly, the main procedures of the proposed algorithm under step down input voltage transient are explained below:

1. It is assumed that an ultra-fast input voltage step down transient ends at the time point $t_0$, and the transient event detector will trigger the optimal controller, immediately. And the proposed digital CBC controller will set DPWM output to high (ON);

2. After a short period of delay for blanking the transition noise, the extreme voltage detector will be monitored by the DSP;

3. When the falling edge of the voltage detector is responded by the DSP as an external interrupt at $t_1$, the output voltage will be sampled;

---

Figure 3.11 Inductor current and capacitor voltage waveforms under input voltage step down transient
4. The CBC controller will calculate the $V_{SW}$ (using (3.27), but with calculated $d=V_o/v_{in}$ due to the variable input voltage) where the DPWM should be set to low (OFF, at $t_2$);

5. At $t_3$, the output voltage recovers to the desired voltage $V_{ref}$ and the conventional PID controller is reactivated for output voltage regulation.

For input voltage step up transient case, the proposed controller can be operated similarly, but instead of sensing the voltage valley $V_{min}$ and converting to $V_{SW}$, $V_{max}$ will be sampled for determining $t_2$ (using (3-19)). Also, the DPWM sequence needs to be changed, that is, to low (OFF) after $t_0$ and to high (ON) at $t_2$.

3.6 Hardware Implementation Diagram of the Proposed Digital Control System

The high-level system diagram of the digital charge balance controller for a synchronous Buck converter is illustrated in Figure 3.12.
3.6.1 Extreme Voltage Detector Design (For $t_1$, Detection)

Based on the phase shaping theory of allpass filter \[63\], the delay equalization transfer function in (3.22) is studied in this section for a design guideline. The delay equalization stage is expressed in the frequency domain in (3.38).

$$G_{delay}(s) = \frac{V_{o\_delay}(s)}{V_o(s)} = \frac{s - 1/R_f C_T}{s + 1/R_f C_T}$$  (3-41)

The frequency response of the magnitude and phase is expressed in (3.39) for the denominator and (3.40) for nominator by substituting $s = j\omega$. 

---

Figure 3.12 Hardware implementation diagram of the digital control system
\[ j\omega + \frac{1}{R_1C_T} = m_1 \angle \phi_1 \]  

(3-42)

\[ j\omega - \frac{1}{R_1C_T} = M_1 \angle \theta_i \]  

(3-43)

So the transfer function \( G_{\text{delay}}(s) \) is simplified in (3.41).

\[
G_{\text{delay}}(s) = -\frac{M_1}{m_1} \angle (\theta_i - \phi_i) = -\angle(\theta_i - \phi_i) = \angle \theta_d
\]  

(3-44).

Since at all values of frequency it is clear that the magnitude of \( G_{\text{delay}}(s) \) is unity, therefore, the only difference in frequency domain by using delay equalization (first Pade approximation) is the phase response, as compared to the ideal delay. The phase angle of \( G_{\text{delay}}(s) \), \( \theta_d \) is

\[
\theta_d = -\pi + \tan^{-1}\left(\frac{\omega}{-1/R_1C_T}\right) - \tan^{-1}\left(\frac{\omega}{1/R_1C_T}\right)
\]  

(3-45)

It is noted that \( \theta_d \) is approaching \(-180^\circ\) for high frequency and \(0^\circ\) for low frequency. This is shown in Figure 3.13, it is demonstrated that since the phase angle \( \theta_d \) is the phase of \( V_{o\_delay} \) with \( V_o \) as the reference, the delayed voltage \( V_{o\_delay} \) can be determined by moving \( V_{o\_delay} \) with constant magnitude through a range of \(180^\circ\) as the frequency increases.

![Figure 3.13 Phasor plot of the delay equalization transfer function](image-url)
While, the phase of the ideal delay function $e^{-\tau}$ is expressed in (3.43).

$$\theta_i = -\tau \omega$$  \hspace{1cm} (3-46)

Figure 3.14 Phase Plot of the Delay Equalization Circuit compared to the Ideal Delay

In Figure 3.14, the phase plots of the delay equalization and ideal delay are illustrated ($\tau=330\text{ns}$). It is demonstrated that the equalization circuit is capable of representing the ideal delay accurately up to very high frequency ($\Theta \tau \approx 3\text{ MHz}$) and also the phase angle (delay) is always lower than the ideal delay case.

As discussed in Section 3.3.2, the adjustable delay $t_{\text{delay}}$ can be tuned by selecting different value of $R_T$ and $C_T$. The proper delay should be selected to compromise two factors: 1) good time detection accuracy; and 2) sufficient voltage error for driving the output edge of the comparator (see Figure 3.3). Using the equation (3.22), the values of $R_T$ and $C_T$ can be calculated.

The experimental results shown in Figure 3.15 demonstrate the aforementioned delay based extreme voltage detector to detect time $t_i$. The pink waveform is the input sinusoidal signal at 100kHz with $1.5V_{pp}$ and the blue waveform is the output signal of extreme voltage detector. The delay time $t_{\text{delay}}$ is set to be 330ns by selecting $C_T$ as 330pF and $R_T$ as 499$\Omega$. 


3.6.2 Signal Conditioning Circuitry Design Guidelines

A single dual-channel analog-to-digital converter (ADC) is employed to sample output voltage error $v_{err, AD}$ and the inductor current $i_{L, AD}$. The inductor current measurement information is only used to implement the extension for AVP technique discussed in Section 3.5.1. As shown in Figure 3.12, the inductor current is re-constructed by matching the corner frequency of the low-pass filter with that of the inductor based on (3.44) to filter the voltage across the output inductor.

\[
R_{2, il_sens} \cdot C_{il_sens} = \frac{L_o}{R_L} \tag{3-47}
\]

The output of the inductor current sensor $i_{L, AD}$, in relation to the inductor current $i_L$ is equated in (3.45).

\[
i_{L, AD} = R_L \cdot \frac{R_{2, il_sens}}{R_{1, il_sens}} \cdot i_L \tag{3-48}
\]

Therefore, the selection of $R_{2, il_sens}/R_{1, il_sens}$ should be based on the maximum expected inductor current and the conversion range of the ADC.
The output voltage error $v_{err,AD}$ is calculated in the analog domain through use of the OPAMP configuration illustrated in Figure 3.12. As will be discussed, the output of the voltage error sensor is used for steady-state operation, and transient detection during a load transient. The output of the voltage error sensor is calculated in (3.46).

\[
v_{err,AD} = R_{f_{err}} \left( \frac{v_o}{R_{1_{AD}}} + \frac{V_{AD\_ref}}{R_{AD\_ref}} - \frac{V_{ref}}{R_{V\_ref}} \right) \tag{3-49}
\]

$V_{AD\_ref}$ represents the upper bound of the ADC conversion range. $R_{f_{err}}/R_{1_{AD}}$ and $R_{f_{err}}/R_{V\_ref}$ should be equal and selected based on the desired gain of $v_{err,AD}$. To level-shift the error voltage to the centre of the ADC conversion range, $R_{f_{err}}/R_{AD\_ref} = 1/2$. $R_{2_{AD}}$ should be selected based on (3.47).

\[
R_{2_{AD}} = \frac{R_{f_{err}}}{1 + \frac{R_{f_{err}}}{R_{V\_ref}} - \frac{R_{f_{err}}}{R_{AD\_Ref}}} \tag{3-50}
\]

By using the aforementioned OPAMP configuration, the voltage error will be centered based on the ADC conversion range. The configuration is also effective at cancelling common-mode noise present on the output voltage and power ground plane. In addition, since an arbitrary gain can be selected, the quantization resolution can be effectively increased without having to increase the number of ADC bits. Figure 3.16 illustrates the output of the voltage error sensor during steady-state operation.
As illustrated in Figure 3.12, the output of the voltage error sensor is also fed into a trans-impedance amplifier configuration. The trans-impedance amplifier is used to asynchronously detect load transients. The trans-impedance amplifier and threshold levels can be designed similar to [33]; however, since the output is not used to determine the capacitor zero cross-over point $t_1$, it is not necessary to precisely match the $C_o$ and $ESR$ time constant of the output capacitor. In addition, a capacitor $C_{f,\text{trans}}$ can be added in parallel with the feedback resistor to attenuate high-frequency noise.

### 3.6.3 Digital PID Compensator Design

In order to avoid the impact of the switching noise, during steady-state operation, the digital output of the ADC will be sampled by the controller at specific moments during the switching cycle. And this moment should be selected based on the following concerns: 1) the maximum duty ratio of the voltage mode controller is set to 80% to ensure necessary dynamic DPWM duty ratio; therefore the output voltage is required to be sampled when the switching noise has been effectively damped. 2) The ADC acquisition delay (10ns) and control law calculation delay (250ns) need to be taken into account, so that after sampling the output voltage, there is enough time to complete the calculation of the subsequent duty cycle before the next switching cycle.
starts (see Figure 3.17). Thus, the output voltage is sampled 260ns before the end of the switching period.

![Diagram](image)

Figure 3.17 Sample and acquisition of digital linear controller used during steady-state

It is noted that although in theory a small DC offset may be present in the measurement of $v_{err, AD}$ due to the fact that the voltage error is sampled near the end of the switching period, an adjustment can be made to the dc reference of the digital controller in the codes.

The digital PID controller design follows the emulation methods [64], so a continuous controller is designed with PID configuration. The two zeros are located at $\frac{1}{2}$ of the double pole frequency and near to the double pole frequency of the output filter to improve the phase margin and the bandwidth. The continuous time PID controller’s transfer function is written in the equation (3-51).

$$G_{PID}(s) = \frac{50s^2 + 5.3 \times 10^6 s + 1.243 \times 10^{11}}{s} \quad (3-51)$$

A very simple but effective method of obtaining a discrete equivalent from a continuous transfer function is derived using pole-zero matching [64]. This method can accurately emulate the frequency response of the continuous system up to $\frac{1}{2}$ of the switching frequency. In the implementation, the Z-transform of the PID controller is expressed in (3-52).
\[ G_{PD}(z) = \frac{2.127 - 3.662z^{-1} + 1.572z^{-2}}{1 - z^{-1}} \]  

(3-52)

The Bode plot of the compensated system is shown in Figure 3.18 with 65kHz bandwidth and 60 deg phase margin.

In order to avoid limit-cycle oscillation issue [65], the DPWM should have a minimum resolution of 10 bit, considering the ADC resolution and the amplifier gain of the circuitry discussed in equations (3.46) and (3.47) of Section 3.6.2.
3.7 Calculation of Voltage Deviation and Settling Time Using Voltage Sensing Based CBC

In addition to improving the dynamic performance of a Buck converter, the proposed controller also simplifies the design of the output filter since its response to a large-signal load transient is predictable. It is possible to calculate the transient response (settling time, voltage deviation) of a converter experiencing an arbitrary load variation. For simplification, the following analysis assumes a properly designed converter in which the input and output voltage remains relatively constant during the transient interval.

3.7.1 Settling Time

Referring to Figure 3.6, $T_1$ and $A_{\text{discharge}}$ (for a loading step) are calculated using (3.49) and (3.50) respectively.

\begin{align}
T_1 &= |\Delta I_o| \cdot \frac{L_o}{V_{in} - V_o} \quad \text{(3-53)}
\end{align}

\begin{align}
A_{\text{discharge}} &= \frac{1}{2} \cdot T_1 \cdot |\Delta I_o| = \Delta I_o^2 \cdot \frac{L_o}{2(V_{in} - V_o)} \quad \text{(3-54)}
\end{align}

$\Delta I_o$ represents the load current transient step value ($\Delta I_o = I_o^2 - I_o^1$). For a loading step, $A_{\text{charge}}$ is calculated using (3.51).

\begin{align}
A_{\text{charge}} &= T_2^2 \cdot \frac{V_{in}(V_{in} - V_o)}{2V_o L_o} \quad \text{(3-55)}
\end{align}

In order for (3.28) to be satisfied, $A_{\text{discharge}}$ must equal $A_{\text{charge}}$. Therefore, (3.50) can be substituted into (3.51) and $T_2$ can be calculated as shown in (3.52).

\begin{align}
T_2 &= \sqrt{\frac{V_{in} L_o^2 \Delta I_o^2}{V_{in}(V_{in} - V_o)^2}} = \frac{L_o |\Delta I_o|}{V_{in} - V_o} \cdot \sqrt{\frac{V_o}{V_{in}}} \quad \text{(3-56)}
\end{align}
A geometric relationship between $T_2$ and $T_3$ is defined in (3.53).

$$T_3 = \frac{V_{\text{in}} - V_o}{V_o} \cdot T_2$$

(3-57)

Therefore, the total settling time for a loading step transient is calculated in (3.54).

$$T_{\text{set,pos}} = T_1 + T_2 + T_3 = \frac{L_o \cdot |\Delta I_o|}{V_{\text{in}} - V_o} \left(1 + \frac{V_{\text{in}}}{V_o} \sqrt{\frac{V_o}{V_{\text{in}}}}\right)$$

(3-58)

Similarly, the settling time for an unloading step is calculated in (3.55).

$$T_{\text{set,neg}} = T_1 + T_2 + T_3 = \frac{L_o \cdot |\Delta I_o|}{V_o} \left(1 + \frac{V_{\text{in}}}{V_{\text{in}} - V_o} \sqrt{\frac{V_{\text{in}} - V_o}{V_{\text{in}}}}\right)$$

(3-59)

It is interesting to note that the settling time of the Buck converter with charge balance controller, undergoing a load transient, is not dependent on the output capacitance $C_o$ and $ESR$ value. For a fixed input and output specifications, in this case 12V-1.5V, the settling time of the Buck converter is only related to output inductance $L_o$. This is quite different from the behavior of a Buck converter controlled by a linear compensator. This is due to the fact that the charge balance controller does not use the output voltage as a feedback mechanism, but rather the occurrence of time instants $t_0$-$t_3$. The intervals between these time instants only depend on the inductor current slew rates and the magnitude of the load current transient.

Figure 3.19 illustrates the calculated settling times for a Buck converter for various values of $L_o$ and different load current step magnitudes (assuming $V_{\text{in}}$=12V and $V_o$=1.5V). Using (3.54) and (3.55), the settling time for a Buck converter ($V_{\text{in}}$ =12V, $V_o$ =1.5V, $L_o$=1μH) undergoing a +10A load step and a -10A load step is calculated to be 4μs and 14μs respectively.
To select a proper inductor, the maximum inductor peak current, for a loading step change, at time $t_2$, is expressed in (3.56).

$$I_{L_{\text{peak, max}}} = \Delta I_{o_{\text{max}}} \left(1 + \frac{V_o}{\sqrt{V_{in}}}\right)$$  \hspace{1cm} (3-60)

$\Delta I_{o_{\text{max}}}$ equals the maximum expected load transient. The saturation current of the inductor should be greater than $I_{L_{\text{peak, max}}}$ since the proposed control method assumes linear inductor behaviour.
3.7.2 Voltage Deviation

Under the proposed controller, it is also possible to estimate the voltage deviation due to an arbitrary load current step change. Using the parabolic functions derived in Section 3.3.1 and Section 3.3.4, the voltage variations can be expressed accordingly.

For loading step transient, the output voltage can be written as (3.57)

\[
v_o(t) = \frac{V_{in} - V_o}{2L_o C_o} \left( t^2 - 2T_1 t \right) + \frac{V_{in} - V_o}{L_o} \left( t - T_1 \right) \cdot ESR + V_{ref} \tag{3-61}
\]

In (3.57), the steady-state output voltage ripple and the equivalent series inductance (ESL) are neglected in the calculation. In order to determine the time when the output voltage reaching its minimum (\(t_{min}\)), it is necessary to calculate the derivative of the output voltage with respect to time, as expressed in (3.58).

\[
\frac{dv_o}{dt} = \frac{V_{in} - V_o}{L_o C_o} \left( t - T_1 + ESR \cdot C_o \right) \tag{3-62}
\]

By equalizing the (3.58) to zero, the time \(t_{min}\) is calculated in (3.59).

\[
t_{min} = T_1 - ESR \cdot C_o = \frac{|\Delta I_o| \cdot L_o}{V_{in} - V_o} - ESR \cdot C_o \tag{3-63}
\]

Also, it is should be noted that the minimum voltage time \(t_{min}\) does not happen at \(t_1\) but undergoes a period of constant lead time depending on the product of output capacitance and ESR.

By substituting (3.59) into (3.57), \(\Delta v_{o,pos}\) is solved in (3.60).

\[
\Delta v_{o,pos} = \frac{ESR^2 C_o^2 \left( V_{in}^2 - 2V_{in} V_o + V_o^2 \right) + \Delta I_o^2 L_o^2}{2 \left( V_{in} - V_o \right) L_o C_o} \tag{3-64}
\]

For loading step transient, the output voltage can be written as (3.61).
\[ v_o(t) = -\frac{V_o}{2L_oC_o} \left( t^2 - 2T_1t \right) - \frac{V_o}{L_o} (t - T_1) \cdot ESR + V_{ref} \]  

(3-65)

In order to determine the time when the output voltage reaching its maximum value (\( t_{max} \)), it is necessary to calculative the derivative of the output voltage with respect to time, as expressed in (3.62).

\[ \frac{dv_o(t)}{dt} = \frac{V_o}{L_oC_o} (t - T_1 + ESR \cdot C_o) \]  

(3-66)

By setting the (3.62) to zero, the time \( t_{max} \) is calculated in (3.63).

\[ t_{max} = T_1 - ESR \cdot C_o = \frac{\Delta I_o \cdot L_o}{V_o} - ESR \cdot C_o \]  

(3-67)

Similarly, the overshoot for an unloading step is calculated in (3.64).

\[ \Delta v_{o_{\text{neg}}} = \frac{ESR^2 C_o^2 v_o^2 + \Delta I_o^2 L_o^2}{2V_o L_o C_o} \]  

(3-68)

Figure 3.20 and Figure 3.21 illustrate the estimated voltage deviation for a Buck converter controlled by the charge balance controller undergoing a loading step and unloading step respectively. It also demonstrates the fact stated in Section 3.3.3 that under loading and unloading transients, the output voltage deviations are asymmetrical.
Figure 3.20 Estimated voltage undershoot for a Buck converter under charge balance control ($V_{in}=12V$, $V_o=1.5V$, $L_o=1\mu H$, $ESR=0.1m\Omega$)

Figure 3.21 Estimated voltage overshoot for a Buck converter under charge balance control ($V_{in}=12V$, $V_o=1.5V$, $L_o=1\mu H$, $ESR=0.1m\Omega$)
Using (3.60) and (3.64), the voltage deviation for a Buck converter \(V_{in}=12\text{V}, V_o=1.5\text{V}, L_o=1\mu\text{H}, C_o=180\mu\text{F}, ESR=0.1\text{m\Omega}\) undergoing a +10A load step and a -10A load step is calculated to be -27mV and 185mV respectively.

### 3.7.3 Estimation Error of Switching Point Voltage

In lieu of calculating time period \(T_1-T_3\), the proposed controller maps the time information to associated voltage samples \(V_{max}, V_{sw},\) and \(V_{ref}\) so that a parameter-insensitive formula set can be derived. However, the assumption that the \(ESR\) is negligibly small influences the accuracy of the time detection, once the Buck converter is with significant \(ESR\) value. Also, it is important to analyze the delay effects of the extreme detector proposed in Section 3.3.2 on the estimation of the SPV \(V_{SW}\).

For loading transient, considering the delay \(t_{delay}\) of the extreme voltage detector, the actually sensed voltage valley is calculated in (3.65) based on the output voltage function in (3.57). 

\[
V_{min\_sen} = V_{ref} - \frac{ESR^2 C_o \left(V_{in}^2 - 2V_{in} V_o + V_o^2\right) + \Delta i_o^2 L_o^2}{2(V_{in} - V_o) L_o C_o} + \frac{(V_{in} - V_o) \cdot t_{delay}^2}{2L_o C_o} \quad (3-69)
\]

In (3.65) the first two terms represent the actual minimum voltage and the third term is the voltage deviation due to the extreme voltage detector delay.

The real switching point voltage \(V_{SW\_ESR\_pos}\) is expressed in (3.66) if the significant \(ESR\) is taken into account.

\[
V_{SW\_ESR\_pos} = V_{ref} - \frac{V_{in} - V_o}{V_{in}} \cdot \frac{ESR^2 C_o \left(V_{in}^2 - 2V_{in} V_o + V_o^2\right) + \Delta i_o^2 L_o^2}{2(V_{in} - V_o) L_o C_o} + ESR \cdot \Delta i_o \cdot \sqrt{\frac{V_o}{V_{in}}} \quad (3-70)
\]

In (3.66), the third term equals the voltage across the \(ESR\) at \(t_2\) or switching point.

On the other hand, because of the impact of \(ESR\) and the \(t_{delay}\), the calculated SPV using (3.27) and the actually sensed minimum voltage \(V_{min\_sen}\) (3.65) is expressed in (3.67).
Similarly, under the unloading transient the sensed maximum voltage $V_{\text{max_sen}}$ and the real switching point voltage considering $ESR$, $V_{SW_{ESR_{neg}}}$ can be expressed in (3.68) and (3.69).

$$V_{\text{max_sen}} = V_{\text{ref}} + \frac{ESR^2 C_o^2 V_o^2 + \Delta I_o^2 L_o^2}{2V_o L_o C_o} \cdot \frac{V_o \cdot t_{\text{delay}}^2}{2L_o C_o}$$  \hspace{1cm} (3-72)

$$V_{SW_{ESR_{neg}}} = V_{\text{ref}} + \frac{V_o}{V_{\text{in}}} \cdot \frac{ESR^2 C_o^2 V_o^2 + \Delta I_o^2 L_o^2}{2V_o L_o C_o} - ESR \cdot \Delta I_o \cdot \sqrt{\frac{V_{\text{in}} - V_o}{V_{\text{in}}}}$$  \hspace{1cm} (3-73)

And the calculated switching point voltage under unloading transient is calculated in (3.70).

$$V_{SW_{sen_{neg}}} = \frac{V_o}{V_{\text{in}}} \cdot V_{\text{max_sen}} + \frac{V_{\text{in}} - V_o}{V_{\text{in}}} \cdot V_{\text{ref}}$$  \hspace{1cm} (3-74)

Based on the equations (3.65), (3.66) and (3.69), (3.70), the estimation error of the SPV is simulated under various output capacitance and $ESR$ conditions for both of the load transient cases and the results are shown in Figure 3.22 and Figure 3.23. Using the SPV method, the peak estimation error is about 4.5% for both of the cases.

It is worth noting that time constant $(ESR \cdot C_o)$ [59] is required to be smaller than the period of $T_1$ in Figure 3.2 and Figure 3.6, which is expressed in (3.71) for loading transient, and in (3.72) for unloading transient. Otherwise, the voltage peak/valley will not happen in the voltage response waveform, meaning the extreme voltage detector is not applicable for detection of $t_1$.

$$ESR \cdot C_o < \frac{\Delta I_o \cdot L_o}{V_{\text{in}} - V_o}$$  \hspace{1cm} (3-75)

$$ESR \cdot C_o < \frac{\Delta I_o \cdot L_o}{V_o}$$  \hspace{1cm} (3-76)
3.8 Simulations and Experimental Verifications

3.8.1 Simulation Results

In order to verify the functionalities of the proposed optimal algorithm, a dc-dc Buck converter model undergoing load step transient conditions is simulated. The design parameters
are listed as follows in the Table 3-1. And the simulated results are shown in Figure 3.24 and Figure 3.25. SABER simulation tools are used in this thesis, which is powerful for simulating a mixed signal power converter system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Table 3-1 Design Parameters of the Dc-Dc Buck Voltage Regulator Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>INPUT VOLTAGE</td>
<td>12 V</td>
</tr>
<tr>
<td>$V_o$</td>
<td>OUTPUT VOLTAGE</td>
<td>1.5 V</td>
</tr>
<tr>
<td>$f_s$</td>
<td>SWITCHING FREQUENCY</td>
<td>350 kHz</td>
</tr>
<tr>
<td>$L_o$</td>
<td>OUTPUT FILTER INDUCTANCE</td>
<td>1 μH</td>
</tr>
<tr>
<td>$R_L$</td>
<td>DC RESISTANCE OF THE INDUCTOR</td>
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</tr>
<tr>
<td>$C_o$</td>
<td>OUTPUT FILTER CAPACITANCE</td>
<td>180 μF</td>
</tr>
<tr>
<td>ESR</td>
<td>EQUIVALENT SERIES RESISTANCE</td>
<td>0.5 mΩ</td>
</tr>
<tr>
<td>ESL</td>
<td>EQUIVALENT SERIES INDUCTANCE</td>
<td>100 pH</td>
</tr>
</tbody>
</table>

Figure 3.24 Simulation results of the Buck converter under a loading step 0 A→10 A
From Figure 3.24 and Figure 3.25, we can observe the similar response waveforms to those in the previous sections by theoretical analysis using proposed CBC controller. SPV $V_{SP}$ is shown in each of the cases for reference. Under a 10 A load transient, the voltage deviation is -35 mV for loading step and 185 mV for unloading step, while, the setting time is 4 $\mu$s for loading case and 14.5 $\mu$s for unloading case, respectively.

Also for comparison, a well-designed digital PID controller (bandwidth: $\approx$65 kHz, Phase margin $\approx$60°) is also simulated by SABER with Z-domain digital controller implementation for regulating the dc-dc Buck converter shown in Figure 3.26 and Figure 3.27. The PWM signal is shown for the comparison between proposed CBC controller ($sw\_CBC$) and linear voltage mode controller ($sw$) in the top section. The inductor current ($i_L$) and output voltage waveforms ($v_o$) are also demonstrated with two types of controllers shown on the bottom sections.
Figure 3.26 Simulation results of loading transient case for comparison between CBC and linear mode of controller (0 A -> 10 A)

Figure 3.27 Simulation results of unloading transient case for comparison between CBC and linear mode of controller (10 A -> 0 A)
To sum up, under the load transient cases, for loading step, the proposed controller improves the dynamic performance by reducing the undershoot (by 70%) and settling time (by 93%), compared to the conventional voltage mode control. While, under unloading transient, the overshoot is reduced by 16% and settling time is shortened by 80% with the help of the proposed digital CBC controller.

As proposed in the previous sections, the robustness of the proposed scheme is tested under the following design conditions in Table 3-2. It demonstrates that even the output inductance or capacitance is doubled, the optimal load transient response performance can still be achieved (see Figure 3.28 and Figure 3.29).

**Table 3-2  Design Parameters of the Robustness Testing and Transient Performance**

<table>
<thead>
<tr>
<th></th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
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<tbody>
<tr>
<td>$L_o$</td>
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<td>1μH</td>
<td>2μH</td>
</tr>
<tr>
<td>$C_o$</td>
<td>360μF</td>
<td>180μF</td>
<td>180μF</td>
</tr>
<tr>
<td>Δ$V_o$ (0A-10A)</td>
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<td>-35mV</td>
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</tr>
<tr>
<td>Setting time (0A-10A)</td>
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<td>Δ$V_o$ (10A-0A)</td>
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<td>185mV</td>
<td>315mV</td>
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<tr>
<td>Setting time (10A-0A)</td>
<td>15μs</td>
<td>14.5μs</td>
<td>27μs</td>
</tr>
</tbody>
</table>

In the simulations, the PID controller is designed by well matching the nominal output inductance and capacitance value in Case 2. Due to the unchanged PID controller, some slight ringing back appears during the transients between CBC and PID controllers in Case 1 and 3. And this ringing back can be minimized by optimally designing the PID controller in each of the circumstances, for example in Case 2, resulting in smooth transition [39][41].
Figure 3.28  Simulation results for robustness testing under inductance and capacitance variations under 0A-10A loading transient

Figure 3.29  Simulation results for robustness testing under inductance and capacitance variations under 10A-0A unloading transient

The voltage deviations and settling time are tabulated in Table 3-2 under 10A load transients.

As discussed in the Section 3.5.1, the proposed digital controller can be extended for adaptive voltage positioning technique. In the simulations shown in Figure 3.30 and Figure 3.31, the droop
resistance is selected to be 5mΩ for the load line regulation. The time instants are also figured in the simulation results to illustrate the CBC principles and the switching point voltage $V_{sw}$ are also shown for $t_2$ detection.

From the simulation, using AVP technique, the undershoot of the output voltage is -60mV with 4.8μs settling time undergoing a 10A loading step. On the other hand the output overshoot is 65mV with 8.5μs settling time following a 10A unloading step transient.
To verify the derived CBC equation for input voltage step transients in Section 3.5.2, 2.5V step input voltage transient is simulated for 10A constant load current.

Figure 3.32  Simulation results of the dc-dc Buck converter following input voltage step down case 7.5 V → 5 V

Figure 3.33  Simulation results of the dc-dc Buck converter following input voltage step up case 5 V → 7.5 V

Using the equation set discussed in the previous sections, the switching point voltage for input voltage case is calculated to achieve optimal settling time. In Figure 3.32 and Figure 3.33, the undershoot is 22 mV with 7 μs settling time for input voltage step down transient, while, under input voltage step up transient, the overshoot is 18 mV with 6μs recovery time.
3.8.2 Prototype Design and Experimental Results

A 12 V-1.5 V prototype is designed using the same parameters in the simulation and a fixed-point 32-bit MCU TMS320F28027 [62] is employed to implement the proposed CBC control algorithm, which is shown in Figure 3.34.

![Experimental prototype of the proposed CBC controlled dc-dc Buck converter](image)

Figure 3.34  Experimental prototype of the proposed CBC controlled dc-dc Buck converter

In order to achieve fast load current transients, a test bench was designed with series and parallel arrays of power resistors and two MOSFETs, as illustrated in Figure 3.35. The specific surface-mount power resistors were chosen based on their low ESL values, allowing for fast current transients. The load test bench was also placed on the same printed circuit board as the prototype. The overall inductance of the entire test bench is estimated to be <3nH, allowing for loading and unloading current changes of slew rates $|\frac{dI_o}{dt}|>250\text{A/μs}$.

A similar load test bench is used for all experiments conducted in subsequent chapters.

All output voltage measurements were measured near the midpoint of the output capacitor bank. In order to mitigate noise effects, a very short probe ground wire was soldered to the ground side of the output capacitor bank. In addition, the bandwidth of the scope was limited to 20MHz.
Figure 3.35 Load test bench used for fast load transients

Figure 3.36 to Figure 3.39 show comparative results for a Buck converter undergoing load step transients using conventional voltage mode controller and proposed voltage sensing based CBC controller. The voltage detector signal is shown for time detection of $t_1$. In order to illustrate the operation of the CBC controller, the charge balance control intervals have been shown in the figures.

Experimental results, shown in Figure 3.36 and Figure 3.38, demonstrate the transient performance of conventional linear voltage mode controller (bandwidth $\approx 65$ kHz, Phase margin $\approx 60^\circ$) under the load current step change between no load (0A) and full load (10A). Limited by the bandwidth, the linear voltage mode controller will cause larger voltage variations and longer recovery time. For loading transient, the voltage undershoot is about $-170$ mV with $61 \mu$s settling time, while, the overshoot is about $185$ mV with $56 \mu$s settling time.
Figure 3.36 Experimental results of Buck converter under loading transient case 0 A - 10 A using linear mode controller

Figure 3.37 Experimental results of Buck converter under loading transient case 0 A - 10 A using CBC controller
It is demonstrated, under a 10A loading step transient, the settling time is reduced from 61\(\mu\)s (using voltage mode controller) to 3.5\(\mu\)s (using CBC). In other words, the settling time of the Buck converter with CBC is shortened by 94.3% compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (4\(\mu\)s) and the simulation result (3.5\(\mu\)s).

Also, it is shown that voltage undershoot is reduced from -170mV (using the linear controller) to -35mV (using CBC). The undershoot of the Buck converter with CBC controller is reduced by 79.4% compared to that of the voltage mode controller Buck converter. And the -35mV undershoot is accordance with the calculated undershoot (-25mV) and the simulated undershoot (-35mV).

Figure 3.38 and Figure 3.39 show a voltage mode controlled Buck converter and the CBC controlled Buck converter undergoing a 10A to 0A load step change, respectively.

![Figure 3.38](image)

**Figure 3.38** Experimental results of Buck converter under unloading transient case 10 A- 0 A using linear mode controller
Figure 3.39  Experimental results of Buck converter under unloading transient case 10 A- 0 A using CBC controller

It is demonstrated, under a 10A unloading step transient, the settling time is reduced from 56 μs (using voltage mode controller) to 13.5 μs (using CBC). In other words, the settling time of the Buck converter with CBC is shortened by 75%, compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (14 μs) and the simulation result (14.5 μs).

Also, it is shown that voltage overshoot is only reduced from 185mV (using the linear controller) to 180mV (using CBC) based of the narrow operating output ratio at 12V-1.5V. But the 180mV overshoot is accordance with the calculated undershoot (185mV) and the simulated (185mV).

The adaptive voltage positioning technique is applied to the proposed analog CBC controller with simple modification on top of the non-AVP proposed analog CBC scheme. And in the
experimental results shown in Figure 3.40 and Figure 3.41, the droop resistance is selected to be 5mΩ.

It is demonstrated that, for a 10A loading step transient, the undershoot is -10mV at -50mV AVP regulation. And the settling time is 5.6μs. The experimental result in Figure 3.41 demonstrates that the overshoot is 115mV above the AVP regulation level of 50mV (165mV in total).
As discussed in the previous sections, the proposed scheme is robust against the variations of output inductance and capacitance. Therefore, a robustness testing has been conducted and the test results are shown in Figure 3.42 to Figure 3.45, the output inductance and capacitance are respectively doubled. However, the voltage mode controller design is unchanged, which is well-designed for matching the double-pole of the nominal output filter ($L_o=1\mu H$ and $C_o=180\mu F$).
Figure 3.42 Robustness test of the proposed controller for a Buck converter with Lo=1μH and Co=360μF under 10A loading step transient

Figure 3.43 Robustness test of the proposed controller for a Buck converter with Lo=1μH and Co=360μF under 10A unloading step transient
Figure 3.44 Robustness test of the proposed controller for a Buck converter with $L_o=2\mu H$ and $C_o=180\mu F$ under 10A loading step transient

Figure 3.45 Robustness test of the proposed controller for a Buck converter with $L_o=2\mu H$ and $C_o=180\mu F$ under 10A unloading step transient
Table 3-3 provides the summarized performance of the robustness testing of the CBC. Referring to the simulated robustness testing in Table 3-2, the experimental results are in close correspondence of the simulations.

<table>
<thead>
<tr>
<th></th>
<th>Figure 3.42</th>
<th>Nominal Case</th>
<th>Figure 3.44</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_o$</td>
<td>1μH</td>
<td>1μH</td>
<td>2μH</td>
</tr>
<tr>
<td>$C_o$</td>
<td>360μF</td>
<td>180μF</td>
<td>180μF</td>
</tr>
<tr>
<td>$Δv_o$ (0A-10A)</td>
<td>-25mV</td>
<td>-35mV</td>
<td>-80mV</td>
</tr>
<tr>
<td>Setting time (0A-10A)</td>
<td>4μs</td>
<td>3.5μs</td>
<td>8μs</td>
</tr>
<tr>
<td>$Δv_o$ (10A-0A)</td>
<td>85mV</td>
<td>180mV</td>
<td>340mV</td>
</tr>
<tr>
<td>Setting time (10A-0A)</td>
<td>13μs</td>
<td>13.5μs</td>
<td>27μs</td>
</tr>
</tbody>
</table>

### 3.9 Conclusions

In this chapter, a voltage sensing based charge balance control algorithm is proposed to optimize the response of Buck converters without relying on design parameters. An extreme voltage detector is employed to detect the critical time instant $t_1$ and switching point voltage concept is applied to implement the CBC controller based on output voltage curve analysis. It is demonstrated through simulations and experimental results, that the proposed parameter-independent algorithm can be implemented for low-ESR designed Buck converter to optimize the transient response performance. Through the comparison experiments, under the load transient cases, for loading step, the voltage undershoot is suppressed by 79% and settling time is improved by 94%, while, for unloading step, the converter overshoot is reduced by 3% and settling time is shortened by 76%. Furthermore, a possibility is shown through verifications that the proposed algorithm can be extended for AVP applications without increasing algorithm complexity. Also, the robustness enhancement of the proposed algorithm is discussed and demonstrated.
Chapter 4

A Parabolic Curve Fitting Based Charge Balance Control Algorithm for Dc-Dc Buck Converter

4.1 Introduction

With the revolution of integration technology, it is possible to fabricate powerful microprocessors with more transistors on chip, but resulting in higher load demand for power supplies. In the meanwhile, to maintain/reduce the overall power consumption of the microprocessor, the output voltage level keeps dropping. As a result, the requirements of voltage regulator (VR) for powering next-generation microprocessor are more and more stringent, that is, lower output overshoot/undershoot and shorter settling time under increasingly large load transients. Due to the undesired voltage deviations, OSCAN or electrolytic capacitors are usually employed to serve as the major output capacitance in parallel with small capacitance ceramic capacitors. Therefore, the impact of ESR on the output voltage during steady-state and load transient is significant.

However, in the previous research of fast dynamic controllers [32]-[41] based on charge balance concept, ESR is always assumed to be negligible low for the simplicity of algorithm derivations and implementation. Although the CBC concept can be easily implemented using digital signal processing devices, such as DSP and FPGA and extensive work has been conducted in designing digital CBC controllers that further improves robustness [35][36], practical performance [37][38] and simplicity of the control system, the applicability of the previously proposed CBC controllers is limited for only low ESR designed Buck converters.

This chapter is organized as follows. In Section 4.2, the ESR effect on the output voltage ripple is outlined in time and frequency domain as a fundamental of the proposed algorithm. After
that, the basic idea of parabolic curve fitting based charge balance control is introduced. Also, in this section, the parameter-independent and current-sensorless mechanism for detecting the critical time points \( t_1 \) and \( t_2 \) is explained. In Section 4.3, the mathematical expressions of the proposed algorithm are derived based on parabolic curve fitting analysis to determine the critical time instants. And this concept can be extended for AVP applications for modern microprocessor voltage regulators (VRs) design guidelines. The simulations and experimental results are shown in Section 4.4 to validate the proposed optimal control algorithm, followed by the main conclusions in Section 4.5, finally.

4.2 Basic Idea of Parabolic Curve Fitting Based Charge Balance Control

4.2.1 Impact of \( ESR \) on the Output Voltage

For reference, Figure 4.1 shows a generally designed synchronous Buck converter. \( Q_1 \) and \( Q_2 \) form a synchronous rectifier (SR) configuration and driven by the SR driver complimentarily with dead time. \( R_L \) is the \( DCR \) of the output inductor \( L_o \). And \( ESR \) represents the equivalent series resistance of the output capacitor \( C_o \).

![Figure 4.1  A generally designed synchronous Buck converter](image)

In most of the Buck converter designs, there exists a capacitor bank at the output end to serve as a filter. And in order to provide enough amount of capacitance, normally, electrolytic or OSCAN capacitors (with large capacitance) are employed in parallel with ceramic capacitors (with small capacitance). In this case, the total \( ESR \) of the output capacitor bank would be
significant and contribute piecewise linear voltage ripple to the output voltage. For example, if a 470μF OSCAN capacitor (with 5mΩ ESR) in parallel with a 47μF ceramic capacitor (with 0.5mΩ ESR), the ac component of the inductor current at the switching frequency will mainly flow through the OSCAN capacitor branch due to the lower impedance. The effect of the ESR in OSCAN capacitor will dominate the total ESR characteristics of the capacitor bank, so the output voltage ripple will be almost piecewise linear and in phase with the inductor current ripple in Figure 4.1. (in green). On the contrary, if we assume the 470μF capacitor has 0.5mΩ low ESR but a significant ESR of 5mΩ in the 47μF capacitor, the result will be different. The total ESR of this capacitor bank will be lower compared to the previous condition. So the output voltage ripple is reduced and near to the ideal capacitor case (in pink).

Figure 4.2 Output voltage ripple on output capacitor with low and high ESR

The aforementioned phenomenon can be also explained in the frequency domain. Referring to the simulation results shown in the Figure 4.2, for 470μF/5mΩ 47μF/0.5mΩ case (in green),
the ESR value will be dominated by the 470μF capacitor at the switching frequency (in 100kHz order). And the total ESR effect can be estimated by calculating the magnitude of the Bode plot, for example at 350kHz, the magnitude is around -46dB, which demonstrates the ESR of $10^{-46\text{dB/20}}$ ($\approx 0.005$) Ω. In the other case, the magnitude of the Bode plot is about -60dB at 350kHz, which is equivalent to a $10^{-60\text{dB/20}}$ ($\approx 0.001$) Ω ESR (in pink).

Unfortunately, in the previous work, the time detection of $t_1$ has been done according to the output voltage peak/valley instant under the assumption that the Buck converter is designed with very low ESR. However, in the reality, voltage peak/valley will appear ahead of $t_1$ because of the ESR effects. It will be discussed in Section 4.3 that the lead time is determined by the product of output capacitance and ESR, which is referred to as the time constant ($\text{ESR} \times C_o$). The simulation shows that when the ESR is larger than 1 mΩ (with $C_o=180\mu\text{F}$) [60], the estimation error of SPV will significantly increase to cause a ringing back issue and even worse to result in instability of the control system. The simulation result shown in Figure 4.3 demonstrates this phenomenon.

Figure 4.3  Bode plots of the capacitor bank with different types of output capacitors (blue: 470μF/5mΩ and 47μF/0.5mΩ capacitor bank; pink: 47μF/5mΩ and 470μF/0.5mΩ capacitor bank solid magnitude response, dotted phase response)
when the original CBC controller regulates the Buck converter with high $ESR$ value (200μF/5mΩ).

**Figure 4.4** Ringing back issue using the digital controller proposed in Chapter 3 caused by large $ESR/ESR*C_0$ time constant impact

To compensate the $ESR$ effects on the time detection but without sacrificing the robustness of the voltage sensing based CBC controller, a parabolic curve fitting based CBC controller is proposed in this chapter. This controller is capable of estimating the design parameters through sampling the output voltage during load transients. After very simple calculation, a voltage reference will be built based on the curving fitting methodology to detect time $t_1$. And two different control schemes can be employed for $t_2$ detection, which are referred to as timing control and $V_{SW}$ control.
4.2.2 Operations of the Parabolic Curve Fitting Based CBC Controller under Load Current Transient Case

Figure 4.5 Inductor current and capacitor voltage waveforms for non-AVP applications ($v_o$: output voltage in red, solid; $v_r$: fitted voltage reference in green, solid; $v_c$: ideal capacitor voltage in blue, dotted line)

Some generally designed Buck converters could have significant time constant $ESR*C_o$ (for example, ceramic capacitors in parallel with a large value of OSCON and/or electrolytic capacitors), but all of the existing schemes assume that the $ESR$ is negligibly low to derive the algorithms [32]-[41]. But when the $ESR$ value is increasing (keep the output capacitor constant), the algorithm error will rise exponentially to an unacceptable range causing ringing-back problem and deteriorating the overall response performance and even the stability.

As shown in Figure 4.4, for a dc-de Buck converter with significant time constant $ESR*C_o$, during unloading step load transient, the waveforms of inductor current $i_L$, output voltage $v_o$ and ideal capacitor voltage $v_c$ are illustrated. Mathematically, under the well-established assumption that the inductor current $i_L$ is piecewise linear, the output voltage waveform $v_o$ will present a parabolic shape. If we express the output voltage waveform $v_o$ (in solid red, see Figure 4.4) and
the ideal capacitor voltage $v_c$ (in dotted blue, see Figure 4.4) using the second order time function in the form of (4.1), the two functions will have exactly the same coefficient $a$ of the quadratic items.

$$v(t) = at^2 + bt + c$$  \hspace{1cm} (4-1)

And this conclusion is always true, even when we consider the parasitic $ESR$ and/or $ESL$ in the output capacitors. More precisely, under the same input $V_{in}$, steady-state output $V_o$ and unloading transient operating conditions, as long as the converters have the identical resonant/corner frequency of the output LC filter (i.e. $1/2\pi\sqrt{L_o C_o}$), the output voltage waveform of generally designed dc-dc buck converters is a family of parabolas which passes the point $(t_1, V_{max})$. The mathematical proof is derived in the equations (4.3)-(4.10) in the next section.

From Figure 4.4, it is observed that when the capacitor current undergoes zero-crossing at $t_1$, the $ESR$ effect on the output voltage will vanish, meaning the voltages $v_o$ and $v_c$ will be equal. So if the shape parameter $a$ in (4.1) is solved by using three sampled data points, the critical instant $t_1$ will be able to detect by comparing a fitted curve $v_r(t)$ in (4.2) with $v_o(t)$. In Figure 4.4, the dashed light blue curve illustrates the fitted voltage reference $v_r(t)$. Another instant $t_2$, when we change the DPWM signal from low (OFF) to high (ON), can be determined by either the pre-calculated time intervals ($T_2$) or the output voltage value (switching point voltage $V_{sw'}$) in this chapter, the two control methods are named as *timing control* and *Vsw control*, respectively.

$$v_r(t) = -at^2$$  \hspace{1cm} (4-2)

The procedures of the proposed algorithm for unloading step transient is listed as follows as an example and applicable for both low and high $ESR$ Buck converter designs:
1. Turn off the main switch $Q_1$ of the Buck converter when an unloading transient happens at $t_0$ and start to count the time simultaneously. Sample and register the initial voltage $V(0)$ after a short period of noise blanking time (about 100ns);

2. Acquire another two sequent voltage samples $v(T_f)$, $v(2T_f)$ from ADC at a fixed sampling interval $T_f$ (1$\mu$s in this case), upon that the shape parameter $a$ of the parabola curve can be calculated;

3. Build an internal discrete reference voltage signal $v_r(k)$ based on the shape parameter $a$ from the Step 2 and the timing information from Step 1;

4. When the sensed voltage sample $v_o(k)$ (in pink) equals (or smaller than) the reference voltage $v_r(k)$ (in green), $t_1$ will be determined. Capture the output voltage at $t_1$ (the ideal peak capacitor voltage referred to as $V_{max}$), in Figure 4.5;

5. Calculate the time period $T_2$ based on $T_1$ or estimate the switching point voltage $V_{SW'}$ (considering the ESR effects) to detect time $t_2$;

6. Turn on the main switch $Q_1$, when $T_2$ ends or the output voltage decreases below the calculated SPV $V_{SW'}$ at $t_2$;

The conventional PID controller will take back over the regulation task, when the output voltage approaches to the desired value $V_{ref}$ at $t_3$. 

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Figure 4.6  Digitalized signals of voltage reference and output voltage of the proposed scheme under unloading step transient

Figure 4.7  Program flowchart for determining time $t_1$ using proposed algorithm
The program flowchart of the proposed algorithm for determining time point $t_1$ and the computation information are shown in Figure 4.6 using a DSP (TMS320F28027, TI[62]). After the transient happens at $t_0$, the transient detector (same to the one used in Chapter 3) will trigger the optimal controller to operate for regulation and the ADC will start sampling three output voltage points. By using the proposed algorithm, the parameter $a$ can be solved in only 6 system clock cycles (<100ns) and the discrete reference $V(k)$ (<67ns/per point) will be built. The microprocessor will monitor the instantaneous output voltage $ADC(k)$ and compare it with the reference $V(k)$, until $V(k)>ADC(k)$ for unloading transient or $V(k)<ADC(k)$ for loading transient.

4.2.3 Operations of for Active Voltage Positioning

Adaptive voltage positioning (a.k.a. Load-line regulation) has increasingly become a requirement in many Buck converter applications, for example, Intel’s CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter along while decreasing power consumption of the load device.

Due to the $ESR$-independent way of determining the time point $t_1$, this proposed method offers a better interface to AVP schemes [38]. Under the charge balance principles, the VRs for powering modern processors like Intel’s CPUs will be able to use only ceramic capacitors to improve the output ripple and reduce the motherboard area. In this case, only simple modification is required for implementing AVP based on this algorithm (see Figure 4.7). In Step 4, we need to estimate the load step $\Delta I_o$ at $t_1$, and use new formulas (4.33) and (4.34) for computing $V_{SW}$. And, finally, the PID controller takes over the regulation task when the output voltage returns to the adaptive voltage position $V_{ref}R_{droop}\Delta I_o$ instead of $V_{ref}$ (where $R_{droop}$ is the droop resistance). Another significant benefit of the proposed algorithm for AVP applications is that the load step
\[ \Delta I_o \text{ (in Step 4)} \text{ can be estimated based on the parameter } a \text{ and the output capacitance. The details will be discussed in the next section.} \]

\[ i_{o1}, i_{o2}, i_L, V_{max}, V_{SW} \]

\[ V_{ref}, V_o, V_{(k)}, t_0, t_1, t_2, t_3 \]

\[ m_1, m_2 \]

\[ m_1 = \frac{V_{in} - V_o}{L_o} \]

\[ m_2 = \frac{V_o}{L_o} \]

\[ \frac{\Delta I_o \cdot R_{droop}}{L_o} \]

**Figure 4.8** Inductor current and capacitor voltage waveforms for AVP applications under unloading step transient case \((R_{droop}; \text{ droop resistance})\)

**4.3 Mathematical Derivations of the Parabolic Curve Fitting Based CBC**

**4.3.1 Fundamental of Output Voltage Curve Analysis under Unloading Transient**

In Figure 4.4, during the load transients, the waveforms of ideal capacitor voltage and output voltage are illustrated and an imaginary coordinate (in blue) is set up as a reference for the time-based analysis. For unloading step transient, during the time period \(t_0-t_2\) and \(t_2-t_3\) the capacitor current (ac component of \(i_L\)) can be approximated as a linear function in (4.3) and (4.4), where \(m_1\) (\(m_1 = V_{in} - V_o / L_o\)) and \(m_2\) (\(m_2 = V_o / L_o\)) are the rising and falling slew rates of the inductor current.

\[ i_C(t) \bigg|_{t_0-t_2} = -m_2 \left( t - t_1 \right) = -\frac{V_o}{L_o} \left( t - t_1 \right) \]  
\[ (4-3) \]
As an alternative approach for solving differential equations, the ideal capacitor voltage can be approximated with a parabolic curve in (4.5) based on the linear output capacitor current in (4.3) and (4.4).

\[
i_C(t)_{\Delta t} = m_3(t-t_3) = \frac{V_o - V_o}{L_o} (t-t_3)
\]  

(4-4)

The output voltage curve can be expressed as (4.6), where we can discover that even though with a significant ESR, the converter output voltage is remaining a parabolic waveform and the quadratic coefficient \(-\frac{V_o}{2L_oC_o}\) is the same as (4.5) which is independent on ESR value.

\[
v_o(t) = -\frac{V_o}{2L_oC_o} (t^2 - 2T_1t) + \frac{V_o}{L_o} (T_1 - t) \cdot ESR
\]  

(4-5)

In the simplified equation (4.7), it reveals that the actual output voltage \(v_o\) is shifted ahead of a period of time \(\Delta t\) with respect to the waveform of the ideal capacitor voltage \(v_c\) in (4.5).

\[
v_o(t) = -\frac{V_o}{2L_oC_o} \left[ t - (T_1 - \Delta t) \right]^2 + \frac{V_o}{2L_oC_o} \left( T_1^2 + \Delta t^2 \right)
\]  

(4-6)

And the lead time \(\Delta t\) is determined by the product of capacitor value \(C_o\) and its ESR value in (4.8).

\[
\Delta t = T_1 - T_o = C_o \cdot ESR
\]  

(4-7)

Even when we consider ESL of the output capacitors in (4.9), it will only affect the constant term of the output voltage polynomial in (4.7) but not the quadratic coefficient.

\[
v_o(t) = v_o(t) = -\frac{V_o}{2L_oC_o} \left[ t - (T_1 - \Delta t) \right]^2 + \frac{V_o}{2L_oC_o} \left( T_1^2 + \Delta t^2 \right) - \frac{V_o}{L_o} \cdot ESL
\]  

(4-8)
Because the impact of the ESL (-$V_o/L_o*ESL$ is not more than mV order) is very minor, ESL is neglected in the following analysis. When the capacitor current undergoes a zero crossover, the capacitor voltage $v_C$, reaches its maximum value $V_{max}$; in the meanwhile, the output voltage $v_o$ has the same value as $V_{max}$, which provides an opportunity to attain the information of $t_1$ in (4.10) (see Figure 4.4). Furthermore, another observation can be made that the actual output voltage waveform of the dc-de buck converters with identical resonant/corner frequency of the LC filter, $V_{in}$, $V_o$ and load transient $\Delta L_o$, is a family of parabolas which passes the point ($T_1$, $V_{max}$).

$$v_o(T_1) = v_c(T_1) = v_r(T_1) = V_{max} = \frac{V_o}{2L_oC_o}T_1^2$$ (4-10)

### 4.3.2 Mathematical Equations for Output Voltage Analysis under Loading Transient Case

For a loading step transient, shown in Figure 4.8, the waveforms of ideal capacitor voltage and output voltage are illustrated. During the time period $t_0-t_2$ and $t_2-t_3$ the capacitor current (ac component of $i_L$) is expressed as a linear function in (4.11) and (4.12), where $m_1$ ($m_1 = V_{in}-V_o/L_o$) and $m_2$ ($m_2 = V_o/L_o$) are the rising and falling slew rates of the inductor current.

$$i_C(t)|_{t_0-t_2} = m_1(t-t_1) = \frac{V_{in}-V_o}{L_o}(t-t_1)$$ (4-11)

$$i_C(t)|_{t_2-t_3} = -m_2(t-t_3) = -\frac{V_o}{L_o}(t-t_3)$$ (4-12)

Similarly, the ideal capacitor voltage can be approximated with a parabolic function in (4.13) based on the linear output capacitor current in (4.11) and (4.12).

$$v_C(t) = \frac{V_{in}-V_o}{2L_oC_o}(t^2-2T_1t) = \frac{V_{in}-V_o}{2L_oC_o}(t-T_1)^2 - \frac{V_{in}-V_o}{2L_oC_o}T_1^2$$ (4-13)
Figure 4.9 Digitalized signals of voltage reference and output voltage of the proposed scheme under loading step transient

Considering the $ESR$ impact, the output voltage curve can be expressed as (4.14), it is noted that the converter output voltage is remaining a parabolic waveform with constant quadratic coefficient $\frac{V_{in}-V_o}{2L_oC_o}$, which is independent on $ESR$ value.

\begin{equation}
 v_c(t) = \frac{V_{in}-V_o}{2L_oC_o} \left( t^2 - 2T_1 \right) - \frac{V_{in}-V_o}{L_o} \left( T_1 - t \right) \cdot ESR
\end{equation}

(4-14)

After simplifying the equation in (4.14), it is worth mentioning that the actual output voltage is also shifted ahead of a period of time $\Delta t$ with respect to the waveform of the ideal capacitor voltage in (4.15).
\[
v_o(t) = \frac{V_{in} - V_o}{2L_o C_o} \left[ t - (T_i - \Delta t) \right]^2 - \frac{V_{in} - V_o}{2L_o C_o} \left( T_i^2 + \Delta t^2 \right)
\]

(4-15)

And the lead time \(\Delta t\) is determined by the product of capacitor value \(C_o\) and its ESR value, which is the same as in (4.8).

\[
\Delta t = T_i - T_0 = C_o \cdot ESR
\]

(4-16)

For loading transient case, similar conclusions can be made: 1) the coefficient \(a\) of the quadratic item of the output waveform is unchanged even when the ESR and/or ESL are taken into account (4.17); 2) the actual output voltage waveform of the dc-dc buck converter with identical resonant/corner frequency of the LC filter, \(V_{in}, V_o\) and \(\Delta I_o\), is a family of parabolas which passes the point \((T_1, V_{min})\) in (4.18).

\[
v_o(t) = \frac{V_{in} - V_o}{2L_o C_o} \left[ t - (T_i - \Delta t) \right]^2 - \frac{V_{in} - V_o}{2L_o C_o} \left( T_i^2 + \Delta t^2 \right) + \frac{V_{in} - V_o}{L_o} \cdot ESL
\]

(4-17)

\[
v_o(T_i) = v_o(T_i) = v_o(T_i) = V_{min} = -\frac{V_{in} - V_o}{2L_o C_o} \cdot T_i^2
\]

(4-18)

4.3.3 \(t_1\) Detection

As previously discussed in Section 4.2.2, the internal reference \(v_r(t)\) is required to detect \(t_1\). And because the constant parameter \(a\) is independent on the ESR, the output voltage samples under transients can be applied to solve the parameter \(a\), so that using equation (4.2) the reference \(v_r(t)\) can be fitted. In general, three equations are needed for solving the three unknowns in the parabola function in (4.19), and the variations between the second and first, the third and first output voltage samples are represented as \(\Delta v(T_f)\) and \(\Delta v(2T_f)\).
And the simplified equations are shown in (4.20) and the shape parameter \( a \) can be immediately solved using (4.21). Notice that the equation (4.21) can be simply calculated by shift operations using DSP in only 6 system clock cycles.

\[
\begin{align*}
\Delta v(T_f) &= v(T_f) - v(0) = aT_f^2 + bT_f \\
\Delta v(2T_f) &= v(2T_f) - v(0) = 4aT_f^2 + 2bT_f
\end{align*}
\]  

(4-20)

\[
a = \frac{\Delta v(2T_f) - 2\Delta v(T_f)}{2T_f^2}
\]  

(4-21)

Based on this parameter, the internal discrete-time parabolic voltage reference \( v_r(k) \) can be built by the formula (4.22) at the sampling period \( T_f/K \), where \( K \) is the constant for resolution adjustment of the reference \( v_r(k) \). If a more powerful DSP is used, \( K \) can be larger than 2. And in this case \( K \) is better to be chosen as a multiple of 2 for simple operation by shift. By comparing \( v_r(k) \) with the recent voltage sample \( v_o(k) \), time \( t_1 \) can be detected.

\[
v_r(k) = -\frac{\Delta v(2T_f) - 2\Delta v(T_f)}{2T_f^2} \left( \frac{T_f}{K} \right)^2 = -\frac{\Delta v(2T_f) - 2\Delta v(T_f)}{2} \left( \frac{k}{K} \right)^2
\]  

(4-22)

Furthermore, it is noted that the same curve fitting method can be applied for both of the transient cases. Based on the equations in (4.9) and (4.17), the ratio \( R_a \) of the fitted parameter \( a \) between loading transient \( (a_p) \) and unloading transient \( (a_u) \) is calculated in (4.23), where \( D \) is the duty cycle. Therefore, in the practical implementation of the proposed curve fitting method, several techniques can be taken into account: 1) registering and averaging the calculated shape parameter \( a \) in (4.21) for several times to increase the accuracy and reliability; 2) after identifying
the system parameter \( a \), the external ADC can be operated in standby mode to reduce the power consumption; 3) after the first loading transient, voltage overshoot samples are employed to calculate \( a_n \), resulting in larger sampling period \( T_f \) and low cost of the external ADC; 4) based on the registered and averaged parameter \( a \), under loading transients, the ratio \( R_a \) is used to calculate \( a_p \).

\[
R_a = \frac{a_p}{a_n} = \frac{V_{in} - V_o}{V_o} = \frac{1 - D}{D}
\]  

(4-23)

### 4.3.4 \( t_2 \) Detection

To determine \( t_2 \), two methods can be employed and referred to as timing control method and SPV control method in the discussion below.

**Timing control method:**

Timing control can be applied, meaning that we exchange the ON/OFF state of the synchronous switches when the calculated time interval \( T_2 \) ends. Time interval \( T_2 \) can be calculated in the equations (4.24) for unloading step load transient cases and (4.25) for loading transient cases. And notice that the formula includes square root calculations in each case. As previously discussed in Chapter 3, the duty ratio variation of well regulated Buck converter is relatively small, so the duty ratio \( D \) can be treated as a constant or can be calculated during steady-state. By this means, the proportional relationship between time interval \( T_1 \) and \( T_2 \) can be established without relying on design parameters \((L_o \text{ and } C_o)\).

\[
T_2 = \sqrt{\frac{V_{in} - V_o}{V_{in}}} T_1 = \sqrt{1 - DT_1}
\]  

(4-24)

\[
T_2 = \sqrt{\frac{V_o}{V_{in}}} T_1 = \sqrt{DT_1}
\]  

(4-25)
In Figure 4.5, alternatively, during the time period $t_1-t_2$ and $t_2-t_3$, the ideal $V_{SW}$ (without $ESR$) can be calculated using (4.26) based on the ideal capacitor voltage $v_c$, where the symbol $T_{sw}$ represents the switching period and the $V_{ref}$ is for the output voltage reference, while the equation (4.27) provides the formula for computing the voltage peak $V_{max}$. Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a very high frequency and narrow duty ratio (12 V-1.5 V), the item $(1/2 DT_{sw})^2$ can be omitted in the equation (4.26).

\[
V_{SW} = \frac{1}{2C_0} m_1 \left[ T_{sw}^2 - \left( \frac{1}{2} DT_{sw} \right)^2 \right] + V_{ref}
\]  

(4-26)

\[
V_{max} = \frac{1}{2C_0} m_2 T_{sw}^2 + V_{SW}
\]

(4-27)

Therefore, the formula of voltage $V_{SW}$ can be derived as (4.28) and simplified in (4.29).

\[
V_{SW} = \frac{m_2 (V_{max} - V_{SW})}{m_1} + V_{ref} = \frac{V_o}{V_{in}} V_{max} + \frac{(V_{in} - V_o)}{V_{in}} V_{ref}
\]

(4-28)

\[
V_{SW} = DV_{max} + (1 - D)V_{ref}
\]

(4-29)

Similarly, the SPV for loading transient case is expressed in (4.30).

\[
V_{SW} = DV_{ref} + (1 - D)V_{min}
\]

(4-30)

Then, based on the relationship between $T_1$ and $T_2$ in (4.24) and (4.25) as well as the initially sampled voltage $V(0)$, the $ESR$ included SPV $V_{SW}'$ can be calculated as (4.31) and (4.32) for unloading and loading steps, respectively. Notice that all the square root calculations can be done offline or during steady-state.
\[ V_{SW}' = V_{SW} - V(0)\sqrt{1-D} = D V_{\text{max}} + (1-D)V_{\text{ref}} - V(0)\sqrt{1-D} \]  
\[ (4-31) \]

\[ V_{SW}' = V_{SW} + V(0)\sqrt{D} = D V_{\text{ref}} + (1-D)V_{\text{min}} + V(0)\sqrt{D} \]  
\[ (4-32) \]

In conclusion, according to the derivations discussed above, in the algorithm, neither inductor nor capacitor value is explicit in the final equations (4.29)-(4.32). Also, the computation in (4.29)-(4.32) is only based on the output voltage information \((V_{\text{max}}/V_{\text{min}})\) and reference voltage \((V_{\text{ref}})\) as well as steady-state duty ratio \(D\).

### 4.3.5 Mathematical Equations for Adaptive Voltage Positioning Extension

As previously discussed, the parabolic curve fitting CBC algorithm can be extended to AVP application with low ESR Buck converter design. Although both of the methods are very suitable for DSP implementation, SPV control method is more preferred for AVP application. On top of equation (4.29) and (4.30), similarly, we can compute \(V_{SW}\) by replacing the voltage reference \(V_{\text{ref}}\) with \((V_{\text{ref}}+R_{\text{droop}}\cdot\Delta I_o)\) for low ESR Buck converter in (4.33) and (4.34) for unloading and loading transients, respectively, shown in Figure 4.7.

\[ V_{SW} = D V_{\text{max}} + (1-D)(V_{\text{ref}} - R_{\text{droop}}\cdot\Delta I_o) \]  
\[ (4-33) \]

\[ V_{SW} = D(V_{\text{ref}} - R_{\text{droop}}\cdot\Delta I_o) + (1-D)V_{\text{min}} \]  
\[ (4-34) \]

Compared to the existing AVP techniques based on CBC, the proposed method has a significant benefit: using \(T_1\) and shape parameter \(a\), an estimation can be made for load current step \(\Delta I_o\) in (4.35) without requiring current sensing to realize the AVP technique. By this means (based on known \(C_o\) and \(T_1\)), we do not need accurate DCR sensing for inductor current or noisy capacitor current sensing for \(\Delta I_o\).

\[ \Delta I_o = -\frac{V_o}{L_o}T_1 = 2aC_oT_1 \]  
\[ (4-35) \]
Substituting the equation (4.35) into equations (4.29) and (4.30), the proposed algorithm for AVP extension is expressed in (4.36) and (4.37) for unloading and loading transients, respectively.

\[
V_{SW} = DV_{\text{max}} + (1 - D) \left( V_{\text{ref}} - R_{\text{droop}} \cdot 2aC_oT_i \right) \quad (4-36)
\]

\[
V_{SW} = D \left( V_{\text{ref}} - R_{\text{droop}} \cdot 2aC_oT_i \right) + (1 - D)V_{\text{min}} \quad (4-37)
\]

### 4.4 Validation of the Parabolic Curve Fitting Based CBC Algorithm

#### 4.4.1 Simulation Results

In order to verify the functionalities of the proposed optimal algorithm, a Buck converter model undergoing different transient conditions is simulated. And the simulated results are shown in the following figures. The simulation model parameters are listed as follows: \( V_{\text{in}}=12\text{V} \), \( V_o=V_{\text{ref}}=1.5\text{V} \), \( f_s=350\text{kHz} \), \( L_o=1\mu\text{H} \), \( R_L=1\text{m}\Omega \), \( C_o=180\mu\text{F} \), \( ESL=100\text{pH} \). And the ESR of the output capacitor is chosen to be 0.5\text{m}\Omega for low ESR design and 30\text{m}\Omega for significant ESR design simulations.

First, the curve fitting methodology is verified by the simulation shown in Figure 4.9. The time point \( t_1 \) when the capacitor current undergoes a zero crossover, the voltage reference (in blue) will be equal to the actual output voltage (in orange). Another observation is that our previous assumption that the capacitor current is piecewise linear is well established and verified in this simulation.
Figure 4.10  Simulation of Curve Fitting Method

Figure 4.10 and Figure 4.11 show the transient response performance of the aforementioned dc-dc buck converter model using parabolic curve fitting based CBC controller. In Figure 4.10 and Figure 4.11, the top section shows the DPWM signal for both of the cases. And the load current (iLoad), output voltage (vo) and inductor current waveforms (iL) are shown in the other two sections on the bottom. The subscripts _lowESR and _highESR represent and distinguish the two different cases. For loading transient, if the converter has low ESR value, the voltage undershoot is much smaller than that with large ESR, but the settling time is quite similar. In addition, under unloading transient, the voltage overshoot is higher for large ESR converter because of the voltage contributed by the ESR and the large load step change. However, the difference of the settling time between low and high ESR buck converter is minor.
Figure 4.11  Simulation results of the dc-dc Buck converter following loading step transient 0 A→10 A (a) low ESR case (undershoot 45 mV and settling time 4.5 μs); (b) large ESR case (undershoot 300 mV and settling time 4.1 μs) using proposed optimal controller;

Figure 4.12  Simulation results of the dc-dc Buck converter following unloading transient 10 A→0 A (a) low ESR case (overshoot 180 mV and settling time 13.5 μs); (b) large ESR case (undershoot 360 mV and settling time 13.5 μs) using proposed optimal controller;
As proposed in the previous sections, the robustness of the proposed scheme is maintained. So through the simulations under the following design conditions in Table 4-1, it demonstrates that even the output inductance and capacitance is doubled, the optimal load transient response performance can be still achieved.

Table 4-1 Design Parameters of the Robustness Testing and the Response performance

<table>
<thead>
<tr>
<th></th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_o$</td>
<td>1$\mu$H</td>
<td>1$\mu$H</td>
<td>2*1$\mu$H</td>
</tr>
<tr>
<td>$C_o$</td>
<td>2*180$\mu$F</td>
<td>180$\mu$F</td>
<td>180$\mu$F</td>
</tr>
<tr>
<td>$\Delta v_o$ (0A-10A)</td>
<td>-25mV</td>
<td>-35mV</td>
<td>-60mV</td>
</tr>
<tr>
<td>Setting time (0A-10A)</td>
<td>6$\mu$s</td>
<td>5$\mu$s</td>
<td>9$\mu$s</td>
</tr>
<tr>
<td>$\Delta v_o$ (10A-0A)</td>
<td>77mV</td>
<td>155mV</td>
<td>310mV</td>
</tr>
<tr>
<td>Setting time (10A-0A)</td>
<td>14$\mu$s</td>
<td>13$\mu$s</td>
<td>27$\mu$s</td>
</tr>
</tbody>
</table>

Figure 4.13 Simulation results for robustness testing under inductance and capacitance variations under 0A-10A loading transient
In the simulations, the digital PID controller is designed by well matching the nominal output inductance and capacitance value in Case 2. Due to the unchanged PID controller, some slight ringing back appears during the transitions between CBC and PID controllers in Case 1 and 3. But this ringing back can be minimized by optimally designing the PID controller such as in Case 2.

### 4.4.2 Design Prototype and Experimental Results

A prototype is designed using the parameters in the simulation. Because the proposed scheme is very suitable for DSP implementation using its system interrupts and peripherals, such as timer, ePWM (150ps resolution), ADC (12-bit) and digital comparator, a fixed-point 32-bit DSP TMS320F28027 [62] is employed to implement the proposed enhanced digital CBC algorithm. To further increase the resolution of the curve fitting method, an OPAMP based signal conditioning circuitry is used to amplify the voltage deviations by 4 times (shown in Chapter 3).
Experimental results, shown in Figure 4.14 and Figure 4.15, demonstrate the transient performance of conventional linear voltage mode controller (bandwidth: ≈65kHz, Phase margin ≈60°) under the load current step change between no load (0A) and full load (10A). Limited by the compensation bandwidth, the linear voltage mode controller will cause larger voltage variations and recovery time than CBC controller. For loading transient, the voltage undershoot is about -170mV with 61μs settling time, while, the overshoot is about 185 mV with 56μs settling time.

Figure 4.15 Experimental results of Buck converter under loading transient case 0 A-10 A using linear mode controller
Experimental results of the proposed optimal controller are shown in Figure 4.16-Figure 4.19, under the load step change between no load (0A) and full load (10A). And in order to demonstrate the applicability of the proposed scheme for any reasonable ESR value, paralleled ceramic capacitors ($ESR \approx 0.5\, \text{mΩ}$, see Figure 4.16 and Figure 4.17) and aluminum electrolytic capacitors ($ESR \approx 30\, \text{mΩ}$, see Figure 4.18 and Figure 4.19) are employed for output capacitance around $180\, \mu\text{F}$. In the experiments, the aforementioned timing control method is used, because of the unified form for low or large ESR cases. The proposed controller demonstrates quite similar improved performance as its analog CBC counterpart [33] and even maintains a good settling performance for significant ESR case.
Figure 4.17 Experimental results of loading transient case 0 A- 10 A using optimal controller for low ESR buck converter

Figure 4.18 Experimental results of unloading transient case 10 A- 0 A using optimal controller for low ESR buck converter
For low ESR cases, compared with the well-designed voltage mode PID controller (see Figure 4.14 and Figure 4.15), under a 10 A loading step transient, the settling time is improved by 94% and the voltage undershoot is reduced by 79%. For a 10 A unloading step transient, although the voltage overshoot is not improved because of the narrow operating duty ratio, the settling time is still shortened by 82% using proposed enhanced CBC controller.

Figure 4.19 Experimental results of loading transient case 0 A- 10 A using optimal controller for large ESR buck converter
150

Figure 4.20 Experimental results of unloading transient case 10 A- 0 A using optimal controller for large ESR buck converter

In order to verify the applicability of the proposed scheme for any reasonable ESR value, paralleled electrolytic capacitors ($C_o=180\mu F$, $ESR=30m\Omega$) are employed as the output capacitor. The experimental results are shown in Figure 4.18 and Figure 4.19, as discussed in the previous sections, although the voltage deviation is larger than that of the low ESR case, the settling time is quite similar. For loading step transient case, the voltage undershoot is 205mV with $4.2\mu s$ settling time. And for unloading step transient, the voltage overshoot is about 440mV and the settling time is $13.5\mu s$.

The adaptive voltage positioning technique is applied to the proposed controller with load step estimation. And in the experimental results are shown in Figure 4.20 and Figure 4.21. The $ESR$ is $0.5m\Omega$ and the droop resistance is selected to be $5m\Omega$. 

150
Figure 4.21 Experimental result of 10A loading step transients under AVP operation using proposed enhanced digital CBC controller

Figure 4.22 Experimental result of 10A unloading transients under AVP operation using proposed enhanced digital CBC controller
It is demonstrated that, for a 10A loading step transient, the undershoot is -10mV at -50mV AVP regulation in Figure 4.20. And the settling time is 6µs. The experimental result in Figure 4.21 demonstrates that the overshoot is 115mV above the AVP regulation level of 50mV (165mV in total) with 13µs settling time under a 10A unloading step transient.

4.5 Conclusions

In this chapter, a parabolic curve fitting method is employed to design the CBC controller. The proposed algorithm can be implemented for generally designed Buck converter to optimize the transient performance. Further, the proposed controller demonstrates quite similar improved performance as its previous counterpart and even maintains a good performance for significant ESR case. Also a promising possibility is shown for current sensorless AVP technique using this scheme for powering modern microprocessors with load current step estimation. It is demonstrated through simulations and experimental results that the optimal transient performance has been achieved for low and significant ESR designed Buck converter. Compared with linear voltage mode controller, both voltage variation and settling time have been improved. The current sensorless AVP technique has been verified under load transients.
Chapter 5

A Novel Analog Implementation of Voltage Sensing Based Charge Balance Controller

5.1 Introduction

Couples of analog controllers and digital control algorithms have been introduced in some previous literatures [31]-[41] to achieve better response performance than conventional schemes such as voltage and current mode controllers. But there are several drawbacks in digital control to hinder its use in VR applications, so most of the existing laptop/notebook computer VR controllers are analog ICs. The digital controller may suffer from one or more limitations below:

1. High power consumption of DSP or FPGA type of digital controllers is the main bottleneck against their wide use for VRs, especially, during standby mode operation of VR. Although the ASIC type of controller is an existing digital controller candidate for VR, the power consumption is still much higher than its analog counterparts. Therefore, the existing digital controllers are only used in higher power VRs for server computers.

2. The propagation delay, calculation delay, sampling delay and aliasing effect in the digital compensation loop make the (linear mode) digital controller slower than analog controller. For VR applications, the digital (linear mode) controller is not that attractive from aforementioned points of view.

3. Digital controller has several applicability issues, such as the limit-cycle oscillation [65] caused by analog-digital converter (ADC) and DPWM resolution mismatching as well as the high ADC power consumption and relatively complex structure of the DPWM generator.
4 Hardware multipliers are required for implementing the control law and specific software and/or interface are needed for programming the arithmetic core, resulting in high cost of the digital controller implementation.

For the analog controllers based on sliding mode control (SMC) [57][58] or capacitor charge balance control (CBC) principles [32], either complex calculation blocks or design parameters matching/tuning [33][41] is required to realize the proposed implementations. On the other hand, latest existing digital schemes [34]-[41], though removing most of the algorithm barriers, such as, the requirement of accurate current sensing for estimation, the need of real time complex calculations (square root/division) and the dependence on the design parameters ($L_{in}$, $C_o$ and $ESR$) [59], as previously discussed, they are still not the best solutions for efficient industrial IC design and fabrication.

To address the aforementioned drawbacks, an analog CBC controller is presented in this chapter. It combines the advantages of optimal control, enhanced robustness, design simplicity, easy fabrication of analog IC and low power consumption. In lieu of ADC and capacitor current sensor, an analog extreme voltage detector is used to detect the capacitor current zero crossing moment. And an analog circuitry based on OPAMP and comparator (OP-COM) circuitry is proposed to carry out the digital function for achieving charge balance [60]. When a low voltage Buck converter for VR is well-designed with low $ESR$ by using ceramic output capacitors, the proposed implementation is parameter-independent, robust and applicable for AVP applications [59].

This chapter is organized as follows. In Section 5.2, the basic idea of the proposed analog implementation of voltage sensing based CBC controller for load transients are introduced. In Section 5.3, the critical mathematical expressions of the proposed scheme are derived. Following the hardware implementation diagrams in Section 5.4, finally, the simulation and experimental
results are demonstrated in Section 5.5 to validate the proposed analog CBC controller. Section 5.6 is conclusion of the chapter.

5.2 Operating Principles of the Proposed Analog Implementation of Voltage Sensing Based CBC

Charge balance principle is a practical solution for achieving minimal settling time [32][33]. For all the CBC based controllers [32]-[41], the time instants \( t_1 \) (capacitor current undergoing zero-crossing) and \( t_2 \) (PWM changing ON/OFF state) are very important to arrange the desired ON/OFF control actions (in Figure 5.1), accordingly. In this chapter, a practical extreme voltage detector is presented to find \( t_1 \). And in place of calculating interval \( T_2 \) [32]-[34], the time information \( t_2 \) is mapped to the switching point voltage (SPV) \( V_{SPV} \), which provides a parameter-independent formula set under load transient cases. Also an extension can be made for AVP application based on this SPV information. And an OP-COM circuitry is used in place of digital functions to achieve the time detection of \( t_2 \). The operations of the proposed controller to minimize the output deviations are discussed in this section.

5.2.1 Minimization of the Output Overshoot under Unloading Transients

Following the load current step transient, the proposed analog CBC controller will firstly sample and hold (S/H) the maximum/minimum output voltage at \( t_1 \) and convert this information into SPV \( V_{SPV} \) to detect \( t_2 \). The main procedures of the control scheme under unloading step transient (in CCM mode with synchronous rectifier, SR) are listed (see Figure 5.1):
Figure 5.1 Typical waveforms of voltage regulator using the proposed CBC controller under unloading step transient

1. Assuming that a load current transient happens at the time point $t_0$, triggering the proposed CBC controller, immediately. And the voltage mode Type III controller will be disconnected from the feedback loop with held controller output, while the proposed CBC controller will set the PWM output to low (OFF);

2. After a short period of delay for blanking the load transition noise such that the output voltage switching ringing will not degrade the performance of the extreme voltage detector, the extreme voltage detector will be activated for detecting $t_1$ (Figure 3.3)

3. When the desired output signal edge (rising edge, shown in Figure 3.3) of the voltage detector happens at $t_1$, the output voltage peak $V_{max}$ will be sensed and held;

4. According to the voltage peak $V_{max}$, the SPV $V_{SW}$ can be calculated using simple OPAMP mathematical functions;
5. The PWM will be reset to high (ON) when the output voltage reduces to $V_{SW}$ at $t_2$;

6. At $t_3$, the output voltage recovers to the desired voltage $V_{ref}$, and the conventional Type III controller is reactivated for output voltage regulation again.

### 5.2.2 Minimization of the Output Undershoot under Loading Transients

The charge balance principles are also applicable for minimizing the output undershoot undergoing a loading step transients. Similarly,

1. It is assumed that a load current transient happens at the time point $t_0$, triggering the optimal controller, immediately. And the voltage mode Type III controller will be disconnected from the feedback loop with held controller output, while the proposed CBC controller will set the PWM output to high (ON);

2. After a short period of delay for blanking the Buck converter load transition noise, the extreme voltage detector will be active for detecting $t_1$;

3. When the certificated output signal edge (falling edge) of the voltage detector happens at $t_1$, the output voltage peak $V_{min}$ will be sensed and held;

4. According to the voltage peak $V_{min}$, the SPV $V_{SW}$ can be calculated using simple OPAMP mathematical functions;

5. The PWM will be reset to low (OFF) when the output voltage reduces to $V_{SW}$ at $t_2$;

6. At $t_3$, the output voltage recovers to the desired voltage $V_{ref}$, and the conventional Type III controller is reactivated for output voltage regulation again.
5.3 Mathematical Analysis of Charge Balance Operation

5.3.1 Charge Balance Principles for a Buck Converter Undergoing an Unloading Step Change

The proposed analog CBC controller is designed based on the digital algorithm presented in Chapter 3. Therefore, the equation (3.1)-(3.35) is applicable for this analog implementation. To save the space, the derivations of the mathematical equations are neglected in this chapter.

Using equation (3-19), it is clear that OPAMP and comparator can be used to determine the time instant $t_2$. The OPAMP serves as an amplifier with constant gain for $V_{\text{max}}$ and $V_{\text{ref}}$ and an adder to sum up the information at the non-inverting port. As shown in Figure 5.1, the voltage $v_{SW}$ is lower than the output voltage during steady-state and before $t_2$ during unloading step transient. So the comparator with hysteresis configuration will capture the crossover point of $v_o$ and $v_{SW}$ at $t_2$ and avoid comparison ringing.
The guidelines of circuit design and parameter calculation will be presented in the Section 5.4.2.

### 5.3.2 Adaptive Voltage Positioning/Load Line Regulation Extension

Load-line regulation (a.k.a. adaptive voltage positioning) has increasingly become a requirement in many Buck converter applications, for example, Intel’s CPU VRs. Load-line regulation essentially involves outputting lower voltages during higher load current conditions. This assists in improving the overall transient performance of the converter along while decreasing power consumption of the load device.

Due to several factors (e.g. complexity, mode transitioning), it is difficult to achieve load-line regulation through analog charge balance control [33]. However, the proposed analog CBC controller can be applied to AVP operation with only simple modifications, such as adding inductor current sensor and one more connection to the inverting input port of OPAMP.

It is observed in Figure 3.9, for AVP application, the difference of operation is in the interval $t_1-t_3$. At time instant $t_3$, instead of recovering the output voltage to $V_{ref}$, the AVP controller maintains the new steady-state output voltage depending on the load line. From the equations derived in (3.34) and (3.35) in Chapter 3, we can simply these equations in (5.1) and (5.2). It is
noted that a negative term is added to the equations and requires the load current line information $\Delta I_o$ and a constant gain of $R_{\text{droop}}(1-D)$ or $R_{\text{droop}}D$ depending on the loading conditions.

$$V_{SW} = DV_{\text{max}} + (1-D)V_{\text{ref}} - (1-D)R_{\text{droop}} \cdot \Delta I_o$$  \hspace{1cm} (5-1)$$

$$V_{SW} = DV_{\text{ref}} + (1-D)V_{\text{min}} - DR_{\text{droop}} \cdot \Delta I_o$$  \hspace{1cm} (5-2)$$

And the hardware modification for AVP operation is also minor, shown in Figure 5.4, the inductor current sensor is required to feed the load line information to the inverting port of the OPAMP to implement the equations (3.34) and (3.35). And the detailed implementation is discussed in Section 5.4.2.

![Figure 5.4 Analog Implementation modification for calculating $V_{SW}$ and $t_2$ determination in AVP applications.](image)

5.4 Implementation of the Proposed Analog Capacitor Charge Balance Controller

The implementation and design of the proposed analog charge balance controller will be discussed in this section. The three main components of the proposed analog charge balance controller are: a) an extreme voltage detector to determine $t_1$ (when the inductor current reaches the new load current level); b) an analog circuitry consisting of OPAMP and comparator to determine the switching instant $t_2$; and c) associated logic to control the components a) and b) and
the converter’s PWM signal. Figure 5.5 shows the high-level block diagram of the analog charge balance control method. In addition, a Type III compensator is designed for steady-state or near steady-state regulation purposes as well as the smooth transition between linear mode and CBC controllers.

![Simplified schematic of the proposed analog CBC controller implementation for computing $V_{sw}$ and detecting $t_2$](image)

In Figure 5.5, the inductor current measurement information is merely used to implement AVP or load-line regulation, as discussed in Section 5.3.

**5.4.1 Extreme Voltage Detector Design (For $t_1$ Detection)**

As discussed in Chapter 3, the adjustable delay $t_{delay}$ can be tuned by selecting different value of $C_T$ and $R_T$. The proper delay should be selected to compromise two factors: 1) good time detection accuracy; and 2) sufficient voltage error for generating the comparator (rising and falling edge) output. Using the equation (3.22), the values of $C_T$ and $R_T$ can be calculated.

The experimental results shown in Figure 5.6 demonstrate the aforementioned delay based extreme voltage detector to detect time $t_1$. The pink waveform is the input sinusoidal signal at
100kHz with $1.5V_{pp}$ and the blue waveform is the output signal of extreme voltage detector. The delay time $t_{\text{delay}}$ is set to be 330ns by selecting $C_T$ as 330pF and $R_T$ as 500Ω.

![Figure 5.6 Experimental result (with $C_T=330\text{pF}$, $R_T=500\Omega$, $t_{\text{delay}}=330\text{ns}$)](image)

**5.4.2 Analog Circuitry Design for $t_2$ Detection**

The design of the analog circuitry for $t_2$ detection is presented in this section and the hardware schematic is shown in Figure 5.4 for AVP application. And for non-AVP operation, the inverting port of the OPAMP will be tied to GND in Figure 5.3.

For AVP operation, the inductor current can be rebuilt by active filtering the voltage across the output inductor. For accurate measurement, the corner frequency of the active low-pass filter should be designed based on (5.3).

$$R_{2L} \cdot C_{1L} = \frac{L_o}{R_L} \quad (5-3)$$

The relationship between output of the inductor current sensor $i_{L\text{sen}}$, and the actual inductor current $i_L$ is equated in (5.4).
In this analog implementation, the critical time point \( t_2 \) can be determined by comparing instant output voltage \( (v_o) \) with switching point voltage \( (V_{SW}) \). And the analog extreme voltage detector is used to decide time \( t_1 \), and the controller logic will feed the proper logic signal to S/H1 for collecting \( V_{max} \), shown in Figure 5.5. For computing the load step value \( \Delta i_L \), two S/Hs (S/H2 and S/H3) are used and the S/H timing is controlled by the controller logic according to \( t_0 \) (from transient detector) and \( t_1 \) (from extreme voltage detector output) in Figure 3.4 Then \( \Delta i_o \) is obtained by subtracting \( i_L(t_1) \) from \( i_L(t_0) \). To implement the equations (3.34) and (3.35), an analog OPAMP adder/subtractor is employed following the formula in (5.5). And the design parameters can be selected using (5.6)-(5.8), referring to (3.34) and (5.5).

\[
i_{Lsen} = R_L \frac{R_{2L}}{R_{4L}} i_L \quad (5-4)
\]

\[
V_{SW} = \left(1 + \frac{R_1}{R_4}\right) \left(\frac{R_2}{R_5 + R_2} V_{max} + \frac{R_2}{R_3 + R_2} V_{ref}\right) - \frac{R_1}{R_4} \Delta i_L \quad (5-5)
\]

\[
D = \left(1 + \frac{R_1}{R_4}\right) \frac{R_2}{R_5 + R_2} \quad (5-6)
\]

\[
1 - D = \left(1 + \frac{R_1}{R_4}\right) \frac{R_2}{R_5 + R_2} \quad (5-7)
\]

\[
(1 - D) \cdot R_{droop} = \frac{R_1}{R_4} \quad (5-8)
\]

Similarly, for loading transients \( V_{SW} \) can be implemented in (5.9), where the design parameters can be selected using (5.10)-(5.12).

\[
V_{SW} = \left(1 + \frac{R_1}{R_4}\right) \left(\frac{R_2}{R_5 + R_2} V_{min} + \frac{R_2}{R_3 + R_2} V_{ref}\right) - \frac{R_1}{R_4} \Delta i_L \quad (5-9)
\]
\[ 1 - D = \left(1 + \frac{R_1}{R_4}\right) \frac{R_2}{R_3 + R_2} \]  
(5-10)

\[ D = \left(1 + \frac{R_1}{R_4}\right) \frac{R_2}{R_3 + R_2} \]  
(5-11)

\[ D \cdot R_{\text{droop}} = \frac{R_1}{R_4} \]  
(5-12)

### 5.4.3 Associated Charge Balance Controller Logic

The controller logic block is responsible for: a) registering a load current transient, b) switching control from the linear controller to the charge balance controller during the transient interval and providing PWM control signals, c) providing control signals to the extreme voltage detector, linear mode controller, and S/Hs during the transient interval, d) registering time instants (at \(t_1\) and \(t_2\)), and e) reactivating the linear controller at the end of the transient interval (at \(t_3\)).

The controller logic using only logic gates is shown in Figure 5.7, which is very convenient to implement using CPLD or FPGA at the cost of only 20 logic elements.

![Simplified schematic of the proposed analog CBC controller logic circuit](image)

Figure 5.7  Simplified schematic of the proposed analog CBC controller logic circuit
5.4.4 Type III compensator design

Following the general Type III Compensator design guideline [66], two zeros are placed at $\frac{1}{2}$ of the output filter double pole frequency and right at the double pole frequency, respectively, resulting in boosted phase margin. And two poles are set at half of the switching frequency and the ESR zero frequency to achieve desired bandwidth at 75kHz and high frequency noise attenuation ability.

Above all, the Type III compensator control output command is required to be held during “linear-CBC-linear” controller transition period. To carry out a smooth transition, two analog switches (single-pole-single-throw, SPST) are placed at $v_o$ output voltage channel and $FB$ pin of the Type III controller shown in Figure 5.8. And these two analog switches are controlled by the inversed signal of Reset. Simulation is conducted in Figure 5.9 to show the smooth transition with the help of the hold function. $v\text{contrl}_w._\text{Hold}$ is the voltage mode controller command with the hold function, while $v\text{contrl}_w/o_\text{Hold}$ is the voltage mode controller command without the hold function. And the waveform of $Vo_CBC_w._\text{Hold}$ shows the output overshoot with hold function and the waveform of $Vo_CBC_w/o_\text{Hold}$ demonstrates the output overshoot without hold function. It is clear that the hold function added to the Type III controller significantly improves the settling time of the proposed analog CBC controller for a smoother transition between voltage mode control and CBC, though the overshoot is not changed. Without the hold function, $Vo_CBC_w/o_\text{Hold}$ (output voltage) appears ringing back issue.
5.5 Simulation and Experimental Verifications

5.5.1 Simulation Results

In order to verify the functionality of the proposed analog controller, a Buck converter undergoing different transient conditions is simulated. And the simulation results are shown in Figure 5.10 and Figure 5.11 for comparison between the proposed analog CBC controller and the conventional voltage mode controller. The nominal design parameters are listed as follows:
$V_{in}=12 \text{ V}, V_o=V_{ref}=1.5 \text{ V}, f_s=450 \text{ kHz}, L_o=1 \mu \text{H}, R_L=1 \text{ m}\Omega, C_o=200 \mu \text{F}, ESR=0.1 \text{ m}\Omega, ESL=100 \text{ p}\Omega$.

The Type III compensator is well-designed with 75 kHz bandwidth and 60° phase margin in the following simulations.

Under 12A loading step transient, compared to voltage mode controller, the voltage overshoot is reduced by 66.7% and the settling time is shortened by 93.3%. Although, under the 12A unloading step load transients, the voltage undershoot is only reduced by 19.0% due to the narrow operating duty ratio, the settling time is still significantly reduced by about 76.7%.

Figure 5.10 Simulation results under 0 A ->12A loading transient (upper section: $I_L_{TypeII}$: inductor current using type III controller; $I_L_{CBC}$: inductor current using proposed analog CBC controller; $I_o$: load current, bottom section: $V_o_{TypeIII}$: output voltage using type III controller; $V_o_{CBC}$: output voltage using CBC controller)
Figure 5.11 Simulation results under 12A ->0A unloading transient (upper section: IL_TypeII: inductor current using type III controller; IL_CBC: inductor current using proposed analog CBC controller; io: load current, bottom section: Vo_TypeIII: output voltage using type III controller; Vo_CBC: output voltage using CBC controller)

As proposed in the previous sections, the robustness of the proposed scheme is tested under the following design conditions in Table 5-1. So through the simulations, it demonstrates that even the output inductance or capacitance is doubled the nominal value, the near-optimal load transient response performance can be still achieved.

| Design Parameters of the Simulated Robustness Testing and Transient Performance |
|-------------------------------|-------------------------------|-------------------------------|
| Case 1                        | Case 2                        | Case 3                        |
| $L_o$                         | $2*1\mu H$                    | $1\mu H$                      |
| $C_o$                         | $200\mu F$                    | $200\mu F$                    |
| $\Delta V_o$ (0A-12A)         | $-95mV$                       | $-50mV$                       |
| $\Delta V_o$ (12A-0A)         | $400mV$                       | $190mV$                       |
| Setting time (0A-12A)         | $9\mu s$                      | $5\mu s$                      |
| Setting time (12A-0A)         | $27\mu s$                     | $13\mu s$                     |

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In the simulations, the Type III controller is designed by well matching the double pole frequency of the nominal output inductance and capacitance value in Case 2. Due to the unchanged design of the Type III controller, some slight ringing back appears during the transients between CBC and Type III controllers in Case 1 and 3. And this ringing back can be minimized by optimal design of the Type III controller.

Figure 5.12  Simulations of robustness testing under loading step transient 0A->12A
5.5.2 Prototype Design and Experimental Results

In Figure 5.14, a 12 V-1.5 V prototype is designed using the same nominal parameters in the simulation and a FPGA (EP2C70F896C6, Cyclone II, Altera) is employed to implement the proposed CBC controller logic (in Figure 5.7). The analog linear mode controller is implemented by using ISL6559 controller (Intersil) [66]. Experimental results are shown in Figure 5.15-Figure 5.18, under the load current step change between no load (0A) and full load (12A). The proposed analog CBC controller demonstrates quite similar enhanced performance as its digital counterpart [60] but facilitating the integration and fabrication of the industrial controller IC products with reduced operating power consumption.
Figure 5.14  Figure of the prototype for verifying the proposed analog controller

Figure 5.15 and Figure 5.16 show comparative results for a Buck converter undergoing a 0A->12A loading step transient using proposed analog CBC controller and conventional voltage mode controller. The voltage detector signal is shown for time detection of \( t_s \). In order to illustrate the operation of the proposed analog CBC controller, the charge balance control intervals have been shown in the figures.
Figure 5.15 Experimental results Buck converter under 0A -12A loading step transients using proposed analog CBC controller.

Figure 5.16 Experimental results of Buck converter under 0A -12A loading step transients using Type III compensator.

It is demonstrated, under a 12A loading step transient, the settling time is reduced from 56\(\mu\)s (using voltage mode controller) to 3.5\(\mu\)s (using proposed analog CBC). In other words, the
settling time of the Buck converter with proposed analog CBC is shortened by 93%, compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (4.2μs) and the simulation result (4μs).

Also, it is shown that voltage undershoot is reduced from -155mV (using the linear controller) to -40mV (using proposed analog CBC). The undershoot of the Buck converter with proposed analog CBC controller is reduced by 74% compared to that of the voltage mode controller Buck converter. And the -40mV undershoot is close to the calculated undershoot (-35mV) and the simulated result (-50mV).

Figure 5.17 and Figure 5.18 show a voltage mode controlled Buck converter and the proposed analog CBC controlled Buck converter undergoing a 12A->0A load step change, separately.

![Experimental results Buck converter under 12A-0A unloading transients using proposed analog CBC controller](image)
Figure 5.18 Experimental results Buck converter under 12A-0A unloading transients using Type III compensator

It is demonstrated, under a 12A load unloading step transient, the settling time is reduced from 56μs (using voltage mode controller) to 13.6μs (using proposed analog CBC). In other words, the settling time of the Buck converter with proposed analog CBC is shortened by 75%, compared to that of the voltage mode controlled Buck converter. And the experimental result is in close correspondence of the calculated settling time (16μs) and the simulation result (14μs).

Also, it is shown that voltage overshoot is only reduced from 190mV (using the linear controller) to 180mV (using proposed analog CBC) because of the narrow operating output ratio at 12V-1.5V. But the 180mV overshoot is accordance with the calculated undershoot (190mV) and the simulated (185mV).

The adaptive voltage positioning technique is applied to the proposed analog CBC controller with simple modification on top of the non-AVP proposed analog CBC scheme. And in the experimental results shown in Figure 5.19 and Figure 5.20, the droop resistance is selected to be 5mΩ.
Figure 5.19  Experimental result of 12A loading transients under AVP operation using proposed analog CBC controller

Figure 5.20  Experimental result of 12A unloading transients under AVP operation using proposed analog CBC controller
It is demonstrated that, for a 12A loading step transient, the undershoot is 0mV at -60mV AVP regulation. And the settling time is 4.6μs. The experimental result in Figure 5.20 demonstrates that the overshoot is 120mV above the AVP regulation level of 60mV (180mV in total).

As discussed in the previous sections, the proposed scheme is robust against the variations of output inductance and capacitance. Therefore, a robustness testing has been conducted and the results are shown in Figure 5.21 to Figure 5.24, the output inductance and capacitance are respectively doubled. However, the voltage mode controller design is unchanged, which is well-designed for matching the double-pole of the nominal output filter.

![Figure 5.21](image)

**Figure 5.21** Robustness test of the proposed controller for a Buck converter controller with Lo=2*1μH and Co=200μF under 12A loading step transient
Figure 5.22 Robustness test of the proposed controller for a Buck converter with $L_o=2\times1\mu H$ and $C_o=200\mu F$ under 12A unloading step transient

Figure 5.23 Robustness test of the proposed controller for a Buck converter with $L_o=1\mu H$ and $C_o=2\times200\mu F$ under 12A loading step transient
Figure 5.24 Robustness test of the proposed controller for a Buck converter with $L_0=1\mu H$ and $C_0=2*200\mu F$ under 12A unloading step transient

Table 3-3 provides the summarized performance of the robustness testing of the proposed analog CBC. Referring to the simulated robustness testing in Table 5-1, the experimental results are in close correspondence of the simulations.

Table 5-2 Circuit Parameters and Transient Performance of the Robustness Testing in the Experimental Results

<table>
<thead>
<tr>
<th></th>
<th>Figure 5.21</th>
<th>Nominal Case</th>
<th>Figure 5.23</th>
<th>Figure 5.24</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_0$</td>
<td>$2*1\mu H$</td>
<td>1\mu H</td>
<td>1\mu H</td>
<td></td>
</tr>
<tr>
<td>$C_0$</td>
<td>200\mu F</td>
<td>200\mu F</td>
<td>2*200\mu F</td>
<td></td>
</tr>
<tr>
<td>$\Delta v_o$ (0A-12A)</td>
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<td>-40mV</td>
<td>-25mV</td>
<td></td>
</tr>
<tr>
<td>Setting time (0A-12A)</td>
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<td>3.5\mu s</td>
<td>4.5\mu s</td>
<td></td>
</tr>
<tr>
<td>$\Delta v_o$ (12A-0A)</td>
<td>440mV</td>
<td>180mV</td>
<td>90mV</td>
<td></td>
</tr>
<tr>
<td>Setting time (12A-0A)</td>
<td>26\mu s</td>
<td>13.6\mu s</td>
<td>13.5\mu s</td>
<td></td>
</tr>
</tbody>
</table>
5.6 Conclusions

In this chapter, an analog CBC controller based on the digital voltage sensing based CBC algorithm (discussed in Chapter 3) [60] is presented. This proposed analog implementation facilitates analog controller IC fabrication to the next-generation VRs. It is demonstrated through simulations and experimental results, that the proposed analog CBC controller can be implemented for low-ESR designed Buck converter to optimize the transient response performance and enhance the robustness against the tolerance and variation of the passive components (output inductance $L_o$ and output capacitance $C_o$). The AVP practice can be implemented with two more S/H circuits. Compared with a well-designed analog voltage mode Type III controller, under a 12A loading step, the settling time and undershoot are improved by 93 % and 74 %, respectively. For a 12A unloading step, although the overshoot is not improved because of the narrow duty ratio, the settling time is still shortened by 75 % using the proposed controller.
Chapter 6

Practical Control Strategies to Improve Unloading Transient Response Performance for Voltage Regulators

6.1 Introduction

As the computing capabilities of high-performance digital devices continue to expand, the demand on the power supplies for powering such devices becomes increasingly stringent. Thus, extensive research has been conducted developing advanced controllers which improve the transient performance of Buck converters to their physical limits. In [32]-[41][57]-[60], controllers have been presented which apply second-order sliding surfaces, pre-calculated switching time intervals or capacitor charge balance methodologies to reduce the voltage deviation and settling time of a Buck converter, undergoing a load transient, to its virtually optimal level. But, in [47], it is demonstrated that for a commonly used 12V-1.5V VR even under optimal control, the undesired large output voltage overshoot still dominates the output capacitance requirement, because of the much worse and marginally improved unloading response performance. To address the asymmetrical response, a two-stage power conversion scheme is presented in [44], which creates a 5V intermediate dc bus voltage to balance the stage conversion ratio close to 50% but adds more power loss, cost and board space to the entire system. Many auxiliary circuitries are reviewed in Chapter 2 to reduce the output voltage overshoot, and the one shown in Figure 6.1 coupled with its control law [33] has the following advantages: 1) predictable behavior allowing for simplified design; 2) inherent over-current protection; and 3) low peak current to average current ratio allowing for use of smaller components. However, the auxiliary converter operates for very high frequency (>MHz) switching during activation under a relatively complex current mode control law, which downgrades the enhancement if applied to a
multiphase Buck converter. In [56], another overshoot reduction solution using the aforementioned auxiliary circuit with an external energy storage capacitor and synchronous rectifier (SR) implementation is provided; however, the practicality is limited due to the additional linear compensator, the subsequent high frequency switching of the auxiliary converter and the unimproved settling time.

In this chapter, a practical auxiliary current control strategy is presented to improve unloading transient performance, which has the following unique advantages: 1) the auxiliary circuit operating at relatively low frequency to reduce the switching loss; 2) further voltage overshoot reduction; 3) predictable auxiliary switching based on the main-auxiliary inductance ratio; and 4) minimizing the settling time of unloading response based on charge balance principles.

This chapter is organized as follows. In Section 6.2, the operating principles of the proposed scheme are presented. The analysis of voltage overshoot and power loss is made in Section 6.3, followed by hardware implementation in Section 6.4. The simulation and experimental results are shown in Section 6.5. Furthermore, a simplified linear control strategy is proposed in Section 6.6 to address the Multiple Consecutive Load Transient issue and meet the industrial CPU VR load transient test requirements. The verifications of the proposed simplified schemes are shown in Section 6.7 through simulations and experimental results. And the 10kHz-100kHz CPU load transient tests have been conducted for proving the practicality of the simplified linear control strategy. The conclusions are drawn in Section 6.8.

6.2 Operating Principles of the Proposed Control Scheme

When a Buck converter follows an unloading transient response, it is important to reduce the current conducting through the output capacitor. As stated in Chapter 3, the load current falls at a much higher slew rate than the inductor current, the capacitor must absorb charge (and thus increase voltage). The voltage overshoot may be reduced by modifying the output filter
parameters, that is, by decreasing the size of the output inductor (resulting in decreased efficiency due to larger peak and thus RMS MOSFET current levels and/or increased switching frequency) or by increasing the size of the output capacitor (resulting in a significantly higher cost of the Buck converter).

Alternatively, the amount of charge absorbed by the capacitor can be reduced by diverting excess current from the output inductor of the Buck converter to the converter’s input through operation of the proposed controlled auxiliary circuit. As will be shown, a large reduction in the output voltage overshoot can be realized by the addition of a small inductor, MOSFET, and diode. The auxiliary circuit can be modeled as a controlled current source, drawing current from the output capacitor of the Buck converter and transferring it to the input of the Buck converter. Figure 6.1 shows the model of such method when used with a synchronous Buck converter. The auxiliary current is only active during step-down load current transients (i.e., before and after an unloading transient, the circuit operates as a conventional Buck or synchronous Buck converter).

![Simplified model of the proposed CAC](image)

Figure 6.1  Simplified model of the proposed CAC

Figure 6.2 shows one possible implementation of the auxiliary circuit used in this chapter. An alternate implementation would involve using a second MOSFET (in lieu of Daux) for synchronous rectification. As is shown, the auxiliary circuit resembles a small boost converter connected in antiparallel with the Buck converter.
In [47][48], a controlled auxiliary current (CAC) is presented to improve the transient response of a Buck converter as shown in Figure 6.3. The duration of activation of the auxiliary current is regulated. That method has the following advantages:

1) predictable behavior allowing for simplified design; 2) inherent over-current protection; 3) low peak current to average current ratio allowing for use of smaller components.

That method also estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lower magnitude. The auxiliary is controlled by using constant off time peak current control scheme.
However, this controller is not suitable for multiphase buck converters due to the high switching frequency of the auxiliary circuit. For example, in order to maintain the average value of the auxiliary current for a two phase VR with 360nH per phase output inductance, the switching frequency of the auxiliary switch will be reaching above 5MHz, resulting in highly increased switching losses, gate drive losses and auxiliary MOSFET driver cost. Also, the controller design is relatively complex with constant $T_{\text{aux\_off}}$ delay time injection, load current estimation, and filtered current sensing. Above all, because of the low initial auxiliary current peak, the overshoot of this control scheme is not optimal/near-optimal, even though the current level is adjustable.

Although a similarly designed auxiliary circuit is employed for improving the unloading transient performance (see Figure 6.2), several unique merits of the proposed control strategy will be discussed in this chapter (through details in Section 6.3). The proposed BCM peak current mode (PCM) controlled auxiliary current (CAC) is shown in Figure 6.4. During steady state operation or step-up loading transient, the CAC is deactivated and the main Buck converter is regulated by an analog charge balance controller (discussed in Chapter 5, but other CBC controllers/schemes are also applicable) [72]. When the unloading transient happens, the CAC will be operated for rapidly removing the extra capacitor charge energy back to the input source through the Schottky diode $D_{\text{aux}}$. The operations of the CAC and the proposed control strategy are described as follows (see Figure 6.4):
1. It is assumed that the unloading transient happens at $t_0$, triggering the proposed control scheme to minimize the output voltage overshoot;

2. The main switch Q1 will immediately turn off to reduce the additional capacitor charge at $t_0$, while, the S/H circuit sets the peak current reference value $I_{aux\_pk-pk}$ by holding the output of the capacitor current sensing circuit (see Figure 6.13);

3. The auxiliary circuit will be controlled using peak current (at $I_{aux\_pk-pk}$) mode method in BCM (see Figure 6.4), which can be approximately modeled as a current source connected between output capacitor and input voltage source to minimize the output voltage overshoot (see Figure 6.1).
4. After a predictable $n$ (to be calculated later in this Chapter) cycles of auxiliary switching, the output voltage will recover to the reference voltage $V_{ref}$ at $t_1$ and the normal CBC controller will take over the regulation such that the settling time can be optimized.

From the settling time point of view, when we set the BCM peak current at $I_{aux\_pk-pk}$, equivalently, the average auxiliary current $I_{aux\_avg}$ will be half of the transient load current step value $\Delta I_o$, that is, $I_{aux\_avg} = 1/2 \Delta I_o$. Compared with a normal CBC controller in [33][59][72] (see Figure 6.4), during unloading transient, the auxiliary current can rapidly balance the capacitor charge at $t_1$. On the contrary, without the help of CAC, the output capacitor will be charged by the current of $(I_L-I_o2)$ until $t_1$. Therefore, the CBC controller requires the negative portion of inductor current to discharge the capacitor. As soon as the capacitor charge is balanced and the output voltage will recover to $V_{ref}$ at $t_3$ for normal CBC controller. In conclusion, the CAC coupled with CBC controller can significantly reduce the settling time.

Furthermore, in Figure 6.5, it reveals that in order to meet the overshoot requirement at 50mV under 10A step-down load transient, 630μF output capacitance is required for CBC controlled Buck converter without CAC, while, by using the proposed BCM PCM controlled CAC, the required output capacitance can be reduced by 73.0% to 170μF. As a result, all the output capacitance can be implemented with ceramic capacitors, resulting in reduced motherboard area and improved output voltage ripple.
Several unique advantages of the proposed control strategy will be discussed in this chapter (through details in Section 6.3). Firstly, the auxiliary current (CAC) will be operated in the boundary condition mode (BCM) at reduced frequency (the CAC falls to zero at the end of each switching cycle), such that the switching power loss can be decreased and a commonly used PWM driver can be used to drive the auxiliary switch. Also, because of the higher initial peak current of the auxiliary inductor, the output voltage overshoot will be lower compared to the previous scheme in [47]. Furthermore, according to the design ratio between main output inductance ($L_o$) and the auxiliary inductance ($L_{aux}$), the number of auxiliary switching cycles is predictable, which enhances the reliability of the proposed control scheme. For example, if the output inductance $L_o=1\mu H$ and the auxiliary induction $L_{aux}\approx100nH$, the number of auxiliary switching cycles will be $n=9$. And the proposed scheme can be simply scaled and extended to
multiphase VR with much lower equivalent output inductance, but on the other hand, in this
circumstance previous schemes may badly suffer from the impossibly high switching or low
auxiliary inductance for maintaining the average auxiliary current level.

6.3 Voltage Overshoot Estimation and Auxiliary Circuit Power Loss
Analysis

6.3.1 Overshoot Estimation with the Proposed Strategy of Controlled Auxiliary
Current

Without loss of generality, it is assumed that the auxiliary circuit is switched for \( n \) times
under BCM PCM control, where integer \( n \) is the number of auxiliary switching cycles. Upon that
the instantaneous output voltage variation can be expressed as (6-1) for two intervals depending
on the ON/OFF state of the auxiliary circuit and the \( N \)th time of switching, where \( T_{aux} \) is the
switching period of the auxiliary current and \( d_{aux} \) is the duty cycle of the auxiliary Boost
converter. More detailed derivations of the equations (6-1) to (6-5) are shown in the Appendix.

\[
\Delta V_o(t) = \begin{cases} 
\frac{1}{C_o} \left[ \frac{\Delta I_o}{2L_o} - \frac{N \cdot \Delta I_o \cdot T_{aux}}{2} - \int_0^{(t-N \cdot T_{aux})} \frac{V_o}{L_o} \cdot t \cdot dt \right] \\
\left( NT_{aux} \leq t < NT_{aux} + d_{aux} T_{aux} \right) (N = 0, 1, 2 \ldots, n) \\
\frac{1}{C_o} \left[ \frac{\Delta I_o}{2L_o} - \frac{N \cdot \Delta I_o \cdot T_{aux}}{2} - \frac{V_{in} - V_o}{2V_{in}} T_{aux} \cdot \Delta I_o \right] \\
- \int_{(t-N \cdot T_{aux} - d_{aux} T_{aux})}^{N \cdot T_{aux}} \frac{(V_{in} - V_o) (T_{aux} - t)}{L_{aux}} dt \\
\left( NT_{aux} + d_{aux} T_{aux} \leq t < (N + 1) T_{aux} \right) (N = 0, 1, 2 \ldots, n)
\end{cases}
\]

The output overshoot/maximum voltage will occur at the time \( t_{ost} \) in (6-2), when the
derivative of the equation (6-1) is zero during the \((N' + 1)\)th switching, where \( N' \) is calculated in the
equation (6-3) depending on the parity of \( n \).
Based on the average auxiliary current $L_{aux, avg}$ without considering the auxiliary inductor current ripple under the BCM peak current control, a simplified equation is provided as practical method to calculate the overshoot in the equation (6-4). The symbols $L_o$, $C_o$, $ESR$, $\Delta I_o$, $V_o$ and $L_{aux}$ represent the output inductance, output capacitance, equivalent series resistance, load step value, output voltage and the auxiliary inductance, respectively.

\[
\Delta V_o \approx \frac{ESR \cdot C_o^2 \cdot V_o^2 + \left(\frac{\Delta I_o}{2}\right)^2 \cdot L_o^2}{2V_o \cdot L_o \cdot C_o} + \frac{\left(\frac{\Delta I_o}{2}\right)^2 \cdot L_{aux}^2}{2V_o \cdot C_o}
\]

(6-4)

Another advantage of the proposed scheme is that under a certain value of step-down load transient, the number $n$ of auxiliary switching can be predicted using the input and output voltage information as well as the inductance ratio of $L_o$ and $L_{aux}$. The number of switching $n$ can be estimated using equation (6-5), where $[\cdot]_{\text{int}}$ indicates the rounding down operation. It is noted that $n$ is independent on the load transient step value $\Delta I_o$.

\[
n = \left[\frac{(V_{in} - V_o)L_o}{L_{aux} \cdot V_{in}} + 0.5\right]_{\text{int}}
\]

(6-5)

Figure 6.6 shows the relationship between the number of auxiliary switching cycles $n$ (as well as the ratio of $L_o/L_{aux}$) and the auxiliary inductance value under different output voltages $V_o$. So based on the power circuit design parameters ($V_{in}$, $V_o$, $L_o$, and $L_{aux}$), the necessary cycles of auxiliary switching for fast recovery the overshoot can be counted by a counter for $n$. By this
means, it becomes very straightforward for the CBC controller to deactivate the CAC (as soon as the count reaches $n$).

Figure 6.6 Number of auxiliary switching cycles $n$ (as well as the ratio of $L_o/L_{aux}$) and the auxiliary inductance value under different output voltages $V_o$

Figure 6.7 illustrates the impact of rounding down operation of $n$ on the settling time. In Figure 6.7(a) $\left\{\frac{(V_{in}-V_o)}{V_{in}\times L_o/L_{aux}}\right\} n < 0.5$, the CAC will be deactivated before the inductor current reaches the new load level $I_{o2}$. A second overshoot occurs and the settling time is longer than the ideal case shown in Figure 6.4. On the contrary, if $\left\{\frac{(V_{in}-V_o)}{V_{in}\times L_o/L_{aux}}\right\} n \geq 0.5$, as shown in Figure 6.7(b), the CAC activates longer than required, so that a voltage undershoot appears and increases the settling time, too. However, it is noted that the output overshoot equations in (6-1) are still valid because they are actually not dependent on the number of $n$. And the time instant $t_{out}$ can be expressed more generally in (6-6) (see the Appendix A for details).
\[
I_{set} = \frac{\Delta I_o + \frac{V_o}{L_{aux}} \cdot NT_{aux}}{\frac{V_o}{L_o} + \frac{V_o}{L_{aux}}} = \frac{\Delta I_o \cdot L_{aux} L_o + V_o \cdot NT_{aux} \cdot L_o}{V_o \left( L_{aux} + L_o \right)}
\] (6-6)

Figure 6.7 The effect of rounding down operation of \( n \) on the settling time, (a) \( \frac{(V_{in}-V_o)}{V_{in}^* L_o / L_{aux}} \cdot n < 0.5 \); (b) \( \frac{(V_{in}-V_o)}{V_{in}^* L_o / L_{aux}} \cdot n \geq 0.5 \)

Figure 6.6 gives the overshoot voltage for various numbers of auxiliary switching cycles using the proposed BCM PCM controlled auxiliary current. By choosing proper auxiliary inductance \( L_{aux} \), the number of auxiliary switching \( n \) can be controlled according to the equation (6-5).
Figure 6.8 Estimated voltage overshoot for various times of CAC switching and different output capacitance for an unloading transient of 10A (\(V_{in}=12V\), \(V_o=1.5V\), \(L_o=1uH\))

For example, as shown in Figure 6.9, \(n=1\) means that in order to meet the overshoot requirement, the auxiliary circuit will be activated for one switching cycle during the unloading transient which can be achieved by selecting \(L_{aux}=875nH\) and output capacitance \(C_o=300\mu F\), as shown in Figure 6.9(a). And for \(n=5\), the auxiliary circuit will be activated for 5 switching cycles with selecting \(L_{aux}=175nH\) and \(C_o=185\mu F\) as shown in Figure 6.9 (b).
It is also noted from Figure 6.8 that the lower the auxiliary inductance $L_{aux}$ is, the more the number $n$ of auxiliary switching cycles and the better the unloading transient performance will be. However, from the simulation result shown in Figure 6.6, the improvement is marginal when the auxiliary inductance $L_{aux}$ becomes too small (i.e. $L_{aux}<100\text{nH}$, $n>9$) but on the contrary, low $L_{aux}$ will increase the auxiliary switching frequency $f_{aux}$ and harm the overall efficiency due to the more cycles of auxiliary switching.

In Figure 6.10, it shows that the switching frequency of the auxiliary FET $f_{aux}$ increases linearly with the number of switching $n$. When the switching frequency $f_{aux}$ is much higher than 1MHz, the cost of the auxiliary MOSFET driver will increase dramatically, resulting in extra/high cost of the CAC implementation. Therefore, design compromise should be made for output voltage overshoot and switching frequency/switching loss the auxiliary circuit.
6.3.2 Auxiliary Circuit Power Loss Analysis

There are three main sources of conduction loss pertaining to the proposed circuit [47]: the auxiliary inductor $L_{aux}$, the auxiliary FET $Q_{aux}$ and the auxiliary diode $D_{aux}$.

By calculating the RMS auxiliary current in (6-7), the inductor conduction loss can be calculated but in the loss analysis due to the very low DCR and sensing resistance $R_{L_{aux}}$ of the auxiliary inductor $L_{aux}$ (about 0.2mΩ in total). The auxiliary inductor conduction loss is in 10mW order and ignored.

$$I_{aux}(rms) = I_{aux \_avg} \sqrt{1 + \frac{1}{3}\left(\frac{I_{aux \_pk-pk}}{2I_{aux \_avg}}\right)^2} \quad (6-7)$$

The RMS current of the auxiliary FET and the average current of the auxiliary diode can be calculated using (6-8) and (6-9).
The conduction loss for the auxiliary FET and auxiliary diode can be calculated using (6.4) and (6-10).

\[ P_{\text{con, aux}} = I_{Q_{\text{aux}}}^2 \cdot R_{Q_{\text{aux}}} \]  

(6-10)

\[ P_{\text{con, Daux}} = I_{D_{\text{aux}}} \cdot V_{\text{diode}} \]  

(6-11)

Since a Schottky diode is utilized, it is assumed that the switching loss of the diode is negligibly small compared to the FET switching loss and the total conduction loss. Generally, the switching loss for the auxiliary FET can be calculated using (6-12), where, \( T_{\text{rise}} \) is the rise time of the auxiliary FET and \( I_{\text{on}} \) is the instantaneous auxiliary current when \( Q_{\text{aux}} \) is turned on, respectively. \( T_{\text{fall}} \) equals the typical fall time of the auxiliary FET. \( I_{\text{off}} \) equals the instantaneous auxiliary current when \( Q_{\text{aux}} \) is turned off, which is equal to the peak auxiliary current.

\[ P_{\text{sw, aux}} = \frac{1}{2} f_{\text{aux}} \cdot V_{\text{in}} \cdot \left( T_{\text{rise}} \cdot I_{\text{on}} + T_{\text{fall}} \cdot I_{\text{off}} \right) \]  

(6-12)

Because of the zero turn-on current under BCM operation of the CAC, the switching loss of the auxiliary FET can be simplified in (6-13).

\[ P_{\text{sw, aux}} = \frac{1}{2} f_{\text{aux}} \cdot V_{\text{in}} \cdot T_{\text{fall}} \cdot I_{\text{off}} \]  

(6-13)

In Figure 6.11, according to the previous equations, the power loss analysis is shown for comparison between the proposed control strategy (BCM) and the existing control scheme (CCM). The conduction loss of auxiliary MOSFET and the Schottky diode, MOSFET switching
loss and total losses are represented as $P_{\text{con\_Qaux}}$, $P_{\text{con\_Daux}}$, $P_{\text{sw\_Qsw}}$ and $\text{Total\_PCM}$ for the proposed control strategy, while, $P_{\text{con\_Qaux\'}}$, $P_{\text{con\_Daux\'}}$, $P_{\text{sw\_Qsw\'}}$ and $\text{Total\_CCM}$ for the existing control scheme [47]. It is noted that the conduction loss of the auxiliary diode is unchanged using the proposed scheme because of the same average current. The conduction loss of the auxiliary MOSFET using proposed BCM PCM controller is higher than that of the auxiliary MOSFET controlled by existing scheme [47] due to the larger inductor current ripple, thus, the RMS current value. However, compared to the existing scheme, the switching loss of the auxiliary MOSFET and the total losses are reduced using the BCM PCM controlled CAC. It is also worth noting that the auxiliary FET switching loss is independent on the load current level.

![Figure 6.11](image_url)

**Figure 6.11** Comparison results of loss breakdown based on different control schemes (the power circuit design parameters: $V_o=1.5V$, $f_s=450kHz$, $L_o=1\mu H$, $R_c=1m\Omega$, $L_{aux}=100nH$, $RL_{aux}=0.2m\Omega$, $RQ_{aux}=30m\Omega$, $V_{diode}=0.32V$, $T_{fall}=2ns$)

Although the total loss of the CAC is around 4.5W under 20A load current, the activation interval is only under unloading transient condition for couples of micro-seconds. As a result, the thermal issue will not be a big problem for this implementation.
The switching losses are simulated under different values of step unloading transients (from 10A to 20A) as shown in Figure 6.12. Compared to \( n=13 \) case, when the number of auxiliary switching cycles \( n \) equals 9, the overshoot is only higher by 1mV (see Figure 6.6) but the switching frequency \( f_{aux} \) and loss \( P_{sw\_Qaux} \) are lower by 1/3. So finally, the auxiliary inductance \( L_{aux} \) is chosen to be 100nH to achieve a good design, considering the trade-off between overshoot improvement and power losses.

![Figure 6.12 The plot of switching loss of the auxiliary FET versus the number \( n \) of auxiliary switching cycles under various load step unloading transients (the power circuit design parameters: \( V_o=V_{ref}=1.5V, f_s=450kHz, \) \( T_{fall}=2ns \))](image)

**Figure 6.12** The plot of switching loss of the auxiliary FET versus the number \( n \) of auxiliary switching cycles under various load step unloading transients (the power circuit design parameters: \( V_o=V_{ref}=1.5V, f_s=450kHz, \) \( T_{fall}=2ns \))

### 6.4 Implementation of the Proposed Strategy Controlled Auxiliary Current

The diagram of the proposed BCM PCM strategy to control the CAC is shown in Figure 6.13. To set the peak current level of the auxiliary current, the load step value is required to be
sensed/calculated. The ac component of the capacitor current during load transient is an alternative representation of the load step $\Delta I_o$. So the capacitor current can be rebuilt by active filtering the output voltage (considering $ESR$ in (6-14)) with an extra pole provided by $C_f$ to attenuate the switching noise.

$$C_{ic} \cdot R_{ic} = \left( \frac{C_o}{k} \right) \cdot (ESR \cdot k) = C_o \cdot ESR$$

(6-14)

The output of the capacitor current sensor $i_{Csen}$, in relation to the actual capacitor current $i_c$ is equated in (6-15).

$$i_{Csen} = \frac{R_{ic}}{k} i_c$$

(6-15)

Also, an improved capacitor current sensing circuit [47] can be applied in this implementation.
The \textit{nCounter} (for counting the cycles of switching) generates the \textit{TransDetect} signal to hold the $I_{aux\_pk-pk}$ value. A differential OPAMP amplifies the voltage across the current sensing resistor $R_{aux}$ to equalize the auxiliary current $i_{aux}$, which is compared with $I_{aux\_pk-pk}$ and GND. And an SR flip-flop is used to create the PWM signal to the auxiliary driver for switching $Q_{aux}$ and implement the BCM operation. When the \textit{nCounter} reaches $n$ (that is, the desired number of auxiliary switching cycles), the \textit{nEnable} (\textit{OUT}) signal of \textit{nCounter} will 1) deactivate the auxiliary current; 2) reset the \textit{EN} signal; and 3) generate the CBC PWM signal for Buck converter.
6.5 Simulation and Experimental Verifications

In order to verify the functionalities of the proposed control strategy, a Buck converter with/without CAC undergoing unloading transient condition is simulated. And the simulation results are shown in Figure 6.14 and Figure 6.15 for comparison between the normal CBC controller in Chapter 5 [72] and the proposed control scheme with BCM PCM CAC during 10A unloading transient. The design parameters are listed as follows: $V_{in}=12V$, $V_o=V_{ref}=1.5V$, $f_s=450kHz$, $L_o=1\mu H$, $R_i=1m\Omega$, $C_o=200\mu F$, $ESR=0.1m\Omega$, $ESL=100pH$, $L_{aux}=100nH$, $R_{aux}=0.2m\Omega$, $R_{Qaux}=30m\Omega$, $V_{diode}=0.32V$, $T_{fall}=2ns$ and $n=9$ (using equation (6-5), $V_{in}-V_o/V_{in}^\ast L_o/L_{aux}=8.75$). And the Type III compensator in the CBC controller is well-designed with 75 kHz bandwidth and 60° phase margin in Section 5.5 of Chapter 5 [72].

In Figure 6.14, the previously discussed CBC control technology is employed for optimal response of the single phase Buck converter. The overshoot is 175mV with 13.6μs settling time under a 10A step-down load transient case.

![Simulation results of CBC controller under 10A ->0A unloading transient without CAC for a single phase Buck converter](image)

Figure 6.14
Applying the proposed BCM PCM controlled CAC, the output voltage overshoot is reduced to 45mV and the settling time is reduced to 6.6μs, compared to the CBC controlled Buck converter without CAC. In other words, the overshoot and the settling time are improved by 74.2% and 51.5%, separately.

![Simulation results of CBC controller under 10 A ->0 A unloading transient with proposed CAC for a single phase Buck converter](image)

A single phase 12V-1.5V prototype is built with CAC using the same parameters in the simulation. Experimental results are shown in Figure 6.16 and Figure 6.17, under the unloading transient between full load (10A) and no load. Using the proposed BCM PCM CAC, the overshoot is decreased by 75.0% and the settling time is shortened by 53.6%, compared with the optimal response provided by an analog CBC controller without CAC (discussed in Chapter 5) [72]. And the number of switching is predictable using (11) and in the experiment the rounded off number $n$ is 9.
Figure 6.16 Experimental results of analog CBC controller under 10A ->0A unloading transient without CAC

Figure 6.17 Experimental results of the proposed BCM PCM controller under 10A ->0A unloading transient with CAC
6.6 A Linear Mode Control Scheme with Independent Loop Design to Address the Multiple Consecutive Load Transients (MCLT)

6.6.1 Introduction and Background

In the real design of 12V-1V two-phase voltage regulator, the larger voltage deviation during unloading transients dominates the output capacitance selection. And the previous scheme achieves significant reduced output voltage overshoot and optimal settling time based on capacitor charge balance control (CBC). However, in multiphase VR application, the settling time with CBC controller is much shorter than required in the industrial standards, especially for step-up load transients.

Above all, the unpredictable CPU load transient frequency can be as high as hundred kHz or even MHz, in this case, one or more load transients would occur before the CBC is accomplished. In this thesis, we call this scenario as Multiple Consecutive Load Transients, and MCLT for short. For all the existing implementations of CBC controller, the control time instants \( t_1 \sim t_5 \) in Chapter 3~5) are detected/calculated following one particular load transient to optimize the converter dynamic performance. A second detection/calculation of time instants can only be enabled, after the previous charge balance is achieved. It means the CBC controller is “blind” to new load transient(s) during CBC intervals. Therefore, the CBC controller will also not be able to well regulate the Buck converter with CAC under MCLT condition.

6.6.2 Basic Idea of the Simplified Control Scheme

In this section, a simplified control strategy with independent loops is presented. Using this strategy, industrial standards for laptop computer VR applications can be met under minimum modifications to conventional VR design but with significantly reduced output capacitance (from \((4*470+528)\mu F\) down to \(528\mu F\) only). This also means that the electrolytic or OSCAN capacitors \((4*470\mu F)\) can be totally removed, resulting in significantly reduced board area and
implementation cost. Instead of charge balance control, this scheme activates/deactivates the CAC only according to the output voltage level. When the output voltage is above the threshold (VID+0.02), the auxiliary circuit is activated to reduce the output voltage overshoot. Otherwise, the auxiliary circuit will be shut down. And to avoid complex small signal analysis for multi-loop system and simplify the controller design in [56], the proposed control scheme employs Type III voltage mode controller to regulate the two-phase VR and the CAC is controlled by an independent controller. The control scheme for the CAC is flexible and we can use BCM CAC (proposed in this thesis) or the existing peak current mode constant off time techniques as shown in Figure 6.3.

The controlled auxiliary current (two phase in parallel and controlled by the same auxiliary PWM driver) in Figure 6.18 is only activated during unloading transients, while the main switches will be controlled by a conventional voltage mode controller all the time for stabilizing the entire system. The compensated current level of the auxiliary current will be fixed to about 20A considering the most frequent unloading step value at 30A in laptop computer applications and the power rating of the selected low profile auxiliary MOSFETs (maximum pulsed current at 15A per phase). After the output voltage recovers to the desired value, the conventional Type III controller will take over the regulation. Instead of CBC control, following loading CPU load transients, Type III controller is used for voltage regulation to achieve the required voltage variations (≤-50mV) and settling time (≤10μs) with all ceramic output capacitors (528μF), upon which design complexity and controller cost can be highly reduced and the entire system will be more reliable and suitable for two-phase VR application. Above all, using this method, the Multiple Consecutive Load Transients (MCLT) issue which exists in CBC controller can be solved.
Figure 6.18 A two-phase VR with multiphase auxiliary converter to improve the unloading transient performance

6.6.3 Hardware Implementation of the Simplified Strategy

The topology configuration is illustrated in Figure 6.18, the two-phase voltage regulator is designed with synchronous switches, which are driven by separate synchronous drivers (Syn. Driver1 and Syn. Driver2). And a paralleled auxiliary Boost converter with two branches is controlled to recover the unloading transient energy to the input voltage source rapidly.

The voltage mode PWM controller can be implemented using conventional two-phase dc-dc Buck converter controller such as ISL6559 [66] as shown in Figure 6.19. The Trans signal in Figure 6.19 is very important for the proposed scheme. Generally speaking, load transient noise is much serious than the switching noise which can be easily filtered out by first or second order low pass filter. In order to prevent the load transient noise from false trigging the controller, the controller output COMP, which is filtered inherently by the Type III compensator, is served as the trigger to enable the auxiliary controller and CAC. When the voltage recovers to VID+0.02V
(the switching noise is filtered by RC low pass filter (LPF)), the Trans signal will be changed to disable state (high in this case). The phase current is sensed by ISL6559 through a sensing resistor connected to the switching node. VDIFF is the output of an internal remote differential amplifier, which is equivalent to the output voltage value. FB is the inverting input of the error amplifier for voltage mode compensation, while, COMP is the output of the error amplifier.

Figure 6.19 The control diagram of proposed simplified strategy to improve unloading transient performance
Load sharing is achieved in ISL6559 by adjusting the duty ratio inversely with the load current condition (with respect to the average current information $I_{avg}$) as shown in Figure 6.20. For example, if the sensed phase current $I_1 > I_2$, the PWM duty cycle of phase 1 will be reduced to balance the $I_1$ with average current.

![Control diagram of load sharing scheme in ISL6559](image)

Figure 6.20 Control diagram of load sharing scheme in ISL6559

A BCM peak current mode controller is used for maintaining the auxiliary peak current level at about 20A, which is determined by the 30A frequent CPU load transient step and the current rating of low-profile SOT-23 package of auxiliary MOSFETs. The auxiliary current level (20A) $I_{aux\_pk-pk}$ can be expressed in (6-16) based on the input voltage $V_{in}$, output voltage $V_o$, and auxiliary inductance $L_{aux}$.

$$I_{aux\_pk-pk} = \frac{V_o T_{on}}{L_{aux}}$$  \hspace{1cm} (6-16)

Another simple implementation of the BCM PCM scheme is to turn on and off the auxiliary MOSFET for pre-calculated constant time intervals $T_{on}$ and $T_{off}$, respectively in (6-17) and (6-18).

$$T_{on} = \frac{i_{aux\_pk-pk} L_{aux}}{V_o}$$  \hspace{1cm} (6-17)
The design parameters are shown in Table 6-1 for the proposed scheme. The OSCAN capacitors are removed (4*470μF). The main inductance is 300nH per phase and total output capacitance is 528μF with 0.5mΩ ESR. The auxiliary inductance \( L_{aux1}=L_{aux2}=75nH \) for an efficient and compact design. The selected auxiliary FETs are low profile SOT-23 package power MOSFETs (FDN359BN) [73] from Fairchild and the auxiliary diodes are Schottky type of diodes (SSC53L) [74] from Vishay to avoid the reverse recovery issue. The synchronous rectifier (SR) is implemented using PowerPak MOSFETs from Vishey. The PWM driver for the main MOSFETs is an SR driver (bootstrap capacitor is required) ISL6612/6613 [75] from Intersil with short through protection and advanced dead time control to optimize the efficiency. The auxiliary MOSFET is driven by a high performance PIN driver EL7156 from Intersil [76].

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( V_o )</th>
<th>( I_o )</th>
<th>( I_{aux _pk-pk} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V</td>
<td>1.2V</td>
<td>18A (light load)−48A (full load)</td>
<td>20A</td>
</tr>
<tr>
<td>( L_{o1}/L_{o2} )</td>
<td>( L_{aux1}/L_{aux2} )</td>
<td>Q11/Q21</td>
<td>Q12/Q22</td>
</tr>
<tr>
<td>SER2010-301MLB</td>
<td>SLC7649S-700KLC</td>
<td>Si7386DP</td>
<td>SiR166DP</td>
</tr>
<tr>
<td>( Q_{aux1}/Q_{aux2} )</td>
<td>( D_{aux1}/D_{aux2} )</td>
<td>Syn. Driver 1/2</td>
<td>Aux. Driver</td>
</tr>
<tr>
<td>FDN359BN</td>
<td>SSC53L</td>
<td>ISL6613</td>
<td>EL7156</td>
</tr>
<tr>
<td>( C_{in}, C_o )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ceramic Capacitor/6.3V X5R 0805

\( C_{in}=22\mu F*5=110\mu F, C_o=22\mu F*24=528\mu F \)
6.7 Simulation and Experimental Verifications

6.7.1 Simulation Results

Simulations are conducted to verify the functionalities of the proposed control strategy in Section 6.6. The design parameters are listed in the following table. In the laptop applications, the desired voltage overshoot should be less than 100mV and the voltage undershoot must be lower than 50mV, both with 10μs settling time requirement. In order to test the load sharing performance, the inductance $L_{o1}$ and $L_{o2}$ are chosen with different value intentionally. The output capacitance is selected based on the value of ceramic capacitors used (22μF*24) in the two-phase laptop VR design provided by ON Semiconductor. The VID table of ISL6559 can be found in the reference [66].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{o1}$</td>
<td>Output Inductance Phase 1: 300nH/1.1mΩ</td>
</tr>
<tr>
<td>$L_{o2}$</td>
<td>Output Inductance Phase 2: 360nH/1.2mΩ</td>
</tr>
<tr>
<td>$C_o$</td>
<td>Output Capacitance:  22μF*24=528μF</td>
</tr>
<tr>
<td>$ESR$</td>
<td>Equivalent Series Resistance: 0.1mΩ</td>
</tr>
<tr>
<td>$L_{aux1}$</td>
<td>Auxiliary Inductance Phase 1: 75nH</td>
</tr>
<tr>
<td>$L_{aux2}$</td>
<td>Auxiliary Inductance Phase 2: 75nH</td>
</tr>
<tr>
<td>$VID$</td>
<td>Voltage Identification Digital: 1.2V</td>
</tr>
<tr>
<td>$F_{sw}$</td>
<td>Switching Frequency per Phase: 500kHz</td>
</tr>
<tr>
<td>$I_{aux_pk-pk}$</td>
<td>Auxiliary Peak Current Level: 20A</td>
</tr>
</tbody>
</table>

In Figure 6.21, the proposed linear mode simplified PCM control scheme is activated under unloading transient for 5μs (eight times of switching). The Trans signal and the PWM signal are also simulated and shown to illustrate the control scheme. Using the proposed scheme, the output voltage overshoot is reduced to 60mV with 10μs settling time under a 30A step-down load transient case. The slew rate of the load step change is set to be 450A/μs.

---

4 The phase output inductors $L_{o1}$ and $L_{o2}$ are chosen to be different intentionally to test the load sharing performance.

5 The phase output inductors $L_{o1}$ and $L_{o2}$ are chosen to be different intentionally to test the load sharing performance.
For design simplicity and MCLT test, a conventional Type III voltage mode controller (BW=75kHz, PM=60deg) is used for step-up load transient regulation but not CBC controller. Under 30A step-up load transient, the undershoot is -43mV with 10μs settling time, which meets the regulation requirements well, as shown in Figure 6.22.

![Simulation result of a 12V-1.2V two-phase VR using the conventional voltage mode controller under 30A (450A/μs) step-down load transient with PCM ($I_{aux_{\text{pk-pk}}}$=20A) controlled CAC](image_url)

**Figure 6.21** Simulation result of a 12V-1.2V two-phase VR using the conventional voltage mode controller under 30A (450A/μs) step-down load transient with PCM ($I_{aux_{\text{pk-pk}}}$=20A) controlled CAC
Figure 6.22 Simulation result of a 12V-1.2V two-phase VR using the conventional voltage mode controller under 30A (450A/μs) step-up load transient without activating CAC.

In Figure 6.23, comparison results are shown with conventional controller (BW=75 kHz, PM=60 deg), the overshoot is 125mV with 100μs settling time, which does not meet the requirements, meaning more output capacitance must be used to suppress the voltage variations.
Figure 6.23  Simulation result of a 12V-1.2V two-phase VR using the conventional voltage mode controller under 30A (450A/\mu s) step-down load transient without activating CAC

In Figure 6.24 and Figure 6.25, the investigation of the proposed controller under MCLT is conducted. And in both of the cases, the proposed controller can maintain the stability of the output voltage and the overshoot is less than 100mV. For each of the transients, the settling time is within the 10\mu s requirements. In Figure 6.24, under a 30A-0A-15A MCLT, the overshoot is 60mV with 10\mu s settling time but the activation time of CAC is reduced due to the second 0A-15A step-up transient. For a 30A-15A-0A MCLT in Figure 6.25, the first overshoot is 25mV and the activation time is 3\mu s for the CAC. The second overshoot at 30mV does not trigger the CAC, so the Type III controller regulates the output voltage, resulting in stable system.
Figure 6.24  Simulation result of a 12V-1.2V two-phase VR using the proposed controller under multiple consecutive transients (30A-0A-15A)

Figure 6.25  Simulation result of a 12V-1.2V two-phase VR using the proposed controller under multiple consecutive transients (30A-15A-0A)
6.7.2 Prototype Design and Experimental Results

A two-phase VR prototype is designed for verifying the proposed scheme. From the Figure 6.26 and Figure 6.27, the extra board size for the CAC topology (14.0mm*13.0mm, including the sensing resistor area) is smaller compared to that of the reduced OSCAN capacitors (≥18.5mm*12.5mm). To implement the fast transient load bank, low inductance resistor is chosen and shielded by copper tape as heat sink. The output voltage is set by a 6-position switch (1.5V or 1.2V in the implementation via VID setting).

![Figure 6.26 The front-side picture of the two-phase VR prototype with the proposed scheme to reduce the unloading transient overshoot](image)

A two-phase VR controller ISL6559 with 5-Bit VID Input (0.800V to 1.550V in 25mV steps) is used for the output regulation and load sharing purposes.
A Cyclone II FPGA evaluation board (DE2-70), shown in Figure 6.28, is employed for 1) detecting the unloading transients; 2) sending the enable signal to the CAC circuitry for activation; 3) controlling the auxiliary boost converter to recover the extra charge from the output capacitor to the input source side; 4) enabling the fast transient resistive load bank; and 5) display functions for PGOOD, OVP, OCP and loading conditions.
In Figure 6.29 to Figure 6.32, the experiments of transient response of the voltage mode controller are shown. The $180^\circ$ phase shift is achieved between the two phases by ISL6559. In Figure 6.29 and Figure 6.30, under a single 40A loading transient, the voltage undershoot is -50mV and the settling time is 10μs. So the voltage mode controller can achieve required regulation even under 40A step-up CPU load transient.
Figure 6.29  A 1.2V-1.2V two-phase VR under a single 40A step-up load transient

Figure 6.30  Zoomed figure for a 1.2V-1.2V two-phase VR under a single 40A step-up load transient without activating CAC
In Figure 6.31 and Figure 6.32, under a single 40A unloading transient, the output voltage overshoot is 180mV and the settling time is 50μs, which does not meet the aforementioned regulation requirements.

Figure 6.31  A 1.2V-1.2V two-phase VR under single 40A step-down load transient without activating CAC
Figure 6.32 Zoomed figure for a 1.2V-1.2V two-phase VR under single 40A step-down load transient without activating CAC

In Figure 6.33, the CAC is activated during unloading transient, and the CAC enable signal is shown. When the output voltage overshoot occurs, the COMP signal will be saturated to 0, triggering the CAC. Once the voltage recovers to the VID+0.02V, the CAC will be disabled and Type III controller will operate for regulation. The output overshoot is reduced to 100mV and the settling time is shortened to 8μs. Therefore, the regulation requirement can be met well.
Figure 6.33 Zoomed figure for a 1.2V-1.2V two-phase VR under single 40A step-down load transient with CAC

Zoomed figures in Figure 6.34 and Figure 6.35 are shown to demonstrate a 10kHz 30A (18A ↔ 48A) CPU load transient test. Details of enable signal for CAC, PWM signal for CAC, output voltage and load transient signal are shown. The transient test requirement band is figured for illustration. It reveals that the voltage overshoot is within 100mV and the settling time is less than 10μs, while, the undershoot is less than -50mV with 10μs settling time.
Figure 6.34 Zoomed figure for a 1.2V-1.2V two-phase VR under 10kHz 30A load transient (18A–48A) with CAC

Figure 6.35 Zoomed-out figure for a 1.2V-1.2V two-phase VR under 10kHz 30A load transient (18A–48A) with CAC
The transient load frequency increases to 50kHz in Figure 6.36. Both the output voltage overshoot and undershoot are within the transient test band (-50mV/100mV). And the 10μs settling time requirements are met in the test under the load transient 18A↔48A.

In Figure 6.37, the load transient frequency is 100kHz so that the MCLT occurs. As previously discussed, the proposed linear mode control strategy is applicable for addressing the MCLT issue. It demonstrates that the voltage regulation requirement is also met well using the proposed controller and CAC under 18A↔48A load transients. As expected, the CAC is only activated during unloading transients to reduce the output voltage overshoot.
6.8 Conclusions

In this chapter, a practical auxiliary current control strategy is presented to improve unloading transient performance, which has the following unique advantages: 1) the auxiliary circuit operating at relatively low frequency to reduce the switching loss; 2) further voltage overshoot reduction; 3) predictable auxiliary switching based on the main-auxiliary inductance ratio; and 4) minimizing the settling time of unloading response based on charge balance principles. The power loss analysis and output voltage overshoot estimation are made in this chapter as a design guideline. To meet the maximum overshoot requirement, the output capacitance can be decreased from 630μF to 170μF. Through simulation and experimental results, it demonstrates that the proposed control strategy reduces the overshoot by 75% and shortens the settling time by 53.6%, under 10A unloading transient.
To further extend the practicality, a simplified linear mode control scheme with independent control loops for CAC is presented. This method can be applied to two-phase VR applications and used to address the Multiple Consecutive Load Transients (MCLTs) issue of the CBC controllers. Simulations and experiments are demonstrated to verify this scheme. Fast transient load tests (10kHz-100kHz) have been conducted. Under 18A↔48A load transients, the regulation requirement (-50mV/100mV) and 10μs settling time can be met well.
Chapter 7
Conclusions and Future Work

7.1 Conclusions

This thesis proposed several novel control technologies and a topology modification to improve the transient response of Buck converters undergoing a rapid load transition. Solutions have been implemented in the digital and analog domain, each offering original and unique features/advantages. By utilizing both the proposed control method and the proposed topology modification, significant transient improvements can be realized for loading and unloading transients.

7.1.1 Digital Charge Balance Controller Based on Output Voltage Sensing

The first contribution is a novel voltage sensing based digital “charge balance controller”. The control method utilizes the concept of capacitor charge balance to achieve a near-optimal transient response for Buck converters. It has been shown in the thesis that unlike previous work, the proposed controller enhances the performance and simplifies the implementation, which does NOT require 1) advanced analog-to-digital converter (ADC) or current sensor for time detection; 2) nominal output inductor or capacitor value to calculate the algorithm; 3) complex calculations such as divisions and/or square roots. Another unique feature for this proposed voltage sensing based controller is to optimize both transients from input voltage and load current using a unified formula. Also, this algorithm can be simply extended to adaptive voltage positioning (AVP) practice for modern microprocessors.

Through the comparison experiments, under the load transient cases, for loading step, the voltage undershoot is suppressed by 79% and settling time is improved by 94%, while for unloading step, the converter overshoot is reduced by 3% and settling time is shortened by 76%.
Furthermore, a possibility is shown through verifications that the proposed algorithm can be extended for AVP applications without increasing algorithm complexity. Also, the robustness enhancement of the proposed algorithm is discussed and demonstrated.

The content of this chapter is subject to patent application for U.S. patent entitled “Parameter-Independent Optimal Control Algorithm with Controlled Auxiliary Circuit for Dc-Dc Buck” filed by Queen’s University (No. 2010-024). The work has been published in the following IEEE conference:


And it has been submitted to the following IEEE journal for publication:


### 7.1.2 Enhanced Digital Charge Balance Controller for General Buck Converters

The second contribution of this thesis is the enhanced CBC concept for generally designed Buck converters. For a generally designed Buck converter, the \( ESR \) of output capacitance can be significant, making the existing CBC controllers inapplicable. In order to extend the CBC concept to a general Buck converter, a novel digital controller is presented. Without sacrificing the robustness of the voltage sensing based scheme, this digital controller can estimate the necessary design parameters by using curving fitting methodology. By this means, the \( ESR \) impact on output voltage is compensated.
Through simulation and experimental results, it is demonstrated that this enhanced digital CBC controller is capable of optimizing load transients for any reasonable ESR Buck converter designs.

The content of this chapter is subject to patent application for U.S. patent entitled “Parameter-Independent Optimal Control Algorithm with Controlled Auxiliary Circuit for DC-Dc Buck” filed by Queen’s University (No. 2010-024). The work has been published in the following IEEE conference:


And it will be submitted to the following IEEE journal for publication:


7.1.3 Analog Charge Balance Controller

The third contribution is an analog implementation of the aforementioned voltage sensing based “charge balance control” concept in Chapter 3. This ready-for-integration analog controller can be also applied for AVP applications to power the modern processors. Furthermore, an operational amplifier (OPAMP) based peak/valley voltage detector is presented to achieve lower cost, lower operating power consumption and fully analog implementation. Unlike previously presented analog approaches, this analog controller does not require analog multipliers, dividers or direct measurement of the capacitor current or load current. The controller only requires relatively simple analog functions such as amplification, voltage comparison, addition and subtraction.
It has been demonstrated through simulations and experimental results, that the proposed analog controller can be implemented for low-ESR designed Buck converter to optimize the transient response performance and enhance the robustness against the tolerance and variation of the passive components (output inductance $L_o$ and output capacitance $C_o$). Also a potential is shown for AVP applications using this scheme without increasing design complexity. Compared with a well-designed analog voltage mode Type III controller, under a 12A loading step, the settling time and undershoot are improved by 93% and 74%, respectively. For a 12A unloading step, although the overshoot is not improved because of the narrow duty ratio, the settling time is still shortened by 75% using the proposed controller.

The content of this chapter is subject to patent application for U.S. patent entitled “Parameter-Independent Optimal Control Algorithm with Controlled Auxiliary Circuit for Dc-Dc Buck” filed by Queen’s University (No. 2010-024). The work has been published in the following IEEE conference:


And it will be submitted to the following IEEE journal for publication:

7.1.4 Controlled Auxiliary Current to Improve Unloading Transient Response

The fourth and fifth contributions of this thesis are control strategies associated with auxiliary topology modification for the VR to improve the converter’s unloading transient response. An auxiliary circuit, consisting of a MOSFET, a diode and an inductor, is added to the VR to divert current from excessively charging the Buck converter’s output capacitors during an unloading transient. The control strategy proposed in Chapter 6 is capable of controlling a 12V-1.5V Buck converter and the auxiliary current. The auxiliary current is controlled in boundary conduction mode for predictable number of auxiliary switching and reduced switching loss, while the charge balance controller minimizes the settling time of the VR.

Through simulation and experimental results, it has been demonstrated that the proposed control strategy reduces the overshoot by 75% and shortens the settling time by 53.6%, under 10A unloading transient. To meet the maximum overshoot requirement of 50mV, the output capacitance can be decreased from $630\mu F$ to $170\mu F$.

To further extend the practicality, a simplified control scheme with independent control loops for two-phase VR is presented in Chapter 6. This method can be applied to laptop applications and used to address the Multiple Consecutive Load Transients (MCLTs) issue of the existing CBC based controllers. Simulations and experiments are demonstrated to verify this scheme. Fast transient load tests (10kHz-100kHz) have been conducted. Under 18A↔48A load transients, the regulation requirement (-50mV/100mV) and 10μs settling time can be met well.

The content of this chapter is subject to patent application for U.S. patent entitled “Parameter-Independent Optimal Control Algorithm with Controlled Auxiliary Circuit for Dc-Dc Buck” filed by Queen’s University (No. 2010-024). The work has been accepted in the following IEEE conference:
7.2 Future Work

This sub-section outlines possible future work for the thesis topics.

7.2.1 Digital Charge Balance Controllers

Although from the algorithm points of review, the proposed controllers have broken most of the barriers for charge balance control concept. The Multiple Consecutive Load Transients (MCLT) issue is still a major headache for CBC. In the future, with a novel and reliable load transient detector, the controller would be informed for MCLT and analyze/distinguish the condition. The recent output voltage is registered as a new initial condition for CBC concept and algorithm.

It may be advantageous to further extend these controllers to multiphase Buck converter with considering the load sharing during CBC operation. This dynamic load sharing would help to avoid the ringing back issue after transition to linear mode controller.

The curve fitting methodology would be able to be implemented using analog components, such as OPAMPs, comparators, switches, etc. This analog implementation is advantageous to reduce the controller cost and controller power consumption, which has been outlined in the aforementioned patent application documents.

7.2.2 Analog Charge Balance Controllers

The analog charge balance controller presented in Chapter 5 has unveiled a new approach toward time-optimal control. Traditionally, it was accepted that multipliers/dividers must be used to implement such control laws. In Chapter 5, the analog charge balance controller was applied to
a Buck converter; however, through modification, it may be possible to extend the concept to other topologies such as Boost and Buck-Boost derived topologies.

It may be advantageous to examine the possibility of using the concept to allow for voltage scaling optimization. Some applications (such as graphics processing units and mobile communication devices) require rapid transition from one output voltage level to another. A similar charge balance solution may be capable of determining the optimal switching intervals.

It may be advantageous to further extend this analog controller to multiphase Buck converter with considering the load sharing during CBC operation. This dynamic load sharing would help to avoid the ringing back issue after transition to linear mode controller.

In addition, it is noted that the experimental prototype was implemented with discrete analog components. Due to the distance that analog signals have to transverse in the discrete configuration, it is possible that excessive switching noise may adversely affect the circuit. Therefore, it would be advantageous to implement the entire controller in a single integrated circuit. This would allow for greater noise immunity and increased accuracy.

### 7.2.3 Controlled Auxiliary Current to Improve Unloading Transient Response

The proposed auxiliary current and related controller were used exclusively for unloading transients in this thesis. For low-duty cycle step-down conversion and low-ESR capacitors, the unloading transient will always be worse than the loading transient. However, for cases with larger duty-cycle conversion ratios or high-ESR capacitors, the loading transient may be as bad or worse than the corresponding unloading transient. Thus, it is proposed that future versions of the proposed auxiliary circuit use a synchronous MOSFET configuration in order to allow bi-direction current transfer. This will allow for improved transient performance for both loading and unloading transients.
In the thesis, both of the control strategies are proposed for non-AVP application. It would be advantageous to implement this controller for AVP application. A load current step estimator would be invented for the AVP operation and this estimator will adjust the detection threshold level according to the load line condition. So the auxiliary current will be disabled when the output voltage recovers to the adaptive voltage position instead of the original voltage reference.
References


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Appendix A

In this appendix, more detailed derivation of estimation error of $V_{sw}$ (in Section 3.7.3) is conducted. Based on the output voltage curve analysis used extensively in Chapter 3, 4 and 5, under loading step transients, the output voltage can be written as (A-1).

$$v_o(t) = \frac{V_{in} - V_o}{2 L_o C_o} (t^2 - 2T_1 t) + \frac{V_{in} - V_o}{L_o} (t - T_1) \cdot \text{ESR} + V_{ref}$$  (A-1)

By substituting (3.59) into (3.57), $\Delta v_{o, pos}$ can be solved in (A-2).

$$\Delta v_{o, pos} = - \frac{ESR^2 C_o^2 (V_{in}^2 - 2V_{in} V_o + V_o^2) + \Delta I_o^2 L_o}{2 (V_{in} - V_o) L_o C_o}$$  (A-2)

However, if we consider the delay time $t_{delay}$ caused by the extreme voltage detector, the actually sensed minimum voltage will be smaller (absolute value) than $\Delta v_{o, pos}$. By using the parabolic output voltage curve in (A-2) during $t_1$ to $t_2$, the difference can be calculated as $(V_{in} - V_o) \cdot t_{delay}^2 / 2 L_o C_o$. So the sensed voltage valley $V_{min, sen}$ can be calculated in (A-3).

$$V_{min, sen} = V_{ref} - \frac{ESR^2 C_o^2 (V_{in}^2 - 2V_{in} V_o + V_o^2) + \Delta I_o^2 L_o}{2 (V_{in} - V_o) L_o C_o} + \frac{(V_{in} - V_o) \cdot t_{delay}^2}{2 L_o C_o}$$  (A-3)

The voltage across the ESR at $t_2$ can be calculated in (A-4) by substituting the relationship between $T_1$ and $T_2$ in (3.52), upon that the actual switching point voltage $V_{SW, ESR, pos}$ can be expressed in (3.66), if the significant ESR is taken into account.

$$V_{ESR} = \text{ESR} \cdot (I_L (t_2) - I_o) = \text{ESR} \cdot \left( \frac{\Delta I_o}{T_1} \cdot T_2 \right) = \text{ESR} \cdot \Delta I_o \cdot \frac{V_o}{\sqrt{V_{in}}}$$  (A-4)

Similarly, the equations (3.67)-(3.69) can be derived.
Appendix B

In this Appendix B, derivations of output voltage overshoot calculation with proposed CAC (in Section 6.3.1) are discussed through details. Without loss of generality, it is assumed that the auxiliary circuit is switched for \( n \) times under BCM PCM control, where integer \( n \) is the number of auxiliary switching cycles. Upon that the instantaneous output voltage variation \( \Delta v_o(t) \) can be expressed for two intervals depending on the ON/OFF state of the auxiliary circuit and the \( N^{th} \) time of switching, where \( T_{aux} \) is the switching period of the auxiliary current and \( d_{aux} \) is the duty cycle of the auxiliary circuit. 

As shown in Figure B-1, during ON state of the auxiliary circuit, the output voltage overshoot can be calculated in (B-1). The capacitor current is equal to the difference between inductor current \( I_L \) and the auxiliary current \( I_{Laux} \). The overshoot is calculated by integrating the capacitor current over time. Alternatively, we can simply calculate the area difference between the trapezoidal area (with stripe) and the shaded area (in yellow). The yellow shaded area can be also considered as the combination of a square (the third term in the right hand side equation of (B-2)) and a triangle (the forth term in the right hand side equation of (B-2)). Finally, the equation can be simplified in (B-2).

\[
\Delta v_o(t) = \frac{1}{C_o} \left[ \int_0^t (I_L - I_{Laux}) dt \right] = \frac{1}{C_o} \int_0^t \left( \frac{\Delta I_o - \frac{V_o}{L_o}}{2} \right) dt - \frac{\Delta I_o \cdot N \cdot T_{aux}}{2C_o} - \frac{1}{C_o} \int_0^{t - N \cdot T_{aux}} \frac{V_o}{L_{aux}} \cdot t \cdot dt
\]  

\[
\Delta v_o(t) = \frac{1}{C_o} \left[ \frac{\Delta I_o \cdot t - \frac{V_o}{2L_o} t^2 - \frac{N \cdot \Delta I_o \cdot T_{aux}}{2}}{2} - \frac{V_o}{L_{aux}} t \cdot dt \right] 
\]

\[
\left( NT_{aux} \leq t < NT_{aux} + d_{aux} \cdot T_{aux} \right) \quad \left( N = 0, 1, 2 ..., n \right) 
\]
Similarly, as shown in Figure B-2, during OFF state of the auxiliary circuit, the output voltage overshoot can be calculated in (B-3).

$$\Delta v_o(t) = \frac{1}{C_o} \int_0^t (I_L - I_{aux}) dt = \frac{1}{C_o} \int_0^t \left( \Delta I_o - \frac{V_o - V_{aux}}{L_{aux}} t \right) dt - \frac{\Delta I_o \left( N + D_{aux} \right) T_{aux}}{2C_o}$$

$$- \frac{1}{C_o} \int_0^t \left( \Delta I_o - \frac{V_{in} - V_o t}{L_{aux}} \right) dt$$

$$= \frac{1}{C_o} \left[ \frac{\Delta I_o \cdot t - V_o t^2}{2 L_o} - \frac{N \cdot \Delta I_o \cdot T_{aux}}{2} - \frac{V_{in} - V_o}{2 V_{in}} T_{aux} \Delta I_o \right]$$

$$= \frac{1}{C_o} \left[ -\int_{(t-N T_{aux} - d_{aux} T_{aux})}^{T_{aux}} \frac{(V_{in} - V_o)(T_{aux} - t)}{L_{aux}} dt \right]$$

$$\left( N T_{aux} + d_{aux} T_{aux} \leq t < (N + 1) T_{aux} \right) (N = 0, 1, 2 \ldots)$$
Figure B.2 Overshoot derivation with CAC during ON interval

The local output maximum voltage will occur during ON state of the auxiliary circuit. The global output overshoot/maximum voltage occurs, when the derivative of the equation (B-2) is zero during the \((N'+1)\)th switching, expressed in equation (B-4).

\[
\Delta I_o = \frac{V_o}{L_o} t - \frac{V_o}{L_{aux}} (t - N T_{aux}) = 0 \quad \text{(B-4)}
\]

So the \(t_{ost}\) instant when the overshoot happens can be solved in (B-5),

\[
t = t_{ost} = \frac{\Delta I_o + \frac{V_o}{L_o} N T_{aux}}{\frac{V_o}{L_o} + \frac{V_o}{L_{aux}}} = \frac{\frac{V_o}{L_o} n T_{aux} + \frac{V_o}{L_{aux}} N T_{aux}}{L_{aux} + L_o} \quad \text{(B-5)}
\]

As it is assumed, \(n\) is an integer. The auxiliary switching cycle \(T_{aux}\) can be expressed as in (B-6).
\[ T_{\text{aux}} = \frac{\Delta I_o L_o}{nV_o} = \frac{\Delta I_{\text{aux}} L_{\text{aux}}}{D_{\text{aux}}V_o} \] (B-6)

Therefore, the integer \( n \) can be calculated based on (B-7).

\[ n = \frac{D_{\text{aux}} L_o}{L_{\text{aux}}} \] (B-7)

And generally, \( n \) can be calculated by rounding down (B-7), which is shown in (6.2). By substituting (B-7) into (B-5), the equation (B-8) can be derived.

\[ t_{\text{aux}} = \frac{D_{\text{aux}} + N'}{D_{\text{aux}} + n} \cdot nT_{\text{aux}} \] (B-8)

For unloading step transient without the CAC, the output voltage can be written as (B-9) using the parabolic curve analysis in Chapter 3 and 4. Based on the average auxiliary current \( L_{\text{aux}} \text{avg} \) without considering the auxiliary inductor current ripple under the BCM peak current control, a simplified equation is provided as a simplified method to calculate the overshoot in the equation (B-9). The symbols \( L_o, C_o, ESR, \Delta I_o, V_o \) and \( L_{\text{aux}} \) represent the output inductance, output capacitance, equivalent series resistance, load step value, output voltage and the auxiliary inductance, respectively. \( A_{\text{aux}} \) equals the extra charge being delivered to the output capacitor while the auxiliary current is ramping to \( I_{\text{aux_peak}} \) following \( t_0 \). \( A_{\text{aux}} \) is expressed in (B-10) and is substituted in (B-9), as show in (6.4).

\[ \Delta V_o(t) = \frac{V_o}{2L_oC_o} \left( t^2 - 2T_1 t \right) + \frac{V_o}{L_o} \left( t - T_1 \right) \cdot ESR + A_{\text{aux}} \] (B-9)

\[ A_{\text{aux}} = \frac{\left( \frac{\Delta I_o}{2} \right)^2 L_{\text{aux}}}{2V_oC_o} \] (B-10)