HIGH FREQUENCY CLASS DE CONVERTER USING A MULTILAYER CORELESS PCB TRANSFORMER

By

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Abstract

In modern power electronics equipment, it is desirable to design a low profile, high power density, and fast dynamic response converter. Increases in switching frequency reduce the size of the passive components such as transformers, inductors, and capacitors which results in compact size and less requirement for the energy storage. In addition, the fast dynamic response can be achieved by operating at high frequency. However, achieving high frequency operation while keeping the efficiency high, requires new advanced devices, higher performance magnetic components, and new circuit topology. These are required to absorb and utilize the parasitic components and also to mitigate the frequency dependent losses including switching loss, gating loss, and magnetic loss. Required performance improvements can be achieved through the use of Radio Frequency (RF) design techniques.

To reduce switching losses, resonant converter topologies like resonant RF amplifiers (inverters) combined with a rectifier are the effective solution to maintain high efficiency at high switching frequencies through using the techniques such as device parasitic absorption, Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), and a resonant gating.

Gallium Nitride (GaN) device technologies are being broadly used in RF amplifiers due to their lower on- resistance and device capacitances compared with silicon (Si) devices. Therefore, this kind of semiconductor is well suited for high frequency power converters.

The major problems involved with high frequency magnetics are skin and proximity effects, increased core and copper losses, unbalanced magnetic flux distribution generating localized hot spots, and reduced coupling coefficient. In order to eliminate the magnetic core losses which play a crucial role at higher operating frequencies, a coreless PCB transformer can be used. Compared to the conventional wire-wound transformer, a planar PCB transformer in which the windings are laid on the Printed Board Circuit (PCB) has a low profile structure, excellent thermal characteristics, and ease of manufacturing.
Therefore, the work in this thesis demonstrates the design and analysis of an isolated low profile class DE resonant converter operating at 10 MHz switching frequency with a nominal output of 150 W. The power stage consists of a class DE inverter using GaN devices along with a sinusoidal gate drive circuit on the primary side and a class DE rectifier on the secondary side. For obtaining the stringent height converter, isolation is provided by a 10-layered coreless PCB transformer of 1:20 turn’s ratio. It is designed and optimized using 3D Finite Element Method (FEM) tools and radio frequency (RF) circuit design software. Simulation and experimental results are presented for a 10-layered coreless PCB transformer operating in 10 MHz.
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<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>FR4</td>
<td>Flame Retardant 4</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>PRC</td>
<td>Parallel Resonant Converter</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<td>Si</td>
<td>Silicon</td>
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<td>SPRC</td>
<td>Series-Parallel Resonant Converter</td>
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<td>SPICE</td>
<td>Simulation Program with Integrated Circuit</td>
</tr>
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<td>SRC</td>
<td>Series Resonant Converter</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero Current Switching</td>
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<td>ZDS</td>
<td>Zero Derivative Switching</td>
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<td>ZVS</td>
<td>Zero Voltage Switching</td>
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Chapter 1

Introduction

1.1 Motivation for Frequency Increases

Power electronic converters play a vital role in nearly all electronic equipment including computers, transportation electronics, telecommunications equipment, medical equipment, industrial electronics, etc. As structure of the power electronic system in Figure 1-1 shows, power stage is including the passive components such as inductor, capacitor and transformer which dominate the size of the power converter [1].

![Figure 1-1: Structure of the power electronic system](image)

In modern applications, power electronics converter design are based on high efficiency and high power density [2], [3]. In order to obtain low profile and high power density converters, the requirement is to reduce the size of passive elements. Value and size of the passive components are inversely proportional to the frequency. So increasing the switching frequency can reduce the size of magnetics (transformers, inductors) and capacitors which results in less requirement for the energy storage per operating cycle and thus the size and cost of the converter get reduced [4], [5]. Furthermore, by operating at high frequency the fast dynamic response can be achieved to the rapid changes in line/load variations [6]. Generally, improved transient performance, converter miniaturization and integration are the major goals that motivate the development of switching power converters operating at increased switching frequencies.
Apart from these advantages, the advances in semiconductor fabrication technology, like GaN devices, have made significant opportunities for improving high frequency converters operation [7], [8]. In fact, switching devices play a crucial role in the converter losses in which GaN devices exhibit improved performance in terms of switching speed and reduced on state resistance compared to existing Si (Silicon) devices.

1.2 Challenges of High Frequency Power Converter Design

In the previous section, the benefits of operating the converter at higher switching frequencies have been discussed. Realizing these advantages, however, requires to mitigate frequency dependent loss mechanisms including switching loss, gating loss, and magnetic loss which increase linearly with frequency [9]–[11]. Therefore, achieving high frequency operation while keeping the efficiency high, requires new advanced devices, higher performance magnetic components, and new circuit topology to absorb and utilize the parasitic components in the conversion process. [12]–[14].

In order to avoid switching losses in dc-dc converters operating at high frequencies while keeping the efficiency high, resonant topologies have to be used [15]–[16]. For the last two decades, research has been done to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc-dc converters [17]. With this type of converter, it is possible to achieve soft switching including Zero Voltage Switching and/or Zero Current Switching. Soft switching technique and in particular ZVS, reduces the switching loss by maintaining a low voltage across the semiconductor device during the on/off transitions [18], [19]. Likewise, resonant gate drivers can reduce gate losses due to gating of the semiconductor device [20], [21]. With conventional gate drives, gate loss is proportional to switching frequency and they are not acceptable for high frequency applications. Therefore, a resonant gate drive circuit uses reactive elements to recover a portion of the gate energy lost in conventional drivers and return it to the power source. One approach that has been used previously is a sinusoidal gate drive [22]. In this approach, a resonant network is used to ring charge on and off the gate such that the gate voltage is sinusoidal.
A further challenge in implementing high frequency converters is skin and proximity effects, increased core and copper losses, and unbalanced magnetic flux distribution generating localized hot spots in the transformer [23]. By increasing the switching frequency of the converter, core and copper losses are increased due to skin and proximity effects induced by the induced eddy currents and thus the overall energy efficiency of the converter is degraded [24] – [26]. In order to eliminate the core losses that are predominant in high frequency applications, coreless PCB transformers can be an effective solution. Also, a proper winding structure of the coreless PCB transformer is required to reduce the skin and proximity effects at higher frequencies. These kind of transformers do not need space to accommodate the magnetic core and have the advantages of low costs, high power density, low profile, no magnetic core loss, and ease of manufacturing.

Parasitic components introduced by the devices, packages and interconnections are another important consideration in high frequency converters. In many high frequency Circuits, the size of some components is comparable to the parasitics. For example, the output parasitic capacitance of semiconductor device $C_{oss}$ has a big impact on the design of the overall converter. According to [27] it depends on output power $P_{out}$, input voltage $V_{in}$ and switching frequency $f_{sw}$ as shown below.

$$P_{out}=\frac{2\pi^2 f_{sw} C_{oss} V_{in}^2}{n_0} \quad (1.1)$$

Therefore, by increasing the switching frequency, topologies that absorb or utilize the parasitic components especially device capacitances, as a part of their operation are required. In this regard, resonant topologies not only reduce the switching losses, but also incorporate the parasitic circuit elements into the resonant tank without degrading performance and hence they are perfectly suited for high frequency applications.

1.3 Thesis Objectives

(a) The objective of this thesis is to design and analysis an isolated 10MHz dc-dc converter using a multilayer coreless PCB transformer with a high voltage transfer ratio. In order
to achieve this goal, it is necessary to choose a proper converter topology by considering parasitic components, since the parasitic components play an important role at high frequency levels. According to the advantages of class DE circuits, class DE inverter and rectifier are proper choice for this application. This thesis addresses a class DE design for a 10MHz, 150W output power, 20 V/400 V input/output voltage converter. During the design, required characteristics of the matching network including series resonant tank and high frequency transformer are revealed. The effective output/input impedances of the inverter/rectifier are calculated to be used for designing the matching network including series resonant tank and high frequency transformer. By creating EM model of the inverter/rectifier PCB layout and carrying out Harmonic Balance simulations, the parasitic inductance of the PCB layout is achieved. Besides, to illustrate how parasitic inductances impact on the inverter function, the currents flowing through the parasitic inductors are analyzed and calculated. Hence, designing the transformer and other magnetic parts becomes possible. Advanced Design System (ADS) is considered as an advanced tool in which the GaN switches as well as SiC diodes models are imported to the design. These models include all parasitic components of the devices and consequently result in an accurate simulation at high frequencies.

(b) This thesis also proposed a multilayer coreless PCB transformer with improved current sharing in the parallel winding structure. The method for designing the multilayer coreless PCB transformer is initiated by background discussions, creating simulations, tuning the parameters, designing the PCB layout and finally by means of testing and measurements. In view of the complexity of accurate analytical methods, for modelling high frequency transformer, 3D Finite Element Method (FEM) tool, is considered as a primary tool prior to the construction of the prototypes. To obtain an efficient transformer design, a range of multilayer coreless PCB transformers with different geometric parameters are fabricated and tested. Furthermore, S-parameters of the
planar PCB transformers are extracted from EM simulator and converted to Z-parameters to calculate the input impedance of the matching network. This matching network including a resonant circuit and a high frequency transformer provides a combination of isolation, voltage transformation, and the required matching between the rectifier and the inverter impedances. The merits of these transformers are verified via high frequency simulations of the designed class DE converter.

(c) After the successful evaluation and simulation of the transformer using the simulation tool, the prototypes are developed using PCB design software and evaluated in a high frequency region. The purpose is to investigate the possibility of using the multilayer coreless PCB transformer for step up conversion applications.

1.4 Thesis Outline
In this thesis the focus is on analyzing and designing a class DE resonant converter operating in 10MHz by using a multilayer coreless PCB transformer. The goal of this work is to implement of a high efficiency step-up 10-layer coreless PCB transformer to enable high frequency operation of the class DE resonant converter.

Chapter 1 gives a brief introduction on basic background and motivation behind the requirement for increasing switching frequency. In this chapter, challenges of high frequency power converter design as well as high switching frequency solutions are presented to minimize frequency dependent losses.

In chapter 2, a literature review of the areas related to the contribution of this thesis will be performed. The merits and demerits of existing technology will be presented.

Chapter 3 presents the design, high frequency analysis of a class DE resonant converter operating in 10 MHz frequency. High frequency analysis for both inverter and rectifier, simulation results of high frequency class DE converter are presented in this chapter. Also, the effective output /input impedances of the inverter /rectifier are calculated to be used for designing the matching network including series resonant tank and high frequency transformer.
Chapter 4 proposes design and analysis of a 10-layer coreless PCB transformer with improved current sharing in the parallel winding structure. In this chapter, a 3D Finite Element Method (FEM) tool, is considered as a primary tool prior to the construction of the prototypes. To obtain an efficient transformer design, a range of multilayer coreless PCB transformers with different geometric parameters are fabricated and tested. Furthermore, S-parameters of the planar PCB transformers are extracted from EM simulator and converted to Z-parameters to calculate the input impedance of the matching network. This matching network including a resonant circuit and the multilayer coreless PCB transformer.

In chapter 5, a prototype of the 10 layer coreless PCB transformer is constructed in order to validate the theoretical studies. Experimental results of high frequency multilayer coreless PCB transformer are presented in this chapter. There is a very good agreement between the results obtained with the simulation and experimental results.

Chapter 6 summarizes the contributions of the research presented in this thesis and gives recommendations for future work.
Chapter 2
Literature Review

As mentioned in the first chapter, achieving high frequency operation while keeping the efficiency high in converters, requires new advanced devices, higher performance magnetic components, and new circuit topology to absorb the parasitic components and to mitigate the frequency dependent losses. This chapter reviews the topics relevant to high frequency dc-dc converters.

2.1 DC-DC Converter Types
Dc-dc converter with high power density and high efficiency is increasingly required in telecommunications and computing applications. Dc-dc converters using these days are switching converters in which switches are operated in the on or off state. These converters can be isolated, or non-isolated. Generally there are two classes of dc-dc converters: pulse width modulation (PWM) and resonant mode.

Most PWM dc-dc converters consist of an inverter, a rectifier, a filter and a transformer for isolation if required. The inverter creates a high frequency square wave voltage which is rectified and then filtered to produce a dc output voltage. Compared to PWM converters, which suffers from decreased efficiency and deteriorated EMI (Electromagnetic Interference) problem at high switching frequency, resonant dc-dc converter is a good alternative due to its advantages of high efficiency, high switching frequency and high power density.

2.2 Merits of Resonant DC-DC Converters
A resonant dc-dc converter which is a class of switched mode power supplies, typically consists of a dc/ac inverter circuit coupled to an ac/dc rectifier circuit by using a matching network as illustrated in Figure 2-1. The matching network including a resonant circuit and a transformer provides a combination of isolation, and voltage transformation [28]. The inverter applies a high frequency square wave voltage to a resonant circuit. The resonant circuit is tuned close to
the switching frequency and has the effect of filtering higher harmonic voltages so that a nearly 
sine wave of current appears at the input of the matching network. This voltage is rectified by 
rectifier and then filtered to produce a dc output voltage.

![Diagram](image)

Figure 2-1: A block diagram of a high frequency dc-dc converter

It can be demonstrated that resonant converters can achieve soft switching techniques including 
zero current switching if operated below the resonant frequency (leading current), or zero 
voltage switching if operated above the resonant frequency (lagging current) [29]. ZVS is a 
better technique than ZCS because with ZVS, both the turn-on and turn-off losses can be 
effectively reduced [30]. In ZCS, only the turn-off loss can be reduced. Therefore, soft 
switching and in particular zero voltage switching, reduces the switching loss by maintaining a 
low voltage across the semiconductor device during the on/off transitions and also reduces the 
EMI due to the sinusoidal nature of the voltages and/or currents. Another advantage of resonant 
converters is that they are often designed to absorb device, components, and interconnect 
parasitic into the resonant circuit. They are therefore well-suited for high frequency operation 
[31].

There are three main types of resonant circuits shown in Figure 2-2, series resonant, parallel 
resonant and series-parallel resonant. Depending on how the resonant circuits are combined 
with other circuit configurations, several types of resonant converters can be obtained. All types 
of resonant converters achieve soft switching, and the use of one over the other depends on the 
requirements of the application.
2.2.1 Series Resonant Converter

The series resonant converter (SRC), shown in Figure 2-3, is the simplest type of resonant converter. The major advantage of this converter is that the series resonant capacitor blocks dc component. Hence, converter can easily be used in full-bridge arrangements without any additional control to control unbalance in the power FET switching times. In addition, since a transformer is required for galvanic isolation, it is beneficial to choose a topology which includes a series dc-blocking capacitor to avoid transformer saturation.

Since the resonant circuit is connected between the inverter and the load, it can be assumed that the current harmonics in the series resonant circuit are very small. Therefore, the gain of series resonant converter can be obtained by using the fundamental equivalent circuit shown in Figure 2-4. For this fundamental circuit, the rectifier load at the primary of the transformer can be represented by an equivalent AC resistance $R_{ac}$.

![Figure 2-3: Structure of a series resonant dc-dc converter](image)

![Figure 2-4: Fundamental equivalent circuit for series resonant converters](image)
\[
\frac{V_p}{V_s} = \frac{1}{1 + j \left( \frac{X_L - X_C}{R_{ac}} \right)}
\]

(2.1)

Where

\[ R_{ac} = \frac{8}{\pi^2} R_L \]  Rectifier load at the primary of the transformer,

\[ Q = \frac{L_{sr} \omega_r}{R_L} \]  Quality factor,

\[ \omega_r = \frac{1}{\sqrt{L_{sr} C_{sr}}} \]  Angular resonant frequency, and

\[ \omega_s = 2\pi f_s \]  operating angular switching frequency.

\[
\frac{V_o}{nV_i} = \frac{1}{1 + j \left( \frac{\pi^2}{8} Q \frac{\omega_s}{\omega_r} \frac{\omega_r}{\omega_s} \right)}
\]

(2.2)

Another advantage of the series resonant converter is that it requires no discrete series resonant inductor, because the inductance can be designed into the transformer. Also, since it has no parallel resonant capacitor, there is no circulating current in the circuit.

The series resonant converter has the main drawback that the output voltage cannot be regulated at reduced load and no load. Another disadvantage of the converter is that the output dc filter capacitor must carry high ripple current which is equal to 48 percent of the dc output current magnitude [32]. This is a significant disadvantage for applications with low output voltage and high current. For this reason the series resonant converter is not considered suitable for low output voltage high output current converters.

### 2.2.2 Parallel Resonant Converter

Figure 2-5 illustrates parallel resonant converter (PRC) which is able to control the output voltage at no load by operating at a frequency above resonance in contrast to the series resonant converter. The parallel resonant converter is suitable for low output voltage, high output current applications due to the use of inductive output filter. In fact, the inductor limits the ripple current.
carried by the output capacitor and hence output capacitor capable of carrying very high ripple currents is not required.

Figure 2-5: Structure of a parallel resonant dc-dc converter

The gain of parallel resonant converter is given by

$$\frac{V_0}{nV_i} = \frac{1}{\frac{\pi^2}{8} \left[ 1 - \frac{\omega_2}{\omega_r} \right] + j \frac{\omega_2}{\omega_r} Q}$$

(2.3)

Where

$$Q = \frac{R_L}{L_{sr} \omega_r}$$ – Quality factor,

$$\omega_r = \frac{1}{\sqrt{L_{sr} C_{pr}}}$$ – Angular resonant frequency, and

The main disadvantage of the parallel resonant converter is that the current carried by the power device and resonant components is somewhat independent of load. In fact, as the load resistance increases which means the load decreases, the frequency of operation increases to regulate the output voltage, but the current flowing through the resonant circuit stays relatively constant. This results in an almost constant conduction loss in the semiconductor device and reactive components as the load decreases (load resistance increases). Therefore, the parallel resonant converter suffers from poor light-load efficiency due to high circulating current through parallel capacitor $C_{pr}$. Moreover, this circulating current increases as the input voltage of the converter increases. So, this converter is not ideal for applications which have a large input voltage range.

**2.2.3 Series-Parallel Resonant Converter**

The combination series and parallel resonant converter (SPRC) show in Figure 2-6, improves the efficiency over the PRC, and regulates the output voltage even at light-load.
Using classical ac analysis techniques, for \( C_{sr} = C_{pr} \) it can be shown that the gain of the series-parallel resonant converter is given by

\[
\frac{V_o}{nV_i} = \frac{1}{\pi^2} \left[ 2 - \left( \frac{\omega_s}{\omega_r} \right) \right] + jQ \left[ \frac{\omega_s - \omega_r}{\omega_r} \right]
\]

Where

\[
Q = \frac{\omega_{sr}}{R_L} \quad \text{Quality factor,}
\]

\[
\omega_r = \frac{1}{\sqrt{L_{sr}C_{sr}}} \quad \text{Angular resonant frequency.}
\]

In fact, this kind of resonant converter attempts to eliminate the weak points of series and parallel converters including lack of no load regulation for series resonant converter and circulating current independent of the load for the parallel resonant converter. This goal is obtained by proper selection of the resonant components but a relative wider frequency range of operation is needed.

### 2.3 Radio Frequency Power Amplifier

In order achieving high frequency operation in converters while keeping the efficiency high, a proper resonant circuit design is required to absorb the parasitic components as an integral part of its operation and to mitigate the frequency dependent losses is required. This performance improvement can be achieved through the use of radio frequency (RF) design techniques. In fact, a number of resonant converter topologies usually draw from radio frequency (RF) amplifier techniques to achieve efficient energy conversion [33], [34] at high frequencies. For more than two decades [17] research has been done to use the resonant RF amplifiers (inverters) combined with a rectifier for dc-dc converters. Similar to switch mode power converters, RF
amplifiers convert the constant input voltages into a high frequency voltage by operating power semiconductor devices in the cut-off or saturation region only.

The most efficient standard radio frequency amplifiers are Class E [35], [36], class F [37], class EF₂ (ϕ₂) [38], and class DE [39] – [42] which incorporate resonant network in order to provide zero voltage switching of the semiconductor switch and consequently to achieve high efficient operation at high frequencies.

The class E converter shown in Figure 2-7 has been widely used in a range of high frequency dc-dc power converters. It consists of a single switch, two inductors, and two capacitors. In an optimum operation, \( \frac{L_{\text{in}}}{2Q_1Q_2} \) is an infinite choke providing a pure dc input current. Class E converter utilizes resonant circuit (\( L_r \) and \( C_r \)) to provide zero voltage switching of semiconductor switch which consequently leads to a reduction of switching loss. With proper selection of the circuit parameter zero voltage switching (ZVS) and zero derivative switching (ZdS) can be achieved. In addition, this type of converter utilizes only a single ground-referenced switch, and absorbs device output parasitic capacitance into the circuit topology. Although class E converter has many advantages, it also has some important limitations like high voltage stress imposed on the switch. The peak voltage stress across the switch in an ideal class E circuit is about 3.6 times the input voltage for a duty cycle of 50% [43]. Moreover, class E converter has the disadvantage of a large input inductor which results in relatively large stored energy in the converter that increases the time for the converter to adjust its operating point (during startup or shutdown).

![Figure 2-7: Structure of the Class E resonant inverter](image)

Another radio frequency amplifier, class F shown in Figure 2-8, uses additional resonant circuit in series with the load to open circuit the switch drain at several odd harmonics. As a result, the
voltage waveform will be similar to a square wave since the generated odd voltage harmonics will tend to flatten the top and bottom of the waveform. This flattening causes reduction in the peak voltage across the switch during the time that it is conducting [44]. However, it is easily seen that even with using complex high order harmonic circuits, class F amplifier operates with significant overlap of device voltage and current. In fact, they are not working fully in switched mode, thus providing unacceptably low efficiency for many power electronics applications [45].

Therefore, in order to reduce the huge peak voltage across the switch of class E converter, class $\text{EF}_2(\phi 2)$ which is a hybrid between the class E and class F has been developed [46]. As Figure 2-9 illustrates, it consists of an extra resonant circuit - $\text{C}_{\text{Mr}}$ and $\text{L}_{\text{Mr}}$ - across the drain and source of the switch with a short circuit at the second harmonic of switching frequency $f_s$. If the resonant circuit tunes correctly, the third harmonic of $f_s$ will be added on top of the sine wave which produces a trapezoidal waveform across the switch. This reduces the peak voltage, but increases complexity by using high order resonant structure with extra energy storage components.
**Class DE** converter shown in Figure 2-10, consists of a matching network including a series resonant circuit, two semiconductor devices, and two capacitances. Each switch has a shunt capacitor in parallel, which includes the parasitic output capacitance of the semiconductor device. The quality factor $Q$ of the matching network is high enough to force the inverter’s output current waveform to be almost sinusoidal. Class DE converter is the topology which takes characteristics of both class D and class E inverters. Therefore, it can achieve ZVS/ZDS condition during switching operation (as class E inverter) and also reduce the peak voltage across the semiconductor device considerably due to the direct connection to the input (as class D inverter) and hence the maximum voltage across the switching devices is limited to the input supply voltage. Class DE converter has two great advantages over the other topologies. It has only a single inductor and due to the lowest stress on the switch, the stored energy is lower. However, the class DE converter requires a high side gate drive and the design of this circuit for high frequency is critical.

![Figure 2-9: Structure of the Class EF resonsant inverter](image1)

**2.4 High Frequency Power Transformer**

As some of single/double ended topologies such as forward, fly-back, half-bridge, and full bridge resonant converters demand electrical isolation, step down/up conversions, and multiple outputs, transformers have become the irreplaceable components in modern power supplies. More importantly, these magnetic components play prominent role in high frequency applications, as they typically dominate the size of power electronic converters.
Conventional transformer shown in Figure 2-11, is usually a core-based wire-wound transformer, which is used to transfer energy while providing galvanic isolation in the circuit. The main reasons for using magnetic cores which are made of ferromagnetic materials, are mostly to provide a high degree of coupling coefficient as well as a low value of leakage inductance.

![Figure 2-11: Conventional core-based wire-wound transformer](image)

This transformer structure has not come across a serious problem in the past, because most transformers were designed for low frequency operations (several hundreds of kilo-hertz). However, by increasing the switching frequency of the converter, several drawbacks come with conventional transformer such as core and copper losses. Skin and proximity effects induced by eddy currents in the windings increase these losses considerably and also cause the unbalanced magnetic flux distribution which generate localized hot spots and reduce the coupling coefficient [47].

In order to eliminate the core losses which are significant in high frequency applications, coreless transformers can be an effective solution. Therefore, coreless wire-wound transformers have been proposed in papers [48], [49] for high frequency applications. Twisted coil transformer without magnetic core presented in [48] was demonstrated that this kind of transformer could achieve a coupling factor of 0.8 at about 1 MHz. However, the parameters of twisted coil transformers cannot be precisely controlled. Moreover, it is difficult to manufacture a large quantity production of the identical twisted coil transformers and also labor cost for manual winding process is considerable.
Due to above mentioned disadvantages, planar PCB transformers are more preferable in high frequency converters [50] – [55]. In planar PCB transformers, the windings are laid on a printed circuit board (PCB) which the dielectric breakdown voltage typically ranges from 15kV to 50kV [56].

The application of the planar PCB transformer with magnetic core has been reported in many recent literature works [57], [58]. Although cored type transformers fabricated on PCB shown in Figure 2-12 eliminate the manufacturing cost of manual windings and also make it possible to manufacture transformers with accurate parameters in an automated manner, the use of magnetic cores in these transformers is still the dominant challenge [59]. In these transformers, space is required to accommodate the magnetic cores.

![Figure 2-12: cored type planar PCB transformer](image)

Therefore, the need for high operating frequency, high power density, and low profile converters has been led to use of the coreless PCB transforms, as they do not have the limitations related to magnetic cores such as core losses and saturation. Coreless PCB transformers occupy a much smaller area than the core-based PCB transformers and ease of manufacturing, excellent thermal characteristic, and increased reliability are other advantages of this type of transformer.

For low voltage and high current applications, the use of only a single layer PCB conductors with the thickness of $\frac{1}{2}$ - 4 Oz is not recommended for designing a high frequency transformer.
So, several layers have to be connected in parallel in order to increase the current handling capacity of the winding to create the multilayer coreless PCB transformer, Figure 2-13, suited for high frequency applications [60]

![Figure 2-13: Multilayer coreless PCB transformer employed in [60]](image)

Even though there is no magnetic core losses in a multilayer coreless PCB transformer, due to the skin and proximity within the conductors, the currents flowing through the parallel layers is not be equally divided among them which consequently results in extra winding resistance. One solution is to apply interleaving structure for primary and secondary of the transformer to minimize the leakage inductance as well as ac winding loss. In recent years, different winding arrangements of multilayer coreless PCB transformer have been proposed in [61]–[64] to uniform the current density distribution within winding layers. However, the winding structure in [61], [63], and [64] is applied to the low frequency transformers (under 500 kHz range) which has the less important issues compared to higher frequency applications. Reference [64] focuses on designing parameters such as leakage inductance and stray capacitance rather than studying about current density distribution in parallel layers. In [62], the application of interleaving between primary and secondary windings for all three cases has not effectively reduced the ac resistance of winding at 1 MHz. Therefore an optimized winding layout arrangement for parallel layers of the multilayer coreless PCB transformer is required to uniform the current density distribution within the windings.
2.4.1 High Frequency Model of Coreless PCB Transformer

The high frequency model coreless PCB transformer [65] is shown in Figure 2-14.

![Diagram of high frequency model of coreless PCB transformer](image)

Figure 2-14: High frequency model of coreless PCB step-down transformer employed in [65]

R₁: Primary winding resistance.
R₂: Secondary winding resistance
Rₐ: Resistive load
L₁ₗ₁: Primary leakage inductance
L₁ₗ₂: Secondary leakage inductance
Lₘ₁: Primary mutual inductance
Lₘ₂: Secondary mutual inductance
Lₘ: Mutual Inductance
C₁: Primary intrawinding capacitance
C₂: Secondary intrawinding capacitance
C₁₂: Interwinding capacitance between primary and secondary windings

For coreless PCB transformer with primary and secondary windings printed directly on the opposite sides of a doubled-sided PCB, the intrawinding capacitance is negligible [66]. The primary/secondary mutual inductances of the transformer are given as:

\[ L_{m1} = L_1 \cdot L_{1k1} \]  
(2.5)

\[ L_{m2} = L_2 \cdot L_{1k2} \]  
(2.6)

Where, \( L_1 / L_2 \) are the self-inductance of the primary/secondary winding. The mutual inductance ‘\( L_m \)’ between the primary and secondary windings of the transformer is given by [67]:

19
\[ L_m = \sqrt{L_{m1}L_{m2}} \]  \hspace{1cm} (2.7)

The coupling coefficient is calculated by dividing the mutual inductance over the geometric mean of primary and secondary self-inductances according to [68]:

\[ K = \frac{L_m}{\sqrt{L_1L_2}} \]  \hspace{1cm} (2.8)

The turn’s ratio ‘n’ of the transformer can be obtained from measured self-inductances of primary and secondary as follows:

\[ n = \sqrt{\frac{L_1}{L_2}} \]  \hspace{1cm} (2.9)

Ac winding resistances of the primary and secondary windings are functions of the operating frequency due to skin effect. They are specifically studied for transformers in [69]. Ac resistances are calculated by using the following expression and by approximating the model to a circular spiral inductor.

\[ R_{AC} = \frac{R_{DC}h}{\delta \left(1 - \exp \left(-\frac{h}{\delta}\right)\right)} \]  \hspace{1cm} (2.10)

Where

- \( R_{DC} \): DC resistance of the winding
- \( h \): Height of the conductor
- \( \delta \): Skin depth in the conductor

The dc resistances of the primary/secondary windings are also calculated as follows:

\[ R_{DC} = \frac{\rho l}{A} \]  \hspace{1cm} (2.11)

Where

- \( \rho \): Resistivity of copper conductor, \( 1.68 \times 10^{-8} \, \Omega \, \text{m} \)
- \( l \): Length of the conductor
- \( A \): Area of copper tracks

The skin depth is obtained by:
\[ \delta = \frac{1}{\sqrt{\pi \mu \sigma}} \]  

(2.12)

Here,

\( f \) : Operating frequency

\( \mu \) : Permeability of the substrate

\( \sigma \) : Conductivity

For a copper conductor, \( \rho = \frac{1}{\sigma} = 1.68 \times 10^{-8} \Omega \text{m} \) and the permeability \( \mu \) is equal to \( \mu_0 \). The skin depth of the copper conductor in 10MHz is 23\( \mu \text{m} \).

### 2.4.2 Performance Characteristics of Coreless PCB Transformer

Optimal operating conditions for using coreless PCB transformer is to minimize the input power consumption and maximize the energy efficiency. By increasing the transformer input impedance \( Z_{\text{in}} \), the primary winding current and hence power requirement are reduced. Moreover, to achieve a high transformer efficiency, the voltage gain \( V_s/V_p \) should be greater than unity.

On the other hand, the apparent problems of a coreless PCB transformer- low coupling factor and high leakage inductance- can be solved by using a resonant technique [66]. An external capacitor is connected across the secondary winding of the transformer to increase voltage gain, \( V_s/V_p \) (to overcome the low magnetic coupling), input impedance \( (Z_{\text{in}}) \), and consequently the energy efficiency \( (\eta) \) of the transformer. This is due to the partial resonant phenomena of the leakage inductance of the transformer and the external resonant capacitor [66]. Since a resonant topology is utilized for the dc-dc converter, the high leakage inductance of the coreless PCB transformer is not considered as an undesired component and can be absorbed into the resonant tank. With the assistance of a high frequency equivalent circuit shown in Figure 2-15, the basic characteristics of coreless PCB transformers such as voltage gain and input impedance are described [70].
Figure 2-15: High frequency equivalent circuit of the transformer referred to primary employed in [65]

Where

\( R_1 \): Primary winding resistance

\( R'_2 \): Secondary winding resistance referred to the primary side

\( R_L \): Resistive load

\( L_{ik1} \): Primary leakage inductance

\( L'_{ik2} \): Secondary leakage inductance referred to the primary side

\( L_m \): Mutual Inductance

\( C_1 \): Primary interwinding capacitance

\( C'_2 \): Sum of the secondary interwinding capacitance and an externally connected capacitance referred to the primary side

\( C'_{12} \): Coupling capacitance between primary and secondary windings referred to the primary side

As described in [71], the external capacitance \( C_2 \) can determine the resonant frequency of the transformer. The no-load resonant frequency of the transformer is given by [72]:

\[
f_r = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \quad (2.13)
\]

\[
L_{eq} = L'_{ik2} + L_{ik1}\parallel L_m \quad (2.14)
\]

\[
C_{eq} = C_1 + C'_2 + C'_{12} \quad (2.15)
\]
It can be seen that the resonant frequency is limited by equivalent capacitance and inductance of the transformer circuit and also the choice of external resonant capacitor $C_2$ is a flexible value to design the optimal operating conditions of the coreless PCB transformer.

2.4.2.1 Energy Efficiency

Since there is no magnetic core loss, the power dissipation of the transformer is dominated by winding loss:

$$P_{\text{loss}} = |i_1|^2R_1 + |i_2|^2R_2$$

Where $R_1$ and $R_2$ are the ac winding resistance of the primary and secondary windings, respectively which are functions of the frequency due the skin effect.

Input power of the transformer is given by:

$$P_{\text{in}} = \left| \frac{V_p}{Z_{\text{in}}} \right|^2 \text{Re}\{Z_{\text{in}}\}$$  \hspace{1cm} (2.16)$$

Where $V_p$ is the primary voltage and $Z_{\text{in}}$ is the input impedance of the transformer. The output power of the transformer is:

$$P_{\text{out}} = \left| \frac{V_s}{R_L} \right|^2 = \left| \frac{G(s) \cdot V_p}{R_L} \right|^2$$

Where $V_s$ is the secondary voltage and $G(s)$ is the voltage gain, $V_s/V_p$, of the transformer in s-domain. Hence, energy efficiency of the transformer is given by:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%$$

$$= \frac{\left| G(s) \right|^2 \left| V_p \right|^2}{\left| V_p \right|^2 \text{Re}\{Z_{\text{in}}\}} \times 100\%$$

$$= \frac{\left| G(s) \right|^2 \left| Z_{\text{in}} \right|^2}{R_L \text{Re}\{Z_{\text{in}}\}} \times 100\%$$  \hspace{1cm} (2.18)$$
2.4.2.2 Voltage Gain and Input Impedance

Voltage gain $V_s/V_p$ and input impedance $Z_{in}$ of the coreless PCB transformer can be obtained based on the high frequency equivalent circuit of the transformer illustrated in Figure 4-2.

The parameters values referred to the primary of the transformer re given by:

$$R'_{2} = n^2 R_2$$  \hspace{1cm} (2.19)
$$L'_{0k2} = n^2 L_{0k2}$$  \hspace{1cm} (2.20)
$$R'_L = n^2 R'_L$$  \hspace{1cm} (2.21)
$$C''_2 = \frac{1}{n^2} C_2 + \frac{1-n}{n^2} C_{12}$$  \hspace{1cm} (2.22)
$$C''_1 = C_1 + \frac{n-1}{n} C_{12}$$  \hspace{1cm} (2.23)
$$C'_{12} = \frac{1}{n} C_{12}$$  \hspace{1cm} (2.24)
$$V'_s = nV_s$$  \hspace{1cm} (2.25)

Here, $C''_2$ is sum of the external resonant capacitance and mutual capacitance between two windings referred to the primary windings. The capacitance of the secondary winding can be ignored in the high frequency model because it is much smaller than the externally added capacitance. Parameter $C''_1$ is combination of primary capacitance and mutual capacitance between two windings. The mutual capacitance $C_{12}$ due to the electrical coupling between the primary and secondary windings can approximately be measured directly by shorting both primary and secondary sides [64]. In order to achieve good EMI, it is required to maintain mutual capacitance as small as possible.

The voltage gain of the coreless transformer can be expressed as follows [65]:

$$H(f) = \frac{V_s}{V_p} = \frac{1}{X_1} + j(2\pi f)C'_{12} Y_1$$  \hspace{1cm} (2.26)

$$Z_{in} = \frac{1}{sC'_{12} \left((1-n)\frac{V_s}{V_p}\right) + \frac{(1-A)}{X_1} + sC'_1}$$  \hspace{1cm} (2.27)

Where

$$X_1 = R_1 + sL_{ik1}$$
$$X_2 = R_2 + sRL'_{4k2}$$
It can be seen from above equations that resonant capacitor $C_2$ is used to design the optimal operating conditions of the coreless PCB transformer such as increased gain, input impedance, and efficiency.

### 2.5 Summary
The elimination of switching loss makes resonant converters acceptable candidates for high frequency power conversion. Merits and demerits of the conventional resonant dc-dc converters including series resonant converters, parallel resonant converters, and series-parallel resonant converters were discussed in this chapter. In order to achieve high frequency operation in converters while keeping the efficiency high, the use of resonant RF amplifiers (inverters) combined with a rectifier is required. Then, a number of the resonant RF amplifiers were discussed which included Class E, class EF₂, and class DE topologies. The advantages and disadvantages of all the topologies were presented in detail. As mentioned in this chapter, class DE converters have great advantages over the other topologies. A class DE inverter is the topology with ZVS condition during switching cycle as well as the lowest stress on the switches due to the direct connection to the input voltage.

Furthermore, since magnetic components play prominent role in high frequency applications, a comparison of all different transformer structures was made based on the core and copper losses, ease of manufacturing, increased reliability, and thermal characteristic. The coreless PCB transformers are the best candidate to cover all above mentioned advantages. Because they do not need space to accommodate the magnetic core and have the advantages of low costs,
high power density, low profile, no magnetic core loss, and ease of implementing. In this chapter, a brief introduction to coreless PCB transformers including the advantages and misconceptions was provided.
Chapter 3

High Frequency Class DE Resonant Converter

As discussed previously, resonant converter topologies with soft switching techniques, ZVS and ZCS, result in very low switching losses and hence allow the converters to operate at higher switching frequencies. For high frequency applications, resonant radio frequency (RF) power amplifiers (inverters) combined with a rectifier have demonstrated the effective way to maintain high efficiencies at high power densities. The purpose of a radio frequency power amplifier is to convert the dc supply voltage into a sinusoidal signal having low harmonics with reasonable efficiency. RF power amplifiers are classified by the operation of their power transistors. Class E, class F, and Class DE are examples of RF power amplifiers conventionally used in high frequency power conversion by operating the transistor as a switch rather than a controlled current source. A class DE inverter is the topology with ZVS condition during switching cycle as well as the lowest stress on the switches due to the direct connection to the input voltage. Therefore, this thesis addresses a class DE design for a 10MHz, 150W output power, 20 V/400 V input/ output voltage converter. Design and high frequency analysis for both inverter and rectifier of an isolated step-up class DE converter are presented in this chapter. During the design, required characteristics of the matching network including series resonant tank and high frequency transformer are revealed. The effective output/input impedances of the inverter/rectifier are calculated to be used for designing the matching network including series resonant tank and high frequency transformer. Simulation results show a peak efficiency of 92.2% at 150 W output power.

3.1 Analysis and Design of the Class DE Resonant Converter

Class DE resonant converters shown in Figure 3-1, are often designed in three parts, a class DE resonant inverter converting the dc input voltage to a sinusoidal output current, a class DE rectifier rectifying the ac current to a dc output voltage, and a matching network placed between
the inverter and rectifier. The matching network that is used to provide a combination of impedance matching, isolation and voltage transformation via a transformer.

![Figure 3-1: Structure of the Class DE DC-DC converter](image)

3.1.1 Conventional Analysis of Series Resonant Converter

In conventional analysis of the resonant converter shown in Figure 3-2-a, although two stages, inverter and rectifier, are designed individually, the design of the inverter is dependent on the input impedance of the rectifier. Therefore, the first step is to design the rectifier for a given load and then design the inverter for the given rectifier input impedance [73].

![Figure 3-2: Schematic of the series resonant converter for conventional analysis, (a) DC-DC Converter, (b) Inverter, (c) Rectifier](image)

For the conventional analysis, it is supposed that the voltage $v_1$ in Figure 3-2-b and voltage $v_2$ in Figure 3-2-c have square waveforms and current $i_1$ is sinusoidal. Since a resonant circuit is connected between the inverter and the load, it can be assumed that the current harmonics in the series resonant circuit are very small. Therefore, in analysis of the converter the fundamental equivalent circuit is only considered. The operating waveforms of the converter are given in...
Figure 3-3. In this figure, $v_{gS1}$ and $v_{gS2}$ represent the gate signal applied to switch $S_1$ and $S_2$ respectively.

![Operating waveforms of the series resonant converter for conventional analysis](image)

Figure 3-3: Operating waveforms of the series resonant converter for conventional analysis

Fundamental voltages and currents of the converter are given by

\[
v_1 = \frac{4}{\pi} V_i \sum \frac{1}{n} \sin n\omega t \quad V_{1-\text{peak}} = \frac{2}{\pi} V_i, \quad V_{1-\text{rms}} = \frac{\sqrt{2}}{\pi} V_i \tag{3.1}
\]

\[
I_1 = \frac{V_1}{Z_1} \quad I_{1-\text{rms}} = \frac{V_{1-\text{rms}}}{Z_1} \tag{3.2}
\]

\[
v_2 = \frac{4}{\pi} V_o \sum \frac{1}{n} \sin n\omega t \quad V_{2-\text{peak}} = \frac{2}{\pi} V_o, \quad V_{2-\text{rms}} = \frac{\sqrt{2}}{\pi} V_o \tag{3.3}
\]

\[
I_o = \frac{1}{2\pi} \int_0^{2\pi} I_{2-\text{rms}} \sin \omega t \quad I_o = \frac{I_{2-\text{peak}}}{\pi}, \quad I_o = \frac{\sqrt{2}I_{2-\text{rms}}}{\pi} \tag{3.4}
\]

As it can be seen in Figure 3-4, for the fundamental circuit, the non-linear effects of the rectification stage are referred to the transformer primary and modeled by an equivalent ac resistance defined by (3.5) and (3.6).
The equivalent ac resistance of the rectifier seen from the primary is given by

\[ R_{ac,\text{prim}} = \frac{2}{N^2 \pi^2} R_L \]  

(3.6)

The resonant frequency of the tank is defined by (3.).

\[ \omega_r = \frac{1}{\sqrt{L_r C_r}} \]  

(3.7)

The quality factor and the relative operating frequency are given by (3.8) and (3.9), respectively. Where \( \omega_0 \) is the radian switching frequency.

\[ Q = \frac{L_r \omega_r}{R_{ac}} \]  

(3.8)

\[ \omega = \frac{\omega_0}{\omega_r} \]  

(3.9)

The converter gain is related to the resonant tank and given by:

\[ V_{gain} = \frac{V_{ac}}{R_{ac} \left( 1 + j (X_L - X_C) \right) R_{ac}} = \frac{1}{1 + j Q \left( \omega - \frac{1}{\omega} \right)} \]  

(3.10)

\[ V_1 = \frac{2}{\pi} V_i \]  

\[ V_{ac} = \frac{2}{N\pi} V_o \]
$$\frac{V_o}{V_i} = \frac{N}{1 + jQ \left( \omega - \frac{1}{\omega} \right)}$$

(3.11)

3.1.2 High Frequency Analysis of the Class DE Resonant Converter

Since the parasitic components introduced by the devices, packages and interconnections are part of the design parameters, they have a significant impact on the design of the overall converter. An example is the output capacitance of the switch device that must be charged and discharged every switching cycle, dissipating energy and thus reducing efficiency. This effect worsens at higher switching frequencies. Therefore in high frequency analysis, the output capacitances of the switches as well as diodes are considered.

The class DE resonant converter shown in Figure 3-5 is designed in three stages: inverter stage, matching network including resonant tank and transformer, and rectifier stages. The resonant tank components such as the inductor $L_r$ and capacitor $C_r$, contribute in shaping the converter waveforms to achieve ZVS condition. Generally, in the case of ZVS converters, the undesirable parasitic elements of the circuit can prove to be useful in achieving the ZVS condition by forming a resonant tank circuit. In this case, $L_r$ includes the transformer leakage inductance, the parasitic wire inductance and probably the external resonant inductor. The output capacitance of the MOSFET, the winding capacitance of the transformer and other parasitic capacitances are considered in the resonant circuit. The structure of the class DE is similar to the structure of the half bridge series resonant converter, but class DE converter operates in a specific operating point which guarantees ZVS and ZCS. At higher frequencies the required dead time to charge and discharge switches output capacitors are comparable with switching period and consequently the inverter and rectifier waveforms are not square waves anymore. Therefore more accurate analysis is required.

The sinusoidal output current $i_1$ swings the voltage from one dc rail to the other during dead time when both switches are open. In high frequency analysis, each stage is designed independently.
3.1.2.1 Class DE Inverter Analysis

Figure 3-6 illustrates the topology of a class DE inverter. It consists of two switches $S_1, S_2$ two shunt capacitances $C_{s1}, C_{s2}$ and a matching network including series resonant tank and transformer. An ideal switch, a diode and a capacitor model each of the two switching devices. The matching network forces the inverter's output current to be almost sinusoidal. The dc input voltage is shown as a center tapped supply to analyze the system more convenient.

The waveforms of the class DE inverter are shown in Figure 3-7. The switch on-duty ratio of the class DE inverter can have any value from zero to somewhat less than 0.5 due to the required dead time [74]. The switches $S_1$ and $S_2$ are driven as shown in Figure 3-7. The driving pattern generates a dead time during the period when one switch has turned off and before the other switch has turned on. In fact, the operation of a class DE inverter has two dead time intervals in one period. During the dead time, the output current $i_1$ charges one shunt capacitance and discharges the other. The inverter output voltage $v_1$ rises from the negative rail to the positive
one at \( t_0 \). Diode \( D_{s1} \) prevents \( v_1 \) from rising further and \( S_1 \) is turned on with ZVS at \( t_0 \). The other half cycle is similar.

Due to device parasitic capacitance, the inverter output voltage, \( v_1 \), is not square and due to the leakage inductance, the current \( i_1 \) lags the voltage \( v_1 \) which allows switches to be turned on with zero voltage.

Due to device parasitic capacitance, the inverter output voltage, \( v_1 \), is not square and due to the leakage inductance, the current \( i_1 \) lags the voltage \( v_1 \) which allows switches to be turned on with zero voltage.

Figure 3-7: Waveforms of the Class DE inverter

The dc input voltage is considered to be \( \pm v_i/2 \) and the inverter output current to be:

\[
i_1(t) = I_{1pk} \sin(\omega t - \phi), \quad \phi \in [0, \pi]
\]  (3.12)

Where \( \omega / 2\pi \) is the switching frequency and \( \phi \) is a phase angle. \( I_{1pk} \) and \( \phi \) both depend on the matching network and the load impedance. If each switch operates with a duty factor \( D_s \in [0, 1/2] \), then

\[
D_s = \frac{(\pi - \phi)}{2\pi}
\]  (3.13)

In order to swing the output voltage from \( -V_i/2 \) to \( +V_i/2 \), the switch capacitances \( C_{s1} \) should be discharged and \( C_{s2} \) should be charged to \( V_i \).

\[
Q_{Cs1} = -C_{s1}V_i = \int_0^{t_0} i_{s1}(t)dt
\]

\[
Q_{Cs2} = C_{s2}V_i = \int_0^{t_0} i_{s2}(t)dt
\]
\[ v_{cs1} + v_{cs2} = v_i , \quad \frac{dv_{cs1}}{dt} + \frac{dv_{cs2}}{dt} = 0 , \quad \frac{dv_{cs1}}{dt} = \frac{i_{cs1}}{C_{s1}} , \quad \frac{dv_{cs2}}{dt} = \frac{i_{cs2}}{C_{s2}} \]

\[ C_{s1} = C_{s2} \Rightarrow i_{cs1} = -i_{cs2} = \frac{1}{2} i_1 \]

\[ Q_t = Q_{cs1} - Q_{cs2} = -2C_s V_i = \int_0^{t_0} i_1(t) dt , \quad t_0 = \frac{\phi}{\omega} \quad (3.14) \]

So the peak value of inverter output current can be obtained:

\[ 2C_s V_i = \int_0^{t_0} -I_{pk} \sin(\omega t - \phi) dt = \int_0^{\phi/\omega} -I_{pk} \sin(\omega t - \phi) dt \]

\[ 2C_s V_i = -I_{pk} \left( \frac{\phi}{\omega} \cos(\omega t - \phi) \right) = \frac{I_{pk}}{\omega} (1 - \cos \phi) \]

\[ I_{pk} = \frac{2\omega C_s V_i}{1 - \cos \phi} \quad (3.15) \]

It can be noted that a small phase angle \( \phi \) implies a large peak current. The inverter output voltage can be calculated by substituting \( i_1 \) into

\[ \frac{dv_1}{dt} = -i_2/2C_s \]

\[ v_2(t) = \int_0^t -I_{pk} \sin(\omega t - \phi) dt - \frac{V_i}{2} \]

\[ = \frac{I_{pk}}{2\omega C_s} (\cos(\omega t - \phi) - \cos \phi) - \frac{V_i}{2} \]

\[ = \frac{2\omega C_s V_i}{1 - \cos \phi} \times \frac{1}{2\omega C_s} (\cos(\omega t - \phi) - \cos \phi) - \frac{V_i}{2} \]

\[ v_2(t) = V_i - 2 \cos(\omega t - \phi) - (1 + \cos \phi) \]

\[ 2(1 - \cos \phi) , \quad t \in [0, t_0] \quad (3.16) \]

It is useful to calculate the output impedance of the inverter for designing the matching network.

To calculate the effective load impedance seen by the inverter \( Z_1 = V_1/I_1 \), it is required to find the fundamental components of \( v_2(t) \) and \( i_2(t) \). As the high Q matching network rejects harmonics, only the fundamental components need to be considered. Current \( i_1(t) \) is represented by a phasor \( I_1 \), and the fundamental component of voltage \( v_2(t) \) is represented by another phasor, \( V_1 \). The fundamental components of \( v_2(t) \) and \( i_2(t) \) can be found by Fourier analysis.
For a periodic quantity \( a(t) = f_w(t) \) with period T, its fundamental component can be expressed as the phasor \( A = \frac{2}{T} \int_0^T f_w(t)e^{-j\omega t} dt \). Since \( v_1(t) \) has similar positive and negative half cycles, the phasor can be expressed for half cycle.

\[
V_1 = \frac{2\omega}{\pi} \left( \int_0^{\phi/\omega} v_1(t)e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} V_i e^{-j\omega t} dt \right)
\]

\[
V_1 = \frac{2\omega}{\pi} \left( \int_0^{\phi/\omega} V_i \frac{2 \cos(\omega t - \phi) - (1 + \cos \phi)}{2(1 - \cos \phi)} e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} V_i \frac{1 - \cos \phi}{1 - \cos \phi} e^{-j\omega t} dt \right)
\]

From 1

\[
\frac{2}{1 - \cos \phi} \int_0^{\phi/\omega} e^{-j\omega t \cos(\omega t - \phi)} dt
\]

\[
= \frac{2}{1 - \cos \phi} \int_0^{\phi/\omega} (\cos \omega t - j \sin \omega t) \cos(\omega t - \phi) dt
\]

\[
= \frac{1}{1 - \cos \phi} \left( \frac{2}{2\omega} \sin \phi + \frac{\phi}{\omega} \cos \phi - j \frac{\phi}{\omega} \sin \phi \right)
\]

From 2

\[
\frac{-(1 + \cos \phi)}{1 - \cos \phi} \int_0^{\phi/\omega} e^{-j\omega t} dt = \frac{(1 + \cos \phi)}{1 - \cos \phi} \frac{1}{j\omega} (e^{-j\phi} - 1)
\]

From 3

\[
\int_{\phi/\omega}^{\pi/\omega} e^{-j\omega t} dt = \frac{1}{j\omega} (e^{-j\phi} + 1)
\]

1+2+3

\[
V_1 = V_i \frac{\phi \cos \phi - \sin \phi - j \phi \sin \phi}{\pi(1 - \cos \phi)} \tag{3.17}
\]

Similarly, \( i_1(t) \) can be obtained by

\[
i_1 = \frac{2\omega}{\pi} \int_0^{\pi/\omega} i_{1pk} \sin(\omega t - \phi) e^{-j\omega t} dt
\]
The effective impedance seen by the inverter is

\[ Z_1 = \frac{V_1}{I_1} \]

\[ Z_1 = \frac{\sin \phi^2}{\pi} + j \frac{\phi - \sin \phi \cos \phi}{\pi} \]

(3.19)

Impedance \( Z_1 \) is normalized by multiplying by \( 2\omega C_s \) to give the dimensionless quantities:

\[ R'_1 = \frac{\sin \phi^2}{\pi} \]

\[ X'_1 = \frac{\phi - \sin \phi \cos \phi}{\pi} \]

(3.20) (3.21)

If \( Z_1 \) is too large, \( I_{1pk} \) will be less than the critical value. Then \( v_1(t) \) will peak before it reaches \( V_i/2 \) and fall back, so ZVS will not be achieved. With small values of \( Z_1 \), \( I_{1pk} \) will be greater than the critical value. The transitions can achieve ZVS (\( dv/dt \neq 0 \)). Inverter output voltage, \( v_1(t) \) reaches \( V_i/2 \) while \( i_1(t) \) is still negative, forcing diode \( D_{s1} \) to conduct. The diode comes out of conduction when \( i_1(t) \) reaches zero. In the case of proper Class DE operation, the value of lag current \( i_1(t) \) is designed such that after discharging the device output capacitor, switch \( S_1 \) turns on under ZVS conditions. In fact, it does not let the diode to conduct. \( v_1(t) \) stays close to \( V_i/2 \) for some time (\( dv/dt = 0 \)).

### 3.1.2.2 Class DE Rectifier Analysis

For the output voltage of 400 V, class DE rectifier shown in Figure 3-8 is suitable as diodes are connected directly to the output and the voltage across them is limited to the output voltage.
Furthermore, the class DE rectifier is not included any inductor and hence offers a much higher power density as the inductor is normally the biggest component.

It is assumed that the rectifier is fed by a sinusoidal current, diodes $D_1$ and $D_2$ are ideal, two capacitances $C_d$ are ideal and linear, and two output capacitances $C_{o1}$ and $C_{o2}$ are infinite. By symmetry, an equal voltage $V_o/2$ is applied on each output capacitance. The dc output load is equal to 1 KΩ.

![Figure 3-8: Half bridge class DE rectifier circuit](image)

According to the waveforms of the rectifier shown in Figure 3-9, at $t = 0$, the input current $i_2$ becomes positive and $D_2$ which was previously conducting, starts to block under zero voltage switching condition. Therefore, the current $i_2$ charges the total diode capacitance $2C_d$. At $t = 0$, $dv_2/dt = 0$ which satisfies the class E switching conditions. Thus diode capacitances and charge storage do not have a deleterious effect. The input voltage $v_2$, rises from the negative output rail to the positive one, and reaches to $V_o/2$ at $t_0$. Then $D_1$ starts to conduct and keeps conducting until $i_2$ changes sign again. The other half cycle is similar. From Figure 3-9 it can be seen that the duty factor of each diode is $D_d = \frac{(\pi - \phi)}{2\pi}$

Generally, the diode $D_1$ and $D_2$ are turned on and off at zero voltage (or diode threshold voltage) and low $dv/dt$. Since the diodes are turned on and off at zero voltage and low $dv/dt$, the diode switching losses are small. In addition, the diodes $D_1$ and $D_2$ are turned off at the instant when the diode currents become zero, which makes the diode reverse recovery currents to be
very small. Moreover, the maximum value of the diode reverse voltages is equal to the output voltage.

![Diagram of class DE rectifier](image)

Figure 3-9: Waveforms of class DE rectifier

Let the input current of rectifier to be \( i_2(t) = I_{2pk} \sin(\omega t) \), and the voltage across each output capacitor \( C_0 \), to be \( V_0/2 \).

Voltage \( v_2 \) is found by using this fact that \( v_2(t) = -\frac{V_0}{2} \), and integrating the equation:

\[
\begin{align*}
\frac{dv_2}{dt} &= \frac{i_2}{2C_d} \\
v_2(t) &= \frac{i_2}{2C_d} \int_0^t i_2(t)\,dt - \frac{V_0}{2} \\
v_2(t) &= \frac{I_{2pk}}{2\omega C_d} (1 - \cos \omega t) - \frac{V_0}{2} 
\end{align*}
\]

(3.22)

At \( t=0 \), \( dv_2/dt = i_2/2C_d = 0 \) which is class E transition. The transition ends at \( t = t_0 \), when \( v_2(t_0) = V_0/2 \). From 8 it can be calculated

\[
\begin{align*}
\frac{V_0}{2} &= \frac{I_{2pk}}{2\omega C_d} (1 - \cos \omega t_0) - \frac{V_0}{2} \\
\phi &= \omega t_0 \\
\cos \phi &= 1 - \frac{2\omega C_d V_0}{I_{2pk}} 
\end{align*}
\]

(3.23)

To design the matching network it is required to obtain the effective input impedance of the rectifier. The phasor of \( v_2(t) \) and \( i_2(t) \) are calculated by using Fourier analysis as done for the inverter.
\[ v_z(t) = \frac{I_{2pk}}{2\omega C_d} \left( 1 - \cos \omega t \right) - \frac{V_o}{2} \]

\[ i_z(t) = I_{2pk} \sin(\omega t) \]

Fundamental components of \( v_z(t) \) and \( i_z(t) \) can be found by Fourier analysis

\[ V_2 = \frac{2\omega}{\pi} \left( \int_0^{\phi/\omega} v_z(t) e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} \frac{V_o}{2} e^{-j\omega t} dt \right) \]

\[ = \frac{2\omega}{\pi} \left( \int_0^{\phi/\omega} \frac{I_{2pk}}{2\omega C_d} (1 - \cos \omega t) e^{-j\omega t} dt - \int_0^{\phi/\omega} \frac{V_o}{2} e^{-j\omega t} dt + \int_{\phi/\omega}^{\pi/\omega} \frac{V_o}{2} e^{-j\omega t} dt \right) \]

From 1

\[ \frac{I_{2pk}}{2\omega C_d} \int_0^{\phi/\omega} (1 - \cos \omega t) (\cos \omega t - j \sin \omega t) dt \]

\[ = \frac{I_{2pk}}{2\omega C_d} \int_0^{\phi/\omega} (\cos \omega t - j \sin \omega t - \cos^2 \omega t + j \sin \omega t \cos \omega t) dt \]

\[ = \frac{I_{2pk}}{2\omega C_d} \int_0^{\phi/\omega} (\cos \omega t - j \sin \omega t - \frac{1}{2} - \frac{1}{4} \cos 2\omega t + \frac{j}{2} \sin 2\omega t) dt \]

\[ = \frac{I_{2pk}}{2\omega C_d} \left( \frac{1}{\omega} \sin \omega t + \frac{j}{\omega} \cos \omega t - \frac{1}{2} - \frac{1}{4\omega} \sin 2\omega t - \frac{j}{4\omega} \cos 2\omega t \right) \]

\[ = \frac{1}{\omega} \times \frac{I_{2pk}}{2\omega C_d} \left( \sin \phi + j \cos \phi - \frac{\phi}{2} - \frac{\sin \phi \cos \phi}{2} + \frac{j \sin^2 \phi}{2} - j \right) \]

From 2

\[ \frac{V_o}{2} \times \frac{-1}{j\omega} (e^{-j\omega t}) = \frac{-V_o}{2j\omega} (e^{-j\phi} - 1) \]

From 3

\[ \frac{V_o}{2} \times \frac{-1}{j\omega} (e^{-j\omega t}) = \frac{-V_o}{2j\omega} (e^{-j\pi} - e^{-j\phi}) \]

Finally phasor \( V_2 \) is calculated from 1, 2, and 3 and knowing

\[ \cos \phi = 1 - \frac{2\omega C_d V_o}{I_{2pk}} \]
\[ I_{zpk} = \frac{2\omega C_d V_o}{1 - \cos \phi} \]

\[ V_2 = V_o \frac{\sin \phi \cos \phi - \phi - j\sin^2 \phi}{\pi (1 - \cos \phi)} \]  \hspace{1cm} (3.24)

For obtaining the current phasor:

\[ I_z = \frac{2\omega}{\pi} \int_0^{\pi/\omega} I_{zpk} \sin(\omega t)e^{-j\omega t} dt \]

\[ = \frac{2\omega}{\pi} I_{zpk} \int_0^{\pi/\omega} \sin(\omega t)(\cos \omega t - j \sin \omega t) dt \]

\[ = \frac{2\omega}{\pi} I_{zpk} \int_0^{\pi/\omega} (\sin \omega t \cos \omega t - j \sin^2 \omega t) \ dt \]

\[ = \frac{2\omega}{\pi} I_{zpk} \int_0^{\pi/\omega} \left( \frac{1}{2} \sin 2\omega t - j + j \cos 2\omega t \right) dt \]

\[ = \frac{2\omega}{\pi} I_{zpk} \int_0^{\pi/\omega} \left( \frac{1}{4} \cos 2\omega t - j \frac{1}{2} t + \frac{j}{4\omega} \sin 2\omega t \right) dt \]

\[ I_z = -j I_{zpk} \]  \hspace{1cm} (3.25)

Substituting (10) and (11) into \( Z_2 = V_2/I_z \)

\[ Z_2 = \frac{\sin^2 \phi}{\pi 2\omega C_d} + j \frac{\sin \phi \cos \phi - \phi}{\pi 2\omega C_d} \]  \hspace{1cm} (3.26)

Then the normalized (to \( 2\omega C_d \)) resistance and reactance of the rectifier are

\[ R'_2 = \frac{\sin^2 \phi}{\pi} \]  \hspace{1cm} (3.27)

\[ X'_2 = \frac{\sin \phi \cos \phi - \phi}{\pi} \]  \hspace{1cm} (3.28)

In the following equations, the important quantities will be calculated.
The charge flowing through $D_1$ into the upper output capacitor $C_{o1}$ during a cycle is

$$Q_{D1} = \int_{\pi/\omega}^{\phi/\omega} i_z(t)dt$$

$$= \int_{\phi/\omega}^{\pi/\omega} I_{2pk} \sin(\omega t)dt$$

$$= \frac{I_{2pk}}{\omega} (1 + \cos \phi), \quad \text{where} \quad \cos \phi = 1 - \frac{2\omega C_d V_o}{I_{2pk}}$$

$$Q_{D1} = \frac{2I_{2pk}}{\omega} - 2C_d V_o \quad (3.29)$$

Additional charge flows through the diode capacitances during the interval $[0, \phi/\omega]$. Also equal charge amount flows out during the interval $[\pi/\omega, (\pi+\phi)/\omega]$ and they cancel each other out.

The charge flowing via $R_L$ during a cycle is obtained from

$$Q_{RL} = \int_{0}^{2\pi/\omega} i_o(t)dt, \quad I_o = \frac{V_o}{R_L}$$

$$Q_{RL} = \frac{2\pi V_o}{\omega R_L} \quad (3.30)$$

In the steady state, $Q_{D1} = Q_{RL}$

$$\frac{2I_{2pk}}{\omega} - 2C_d V_o = \frac{2\pi V_o}{\omega R_L}$$

$$I_{2pk} = V_o \left( \frac{\pi}{R_L} + \omega C_d \right) \quad (3.31)$$

Substituting (3.31) into (3.23) and using the equation of $\cos \phi^2 + \sin \phi^2 = 1$,

$$\cos \phi = \frac{\pi - \omega C_d R_L}{\pi + \omega C_d R_L} \quad (3.32)$$

$$\sin \phi = \frac{\sqrt{4\pi \omega C_d R_L}}{\pi + \omega C_d R_L} \quad (3.33)$$

So the resistive parameters of rectifier input impedance is given by:

$$R'_2 = \frac{\sin \phi^2}{\pi}, \quad \sin \phi = \frac{\sqrt{4\pi \omega C_d R_L}}{\pi + \omega C_d R_L}$$

$$R'_2 = \frac{8R_L'}{(\pi + R_L')^2}, \quad R'_L = 2\omega C_d R_L \quad (3.34)$$
Finally, from (3.32) and (3.23) the total output voltage can be found as

\[ V_o = \frac{I_{2pk} R_L}{\pi + \omega C_d R_L} \]  

(3.35)

For \( V_o = 400 \, V \), \( I_{2pk} \) is calculated to 1.5A.

### 3.2 Components Selection

The design procedure of class DE converter requires careful components selection. The device selected for the main switching element of the inverter stage is a Gallium nitride (GaN) with specifications shown in the Table 3-1. GaN devices, which have been first developed for RF applications, have received attention in power electronics [75] due to the device properties compared to silicon power device technologies. This semiconductor device offers the required characteristics needed to operate at high frequencies such as faster switching speed and reduced on-state resistance, which are often quantified by means of the \( Q_g \times R_{dson} \). The benefits of using the GaN FETs compared to the Si MOSFETs in terms of their performance parameters discussed in [76] is that in high frequency applications, the reduction in Output capacitance can decrease circulating energy and commutation time required to achieve ZVS, thus increasing the effective power delivery intervals and improving overall efficiency. In addition, the reduction in Gate capacitance provided by the GaN FETs results in faster switching speeds, at reduced driving voltages, which provide reduced gate drive losses. Putting GaN FETs to work in high frequency applications can help push the frequency without sacrificing converter performance.

Therefore GaN FETs provide promising results at higher switching frequencies and consequently the energy efficiency of the converter can be improved.

<table>
<thead>
<tr>
<th>Table 3-1: GaN device specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
</tr>
</tbody>
</table>
| eGaN® FET | \( V_{GS} = 5V \)  
\( I_D = 31A \) | \( V_{DS} = 30V \)  
\( V_{GS} = 0V \) | \( V_{DS} = 30V \)  
\( I_D = 31A \) |
To design and simulate the rest of the converter the rectifier diodes have to be chosen as well. The C3D1P7060Q schottky SiC diodes are chosen as they have low forward voltage drop, 1.5 V. The breakdown voltage of these diodes are 600 V.

In order to select the GaN switch and SiC diodes, besides desired devises specifications, it is required to choose those GaN switches and SiC diodes that have the SPICE (Simulation Program with Integrated Circuit Emphasis) model. By importing the accurate model of switches and diodes into the software, the more precise results can be obtained.

### 3.3 Simulation Results of the Class DE Resonant Converter

The class DE converter, designed to meet the specifications listed in Table 3-2, is simulated in ADS (high frequency software) and LTSpice simulations with detailed SPICE models of the GaN chips, EPC2020, and an ideal transformer. Analysis, design, and measured s-parameter model of the multilayer coreless PCB transformer will be studied in the next chapter.

<table>
<thead>
<tr>
<th>f_s</th>
<th>V_{in}</th>
<th>V_{out}</th>
<th>P_{out}</th>
<th>R_L</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>20 V</td>
<td>400 V</td>
<td>150 W</td>
<td>1 KΩ</td>
</tr>
</tbody>
</table>

The circuit with rectifier, inverter, and matching network including resonant tank and ideal transformer are shown in Figure 3-10. The SPICE model of GaN switches (EPC2020) and SiC diodes (C3D1P7060Q) have been imported to the schematic. In this schematic an ideal transformer model has been used.
Based on the equations from section 3.1.2, the values of all parameters have been calculated which show a good agreement with simulation results. From (3-19) and (3-26), the effective impedances of inverter and rectifier can be obtained respectively.

\[
Z_1 = \frac{\sin \phi^2}{\pi 2\omega C_s} + j \frac{\phi - \sin \phi \cos \phi}{\pi 2\omega C_s}, \quad Z_1 = 0.4 + j0.12 \tag{3.36}
\]

\[
Z_2 = \frac{\sin \phi^2}{\pi 2\omega C_d} + j \frac{\sin \phi \cos \phi - \phi}{\pi 2\omega C_d}, \quad Z_2 = 162.16 - j76.866 \tag{3.37}
\]

The effective output/input impedance of the inverter/rectifier can be used to determine the values of series resonant tank parameters and also turn’s ratio of the required transformer.

Based on this fact that these two inverter’s and rectifier’s impedances should be matched by using the matching network including resonant tank between them, the value of resonant tank can be calculated to provide the ZVS conditions for the inverter as shown in Figure 3-11. The series resonant tank parameters are not able to compensate the real part of rectifier. So a turn’s ratio of N equals to 20 is required to transfer the rectifier real part (162.16Ω) into the inverter real part (0.4Ω). In addition, to compensate the imaginary part of the rectifier’s impedance (\(-j76.866/N^2\)), minimum value of 5nH is obtained for the series resonant inductor.

A high Q resonant tank forces the inverter’s output current waveform to be almost sinusoidal, but results in higher voltage stress and conduction loss as the reactive component value becomes larger. I this converter design, Q factor of 1.7 is selected. Appropriate values can be found through straight parametric search using a simulation tool such as LTSpice. The obtained
resonant inductance and capacitance of the circuit are 11nH and 50nF respectively. In chapter 4, it is mentioned that the primary leakage inductance of the transformer is around 11nH, which is sufficient to meet the ZVS condition.

A series resonant inductor \(L_r\) of 11 nH and a series capacitor \(C_r\) of 50 nF are utilized in the resonant tank and therefore resonant frequency of the converter is 6.7 MHz that is obtained as follows:
\[ f_r = \frac{1}{2\pi L_r C_r} \]  
\[ (3.38) \]

The characteristic impedance "Z_r" of the circuit is given as

\[ Z_r = \frac{L_r}{\sqrt{C_r}} \]  
\[ (3.39) \]

The quality factor "Q_r" of the converter is obtained from the characteristic impedance "Z_r" and load resistance "R_L"

\[ Q_r = \frac{Z_r}{R_L} \]  
\[ (3.40) \]

As ZVS is preferred compared to ZCS, the optimal operating condition of the converter is obtained above resonant frequency "f_r" of tank circuit. Therefore, the switching frequency of the converter should be greater than 6.7 MHz. In this region, the converter is ensured to be operated in ZVS conditions and hence the turn-on losses in switching devices get minimized that increases the overall energy efficiency of the converter.

### 3.4 Effect of Parasitic Components on the Circuit Function

Since parasitic components play a significant role at higher frequencies, careful component selection and PCB layout design is essential. In order to calculate the inverter output impedance and rectifier input impedance, it is critical to consider all inductive parasitics.

In this regard, semiconductor packaging technology has advanced to minimize the parasitic inductance of the connection from the die to the outside world. Therefore, in this design the GaNFET switch in passivated die form is selected. In this case, the inductance is at its absolute minimum possible value since the gate, source, and drain are soldered to the PCB and; thereby eliminating all bond wires.

On the other hand, the printed circuit board should be designed carefully to minimize parasitic inductance. As shown in Figure 3-13, the PCB layout parasitic inductance of the inverter and rectifier have been simulated by using EM model and Harmonic Balance simulator in ADS. The simulated parasitic inductance of the inverter layout is about 5% of the series resonant inductor. Hence the effect of this parasitic inductance on the circuit function is very small and
can be ignored in the analysis. In the same way, the rectifier parasitic inductance does not impact on the rectifier operation.

In order to illustrate how parasitic inductances impact the inverter function, Figure 3-14 is analyzed to calculate the currents flowing through the inductors when the lower switch turns on at \( t_{0.2868} \). In this figure \( L_{0.2869} \) includes the total inductances of the first switch current path containing PCB traces, ESL of the input capacitor \( C_{in} \). Component \( L_{0.28n0} \) is the total inductances of the second switch current path. Since the input capacitor and the resonant inductor are big enough compared to the parasitics, they are considered as voltage and current sources respectively.

Since the same switches are used in the inverter design, their parasitic capacitances are assumed to be equal. \( C_1 = C_2 \). It should be noted that these parasitic capacitances were previously
considered in impedance calculations. Before \( t_0 \), switch \( S_1 \) is off and \( S_2 \) is on, and the inverter current is flowing through \( L_2 \). The equivalent circuit at \( t_0 \) is presented in Figure 3-15 which can be solved through the Superposition principle. Where \( V_{\text{init}} \) and \( I_{\text{init}} \) represent the initial voltage and current of \( C_1 \) and \( L_2 \) respectively.

\[ V_{\text{init}} \]
\[ I_{\text{init}} \]

Figure 3-15: Superposition principles for the inverter circuit including parasitics

Circuits 1 to 4 represent equivalent circuits for each source. As it can be seen in Figure 3-15 the voltage sources have opposite directions and consequently they cancel each other out. Therefore, only circuit 3 and 4 are analyzed.
The Laplace transform of the inverter current $i_{inv}$ is given by Eq. (3.41).

$$i_{inv}(t) = I_{peak} \sin(\omega t - \phi)$$

$$I_{inv}(s) = \frac{I_{peak}(\sin(-\phi)s + \omega \cos(-\phi))}{s^2 + \omega^2} \quad (3.41)$$

$$I_{inv}(s) = I_{1_{inv}}(s) - I_{2_{inv}}(s)$$

$$I_{1_{inv}}(s) \left( sL_1 + \frac{1}{C} \right) = -I_{2_{inv}}(s) \left( sL_2 + \frac{1}{C} \right)$$

$$I_{inv}(s) = I_{1_{inv}}(s) \left( 1 + \frac{L_2}{L_1} + \frac{2}{CL_2} \right)$$

$$I_{1_{inv}}(s) = I_{inv}(s) \frac{CL_2s^2 + 1}{2 \left( \frac{(L_1 + L_2)}{2} C s^2 + 1 \right)} \quad (3.42)$$

$$I_{2_{inv}}(s) = I_{1_{inv}}(s) - I_{inv}(s) = I_{inv}(s) \frac{-CL_1s^2 + 2}{2 \left( \frac{(L_1 + L_2)}{2} C s^2 + 1 \right)}$$

$$I_{2_{inv}}(s) = I_0(s) \frac{-CL_2s^2 + 1}{2 \left( \frac{(L_1 + L_2)}{2} C s^2 + 1 \right)} \quad (3.43)$$

To simplify the equations:

$$A = \frac{CL_2}{2}, \quad B = \frac{(L_1 + L_2)}{2} C$$

$$M = I_{peak} \sin(-\phi), \quad N = \omega \cos(-\phi)$$

$$I_{1_{inv}}(s) = \frac{MS + N}{s^2 + \omega^2} \times \frac{As^2 + 1/2}{Bs^2 + 1} \quad (3.44)$$
Figure 3-17: Equivalent inverter circuit (4)

\[
i_{L2}(t) = -I_{\text{peak}} \sin(\omega t - \phi) \quad t \leq 0
\]

\[
I_{\text{init}}(0) = -I_{\text{peak}} \sin(-\phi)
\]

\[
I_{\text{init}}(s) = \frac{I_{\text{peak}} \sin(\phi)}{s}
\]

\[
I_{\text{init}}(s) = I_{1\text{init}}(s) - I_{2\text{init}}(s)
\]

\[
I_{1\text{init}}(s) \left( sL_1 + \frac{2}{Cs} \right) = -I_{2\text{init}}(s)sL_2
\]

\[
I_{\text{init}}(s) = I_{1\text{init}}(s) \left( 1 + \frac{L_2}{L_1} + \frac{2}{CL_2 s^2} \right)
\]

\[
I_{1\text{init}}(s) = I_{\text{init}}(s) \frac{CL_2 s^2}{2 \left( \frac{L_1 + L_2}{2} Cs^2 + 1 \right)}
\]

\[
I_{2\text{init}}(s) = I_{1\text{init}}(s) - I_{\text{init}}(s) = I_{\text{init}}(s) \frac{-CL_1 s^2 + 2}{2 \left( \frac{L_1 + L_2}{2} Cs^2 + 1 \right)}
\]

\[
I_{2\text{init}}(s) = I_{\text{init}}(s) \frac{CL_2 s^2}{2 \left( \frac{L_1 + L_2}{2} Cs^2 + 1 \right)}
\]

To simplify the equations:

\[
A = \frac{CL_2}{2}, \quad B = \frac{(L_1 + L_2)}{2} C
\]

\[
M = I_{\text{peak}} \sin(-\phi)
\]

\[
I_{1\text{init}}(s) = \frac{-M}{s} \times \frac{As^2}{Bs^2 + 1}
\]

\[\text{(3.48)}\]
Based on Superposition principle, the total current flowing through the $L_1$ is given by
\[ I_1(s) = I_{i_{\text{inv}}}(s) + I_{i_{\text{init}}}(s) \]

By substituting (3.44) and (3.48) into above equation:
\[ I_1(s) = \frac{Ms + N}{s^2 + \omega^2} \times \frac{As^2 + 1/2}{Bs^2 + 1} + \frac{-M}{s} \times \frac{As^2}{Bs^2 + 1} \]

Time domain equation of $L_1$ current can be obtained by using MATLAB.

\[ i_1(t) = \frac{N - 2AN \omega^2}{\omega(2B \omega^2 - 2)} \sin(\omega t) + \frac{M \omega - 2AM \omega^3}{\omega(2B \omega^2 - 2)} \cos(\omega t) \]
\[ + \frac{BN - 2AN}{\sqrt{B}(2B \omega^2 - 2)} \sin\left(t/\sqrt{B}\right) + \frac{M - 2AM \omega^2}{(2B \omega^2 - 2)} \cos\left(t/\sqrt{B}\right) \quad (3.49) \]

Where
\[ B = \frac{(L_1 + L_2)}{2} \quad C \]
\[ \omega_r = \frac{1}{\sqrt{B}} \]

Therefore, the parasitic inductor current ($L_1$) consists of two 10MHz component ($I_{low}$) as well as a high frequency component ($I_{high}$). The parasitic inductor current of $L_2$ is calculated in the same manner.

\[ i_1(t) = I_{low} \sin(\omega t + \phi_1) + I_{high} \sin(\omega_r t + \phi_2) \quad (3.50) \]

Where
\[ I_{low} = \sqrt{\left(\frac{N - 2AN \omega^2}{\omega(2B \omega^2 - 2)}\right)^2 + \left(\frac{M \omega - 2AM \omega^3}{\omega(2B \omega^2 - 2)}\right)^2} \]
\[ I_{high} = \sqrt{\left(\frac{BN - 2AN}{\sqrt{B}(2B \omega^2 - 2)}\right)^2 + \left(\frac{M - 2AM \omega^2}{(2B \omega^2 - 2)}\right)^2} \]
\[ \phi_1 = \tan^{-1}\frac{M \omega - 2AM \omega^3}{N - 2AN \omega^2} \]
\[ \phi_2 = \tan^{-1}\frac{M - 2AM \omega^2}{BN - 2AN} \]

By substituting the circuit parameters values into equation (3.50), it can be seen that there is slight difference in 10MHz components $I_{low}$ with and without parasitic inductances. In fact, the impact of these components is less than %0.1. The high frequency component which is around 200MHz will eventually be damped in the system and does not have any significant effect on the circuit function.
3.5 Loss mechanisms

The purpose of dc-dc converters is to increase or decrease the output voltage with respect to the input. The efficiency of a converter is a measure of the ratio of the output power supplied to the load with respect to the input power. Achieving high efficiency in dc-dc converters operating at high frequencies requires to keep the converter losses minimum.

3.5.1 Semiconductor Device Loss

The greatest sources of loss are in the converter switching power devices. Figure 3-18 shows the switching device equivalent circuit. This model includes effective terminal capacitances, which are device parasitics due to the physical structure.

![Figure 3-18: Simplified device model including the parasitic terminal capacitances](image)

In some cases, all device terminal capacitances ($C_{ds}$, $C_{dg}$, $C_{gs}$) can be represented by input capacitance, $C_{iss}$ and output capacitance, $C_{oss}$. As shown in Figure 3-19, each of these capacitances also includes an equivalent series resistance.

![Figure 3-19: Switching device equivalent circuit including the parasitic capacitances and resistances](image)
These device parasitic resistances and capacitances result in loss mechanisms that determine device performance at high frequency.

### 3.5.1.1 Gate Loss

One of the challenges in implementing high frequency converters is reducing the losses due to charging and discharging the devices gate capacitances, \( C_{ds}, C_{gs} \) each switching cycle. The energy required for gating the semiconductor devices is usually dissipated through the gate resistance, \( R_G \). The gate loss, \( P_g \) is given by (30.41), where \( Q_g \) is the total gate charge is mentioned in the semiconductor device datasheet, \( f_s \) is the switching frequency and \( V_{dd} \) is the driver voltage. It can be seen that gate loss is a function of the switch device geometry, drive voltage, and switching frequency.

\[
P_g = Q_g V_{dd} f_s \tag{3.51}
\]

The total gate loss of the converter is given by (3.42); where \( P_{g,S1} \) and \( P_{g,S2} \) represent the gate loss of the switches \( S_1 \) and \( S_2 \) respectively.

\[
P_{g,\text{total}} = P_{g,S1} + P_{g,S2} \tag{3.52}
\]

### 3.5.1.2 Switching Loss

The other frequency dependent loss of switch device is switching loss which occurs during switching transitions as given by (3.43). The rise and fall times of the semiconductor device, \( t_r \) and \( t_f \) can be obtained from datasheets. \( I_{ds} \) represents the switch current and \( V_{ds} \) represents the voltage across the drain to source.

\[
P_{sw} = \frac{1}{2} (t_r + t_f) V_{ds} I_{ds} f_s \tag{3.53}
\]

The goal of soft switching and in particular zero voltage switching (ZVS) is to reduces the switching losses by maintaining a low voltage across the semiconductor device during the on/off transitions.
3.5.1.3 Output Capacitance Loss

The output capacitance loss, \( C_{oss} \) is energy lost when the switch output capacitance is discharged during turn on as given by (3.44). In the equation, \( C_{oss} \) is the output capacitance of the switch. By using ZVS technique, this loss can be eliminated.

\[
P_{coss} = \frac{1}{2} C_{oss} V_{in}^2 f_s
\]  
(3.54)

3.5.1.4 Conduction Loss

When the switch is on, it does not behave as an ideal switch with zero impedance, but it presents a resistance called on state resistance, \( R_{ds-on} \). This resistance corresponds to an important non frequency dependent loss: conduction loss, \( P_{\text{cond}} \). The conduction loss of the switch device is given by (3.45), where \( i_{ds,rms} \) is the RMS value of the switch current.

\[
P_{\text{cond}} = i_{ds,rms}^2 R_{ds-on}
\]  
(3.55)

3.5.2 Transformer Loss

There are two major loss mechanisms associated with a core based transformer, core loss and copper loss.

3.5.2.1 Copper Loss

It is common to assume that resistance is independent of frequency, so the dc resistance \( R_{dc} \) is equal to the ac resistance \( R_{ac} \). However, due to the skin and proximity effects, this assumption can become inaccurate as frequency increases. Therefore, by increasing the switching frequency of the converter, the copper losses in the transformer is increased due to the skin and proximity effects induced by the eddy currents. The copper loss can be calculated by measuring the primary/secondary winding ac resistance as well as the RMS currents flowing through the primary/secondary windings of the transformer.

\[
P_{\text{copper loss}} = (i_{p}^2 R_{ac,p} + i_{s}^2 R_{ac,s})
\]  
(3.56)

3.5.2.2 Core Loss

The core loss can be obtained by using the classical power law or “Steinmetz” model:

\[
P_{\text{core}} = V_{core} C_M \rho \alpha \beta
\]  
(3.57)
Where $V_{\text{core}}$ is the core volume, $f$ is the operating frequency, $B_{ac}$ is the sinusoidal ac flux density in the core and $C_M$, $\alpha$ and $\beta$ are parameters chosen to fit the model to measured loss data. For typical ferrite materials, $\alpha$ is in the range of 1.4-2.0 and $\beta$ is in the range of 2.4 - 3.0 where specific parameters may need to be selected for a particular frequency range.

Since a coreless transformer is using in this thesis, the only major loss mechanism that should be dealt with is copper loss.

### 3.6 Summary

In this chapter, design and high frequency analysis of an isolated class DE resonant converter operating at 10 MHz switching frequency with 150 W nominal output was described. The power stage consists of a class DE inverter using GaN devices along with a sinusoidal gate drive circuit on the primary side and a class DE rectifier on the secondary side. The design equations of class DE were derived in this chapter. The effective output/input impedances of the inverter/rectifier were calculated to be used for designing the matching network including series resonant tank and high frequency transformer in the next chapter. The amount of inductance required for the multilayer coreless PCB transformer was estimated. In those impedance equations, all devices’ output parasitic capacitance were considered. By creating EM model of the inverter/rectifier PCB layout and carrying out Harmonic Balance simulations, it was confirmed that the parasitic inductance of the PCB layout is negligible. In this chapter, EM model was combined with the Harmonic balance techniques to accurately obtain the parasitics of the circuit. Besides, to illustrate how parasitic inductances impact the inverter function, the currents flowing through the parasitic inductors were analyzed and calculated. Those calculated impedances are utilized in designing high frequency transformer in Chapter 4. Finally, the simulation results of the class DE converter were presented and compared to analytical results. The comparison showed a close agreement with the theoretical analysis,
which proves the accuracy of the equations. Next step is to design the high frequency transformer utilized in the converter.
Chapter 4

Multilayer Coreless PCB Transformer

Due to disadvantages of the core-based wire-wound transformer mentioned in chapter 2, multilayer coreless PCB transformer has become an excellent choice in high frequency power converters. Coreless PCB transformer does not require space to incorporate the magnetic core and has no core limitations such as core losses and saturation. Also, the planar structure of this type of transformer provides the advantages of low profile, high power density, excellent repeatability due to elimination of manual winding, and ease of manufacturing. Therefore, for obtaining the stringent height converter in this thesis, isolation is provided by a 10-layered coreless PCB transformer of 1:20 turn’s ratio designed and optimized using 3D Finite Element Method (FEM) tools and radio frequency (RF) circuit design software. Since one of the challenges of the multilayer planar PCB transformer especially for low voltage and high current applications is to sustain large current, this thesis presents an optimized winding arrangement design. This structure makes current to be distributed more equally within parallel layers by changing the geometric parameters of conductors including innermost radius and conductor width. The factors affecting current density distribution and ac winding loss in parallel connection are analyzed and simulated. This method is applied to develop a high frequency coreless multilayer PCB transformer operating at 10 MHz, with low profile of 3.81mm, diameter of 20mm and the efficiency of %97. Simulation and experimental results are presented for a step-up converter operating in 20V/400V input/output voltage.

4.1 Structure of the 10-Layer Coreless PCB Step-Up Transformer

A coreless PCB transformer consists of two parts, which are the dielectric material of FR4 and copper traces on PCB substrate. FR4 material is the most commonly used material as an electrical insulator whose breakdown strength is 50kV/mm. The primary and secondary windings of the transformer are etched on both sides of the PCB substrate. However, for low voltage and high current applications, the use of only a single layer PCB conductors with the
thickness of ½ - 4 Oz is not recommended for designing a high frequency transformer. So, several layers have to be connected in parallel in order to increase the current handling capacity of the winding. As it mentioned in previous chapter, the primary winding is required to carry large amount of currents 27A. Based on Conductive Material Requirements in IPC-2221 standard (The minimum width and thickness of conductors on the PCB shall be determined primarily on the basis of the current carrying capacity required), the minimum required conductor width for internal layers is 4mm for the current of 5.4A and conductor thickness of 2oz. Similarly, the required conductor width for external layers in air is 1.54mm. Therefore, the primary winding structure contains five layers- each layer has one turn- wired in parallel. The conductor width of all five layers in primary winding is chosen to be 6mm.

In order to maximize coupling coefficient and to minimize ac winding loss, the interleaving structure for primary and secondary of the transformer is utilized [77]. On the other hand, a turn’s ratio of 20 is required to transfer the rectifier impedance real part (162.16Ω) into the required inverter impedance real part (0.4Ω). Hence, the secondary winding is made of five layers- each layer has 4 turns- connected in series. Figure 4-1 illustrates winding arrangement of 1:20, 10 layer coreless PCB transformers in which each layer has a port and these ports are connected by electrical via holes to form the primary and secondary windings. The geometrical parameters of the secondary winding is described in the section 4.3.
4.2 Current Distribution within Parallel Layers in Primary Winding

With a series connection, the currents in each secondary layer remain the same, resulting in the same magnetic field strengths on each layer. However, with a primary parallel connection, due to the skin and proximity effects, the currents flowing through the parallel layers is not be equally divided among them which consequently results in extra winding resistance. One solution is utilizing the interleaving structure for primary and secondary of the transformer to minimize the leakage inductance as well as ac winding loss [77]. In this thesis, in addition to interleaving structure, an optimized winding layout arrangement for five parallel layers is applied, which has a significant effect on the current distribution in parallel layers and consequently winding losses of planar transformers. In this design, geometrical parameters of parallel layers such as conductor width and innermost radius are required to be chosen in an optimal manner. Therefore, current will be shared equally and in-phase among parallel windings which can equalize thermal stress among the different parallel layers.

In order to illustrate the eddy current effect in five parallel layers, a Finite Element Method (FEM) tool as well as a Momentum technique and a Visualization tool of ADS are used to analyze current distribution inside the conductors of three different parallel structures. Figure 4-2-a illustrates the eddy current distribution along the winding structure 1 with five parallel layers. All conductors in parallel layers have the same width of 6mm as well as the same innermost radius which are filled with one turn going to the centre of the winding.

As it can be seen, when layers are connected in parallel, both skin and proximity effects lead not only the most of the current to be flown through the interior edges of the conductors, but also the current density to be shared unequally among parallel layers. Therefore, the interior edges of the conductor have relatively high contribution to the total winding loss due to carrying high current density which causes hot spots inside the conductor. From Fig. 4-2-b, it is clearly seen that different parallel layers show a great difference in eddy current distributions and hence
different ac winding losses. The layers placed in the middle of scheme contain much less current than the top and bottom layers.

![Figure 4-2: Current density distributions in each parallel layer of structure 1, (a) parallel winding structure 1, (b) current density distribution](image)

Therefore, to suppress the current crowding effect in conductors, an effective way is to remove the conductor trace out of the central region where current density is large by considering the acceptable minimum conductor width mentioned in IPC-2221. It means that inside edges should be eliminated from the winding structure. In fact, the path on the inside edges is much shorter than that on the outside edge and therefore the impedance is reduced on the inside and consequently current density is increased. As it can be seen in Figure 4-3-a, elimination of inside conductors causes the current density to be distributed more evenly within each layer in structure 2, but layer 1 and 5 still carry much more current than other layers. Therefore, different geometry design should be separately applied for each parallel layer.

![Figure 4-3: Current density distributions in each parallel layer of structure 2, (a) parallel winding structure 2, (b) current density distribution](image)
Therefore, an optimized winding layout arrangement for parallel layers is required to make the current density distributed more even within parallel layers. The impedance of each parallel winding layer depends on its length, its relative position in the winding arrangement and the frequency. It is reasonable then to assume that an inverse relationship exists between the current sharing and the radius. Therefore, to increase the current in the middle layers, their width is considered greater than other layers while their innermost radius is less than top and bottom layers. The influence of the conductor trace width on the ac resistance of the winding has been discussed in [78]. The equal current distribution in the different parallel layers of the parallel winding of structure 3 is presented in this Figure 4-4.

![Figure 4-4: Current density distributions in each parallel layer of structure 3, (a) parallel winding structure 3, (b) current density distribution](image)

It should be noted that all simulations are run for an interleaving structure with the presence of the secondary windings. In order to see the current flowing in parallel layers clearly, those secondary layers are turned off in figures. The design procedure of secondary winding is presented in the next section.

For in-depth analysis, the ac winding losses vs. frequency is characterized for the three parallel structures in Figure 4-5. It shows different parallel structures have different ac winding loss behaviors. Even though, there is a slight difference between the winding resistance of structure 2 and 3, the current sharing is better improved in all parallel layers of the structure 3 which consequently results in less power dissipation in layers.
Therefore, the optimized parallel structure 3 is utilized for designing the high frequency transformer as a primary winding in the next section.

### 4.3 Geometrical and Electrical Parameters of 10-Layer Coreless PCB Transformer

In case of coreless PCB transformer, the electrical parameters such as resistance, capacitance and inductance depend on geometrical parameters [79] such as:

1) Outermost radius;

2) Number of turns;

3) Conductor width;

4) Substrate thickness;

5) Conductor thickness.

So it is required to choose these parameters in an optimal method in order to design an efficient transformer. In this case, the spiral winding structure is considered because the higher value of the inductance can be obtained when compared to other structures such for the given geometrical parameters [80]. From this it can be also observed that, for a given amount of
inductance, the spiral structure for the transformer gives the lower value of resistance compared to the other structures.

Based on required inverter output impedance and rectifier input impedance, the turn’s ratio of 20 is obtained. Inductive parameters of coreless PCB transformer such as self, mutual and leakage inductance can be calculated by using the Hurley and Duffy method [81]. In this method, each turn of the windings is assumed to be a complete circle. For large radius, this approximation gives properly accurate results. However, as the size of the planar PCB transformer becomes small, more precise methods should be considered. In addition, the most outstanding work as a calculation method of the ac resistance for any current waveform can be found in Dowell method [82]. However, with the Dowell model, the currents in each winding layer should be given. For series connected turn layers, the currents in each layer are given. However, for parallel connected turn layers, only the sum of the currents in all the parallel layers are known. So the key for modeling of parallel winding is to determine the currents in each parallel layer.

Therefore, in view of the complexity of accurate analytical methods, the transformer has been designed using 3D finite element method (FEM) tools like Advanced Design System (ADS). This tool is used to solve Maxwell's electromagnetic equations for planar structures embedded in a multilayered dielectric substrate which enables engineers to analyze and choose an optimum winding design. In this regard, the initial physical parameters are obtain as the following assumptions and then more than ten different transformers with various physical parameters such as different outermost radius with the same number of turns, different conductor width, and different track separation are simulated.

In a spiral PCB transformer shown in Fig. 4-6, the flux density in the inner turns is higher resulting in a higher ac resistance in inner turns compared to the outer turns. Also, since the length of these inner turns are shorter than the length of the outer ones, they contribute less to the overall inductance of the transformer. Hence, in order to increase the quality factor of the planar PCB transformer the hollow factor which is defined as the ratio of the innermost radius
“Ri” to the outermost radius “Ro”, should be greater than 0.45 [83]. Another consideration is that to increase inductance in a given footprint without affecting the quality factor significantly, the width of the conductor’s traces “w” are selected at least ten times of the skin depth at 10 MHz [83]. Furthermore, the distance between conductor’s traces “s” are designed as small as possible, so that more traces can be fit in a given radius which leads to increase the amount of inductance of the winding.. In this case, it was considered as half of the width of the trace width “w”. This gives a larger amount of inductance with high-quality factor and low ac resistance. More detailed explanations behind these guidelines are provided in [83].

![Figure 4-6: Spiral planar PCB transformer](image)

Based on skin depth at 10 MHz, the multilayer PCB transformer is embedded in a dielectric substrate “t” with 70µm conductor thickness in order to minimize the proximity effect loss and also to maximize the copper utilization. To meet the high fill factor and isolation requirements between primary and secondary windings, the substrate thickness “h” of 0.381mm is considered resulting in the total height of the transformer “T” as 3.83 mm. Transformer’s dielectric substrate is FR4 (Flame Retardant 4) material whose breakdown voltage is of 50 kV/mm.

Figure 4-7 shows a 10 layer coreless PCB transformer designed and simulated in ADS. This transformer has an interleaving structure S-P-S-P-S-P-S-P-S-P to uniform the current density distribution inside the conductors which consequently minimizes ac winding resistance.
Once an initial design is finalized using the 3D FEM simulation technique described above, EM model of the transformer is exported to schematic editor. Time-domain and frequency-domain simulations are then performed to validate the performance of the transformer design. Based on the simulation results, disagreements between expected and observed performance are identified, and the design parameters can be further repeated. For instance, it was observed that increasing the outermost radius while maintaining the same number of turns increases the inductive parameters of the transformer. In this case, the increase of mutual inductance is greater than that of leakage inductance. Thus, the coupling coefficient of a coreless PCB transformer can be improved by increasing the transformer area. Separation between the primary and secondary windings defined by the substrate thickness plays an important role in coupling factor of a coreless PCB transformer design. As separation increases, the magnetic coupling between the primary and secondary windings decreases. The variation of conductor thickness does not affect the inductive parameters significantly. The winding geometric parameters of the final transformer design are given in the Table 4-1. After tuning each parameters, the tuned transformer is tested in class DE converter to find the better overall converter efficiency.
### Table 4-1: Geometrical parameters of the optimized multilayer coreless PCB transformer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of primary turns</td>
<td>(N_p)</td>
</tr>
<tr>
<td>Number of secondary turns</td>
<td>(N_s)</td>
</tr>
<tr>
<td>Outermost radius of transformer</td>
<td>(R_o) 10 mm</td>
</tr>
<tr>
<td>Separation between secondary tracks</td>
<td>(S_s) 0.5 mm</td>
</tr>
<tr>
<td>Conductor width of secondary winding</td>
<td>(W_s) 1 mm</td>
</tr>
<tr>
<td>Innermost radius of secondary winding for 5 layers</td>
<td>(R_{i,s}) (= 4) mm</td>
</tr>
<tr>
<td>Innermost radius of primary winding for 5 layers</td>
<td>(R_{i,p}) (R_{i,p1}= R_{i,p5} = 6.8) mm (R_{i,p2}= R_{i,p4} = 4.2) mm (R_{i,p3}= 4.8) mm</td>
</tr>
<tr>
<td>Conductor thickness</td>
<td>(h) 70 µm</td>
</tr>
<tr>
<td>Dielectric substrate thickness</td>
<td>(t) 14 mil</td>
</tr>
</tbody>
</table>

### 4.4 Transformer Function as a Matching Network

Figure 2-1 in the second chapter shows a basic structure for a high frequency resonant dc-dc converter, comprising a resonant inverter, a rectifier, and a matching network. This matching network including a resonant circuit and a high frequency transformer provides a combination of isolation, voltage transformation, and the required matching between the rectifier and the inverter. As explained in previous chapter, the system is designed such that the nonlinear effects of rectification stage are modeled by equivalent impedance of \(Z_{rec} = 162-j076.86\) and it should be matched to the inverter’s required output impedance \(Z_{inv} = 0.4+j0.12\) by the action of the matching network during the transformer design process. Also, the resonant inductor should be incorporated into transformer leakage inductance. Therefore, the functions of this matching network including resonant circuit and transformer is to force the inverter’s load current to be nearly sinusoidal and to provide a means of scaling the voltages of the inverter to a level at which the rectifier can operate efficiently. Also for the given value of \(Z_{rec}\), it should give a value of \(Z_{inv}\) such that ZVS can be achieved for switches.
Once the design optimization is finalized using the 3D FEM simulation technique described in previous section, the S-parameters of the planar PCB transformer shown in Figure 4-8 are extracted from EM simulator and converted to Z-parameters through the following equations. These Z-parameters are utilized for designing the matching network.

![Figure 4-8: Extracted S-parameters of the coreless PCB transformer from EM simulator](image)

Conversion between Z-parameters and S-parameters are given by:

\[
Z_{11} = \left[ \frac{(1+S_{11})(1-S_{22})+(S_{12}S_{21})}{(1-S_{11})(1-S_{22})-(S_{12}S_{21})} \right] Z_0 \quad (4.1)
\]

\[
Z_{12} = \left[ \frac{2S_{12}}{(1-S_{11})(1-S_{22})-(S_{12}S_{21})} \right] Z_0 \quad (4.2)
\]

\[
Z_{21} = \left[ \frac{2S_{21}}{(1-S_{11})(1-S_{22})-(S_{12}S_{21})} \right] Z_0 \quad (4.3)
\]

\[
Z_{22} = \left[ \frac{2S_{22}}{(1-S_{11})(1-S_{22})-(S_{12}S_{21})} \right] Z_0 \quad (4.4)
\]
All of those parameters are impedances with dimensions of ohms. The input impedance of the two-port transformer network is given by:

$$Z_{\text{in,Tr}} = Z_{11} \frac{Z_{12} Z_{21}}{Z_{22} + Z_{L}}$$  \hspace{1cm} (4.5)

Where $Z_L$ is the impedance of the load which is the rectifier input impedance. This input impedance should be matched with the impedance seen by the inverter $(0.4 + j0.12)$. It can be done with the assistance of the external capacitor $C_{\text{ext}}$ connecting along the secondary and also the resonant capacitor $C_r$. Also, by adding the external capacitor connected across the secondary winding of the transformer, there is the possibility of increasing voltage gain, $V_s/V_p$ (to overcome the low magnetic coupling), input impedance ($Z_{\text{in}}$), and consequently the energy efficiency ($\eta$) of the transformer. This is due to the partial resonant phenomena of the transformer and the external resonant capacitor. By tuning these two capacitors shown in Figure 4-9, the value of $Z_{\text{in}}$ for matching network is obtained similar to the output impedance of the inverter.

![Figure 4-9: Matching Network including the high frequency transformer, resonant tank and external capacitor loaded by to the rectifier input impedance](image)

The input impedance of the matching network (resonant capacitor and transformer) is given by:

$$Z_{\text{in}} = -jX_{C_r} + Z_{11} \frac{Z_{12} \times Z_{21}}{Z_{22} + Z_{L}}$$

Where $Z_L$ is the load impedance and for reciprocal networks $Z_{12} = Z_{21}$. 68
In Figure 4-9, the load impedance is rectifier load in parallel with the external capacitor.

\[ Z_{12} = Z_{21} \]
\[ Z_l = R + jX \]

In order to simplify the network, transformer impedances can be assumed inductive impedances.

\[ Z_{11}, Z_{22}, Z_{12}, Z_{21} \approx \text{Inductive} \]

\[ Z_{in} = -jX_{c_r} + jX_{11} - \frac{jX_{12} \times jX_{21}}{jX_{22} + R + jX} \]
\[ Z_{in} = -jX_{c_r} + jX_{11} + \frac{X_{12}^2}{jX_{22} + R + jX} \]
\[ Z_{in} = -jX_{c_r} + jX_{11} + \frac{X_{12}^2}{R^2 + (X + X_{22})^2}(R - j(X_{22} + X)) \]  (4.6)
\[ Re\{Z_{in}\} = \frac{X_{12}^2}{R^2 + (X + X_{22})^2} R \]  (4.7)
\[ Im\{Z_{in}\} = -jX_{c_r} + jX_{11} + \frac{X_{12}^2}{R^2 + (X + X_{22})^2}(-j(X_{22} + X)) \]  (4.8)

As it can be seen \( Re\{Z_{in}\} \) is dependent on real part of load impedance and \( Im\{Z_{in}\} \) is a function of both real and imaginary of load impedance.

In Figure 4-9, the load impedance is rectifier load in parallel with the external capacitor.

\[ Z_L = Z_{rec}||Z_{ext} \]
\[ Z_L = (R_{rec} - jX_{rec})||-jX_{ext} \]
\[ Z_L = \frac{-jX_{c_{ext}} \times (R_{rec} - jX_{rec})}{R_{rec} - j(X_{rec} + jX_{c_{ext}})} \]
\[ Z_L = \frac{-jX_{c_{ext}} \times R_{rec} - X_{c_{ext}}X_{rec}}{R_{rec} - j(X_{rec} + jX_{c_{ext}})} \times \frac{R_{rec} + j(X_{rec} + jX_{c_{ext}})}{R_{rec} + j(X_{rec} + jX_{c_{ext}})} \]
\[ Z_L = \frac{-jX_{c_{ext}} \times R_{rec} - X_{c_{ext}}X_{rec}}{R_{rec}^2 + (X_{rec} + jX_{c_{ext}})^2} \times \frac{R_{rec} + j(X_{rec} + jX_{c_{ext}})}{R_{rec} + j(X_{rec} + jX_{c_{ext}})} \]
\[ Z_L = \frac{X_{c_{ext}}R_{rec}(X_{rec} + jX_{c_{ext}}) - R_{rec}X_{c_{ext}}X_{rec}}{R_{rec}^2 + (X_{rec} + jX_{c_{ext}})^2} + \frac{-jX_{c_{ext}}(X_{rec}^2 + R_{rec}^2 + X_{c_{ext}}X_{rec})}{R_{rec}^2 + (X_{rec} + jX_{c_{ext}})^2} \]

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\[ R = Re\{Z_L\} = \frac{X_{c_{ext}}R_{rec}(X_{rec}+jX_{c_{ext}}) - R_{rec}X_{c_{ext}}X_{rec}}{R_{rec}^2 + (X_{rec}+X_{c_{ext}})^2} \]  \hspace{1cm} (4.9)

\[ X = Im\{Z_L\} = \frac{-jX_{c_{ext}}(X_{rec}^2 + R_{rec}^2 + X_{c_{ext}}X_{rec})}{R_{rec}^2 + (X_{rec}+X_{c_{ext}})^2} \] \hspace{1cm} (4.10)

By substituting (4.9) and (4.10) into (47) and (4.8), the values of resonant capacitor and external capacitor can be obtained 24pF and 37pF respectively.

**4.5 Simulation results of the optimized multilayer coreless PCB transformer**

In order to illustrate how equal are the current density through the optimized parallel layers, a 10-layer, 1:20 coreless PCB transformer by using two different structure 1 and optimized structure 3 has been modeled and simulated using 3D finite element Method (FEM) tools, ADS which is a radio frequency (RF) circuit design software. In winding strategy of the transformer, shown in Figure 4-10, the secondary is made of five layers- each layer has 4 turns- connected in series and the primary winding contains five layers- each layer has one turn- wired in parallel. Each layer has a port and these ports are connected by electrical vias to form the primary and secondary windings.
Based on skin depth at 10 MHz, the multilayer planar transformer is embedded in a dielectric substrate with 35µm conductor thickness in order to minimize the proximity effect loss and also to maximize the copper utilization. Figure 4-11 demonstrates that all layers are separated by FR4 dielectric substrate with thickness of 0.381mm to obtain high fill factor.
The first transformer (Tr1) is simulated by using the parallel winding structure 1 to be compared with the optimized transformer (Tr2) with an optimized parallel winding structure 3. The simulated ac resistance of the primary winding of the two transformers, is illustrated in Figure 4-12. As it can be seen, the ac winding resistance of the second transformer using optimized parallel winding design is clearly reduced (0.16 mΩ at 10MHz). Because the currents are fully and equally shared by the five parallel layers in the primary winding. The ac resistance of both primary/secondary winding of the optimized transformer is illustrated in Fig.4-13. The energy efficiency of the transformer Tr2 plotted in Figure 4-14 (under different loaded conditions) is approximately 97% at the frequency of 10MHz with the load resistance of 150Ω. Comparison of energy efficiency for both transformer can be observed from Figure 4-15.

Figure 4-12: AC resistances of the primary winding of the transformers with winding structure 1 and optimized winding structure 2
Figure 4-13: AC resistance of primary/secondary windings of the optimized multilayered coreless PCB transformer Tr2

Figure 4-14: Energy efficiency of optimized coreless PCB transformer Tr2 for different loads

Figure 4-15: Energy efficiency Comparison of both coreless PCB transformers
The electrical parameters for the final transformer design were estimated by using the FEM method as discussed before are given in table 4-2.

| Table 4-2: Electrical parameters of the optimized multilayer coreless PCB transformer |
|---------------------------------|-----------------|---------------|
| Primary/Secondary DC resistance | R_p/R_s          | 0.15/0.56     |
| Primary/Secondary self-inductance | L_p/L_s         | 16.7 nH/3.44 μH |
| Primary/Secondary leakage inductance | L_lkp/L_lks    | 10.5 nH/623 nH |
| Primary/Secondary mutual inductance | L_mp/L_ms      | 6.2 nH/2.8 μH |
| Interwinding capacitance         | C_ps            | 133 pF        |
| Coefficient coupling             | K               | 0.65          |

**4.6 Summary**

In this chapter, the design and analysis of 10 layer coreless PCB step-up transformers operating in 10 MHz was discussed. In view of the complexity of accurate analytical methods, the transformer was designed using 3D finite element method (FEM) tools like Advanced Design System (ADS). To obtain the optimized transformer design, a range of multilayer coreless PCB transformers with different geometric parameters were designed by using optimization tool in Harmonic Balance simulator, and then simulated in class DE converter. Furthermore, S-parameters of the planar PCB transformer were extracted from EM simulator and converted to Z-parameters to calculate the input impedance of the matching network. This matching network including a resonant circuit and a high frequency transformer provides a combination of isolation, voltage transformation, and the required matching between the rectifier and the inverter impedances.

In this chapter, in addition to interleaving structure S-P-S-P-S-P-S-P-S-P-S-P used for high frequency transformer, an optimized winding layout arrangement for the primary parallel layers was also applied to make the current density distributed more even within parallel layers. The current density distribution inside the conductors of three different parallel layer structures were studied via Momentum technique and a Visualization tool of ADS.
Finally, the simulation results of the proposed multilayer coreless PCB transformer were presented and compared with the first structure. The comparison showed an improvement in terms of winding resistance and efficiency.
Chapter 5

Simulation and Experimental Setup

Previous chapters have discussed major design concepts and tuning procedures of a power stage and PCB transformer for a dc-dc converter which targets the specifications listed in Table 3-2. To verify these analysis and calculation, simulations and experiments of the class DE resonant converter with a 10 layer coreless PCB transformer utilizing sinusoidal gate drive and on/off control were carried out in this chapter. The analysis and simulation results of sinusoidal gate drive and control circuits were presented in appendix A and B respectively.

5.1 Layout PCB

PCB layout is an important step of the design process for converters operating in high frequency region, where undesirable parasitic components can significantly affect the switching waveforms and deteriorate the overall performance of a converter [84]. Although parasitic capacitances and inductances are absorbed as a function of the resonant tank, in some cases additional inductances related to the device packages and PCB traces can be problematic. Therefore, choosing devices with small packaging inductance is an important criteria in devices selection. The converter (inverter and rectifier stage) was constructed on a 4-layer PCB, using Altium Design. As explained in [85], the reason that prototype was implemented on a 4-layer PCB is to minimize parasitic inductances, as the parasitic inductances of 4 layer PCB (with the inner two layers used as gate signal and gate return) are much reduced than a 2-layer FR4 board. In addition, components are placed as close to each other as possible. Besides these considerations, by using ADS software as a PCB designer and simulator, it was possible to simulate the PCB layout of the entire converter along the 10 layer coreless PCB transformer. In this kind of simulation, all the parasitic elements presented in the PCB traces between components were considered while the converter was being simulated.
5.2 Simulation Results

The Class DE resonant converter with 10-layer coreless PCB transformer is simulated in Agilent ADS software with models of the GaN switches, SiC diodes, and the measured s-parameter model of the PCB transformer. Advanced Design System (ADS) is a high frequency design automation software system produced by Keysight EEsof EDA which supports every step of the design process such as schematic capture, layout, design rule checking, frequency-domain and time-domain circuit simulation, and electromagnetic field simulation. A representative Schematic is shown in Figure 5-1 to 5-4. As it can be seen, the EM model of the PCB transformer is imported to the schematic environment to model the transformer accurately by using the S-parameters generated by an EM simulation. In addition, the Spice model of both switches and diodes are added to ADS simulator such that a more accurate simulation can be performed. The Results of the simulation are shown in Figure 5-2. Given the input voltage is 20V, the switching frequency is 10MHz, and the gate capacitance of the power MOSFET is 1.8nF, the proposed converter has the efficiency of 92.2%.

Figure 5-1: Schematic of the class DE converter with sinusoidal gate drive circuit and 10 layer coreless PCB transformer
Figure 5-2: Schematic of the class DE inverter with sinusoidal gate drive circuit

Figure 5-3: Schematic of the class DE rectifier
The simulated inverter output voltage and current are shown in Figure 5-5. The inverter output current is phase shifted to ensure ZVS transition in the class DE inverter. Figure 5-6 illustrates the input voltage of the rectifier shown in Figure 3-8. For the simulation shown, $C_d$ is the device capacitance of the diode (C3d1p7060q SiC Schottky diode), $V_{out} = 400$ V, and the sinusoidal input current $I_s = 1.8$ A at a frequency of 10MHz. The average power delivered to the load under these conditions is 153W shown in Figure 5-7 and 5-8. As can be seen from the efficiency plot in Figure 5-9, the energy efficiency is 92.2% at 10MHz.
Figure 5-6: Input voltage waveform of the rectifier

Figure 5-7: Output voltage of the converter

Figure 5-8: Output power of the converter
5.3 Experimental Results

Other than simulation, some experiments were also carried out for verification. The inverter, rectifier and transformer which is 20 mm in diameter are constructed on separate PCB. A prototype of the 10 layer coreless PCB transformer was constructed. Figure 5-10 is a picture of the transformer. The electrical parameters of the designed coreless PCB transformer are measured by using the Precision Impedance Analyzer 4294A by open circuiting or short circuiting the opposite winding of the transformer. The measured values compared to the simulated ones are shown in Figure 5-11 to 5-14.

Figure 5-9: Energy efficiency of the converter
Figure 5-10: A prototype of 10 layer coreless PCB transformer, (a) Top view (b) Bottom view

(a) Schematic of the transformer in ADS
(b) Simulated inductance and resonant frequency: 16.78nH & 25.8MHz

(c) Measured inductance and resonant frequency: 16.53nH & 24.87MHz

Figure 5-11: Inductive value and resonance frequency seen from primary while secondary is open circuit

(a) Schematic of the transformer in ADS
(b) Simulated inductance: 10.54nH  
(c) Measured inductance: 9.37nH

Figure 5-12: Inductive value seen from primary while secondary is short circuit

(a) Schematic of the transformer in ADS
(b) Simulated inductance and resonant frequency: 3.44\( \mu \)H & 25.81MHz

(c) Measured inductance and resonant frequency: 3.21\( \mu \)H & 25.44MHz

Figure 5-13: Inductive value and resonance frequency seen from secondary while primary is open circuit

(a) Schematic of the transformer in ADS
(b) Simulated interwinding capacitance: 133pF

(c) Measured interwinding capacitance: 162.3pF

Figure 5-14: Interwinding capacitance between primary and secondary by solder shorting the windings of the transformer
Chapter 6

Conclusion and future Work

6.1 Summary
In this thesis, a high frequency Class DE converter using a 10-layered coreless PCB step-up transformer was analyzed, designed, implemented. Converter topology was developed based on a half bridge series resonant converter operating at the specific working point with the objective of considering the significant dead time for charging and discharging the output parasitic capacitance of the switches in high frequency analysis. The high frequency analysis to achieve the good performance of the converter was described. Conduction loss, switching loss and the gate drive power consumption were the primary loss mechanisms considered in the analysis of class DE converter to select the switching devices with minimum $R_{on,ds}$ and also smaller input and output capacitances of the device. Based on this considerations, the EPC GaNFET semiconductor EPC2020 was identified as a switching device for the converter operating at 10 MHz. The converter utilizes a low loss sinusoidal gate drive and an on/off control method modulating at fix frequency which were designed and analyzed in Appendix A and B respectively. Resonant gate drive circuit was developed to drive both low side and high side EPC2020 switches with a sinusoidal gate signal. Commercial inverter was applied as a drive stage to drive a resonant network in the gate drive circuit.

Although resonant converters such as Class DE converters are theoretically able to operate at high frequency, implementation issues related to core based transformers limit their performance. The motivation behind this work was to design a coreless PCB transformer that aid in reducing the difficulties due to magnetic cores and in achieving advantages of low costs, high power density, low profile, no magnetic core loss, and ease of manufacturing. The merits of this transformer are verified via high frequency simulation of the 10 MHz class DE converter with an input voltage range of 20V, an output voltage range of 400V and a rated output power of 150W.
The experimental results of the 10-layered coreless PCB transformer show the potential of utilizing this ‘coreless PCB transformers’ for various stringent height dc-dc converter applications where the total height of the converter is a major concern.

6.2 Contribution

(a) The main contribution of this thesis was to design and analysis of the multilayer coreless PCB transformer for high frequency applications. This multilayer coreless PCB transformer aids in reducing the difficulties due to magnetic cores and in achieving advantages of low costs, high power density, low profile, no magnetic core loss, and ease of manufacturing. In the high frequency transformer, which includes parallel-connected layers, in addition to interleaving structure, an optimized winding layout arrangement for parallel layers was also applied to make the current density distributed more even within parallel layers. To obtain the optimal transformer design, a range of multilayer coreless PCB transformers with different geometric parameters have been fabricated and tested. In view of the complexity of accurate analytical methods, for modelling high frequency transformer, 3D Finite Element Method (FEM) tools, ADS, was considered as a primary tool prior to the construction of the prototypes. In this thesis, also a Momentum technique and a Visualization tool of ADS were used to analyze current distribution inside the parallel layers.

(b) Then, the merits of this transformer were verified via high frequency simulations of a 10 MHz class DE converter with an input voltage range of 20V, an output voltage range of 400V and a rated output power of 150W. In this thesis, high frequency model of the class DE converter was simulated by considering parasitic components, since the parasitics play an important role at high frequency levels. During the design, required characteristics of the matching network including series resonant tank and high frequency transformer were revealed. The effective output /input impedances of the inverter /rectifier were calculated to be used for designing the matching network including series resonant tank and high frequency transformer. By creating EM model
of the inverter/rectifier PCB layout and carrying out Harmonic Balance simulations, the parasitic inductance of the PCB layout was achieved. Besides, to illustrate how parasitic inductances impact on the inverter function, the currents flowing through the parasitic inductors were analyzed and calculated. Hence, designing the transformer and other magnetic parts became possible.

(c) After the evaluation and simulation of the high frequency transformer using the simulation tool, the prototypes were developed using PCB design software and evaluated in a high frequency region. There was a very good agreement between the results obtained with the simulation and experimental results. The purpose was to investigate the possibility of using the multilayer coreless PCB transformer for step-up conversion applications.

6.3 Future Work

Unlike transformers working at low frequency, there is a lack of literature about design of high frequency transformers, and both the theory and fabrication of these transformers applied in high frequency resonant dc-dc converters are not very clear. At high frequencies, the impact of parasitics must be carefully considered. A PCB planar transformer is the best candidate to absorb and utilize the parasitic components. Therefore, the modeling, design, integration and fabrication techniques of a high frequency planar transformers are required to be further explored.

In addition, the EMI generated by high frequency resonant dc-dc converter using a PCB transformer needs to be characterized and evaluated in the future works. The results should be compared to industry standards.
References


Appendix A

Gate Drive Circuitry for Class DE Converter

For the double ended converter topologies such as class DE converters, the drain source voltage is clamped to the input voltage and hence the lowest stress will be imposed on both switches. In fact, the stress of the single switch in the single ended topologies can be shared by two MOSFETs in doubled ended topologies. In addition to this, for a given power transfer application, the size of the transformer can be reduced in double ended converters due to its full utilization as compared to that of the transformer in single ended converter topologies. However, this topology requires a high side gate drive circuits.

In all the double ended converter topologies such as half-bridge, full-bridge and resonant converters, floating gate drive circuitry is required. For this isolation purpose, a gate drive transformer can be utilized. In this case, the function of using a gate drive transformer is to transfer the ground referenced signals with galvanic isolation in order to drive the high side GaNFET gate with regard to floating ground on the other side.

On the other hand, for high frequency applications, a resonant gate drive circuit is used to recover a portion of the gate energy lost in conventional drivers. One approach that has been used previously is a sinusoidal gate drive.

6.3.1 Sinusoidal Resonant Gate Drive Circuit

Figure A-1 shows a schematic of the resonant gate drive circuit consists of a drive stage, a resonant tank to reduce the switching losses and a transformer.

![Sinusoidal Resonant Gate Drive Circuit](image)

Figure A-1: Sinusoidal resonant gate drive circuit for high and low side switches

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Drive stage which is the drive inverter, can be applied for hard switching or to drive a resonant gate drive circuit via a tuned resonant tank. This structure is used to enhance the drive capacity. Two design considerations are the current handling capability and losses associated with the drive switches. The drive stage can be built with discrete MOSFETs or can be used as a commercially designed drive inverter stage.

The resonant tank includes a series branch $L_1 \cdot C_1$ and a shunt branch $L_2$. The shunt branch, $L_2$ carries a portion of the reactive current which consequently results in reduction of the loss in the drive inverter. $L_2$ resonates with the gate capacitor below the switching frequency, $f_s$, so that it looks capacitive. The inductor value is chosen so that the shunt branch has a higher impedance at the desired frequency than $C_{gs}$ which relates to a lower equivalent capacitance. In fact, the effective equivalent impedance looks like an equivalent capacitance which is smaller than the initial gate capacitance $C_{gs}$. This leads to increase the $Q$ of the resonant gate drive as described by equation $Q=1/R \sqrt{L/C}$. The effect of the shunt branch on the transfer function from inverter to gate is equivalent to reduce the capacitance seen across the gate, increasing the transfer function and providing a strong drive signal for the device.

The series branch, comprising $L_1$ and $C_1$, set the transfer function from the inverter to the gate. While $C_1$ acts as a dc blocking capacitor, $L_1$ resonates with the equivalent capacitor (combination of the $L_2$ and $C_{gs}$) close to $f_s$ such that there is a significant voltage gain from the drive inverter to the gate at the switching frequency. Although higher gain of the transfer function can be obtained by increasing the value of $L_1$ (which corresponds to smaller equivalent gate capacitance), larger value of $L_1$ results in some disadvantages. First, larger value of $L_1$ slows the gate drive start-up which may reduce the efficiency of the overall system. It may also cause the MOSFET to self-oscillate. The choice of $L_1$ is a trade-off between these considerations. A signal transformer is inserted into the gate drive circuit as shown in Figure A-1. Therefore the gate drive circuit can drive both high side and low side switches.
The gate resistance and gate capacitance of the main switch are 0.4Ω and 1.8nF respectively. The resulting component values are listed in Table A-1.

<table>
<thead>
<tr>
<th>$L_1$</th>
<th>$C_1$</th>
<th>$L_2$</th>
<th>Drive Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 nH</td>
<td>100 nF</td>
<td>120 nH</td>
<td>LM5134</td>
</tr>
</tbody>
</table>

### 6.3.2 Simulation Results of Sinusoidal Resonant Gate Drive

In this section, simulations were performed to verify the gate drive circuit shown in Figure A-2 by using PSIM and LTSPICE software. The power device is a GaNFET - EPC2020 - with specification in Table A-1. The simulated waveforms of the gate drive circuit for duty cycle ratios of 44% at an operating frequency of 10 MHz are depicted in Figure A-3.

Figure A-2: Schematic of the sinusoidal resonant gate drive circuit

Figure A-3: Waveforms of the sinusoidal resonant gate drive circuit
Appendix B

Control Strategy

Once it is accepted that resonant converters are suitable for high frequency applications, the next challenge is implementing a control method that provides the requirements of the converter without degrading its performance. In all switching converters, the output voltage is a function of the input voltage, the duty cycle, the switching frequency, and the load current as well as the converter circuit element values. In a dc-dc application it is desired to obtain a constant output voltage in spite of disturbances in $v_{in}$, $i_{load}$ and $f_s$ and in spite of variations in the converter circuit element values. So a control loop system is needed. There are different methods of regulating the output of a resonant converter with their own merits and demerits [86], [87].

Resonant converters are conventionally controlled by varying the switching frequency of the square wave produced by the inverter [88] to modulate the impedance of the resonant tank which leads to vary the gain of the converter. A main drawback of this control method is the wide range of operating frequencies required to regulate the output. This results in complication in designing magnetic component. So, efficiency and performance are degraded. The problem of the variable frequency control applied to the series resonant converter is that output voltage control is lost at light-load.

Constant frequency control of resonant converters solves many problems related to the variable frequency control. It can be achieved by controlling the on-time of the switch (PWM control) or the on-time of the converter (on/off control) [89], [90]. In a PWM control, the compensated voltage error is compared to a sawtooth waveform to generate a pulse signal with duty cycle $D$. The duty cycle variation of the switches changes the shape of the ac waveform of the tank. But this method introduces some disadvantages. As the input voltage increases, or the load reduces, the duty cycle must be reduced, which causes increased harmonic content in the drive voltage.
and resonant current. Furthermore, by reducing the duty cycle, soft switching cannot be guaranteed.

In high frequency converters, it is beneficial to split the conversion function from the regulation function of the converter [91]. Therefore, the converter is designed for full load power and the average delivered power and consequently output voltage is regulated by modulating the entire converter on and off at the modulation frequency which is far below the switching frequency. By using this technique, the magnetics of the power stage are designed and sized for high power conversion.

Therefore, the control technique used in this thesis is the on/off control. This technique is also called burst-mode or bang-bang control. With on/off control method, the converter is turned on and off to regulate the output voltage. This technique is used to obtain extreme efficiency improvements at light load by the simple fact that the converter is not operating most of the time. A schematic of a class DE resonant converter under on/off control is shown in Figure B-1. In this structure, a voltage sensor and two comparators are used to sense the output voltage and feed a command signal into the controller. The modulation frequency $f_M$ is determined by the output capacitor and load.

![Schematic of the class DE resonant converter under on/off control](image)

Figure B-1: Schematic of the class DE resonant converter under on/off control

Steady-state waveforms are shown at different load levels in the following figures. The on intervals start and end with zero current switching, while keeping zero voltage switching in the middle.
$V_{o2}$ is the converter output voltage; $V_r$ is the drain-source voltage of the switch; $I_r$ is the resonant current; $V_{gs1}$ and $V_{gs2}$ are the gate voltages of the high and low switches respectively. As the load reduces, the density of the pulses reduces, and the off-time duration increases.

Figure B-2: Steady-state waveforms at 133W load

Figure B-3: Steady-state waveforms at 100W load
Figure B-4: Steady-state waveforms at 50W load

Figure B-5: Steady-state waveforms at 25W load, $f_M=30$KHz

Results of the transient at on-time as well as off-time are shown in the Figure B-6 and Figure B-7 respectively. $V_r$ is the rectifier input voltage.
Figure B-6: Transient waveforms at on-time

Figure B-7: Transient waveforms at off-time

Figure B-8 illustrates the load step from 50W to 100W.
Figure B-8: Load step waveforms