HIGH PERFORMANCE DIGITAL CONTROL TECHNIQUES FOR POWERING MICROPROCESSORS

by

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Abstract

Increasing power consumption and heat dissipation are becoming urgent challenges for processors today and in the future. Digital power control architectures in which processors closely interact with voltage regulators are becoming necessary to enhance system energy efficiency. Digital techniques offer advantages such as flexibility, fewer external components and reduced overall cost as compared to conventional analog techniques.

The primary objective of this thesis is to develop new digital control architecture for processor voltage regulators with low complexity and high dynamic performance. A digital control technique to naturally implement the desired output impedance is proposed. In this technique, Adaptive Voltage Positioning (AVP) is implemented by generating a dynamic voltage reference and a dynamic current reference to achieve the desired output impedance. A dual-voltage-loop control with dynamic reference step adjustment, non-linear control and a dedicated transient detection circuit is proposed to improve the dynamic performance. The dynamic reference step adjustment method lowers the high speed requirement of reference update clock; the non-linear control minimizes the transient-assertion-to-action delay and maximizes the inductor current slew rate; and the transient detection circuit recognizes the load transient state in a manner adaptive to the amount and slew rate of load transient. Theoretical, simulation and experimental results prove the effective operation and excellent performance of the controller.

Finally, the dynamic performance of the voltage regulator with the proposed digital controller under large-step load oscillations is proven by simulation and experimental results.
In memory of my father, Dengde Pan

To my mother, Aiyu Wu

And to my wife, Na Lei
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Statement of Originality

(Required only for Division IV Ph.D.)
I hereby certify that all of the work described within this thesis is the original work of the author. Any published (or unpublished) ideas and/or techniques from the work of others are fully acknowledged in accordance with the standard referencing practices.

(Shangzhi Pan)

(July, 2008)
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List of Symbols and Acronyms

Acronyms:

AC: Alternating Current
ADC: Analog-to-Digital Converter
ASIC: Application-Specific Integrated Circuit
AVP: Adaptive Voltage Positioning
CAD: Computer-Aided Design
CAN Bus: Controller Area Network Bus
CCM: Continuous Current Mode
CPU: Central Processing Unit
DAC: Digital-to-Analog Converter
DC: Direct Current
DPWM: Digital Pulse-Width Modulator
DSP: Digital Signal Processor
EEPROM: Electrically Erasable Programmable Read-Only Memory
ESL: Effective Series Inductance
ESR: Effective Series Resistance
FPGA: Field-Programmable Gate Array
HPS: Hybrid Power System
IC: Integrated Circuit
I2C Bus: Inter-Integrated Circuit Bus
LSB: Least Significant Bit
MLCC: Multi-Layer Ceramic Capacitor
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
MPZ: Matched Pole-Zero
MUX: Multiplexer
PID: Proportional-Integral-Derivative
PMBus: Power Management Bus
PSI: Power Status Indicator
PWM: Pulse-Width Modulator
RAM: Random Access Memory
ROM: Read-Only Memory
SMBus: System Management Bus
SPI Bus: Serial Peripheral Interface Bus
USB: Universal Serial Bus
VID: Voltage Identification
VR: Voltage Regulator
VRM: Voltage Regulator Module
ZOH: Zero-Order Hold

Symbols:

\( i_L \): inductor current
\( I_{pk} \): the peak inductor current
\( I_c \): current through the filtering capacitor \( C \)
\( I_{ref} \): peak current reference
\( V_{ref} \): voltage reference
\( \Delta I_{ref} \): the predefined adjustment step of the peak current reference \( I_{ref} \)
Δ$V_{\text{ref}}$: the predefined adjustment step of the voltage reference $V_{\text{ref}}$

$<I_{\text{ref}}>$: the average peak current reference

$<V_{\text{ref}}>$: average voltage reference

$<I_L>$: the average inductor current

$<V_o>$: the average output voltage

$R_i$: current sensing gain

$H$: voltage sensing gain

$\Delta V_{p-p}$: the output voltage ripple

$\Delta I$: the current ripple

$t_d$: this circuit delay

$I_{pk}$: peak to reference current error

$V_{in}$: the line voltage

$V_o$: the output voltage

$I_o$: the load current

$R_o$: the output impedance

$Z_{oc}$: closed-loop output impedance

$ESR$: equivalent series resistance of the output capacitor $C$

$T_{sw}$: the switching period

$f_{sw}$: the switching frequency

$D$: the duty ratio

$\Delta V_{\text{tol}}$: the maximum allowed voltage tolerance

$\Delta I_{\text{ref,LSB}}$: the least significant bit (LSB) of the current DAC

$\Delta V_{\text{ref,LSB}}$: the least significant bit (LSB) of the voltage DAC

$V_{o,\text{max}}$: the largest output voltage
List of Symbols and Acronyms

$I_{\text{refmax}}$: Maximum peak current reference

$\Delta V_{\text{reg}}$: voltage regulation tolerance requirement

$\Delta I_{\text{eff}}$: effective inductor current step

$\Delta I_{L,\phi}$: the peak-to-peak inductor current ripple of a single phase buck converter

$\Delta I_{L}$: the total inductor current ripple of an $N$-phase interleaving buck converter

$\Delta V_{o,r,c}$: the output voltage ripple due to the charge variation of the capacitors

$\Delta V_{o,r,ESR}$: the output voltage ripple due to the ESR of the capacitors

$\Delta V_{o,r}$: the combined output voltage ripple
Chapter 1
Introduction

1.1 Challenges of Power Management

For more than four decades semiconductor manufacturers have been able to continually produce new and innovative products that deliver higher levels of performance and other user-valued capabilities. Most of these advances have resulted principally from the industry’s ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits, as shown in Fig. 1-1. The number of transistors on a chip continues to follow Moore’s law, doubling roughly every 18-24 months, while the feature size scales down by a factor of approximately 0.7 times during the same period [1-4]. According to Intel’s roadmap [5][6], over one billion transistors have been integrated in a single processor (Dual Core Intel® Itanium® 2 processor 9000 series, 1.72 billion transistors, 90nm manufacturing technology).

![Fig. 1-1 Continuous advancement of process technologies](chart.png)
Through advances in silicon technologies, the clock speed of Intel’s processors has dramatically increased from 0.1MHz to 3.2GHz in the years from 1971 to 2005, as shown in Fig. 1-2 [7-9]. However, while more and more transistors are integrated into one smaller die and operate at a higher frequency, processors will consume more power and generate more heat. The supply voltage must decrease to reduce power consumption. Fig. 1-3 shows Intel’s roadmap for the processor’s required current and voltage. In the near future, the supply voltage is going to drop to a level of 0.7V, while current is going to rise tremendously to a level of over 200A, which is a significant increase in total power consumption. Fig 1-4 shows industry’s history and forecast outlining the increasing power consumption of processors. Increasing power consumption and heat dissipation are becoming urgent challenges to today’s and future processors. Moore’s Law eventually will have to confront the laws of physics: those of power and thermal limitations. [85]
Fig. 1-3 Roadmap of the processor’s required voltage and current

Fig. 1-4 Increasing power consumption of processors

Power management is becoming more challenging than ever before in all segments of computer-based systems. While in the server domain, the cost of the electricity drives the demand
for low power systems, in mobile applications, battery life and thermal limitations are more important. As shown in Fig.1-4, power consumption was continuously and sharply increased before 2007, but due to the slow improvement of the thermal removal technology, the increasing speed of power consumption will slow down. By 2002, however, increasing power densities and the resultant heat began to reveal some limitations in predominantly using clock frequency as a way of improving performance. New thinking was required as to how to deliver new levels of performance within a given power envelope.

The best example of this new thinking is multi-core processors. Multi-core processors take advantage of a fundamental relationship between power and frequency. By incorporating multiple cores, each core is able to run at a lower frequency, dividing among them the power normally used by a single core. Fig. 1-5 illustrates this key advantage, showing that increasing the clock speed by 20% provides a 13% performance boost but a 73% increase in power consumption, while a dual-core approach results in a 73% performance boost for almost the same power. [9]

![Fig. 1-5 Multi-core energy efficiency performance](image)

Designing for energy-efficient performance is the key idea behind using multi-core processor technology to extend Moore’s law. One may expect high performance platforms using processors with tens or even hundreds of cores in the next decade. Such architectures will require
considerably more research into advanced power management technologies. Dynamically enabling/disabling one or multiple cores according to the workloads of the processor challenges the voltage regulator to maintain voltage regulation under high dynamic load, and deliver power efficiently. To enhance energy efficiency, system power management architectures with intelligent power capabilities are employed, in which processors need to closely interact with the voltage regulator (VR). At low CPU utilization, VR power losses may waste as much power as the processor consumes. The power losses of the VR are due to the need to deliver high current with quick response times. Communication between the CPU and the VR will help to improve power delivery efficiency by increasing VR efficiency. The CPU tracks its activities at all times and notifies the VR of its power status. The VR should have the ability to optimize its efficiency by entering either a dynamic phase enabling mode or an asynchronous operation mode depending upon the CPU utilization level. This feature is essential as computers spend a majority of their time in low utilization conditions. [11-13] [42-43]

These advanced control algorithms are resident in the VR controller. The voltage regulator must remain stable and satisfy all load line and tolerance band requirements when switching phases on and off, or using asynchronous operation mode. All these features are a challenge for VR controller design to provide intelligent power management ability and flexibility.

As shown in Fig. 1-6, in today’s processors, the CPUs keep in communication with the VR by Voltage ID and PSI-2 signals. In future processors, a dedicated power management bus may be needed for more advanced power management protocols. The intelligent management ability of the voltage regulator to handle more complicated communication will be necessary for future processors to enhance energy-efficiency performance. The next generation of voltage regulator modules (VRMs) may require digital power management control, beyond the capabilities of Voltage ID signals. A power management bus (PMBus), used to communicate with the host
system will be necessary to do system level power management to achieve high overall efficiency and good regulation. Depending on different applications, a communication bus may be chosen from among the following: I²C, SMBus, RS232/RS485, SPI bus, CAN bus, Ethernet, and USB [91-93]. Such system optimization through communication is just not achievable with today’s analog controllers.

![Communication interface between the CPU and the Voltage Regulator](image.png)

**Fig. 1-6 Communication interface between the CPU and the Voltage Regulator**

Great opportunities have been opened for digital control technologies since they exhibit significant advantages over conventional analog control methods for use in intelligent power management. Digital control has been receiving more and more attention, and the next generation VRM standard will put more emphasis on digital control because of how it facilitates the system level power management and efficiency improvement.

### 1.2 Power Delivery Architecture

Due to the large power levels in today’s processors, it is not uncommon to design a power delivery network with a sub-milliohm impedance target. With a traditional centralized power system, a silver box would deliver power directly to the CPU (such as a 486 processor), memory, hard drive and other parts in the computer. However, when Pentium processors were introduced
in the late 1990s, a dedicated voltage regulator module (VRM), usually drawing power from a 12V distributed bus, had to be placed as close as possible to processors to reduce the impedance associated with power delivery path [14]. Such a power delivery structure, called a hybrid power system (HPS), is shown in Fig.1-7. Multi-phase interleaved synchronous buck converters are common practice in today’s VRM designs, as shown in Fig.1-8 [14] [16-20].
With the increasing power consumption of processors, the dedicated VRM is placed as close as possible to the microprocessor to reduce the impedance of the power delivery path. Fig. 1-9 shows the typical power solution for today’s processors on LGA775 sockets. A three-phase synchronous buck converter is used as the dedicated VRM, which is placed so as to surround the microprocessor and delivers power to the microprocessor. Since the current drawn by the processor may increase suddenly, the impedance target needs to meet across a range of frequencies. A multi-stage decoupling solution with different types of capacitors is used. The high-frequency capacitors are placed on the land-side of the package, ceramic capacitors are used for mid-frequency decoupling and placed on the motherboard inside the socket cavity, and bulk capacitors are placed at the output of the voltage regulator to address low-frequency decoupling needs.

![Fig. 1-9 Power delivery solution for today’s processors](image)

The power delivery path can be modeled as the equivalent circuit shown in Fig.1-10 [42-43]. It includes the printed circuit board trace (represented in Fig 1-10 as "MB"), CPU socket ("Socket"), the interposer layer and the land grid array interconnects ("Package"), which could account for around 1mΩ of parasitic resistance and 120pH of parasitic inductance. However, in
future, with current requirements reaching over 200A, these interconnection parasitic resistances alone will produce a 40W power loss. [21][23]

![Fig. 1-10 The equivalent model of the power delivery path](image)

![Fig. 1-11 Intel’s roadmap for the processor’s maximum current slew rate](image)

Dynamic power management control in the multi-core processors switches from state to state according to computational needs [12]. The high clock frequency of the multi-core processors induces a very fast current slew rate (di/dt) when the processor changes from sleep state to full
power state and vice versa, or dynamically disables/enables one or multiple cores. The state transition frequency could reach up to hundreds of KHz. As shown in Fig. 1-11, the dynamic current slew rate will go up to 120 A/ns [4] [10]. The continuously decreasing supply voltage and very fast load transient slew rate, along with interconnection parasitic resistance and inductance on the power delivery path, have together raised a serious challenge for voltage regulation, especially since the allowed voltage regulation window has also become narrower to ensure effective logic identification. It will be very difficult for VRMs to meet the expected output voltage regulation window required by the next generation of processors.

Determining how to keep the output voltage within even narrower tolerance range will be the critical problem for VRM design. It could be predicted that a large number of output filter capacitors would be implemented to maintain the output voltage while enduring such a huge current transient slew rate. Fig. 1-12 shows a recommended example of a motherboard decoupling solution for Intel dual-core Xeon processor-based server platform [42-43]. It can be found that 17 Aluminum-Polymer bulk capacitors and a total of 54 ceramic capacitors were already employed. However, to handle the growing power consumption and increasingly violent load transients at low supply voltage required by future processors, the total decoupling capacitance required could reach 16.8mF with current VRM topology designs, occupying up to 30% of the motherboard area. It seems impossible to implement such a large number of capacitors within the tight space of the motherboard [21-22] [85]. With such a design, VRM manufacturing cost will also increase dramatically, which is unacceptable in very cost-competitive mass markets such as those for laptops and desktop PCs. Fig. 1-13 shows the cost breakdown of the voltage regulator.
Fig. 1-12 Motherboard decoupling solution for Intel dual-core Xeon processor-based server platform

In order to reduce the number of decoupling bulk/ceramic capacitors, the VRM should have fast transient response ability. With an analog control, the VRM must be able to operate at a significantly higher switching frequency to achieve a high control bandwidth. When the switching frequency was set at 2MHz and the control bandwidth was pushed to 350 KHz, only 1500uF ceramic capacitors were used [22][55]. However, with a multi-MHz switching frequency, switching losses, copper losses, and gate driving losses will significantly increase. It is even
worse in high-current applications, where large-die power MOSFETs or more parallel MOSFETs are used. This situation not only degrades efficiency, but also pushes the gate drivers to their thermal limitations, already a hot spot in VRM design.

Digital control methods have been introduced into VRM application areas, which enables the use of complicated control algorithms to achieve very fast transient responses. Non-linear control can break the relationship between the control bandwidth and the transient response in buck converters, which was investigated earlier for analog controls in [22][55][85]. In analog control designs, the feedback loop compensation is a compromise between stability and dynamic response performance. Using digital control techniques it is possible to construct non-linear, or adaptive, control loops that change the compensation as a function of operating conditions, which make it possible for a low-bandwidth VRM to exhibit very fast transient response. Fewer output decoupling capacitors will be required to ensure a given voltage tolerance with resulting savings in cost and component space.

1.3 Digital Power Management Control

Digital control techniques inherently enable intelligent power management ability, which is necessary for VRs delivering power to future processors. Digital control in power supplies is considerably more flexible than analog control in its ability to adapt to changes and digital control inside the power supply results in advantages to the overall system such as improved efficiency, fewer external components and reduced overall cost. The embedded digital control circuitry in the power supply can also be used for system power management purposes. Flexibility is one of its key attributes, such that power system designers may choose features and capabilities that are important for a specific application. Various analysis, design and implementation aspects of this emerging area are receiving increasing attention. [24-34] [86]
Fig. 1-14 Typical block diagram of a digital power management controller

Fig. 1-14 shows a typical block diagram of a digital power management controller for a switching-mode power converter delivering power to a microprocessor. Typically, the digital power controller uses analog-to-digital converters (ADCs) to sample analog power supply variables, such as voltages, currents, and temperature. These quantities are processed by a digital control algorithm unit implemented in the controller. The control algorithms are stored in the on-chip ROM and downloaded from the ROM at power-up or reset. These control algorithms calculate control signals that are converted to switch on/switch off command sequences by a digital pulse-width modulator (DPWM). All values of parameters such as output voltage, output current and temperatures are stored in an EEPROM at manufacturing or via transfer with a communications bus. The EEPROM content is downloaded to the RAM during power-up and the embedded microprocessor then uses this part of the memory for read/write operations. Complicated power management functions such as efficiency optimization, control-law adaptation and fault diagnostics are performed by the embedded microprocessor, which communicates with both the microprocessors and the power management host system.
1.3.1 Advantages

The use of digital techniques enables capabilities for performance improvement both in the power supply and system levels that are not possible with analog techniques. Salient features of the digital-power-controller architecture are listed below.

1) Enables complex control algorithms

Digital controllers allow the use of control algorithms that are considered impractical for analog realization. Digital control algorithms can be arbitrarily described at the function level using a high level language or a hardware description language. Non-linear decision-making, which is possible with digital control allows for algorithms not possible or overly cumbersome with analog circuits. The use of advanced control methods can improve the converter performance in a number of ways. The feedback and feed-forward control laws can be adaptively tuned to optimize system performance, and on-line system identification and control-law tuning can reduce the need for application-specific customization and the co-requisite human designer expertise. Estimators or state observers can be implemented to simplify sensing requirements, and an adaptive mode control can be used to maximize efficiency over a wide range of loading conditions and component tolerances. [87][94]

Moreover, in analog control designs, feedback loop compensation is a compromise between stability and dynamic response performance. However, by using digital control techniques it is possible to construct non-linear, or adaptive, control loops that change the compensation as a function of operating conditions. That is, the power supply can display fast response when it needs to and slower response in other situations, thus optimizing steady state as well as transient response. The relationship between the control bandwidth and the transient response can be decoupled by non-linear control, thus requiring fewer output decoupling capacitors for a given voltage tolerance, with resulting savings in cost and component space.
2) **Flexible, synthesizable and programmable**

   The use of software or programmable memory to change the controller functionality makes a system based on a digital controller very flexible. The digital controller offers the ability to add, eliminate or change system parameters in order to meet new requirements, and the configurability of a system with digital control can allow it to cope with significantly different operating conditions. For example, the same voltage regulator module (VRM) can be programmed to meet different design specifications, allowing the supplier to have a single module that meets several design points. Moreover, a large portion of the digital controller circuitry, except for the analog-to-digital interface, is synthesizable. Existing computer-aided design (CAD) tools can be used to reduce design effort and facilitate portability to new processes, and hence decrease the time-to-market [87] [94].

3) **Insensitive to component tolerance**

   Analog controllers suffer from component tolerance variation and drift due to ambient conditions and aging. A digital compensator can precisely position poles and zeros to the frequency tolerance of the system clock, whereas component tolerances result in 10% or higher pole/zero variations in an analog controller. A digital control also offers adaptability of the system to compensate for analog components’ aging. [94]

4) **Allows intelligent management**

   Due to the ease of integrating communication capabilities, the digital controller can communicate with other host systems to store voltage or current data and to do real-time optimization. Moreover, it is feasible for a digital power management controller to communicate with the processor it is supplying, which will help improve power delivery efficiency—including VR efficiency. According to processor utilization, the VR should have the ability to optimize its efficiency by entering either a dynamic phase enabling mode or an asynchronous operation mode.
This feature is essential as PC processors spend 80% of their time in low utilization conditions [88-89]. Light load efficiency and power loss improvements can be accomplished by dynamic phase enabling, providing roughly a 2% improvement in efficiency [43]. Dynamic voltage scaling is another commonly-used method in microprocessor systems to improve efficiency [34-35]: the microprocessor estimates its workload and commands the voltage regulator to adjust the supply voltage, ensuring high throughput at heavy load, and low power at light load. In the future, the microprocessor could also provide a fast, predictive, load-current estimate to the voltage regulator, improving the converter transient response [87] [94].

1.3.2 Recent advances in Digital Control Technologies

With the advances in digital technology, digital control has become increasingly attractive. Solutions using a digital controller have become more feasible, varying from the use of DSP, microprocessors, and FPGA, to software-programmable mixed-signal ICs. A lot of research has been performed in digital control of switching power converters, which are applied in the voltage regulators for processors, and significant progress has been made.

Normally, analog control provides a very fine resolution to position output voltage. Output voltage can be adjusted to any arbitrary value, limited only by loop gain and noise levels. However, a digital controller has a finite set of discrete levels, since quantizing elements—the ADC and the DPWM—exist in the digital control loop. Thus, quantization of the ADC and DPWM is critical to both the static and dynamic performance of power converters.

1.3.2.1 Analog-to-Digital Converters

The resolution of the ADC has to be such that the output voltage error of the power modules tightly falls within the allowed voltage range. That is, the product ($V_{LSB}$) of the least significant bit (LSB) of the ADC has to be less than the allowed maximum scaled output voltage variation
(\Delta V_o \times H), where \( H \) is the scaled factor of the voltage sensor. For a VRM with a 1.5V output voltage and a 5mV allowed voltage variation, if the reference voltage is 1.5V and the voltage scale range of the ADC is 1.8V, a minimum of 9 bit resolution will be required for the ADC.

Dedicated VRMs for recent or future processors supply a large current with a very fast current slew rate. Thus, high dynamic performance is necessary for VRMs, and extremely fast response is one of the most important dynamic criteria. When the AD converter is involved in the digital control loop, ADC architectures with low latency are desirable, since an ADC adds a delay according to \( e^{-aT_{adc}} \), introducing a phase shift into the loop that may degrade system response. \( T_{adc} \) is the sampling period of the ADC. Therefore a very high operating clock is needed for the ADC to achieve high dynamic performance.

1.3.2.2 Digital pulse width modulator

A digital pulse width modulator (DPWM) produces a discrete and finite set of duty ratio values. From the output point of view in steady state, only a set of discrete output voltages is possible. The resolution of the DPWM must be high enough to avoid a phenomenon known as limit cycle oscillation, where the output goes into an oscillation of fixed amplitude and frequency irrespective of the initial state. A necessary condition to avoid limit cycle oscillation is that the change in the output voltage caused by one LSB change in the duty cycle ratio has to be smaller than the analog equivalent of the LSB of the ADC. The minimum number of DPWMs depends on the topology, the output voltage and the ADC resolution.

Three types of DPWM topologies are usually used in contemporary designs: the fast counter-comparator scheme, the tapped delay-line scheme, and the ring-oscillator-MUX scheme.

1) Fast counter-comparator scheme
The simplest method to generate DPWM signals is the fast counter-comparator scheme [36] [37], which uses a system counter \((n\) bits) to generate the fixed sampling. The resolution of DPWM signals is therefore \(1/2^n\). By comparing the counter value and the numerical duty cycle value, the switch of the converter is turned on/off. This scheme is very simple and easy to implement. The fast counter-comparator takes a reasonably small die area but the power consumption is relatively large, since a high frequency clock and other related fast logic circuits are needed to achieve a high enough resolution based on a high switching frequency. For a 10 bit DPWM based on a 1MHz switching frequency, the clock frequency required would be 1.024GHz. This is far too high and unacceptable for practical use. For VRMs with a multi-phase synchronous buck converter architecture, the system counter can be shared by all phases, shifting the turn-on signal for each phase by a certain phase degree.

2) Tapped delay-line scheme

A tapped delay-line scheme is proposed in [24]. Power is significantly reduced with respect to the fast counter-comparator scheme since the fast clock is replaced by a delay line that runs at the switching frequency of the converter. In this scheme, a pulse from a reference clock starts a cycle and sets the DPWM output to go high. The reference pulse propagates through the delay line, and when it reaches the output selected by the multiplexer, the DPWM output goes low. The total delay of the delay-line is adjusted to match the reference clock period.

The main drawback is that the size of the MUX grows exponentially with the number of resolution bits \(n\). In a multiphase controller, precise delay matching among the phases places a stringent symmetry requirement on the delay line, so it is not well suited for multiphase applications [33]. However, these concerns may be relieved to a certain degree by the combination of a delay-line and counter-comparator scheme, which is presented in [25].
3) **Ring-Oscillator-MUX scheme**

A ring-oscillator-MUX scheme is presented in [33]. It has area and power considerations similar to those of the delay line approach. In this scheme, the ring oscillator in the DPWM runs in current starved mode, and the frequency can be controlled by adjusting the supply current to the entire ring. Thus, the switching frequency of the converter can be locked to an external clock by controlling the DPWM ring current. The advantage of ring-oscillator-MUX over the delay line structure is that it has a symmetric structure. Therefore, it is well suited to multi-phase applications.

However, for all these DPWM topologies, power consumption and core area will increase significantly when the number of bits of DPWM reaches 10 to 12, which is usually needed in most VRM designs.

To decrease power consumption and core area, a dithering method is proposed as a soft method to increase the effective resolution of a DPWM module without increasing the hardware resolution. The idea behind digital dither is to vary the duty cycle over a few switching periods, so that the average duty cycle has a value between two adjacent quantized duty cycle levels. The averaging action is implemented by the output filter. However, the drawback of the dithering method is low system bandwidth and low-frequency output voltage ripple [32].

### 1.3.2.3 Digital control algorithms

The most important advantage of digital control is enabling advanced control algorithms. When high enough resolution ADC and DPWM make it viable for power converters, new advanced digital control algorithms can take advantage of digital circuits and improve the system performance, especially dynamic performance. A body of research has investigated digital control algorithms. Architecturally, digital control falls into three structures: linear control, non-linear
control and hybrid versions. Linear digital control methods, such as z-domain PID control, are translated directly from those widely used in analog control circuits, while providing comparable performance. By comparison, non-linear digital control method, such as sliding mode, hysteretic, table lookup, fuzzy control, predictive control, adaptive control, and multi-mode control can improve dynamic performance, as well as static performance. Non-linear control may also be added to linear control to form a hybrid linear-non-linear control.

However, the drawback of these higher dynamic and static performances is heavy computing effort in the digital controller, which may result in significant delay, large power consumption and a big core area.

1.3.2.4 Digital Controller with Digital-To-Analog Converters

A digital controller with two digital-to-analog converters (DAC) was proposed in [95], which was based on variable frequency peak current mode control. Two low-resolution DACs were used to replace the high resolution ADC and DPWM, thus significantly reducing system complexity and die area. The basic idea behind this control method was trying to generate a voltage sawtooth waveform in each period or phase period, compared to the feedback error voltage (fixed voltage reference) to generate control signal, which is like its analog counterpart.

Main drawbacks of this digital controller are listed as follows:

a) **Low dynamic performance**: the peak current reference is updated every switching cycle, which cannot take advantage of high speed clock. Hence, the delay is significant, which degrades dynamic performance.

b) **High speed clock required**: the clock of target FPGA/DAC is limited by the switching frequency, the number of phases and switching frequency variation range. It is difficult to design a 5 phase 1MHz/phase buck converter at 80MHz clock with this approach.
c) **Variable frequency operation:** it may result in larger sizes of input and output filters.

### 1.4 Thesis Objective

In general, when digital control is applied in a processor-dedicated voltage regulator, the most significant technical limitation is the delay associated with the sampling process and discrete-time computation. There is generally a trade-off between the sampling and computation frequency, and the controller power use and the controller cost. Thus, a strong reduction of system complexity, die area and dissipated power, while maintaining high performance that meets the voltage regulator requirements, is a key design goal, especially when high-volume, low-cost integrations are targeted. The current approaches of designing the digital controllers, as described above, are good but do not meet all these requirements concurrently.

The following are the objectives of this thesis:

1) Development of high performance digital control techniques for powering microprocessors, which should have a low complexity architecture and high dynamic performance. Simple DACs should be used to replace high resolution ADCs; and the duty cycle command should be updated every DAC clock to improve the load transient response.

2) Modeling and analysis of the voltage regulators with the proposed digital controller to study their steady-state and dynamic performance.

3) Development of advanced control algorithms to further improve dynamic performance, while lowering high speed requirement of DAC clock.

4) Simulations and experimentations to verify the proof-of-concept and performance.
1.5 Thesis Organization

In Section 1.2, it was predicted that the VRM must use many output capacitors to sustain the output voltage required to meet processor load transient requirements. The tremendous bulk capacitors result in large sizes and high costs. To reduce the size and cost, the adaptive voltage positioning (AVP) concept has been widely used in recent voltage regulator designs. With AVP control, the output capacitors can be roughly halved [44-46].

In Chapter 2, a novel digital adaptive voltage positioning (digital AVP) technology is introduced. An AVP control unit is generalized to achieve AVP for VRMs, which is identified by the uniqueness of dynamic voltage reference and dynamic current reference. As one possible configuration, a digital controller with fixed-frequency peak current mode control is used to demonstrate the operation. Two digital-to-analog converters (DACs) are used instead of analog-to-digital converters. Compared to ADCs, DACs are much simpler, have less delay, and save core area and power consumption. A straightforward control law is implemented to realize the AVP control and no compensator is involved in the control loop. Only the addition computation and simple control logic are needed in the controller, which also significantly reduces the computation delay. Since the duty cycle is updated at every DAC clock, the VRM with the proposed digital controller exhibits a very fast transient response. Steady state analysis is performed to demonstrate the digital controller operation. After that, a small signal model is explored to determine system stability. Then, a switching stability constraint is derived to give the minimum output capacitance requirement. Finally, a two-phase 12V-to-1V/40A 250 KHz synchronous buck converter with proposed digital controller is designed to verify the theoretical analysis by simulations and experiments.

In Chapter 3, the output voltage variation is explored during a large step load transient, which also gives the critical output capacitor requirement during load transient up/down. After that, the
relationship between the transient response and the DAC operation clock (or reference update clock) is derived, stating that when the constraints on the DAC operation clock are not met, the critical output capacitor requirement should be modified. To break the constraints on the DAC operation clock reference, a dynamic reference step adjustment is introduced. With this method, both the transient response and steady-state performance will not degrade when the DAC operation clock decreases. To reduce the transient-assertion-to-action delay, non-linear control is introduced into the controller. With this control, the maximum inductor current slew rate is obtained and the transient-assertion-to-action delay is minimized to save on the number of output capacitors. Then, a dedicated transient detection circuit is implemented to detect the load transient, so that the larger the load current transient step or the faster the load current transient slew rate, the faster the output voltage drops or ascends, and the earlier the transient state status will be asserted. Finally, the dual voltage loop control is addressed, which integrates all these methods to achieve a fast transient response speed. Simulation and experimental results demonstrate a dynamic performance improvement using these methods.

In Chapter 4, the power delivery path impedance with the proposed digital control is analyzed. The power path impedance over a wide range of frequencies is given. When load oscillation frequency approaches or exceeds the VR control bandwidth, the power delivery path impedance will be dominated by the bulk capacitors, the filtering capacitors and interconnection resistance/inductance. Time domain validations must be done to ensure that the output voltage does not violate the tolerance range under large-step load oscillation over frequencies from DC to \( F_{\text{break}} \). Load oscillation testing in simulation and experiment prove the operations of the voltage regulator with the proposed digital controller, without violating the voltage tolerance range under large-step load oscillation over the wide range of frequency.
Finally, Chapter 5 summarizes the contributions of this dissertation and suggests directions for future research.
Chapter 2

Digital Adaptive Voltage Positioning Techniques

2.1 The Concept of Adaptive Voltage Positioning Control

As the dedicated power supply for processors, the VRM must deliver a large amount of current to processors with a large current step change and high current slew rate, while maintaining a low output voltage within a tight tolerance range. The parasitics (equivalent resistance and inductance) of the power delivery make it even more difficult to maintain the supply voltage within the tolerance range.

To meet such load transient requirements, the VRM must use many output capacitors to sustain the output voltage. The large number of bulk capacitors result in large sizes and high costs. To reduce size and cost, the adaptive voltage positioning (AVP) conception has been widely used in recent voltage regulator designs. The AVP feedback control will not always keep the output voltage fixed at the same level regardless of the load current, but rather will position the output voltage at different levels according to the load, a slightly lower level at heavy load and a slightly higher at light load. As a result, the whole voltage tolerance range can be used for the voltage overshoot or undershoot limit during the transient. Fig. 2-1 illustrates the concept of AVP. Obviously, with the AVP control the voltage undershoot or overshoot window during load transient is larger than the voltage undershoot or overshoot window of non-AVP control. While non-AVP control only uses part of the tolerance range during load transient up or down, the AVP control takes advantage of the whole tolerance range. Thus fewer output capacitors are required in VRMs with AVP control, resulting in smaller sizes and less cost. [38-47]
Design specifications for today’s processor voltage regulators require that the processor supply voltage follows a prescribed load line with a slope of about one milliohm [42-43]. To ensure processor reliability and performance, the power delivery platform—including voltage regulators and decoupling capacitors—should always keep platform transient-droop and overshoot noise level contained in the load-line window \((V_{\text{min}} - V_{\text{max}})\) over the load oscillation frequency range from DC up to 1MHz. Fig. 2-2 shows an example of the required power distribution impedance over the frequency range [42-43]. To take advantage of the entire voltage tolerance window during load transient, any large oscillations after load transient between the two steady-state stages are not accepted. Hence, this necessitates tight regulation of the VR output impedance within its bandwidth.
Chapter 2 Digital Adaptive Voltage Positioning Techniques

Fig. 2-2 Power distribution impedance over DC to 1MHz frequency range [43]

Carefully comparing the current and the related output voltage waveforms in Fig. 2-1, in the steady state, the VRM is an ideal voltage source in series with a resistor $R_o$, whose output voltage is expressed as

$$V_o = V_{o\text{max}} - I_o \cdot R_o \ .$$  \hspace{1cm} (2.1)

The equivalent circuit of a VRM with ideal AVP control is illustrated in Fig. 2-3.
Hence, carefully designing a feedback loop to ensure that the converter has constant output impedance is the basic idea to achieve AVP. To suppress the voltage oscillation after large load transients, the output impedance should be optimized to be resistive. Much research has been conducted to try to improve the static or dynamic performance of a VRM based on this concept [44-52].

AVP control based on active droop feedback control [45], feedback current-mode control [49,54,55] and feedback voltage-mode control with load current injection [47, 53, 55], have been presented in the literature, using power trains with electrolytic output capacitors, where the closed-loop output impedance is set equal to the output capacitor effective series resistance (ESR). However, it is sometimes impossible to design constant output impedance with voltage mode control. In current-mode control, the AVP design depends on the accuracy of the DC gain. An active droop control method may solve these problems by using an infinite DC gain design [85]. However, the time constant of the output filtering capacitor has a significant impact on the feedback loop design and the converter performance. It is difficult to precisely achieve the desired output impedance.

2.2 Proposed Digital Controller with AVP Control

2.2.1 The AVP Control Unit

As mentioned above, the nature of AVP is to design the output impedance ($R_o$) of the VRM to be a constant value. With AVP control, the output voltage ($V_o$) will decrease while the output current ($I_o$) increases and vice versa, which has been expressed in equation (2.1).

Differentiating equation (2.1), the output impedance of the VRM can be derived as
\[ R_o = -\frac{dV_o}{dI_o}, \quad (2.2) \]

and by digitalizing this equation, the digital expression of the output impedance will be obtained:

\[ R_o = -\frac{\Delta V_o}{\Delta I_o}. \quad (2.3) \]

Based on equation (2.3) above, an AVP control unit is proposed here to achieve the desired AVP control. The idea is to separately adjust the voltage reference \( V_{\text{ref}} \) and the current reference \( I_{\text{ref}} \). Related to the nature of AVP, the voltage reference \( V_{\text{ref}} \) should decrease while the current reference \( I_{\text{ref}} \) should increase, that is, \( V_{\text{ref}} = V_{\text{max}} - I_{\text{ref}} R_o \). By closing the current/voltage control loop, the output voltage can be regulated by the relationship

\[ V_o = V_{\text{ref}} = V_{\text{max}} - I_{\text{ref}} R_o = V_{\text{max}} - I_o R_o, \]

where \( R_o \) is the desired output impedance of the regulator. Obviously, the AVP can be realized naturally here.

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**Fig. 2-4 Block diagram of the proposed control idea**
Fig. 2-4 shows a block diagram of the AVP control unit, which generates voltage and current references according to the desired output impedance. It is identified by the uniqueness of dynamic voltage/current reference. To generalize this control idea, a control function $f(z)$ is used to represent the relationship function between the voltage reference variation step $\Delta V_{ref}$ and the current reference variation step $\Delta I_{ref}$, which is expressed as

$$\Delta I_{ref} = f(z) \cdot \Delta V_{ref}.$$  

(2.4)

Since AVP is related to the steady state operation of the regulator, the AVP control will be achieved if we make

$$f(z \to 1) = -1 / R_o.$$  

(2.5)

Obviously, the simplest control function is

$$f(z) = -1 / R_o.$$  

(2.6)

The AVP control discussed here is for steady state operation only. Making a smooth transition between two steady-states to achieve good dynamic performance is another task of the controller. To this end several control methods can be utilized in addition to AVP control, such as dynamic reference step adjustment or non-linear control.

### 2.2.2 Basic Configuration and Control Law

From the description of the control idea, we know that the inductor current is regulated by the current reference, therefore current mode control must be used to tightly regulate the output current in this case. Either peak current mode control or average current mode control can be applied. The voltage reference is passively adjusted to follow the output voltage. The driving factor for adjustment drive is the change in load current: the difference between the load current
and the average inductor current results in an output voltage variation that the voltage reference will follow/mimic.

There are a number of options for constructing such an AVP control model, including decisions about where the analog-to-digital conversion or the digital-to-analog conversion is performed and whether to use peak or average current control. Four potential configurations to implement an AVP control unit will be examined.

Fig. 2-5 Configurations of the digital controller with peak current mode control

Fig. 2-5 shows two possible configurations of the digital controller with peak current mode control. The AVP control function $f(z)$ is the key method of realizing AVP control, which generates digital current and voltage references. In Fig. 2-5 (a), two digital-to-analog converters are implemented to generate the current and voltage references. One analog comparator is used to compare the output voltage with the voltage reference and another is used to compare the inductor current with the (peak) current reference. In Fig. 2-5 (b), one analog-to-digital converter
replaces the digital-to-analog converter for digitalizing the sensed output voltage and the voltage comparator is moved into the digital block. One digital-to-analog converter is also used to generate the peak current reference, which is compared with the inductor current to achieve current regulation.

**Fig. 2-6 Configurations of the digital controller with average current mode control**

Fig. 2-6 shows two configurations of the digital controller with average current mode control. Once again \( f(z) \) is the key to realizing AVP control, but in this case, an average current compensator is implemented to calculate the duty cycle. In Fig. 2-6 (a), one analog-to-digital converter is used to digitalize the sensed inductor current while a digital-to-analog converter generates analog voltage reference from the digital voltage reference. One analog comparator is used to compare the output voltage with the voltage reference. In Fig. 2-6 (b), just as in Fig. 2-5 (b), the digital-to-analog converter is replaced by an analog-to-digital converter for digitalizing the sensed output voltage and the voltage comparator is moved into the digital block.
All four of these configurations can realize AVP control by implementing the AVP function \( f(z) \) block. The digital controllers with peak current mode control have simple structures, but they may suffer poor noise immunity, slope compensation may be required in some high-conversion-ratio applications and there is often peak-to-average current error. The digital controllers with average current mode control can eliminate these problems, but they have complicated structures. The average current compensator increases the computing effort of the controller, and high resolution ADC and DPWM are needed, which results in a large core size and a high cost.

The digital controller with peak current mode control in Fig. 2-5 (a), which has the simplest structure, will be used to illustrate the operation of the proposed digital controller with AVP control.

The configuration of the proposed digital controller with peak current mode control is redrawn in Fig. 2-7 along with a single phase synchronous buck converter. The digital controller consists of a Digital Control Algorithm Block, a Digital Pulse Width Modulation (DPWM) Block, two Digital-to-Analog Converters (\( DAC_{Iref} \) for current reference and \( DAC_{Vref} \) for voltage reference), and two comparators (Comparator \( I \) and Comparator \( V \)). The control algorithm is implemented in the digital control algorithm block to obtain the desired reference current data and the desired reference voltage data. The DAC (\( DAC_{Iref} \)) receives the reference current data from the digital control algorithm block to generate the peak current reference \( I_{ref} \). The other DAC (\( DAC_{Vref} \)) receives the reference voltage data from the digital control algorithm block to generate the voltage reference \( V_{ref} \). Comparator \( I \) compares the generated peak current reference \( I_{ref} \) with the inductor current \( i_L \) which is sensed by the \( R_i \) block. The comparison result \( CI \) is sent to the digital control algorithm block and the DPWM block. The DPWM block generates the gate driving signals to control the MOSFETs (\( M_1 \) & \( M_2 \)). Comparator \( V \) compares the generated voltage reference \( V_{ref} \) with the output voltage \( V_o \) that is sensed by the \( H \) block. The comparison result \( CV \)
is sent to the digital control algorithm block which adjusts the current reference data and the voltage reference data according to the control law.

![A single phase buck converter with the proposed digital controller](image)

**Fig. 2-7 A single phase buck converter with the proposed digital controller**

The proposed digital controller will operate in fixed-frequency peak current mode control (PCM). The turning-on of the high-side switch M1 and the turning-off of the low-side synchronous switch M2 are scheduled by the timing of the DPWM module. The high-side switch M1 and the low-side synchronous switch M2 are turned off and on, respectively, according to the comparison result \( CI \); that is, if the inductor current reaches the peak current reference set by the DAC (\( DACI_{\text{ref}} \), high-side switch M1 will be turned off and low-side synchronous switch M2 will be turned on.
In order to implement adaptive-voltage-positioning (AVP), the voltage reference $V_{\text{ref}}$ should decrease while the current reference $I_{\text{ref}}$ increases, and vice versa. The variation of the current reference $I_{\text{ref}}$ should be tracked tightly by the variation in the voltage reference $V_{\text{ref}}$. However, in view of a practical controller, the variation of the current reference is driven by the variation of the voltage reference. The load current variation first results in the variation of the output voltage, because the current difference between the load current and the inductor current is absorbed by the output bulk capacitors. So, a main idea of the control law is to ensure that the voltage reference tightly follows the output voltage. If the load current increases, the output voltage will drop, then the voltage reference will also decrease to follow the output voltage, and in the AVP concept, the current reference should increase correspondingly, until a new steady state is established. If the load current decreases, the output voltage will rise, the voltage reference will also increase and the current reference should decrease correspondingly, until a new steady state is established.

Therefore, this straightforward adjustment control law to achieve AVP is summarized as follows:

a. If logic signal $CV$ is high ($CV=1$), that is, the output voltage $v_o$ exceeds the voltage reference $V_{\text{ref}}$ set by the voltage DAC, the voltage reference $V_{\text{ref}}$ will increase by a small amount $\Delta V_{\text{ref}}$ and the peak current reference $I_{\text{ref}}$ will decrease by a small amount $\Delta I_{\text{ref}}$. If $V_{\text{ref}}$ reaches its allowed maximum value, no change will be made on $V_{\text{ref}}$.

b. If logic signal $CV$ is low ($CV=0$), that is, the output voltage $v_o$ is smaller than the voltage reference $V_{\text{ref}}$, the voltage reference $V_{\text{ref}}$ will decrease by a small amount $\Delta V_{\text{ref}}$ and the peak current reference $I_{\text{ref}}$ will increase by a small amount $\Delta I_{\text{ref}}$. If $V_{\text{ref}}$ reaches its allowed minimum value, no change will be made on $V_{\text{ref}}$. 

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Obviously, no compensator is involved in this control law, and only the addition computation and simple control logic are required in the controller. The use of low-complex DACs and straightforward control law make the proposed digital controller very suitable for high-volume low-cost low-dissipated-power integrations.

2.2.3 Steady State Operation

![Waveforms](image)

Fig. 2-8 Typical steady-state operation waveforms

Fig. 2-8 shows the steady state operation waveforms of the buck converter with the proposed digital controller. As described above, the buck converter is operating under fixed switching frequency peak current mode control. The turn-on of high side switch M1 and the turn-off of the low side switch M2 are scheduled by the system clock, which serves as a low resolution DPWM. The inductor current $i_L$ is sensed by the gain $R_i$ and compared to the current reference $I_{ref}$ that is
generated by the current reference DAC (\(DAC_{\text{Iref}}\)). Once the inductor current reaches the set peak current reference \(I_{\text{ref}}\), the high side switch M1 is turned off and low side switch M2 is turned on.

The following assumptions are made to simplify the steady state analysis:

1) the clock works as the operating clock for both the target FPGA and the two DACs;
2) there are four clock periods in one switching cycle;
3) the output voltage ripple is neglected to simplify the analysis; and
4) circuit delay is assumed to be zero.

In Fig. 2-8, before \(t_0\), the power circuit operates in a steady state. At \(t_0\), the rising edge of the first clock cycle in one switching cycle, the switch M1 is turned on and the switch M2 is turned off as scheduled in the DPWM module, while the inductor current \(i_L\) increases linearly. At \(t_1\), the sensed inductor current \(i_L\) reaches the peak current reference \(I_{\text{ref}}\), and the logic comparison result \(C_I\) shown in Fig. 2-7 turns high, logic ‘1’. Then switch M1 is turned off, switch M2 is turned on, and the inductor current \(i_L\) decreases linearly. In the first clock period, the voltage reference \(V_{\text{ref}}\) is larger than the output voltage \(v_o\), and the logic comparison result \(CV\) becomes the low level, logic ‘0’. As a result, at \(t_2\), the rising edge of the second clock cycle, the voltage reference \(V_{\text{ref}}\) decreases by a small amount \(\Delta V_{\text{ref}}\) and the peak current reference \(I_{\text{ref}}\) increases by a small amount \(\Delta I_{\text{ref}}\). During the second clock period, the voltage reference \(V_{\text{ref}}\) is smaller than the output voltage \(v_o\), and the logic comparison result \(CV\) becomes high, logic ‘1’. As a result, at \(t_3\), the rise edge of the third clock cycle, the voltage reference \(V_{\text{ref}}\) will increase by a small amount \(\Delta V_{\text{ref}}\) and the peak current reference \(I_{\text{ref}}\) decreases by a small amount \(\Delta I_{\text{ref}}\). Both the voltage reference \(V_{\text{ref}}\) and the current reference \(I_{\text{ref}}\) vary by steps (\(\Delta V_{\text{ref}}\) and \(\Delta I_{\text{ref}}\)) according to the logic comparison result \(CV\) in the previous clock period, and so on. At \(t_4\), new switching cycle begins.
According to the above description, it is found that the digital controller updates the voltage reference and the current reference at every DAC clock cycle. Normally, the DAC clock is much faster than the switching clock. Hence, this digital controller exhibits big advantages in load transient response performance over other digital controllers, which only update duty cycle at every switching clock.

2.2.4 Steady State Analysis

In Fig. 2-8, we can see that even in the steady state both the voltage reference and the current reference are always varying. This is a feature unique to this proposed digital controller. In the steady state, the average output voltage $< V_o >$ tracks tightly with the average voltage reference $< V_{ref} >$, while the error between them is within $\Delta V_{ref}$. If $\Delta V_{ref}$ is smaller than the voltage ripple $\Delta V_{p-p}$, the voltage reference also will reflect the shape of the voltage ripple. Also, the peak inductor current $I_{pk}$ keeps tightly in step with the peak current reference $I_{ref}$, which has a similar shape to $V_{ref}$ and has the average value $< I_{ref} >$.

For the buck converter in continuous current mode (CCM), the average inductor current $< I_L >$ is estimated as

$$I_o = (< I_L >) = I_{pk} - \frac{\Delta I}{2} = I_{pk} - \frac{V_o \cdot (1 - D) \cdot T_{sw}}{2L_f},$$  \hspace{1cm} (2.7)

where $D$ is the duty ratio, $T_{sw}$ is the switching period, and $\Delta I$ is the current ripple amplitude.

The circuit delay from command to action results in a current error between the peak current reference $I_{ref}$ and the peak inductor current $I_{pk}$, calculated as
\[ I_{err} = I_{ref} - I_{pk} = -t_d \frac{V_o \cdot (1 - D)}{D \cdot L_f}, \quad (2.8) \]

where this circuit delay \( t_d \) includes the high-side MOSFET M1 turn-off delay, current detection delay, and controller computing delay. It should be carefully evaluated during design to achieve accurate AVP control.

For a given design, which is assumed to have constant input voltage and output voltage, the duty cycle \( D \) is constant; therefore, combining (2.7) and (2.8) and differentiating, the variations on the output current \( I_o \) and the current reference \( I_{ref} \) are given as

\[
\Delta I_o = (\Delta < I_L >) = \Delta I_{pk} = (\Delta < I_{ref} >) = \Delta I_{ref}.
\]

(2.9)

With the outer voltage loop closed, the voltage reference follows the output voltage. Hence, variations on the output voltage and the voltage reference can be calculated as

\[
\Delta V_o = (\Delta < V_o >) = (\Delta < V_{ref} >) = \Delta V_{ref}.
\]

(2.10)

If an \( m \)-bit digital-to-analog converter is used for generating the current reference and an \( n \)-bit digital-to-analog converter is used for generating the voltage references, then
\[
\Delta I_{\text{refLSB}} = \frac{I_{\text{ref max}}}{2^m},
\]

(2.11)

\[
\Delta V_{\text{refLSB}} = \frac{\Delta V_{\text{tol}}}{2^n},
\]

(2.12)

\[
\Delta I_{\text{ref}} = M \cdot \Delta I_{\text{refLSB}}, \quad \text{and}
\]

(2.13)

\[
\Delta V_{\text{ref}} = N \cdot \Delta V_{\text{refLSB}},
\]

(2.14)

where \(\Delta I_{\text{ref}}\) is the predefined adjustment step of the peak current reference \(I_{\text{ref}}\) which is \(M\) times the least significant bit (LSB) of the current DAC (\(DAC_{\text{Iref}}\)), and \(\Delta V_{\text{ref}}\) is the predefined adjustment step of the voltage reference \(V_{\text{ref}}\) which is \(N\) times the least significant bit (LSB) of the voltage DAC (\(DAC_{\text{Vref}}\)); \(\Delta V_{\text{tol}}\) is the maximum allowed voltage tolerance.

Fig. 2-10 The equivalent circuit of the buck converter with the proposed digital controller

According to the control law described above, when the output current \(I_o\) increases by \(\Delta I_o\), the output voltage \(V_o\) decreases by \(\Delta V_o\), vice versa. Obviously, while there is no load (\(I_o\)), the output voltage \(V_o\) has its largest value (assume to be \(V_{\text{omax}}\)). So, the buck converter with the proposed digital controller can be modeled as an ideal voltage source \(V_{\text{omax}}\) in series with an equivalent resistor \(R_o\). The equivalent circuit is shown in Fig. 2-10. \(R_o\) is approximated as
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\[
R_o = \frac{\Delta V_c}{\Delta I_o} = \frac{\Delta V_{\text{ref}}}{\Delta I_{\text{ref}}} = \frac{\Delta V_{\text{tol}}}{I_{\text{ref max}}} \cdot \frac{N}{M} \cdot 2^{m-n} \quad . \tag{2.15}
\]

Obviously, constant output impedance \(R_o\) is achieved with this proposed controller, which is independent of the equivalent series resistance \(ESR\) of the output capacitor \(C_f\). From the equivalent circuit, we can conclude that

\[
V_o = V_{\text{omax}} - I_o \cdot R_o \quad . \tag{2.16}
\]

Therefore, typical adaptive voltage position (AVP) control is realized in the steady state, without considering the effect of the output capacitors at high frequency domain. Obviously, varying the ratio \(N/M\) will adjust the output impedance \(R_o\). Normally, to make a design simple, we will let \(n\) equal \(m\) and \(N\) equal \(M\) \((N=M=1)\).

Fig. 2-11 shows the current source equivalent circuit of the buck converter with the proposed digital controller. To obtain purely resistive output impedance, an \(R_f-C_f\) low-pass filter is used for this
sensing network with a pole at $\omega_{ESR} = 1/(ESR \cdot C)$, which ideally cancels the capacitor ESR zero and chooses $C >> C_f$. When we include the effect of the output capacitors, the closed-loop impedance $Z_{oc}$ is found to be

$$Z_{oc} = R_o \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot R_o \cdot C}.$$ \hspace{1cm} (2.17)

The bode plot of the closed-loop output impedance is plotted in Fig. 2-12.

Fig. 2-12  Bode plot of the output impedance

2.2.5 Effect of Quantization and Dithering

The voltage regulation tolerance is determined by the least significant bit (LSB) of the voltage DAC (which has $n$ bits), as shown in (2.14), where $N$ is assumed to be 1. For a given VRM design, if the voltage regulation tolerance requirement is $\Delta V_{reg}$ and the allowed voltage variation range is $\Delta V_{tol}$, the minimum number $n$ of bits required in the voltage DAC is given by
where the function \( \text{int} \) takes the upward-rounded integer value of its argument. For example, if the allowed output voltage tolerance is 120mV and the required voltage regulation resolution is 1mV, a 7-bit DAC should be chosen by (2.18).

\[
n = \text{int} \left[ \log_2 \left( \frac{\Delta V_{\text{tol}}}{\Delta V_{\text{reg}}} \right) \right], \quad (2.18)
\]

Fig. 2-13 Enlarged view of the output voltage and voltage reference (simulation)

To meet the voltage regulation tolerance requirement, the minimum adjustment step \( \Delta V_{\text{ref}} \) of the voltage reference should be less than \( \Delta V_{\text{reg}} \). If \( \Delta V_{\text{ref}} \) is larger than the voltage ripple \( \Delta V_{\text{p-p}} \), the voltage reference will be same as the waveform in Fig. 2-8. If \( \Delta V_{\text{ref}} \) is smaller than the voltage ripple \( \Delta V_{\text{p-p}} \), the voltage reference will reflect the shape of the voltage ripple. Fig. 2-13 shows an enlarged view of the shape of the voltage reference (from simulation results, ESL of the output capacitors is ignored) when \( \Delta V_{\text{ref}} \) is smaller than the voltage ripple \( \Delta V_{\text{p-p}} \); note that the voltage reference also will have the same shape as the voltage ripple and the difference between their average values is always less than \( \Delta V_{\text{ref}} \).
Because of the quantization of the current reference DAC, the average inductor current \(<I_L>\) only has a finite number of discrete levels defined by the least significant bit (LSB) of the current DAC (which has \(m\) bits). Therefore, a current difference exists between \(I_o\) and \(<I_L>\). The maximum current difference is \(\Delta I_{ref}\), which will be absorbed by the output capacitors. As shown in Fig. 2-11, if the inductor current ripple is well averaged and not considered here in this analysis, the DC current \(I_c\) through the filtering capacitor \(C\) is given by

\[
I_c = <I_L> - I_o \leq \Delta I_{ref}, \tag{2.19}
\]

where we know that

\[
-|\Delta I_{ref}| \leq <I_L> - I_o \leq |\Delta I_{ref}|. \tag{2.20}
\]

Thus, the voltage variation on the filtering capacitor is calculated by

\[
\Delta V_o = ESR \cdot I_c + \frac{1}{C} \int_0^T I_c \cdot dt. \tag{2.21}
\]

In the steady state, over several DAC sampling periods (assume a total of \(i\) periods), when the accumulated voltage variation \(\Delta V_o\) reaches \(\Delta V_{ref}\), the (average) voltage reference \(V_{ref}\) is adjusted by one step \(\Delta V_{ref}\) and \(I_{ref}\) also is adjusted by one step \(\Delta I_{ref}\). After that, the output voltage changes in the opposite direction until \(\Delta V_o\) reaches \(\Delta V_{ref}\) again (assume a total of \(j\) periods). The effective inductor current step \(\Delta I_{eff}\) over the \((i+j)\) periods is given as:

\[
\Delta I_{eff} = \frac{i \cdot \Delta I_{ref}}{i + j}. \tag{2.22}
\]

where \(i\) and \(j\) depend on various factors such as \(\Delta V_{ref}, \Delta I_{ref}\), and \(I_c\). The right-most item indicates the \(I_L\) variation (\(\Delta I_L\)) caused by \(\Delta V_{ref}\).
The low-frequency automatic oscillation described above is similar to the dithering method introduced in [32], which increases the effective duty cycle resolution without increasing the hardware cost. However, the automatic dithering method here is passive, resulting as a side effect of the control idea itself, so it does not require any extra computation.

Another advantage is that the low frequency oscillation caused by this automatic dithering has a well-controlled amplitude (\(\Delta V_{\text{ref}}\)), which can be made negligibly small. However, the oscillation frequency is uncertain, depending on various factors such as \(\Delta V_{\text{ref}}\), \(\Delta I_{\text{ref}}\), and \(I_c\). This low frequency oscillation can be eliminated if the following condition is met:

\[
\Delta I_{\text{ref}} \leq \frac{\Delta V_{\text{ref}} \cdot (1 - D)}{2 \cdot L_f \cdot f_{\text{sw}}}.
\]  \hfill (2.23)

### 2.2.6 Interleaving Multiphase Structure

Interleaving technology not only reduces the amplitude of the current ripple in the total output current, but also increases the total output current ripple frequency. The ripple frequency of the total inductor current is \(n\) times the frequency of each channel. Thus interleaving significantly reduces the output filter capacitor requirement. In the same way, the interleaving approach can also significantly reduce the input filter capacitor requirement. [14][16-19]

However, interleaving VRMs require more complicated controllers not only because they have more control signals but also because of the timing and matching of control signals in different channels. In interleaving VRMs, current sharing control among channels is usually a necessity in order to balance the load among the channels.
Fig. 2-14 Circuit configuration of an N-phase buck converter with the proposed controller

The proposed digital controller can be easily applied to an interleaved multiphase buck converter. The timing of the control signals is easily arranged using the digital method and an active current sharing ability is inherently achieved at no extra cost due to the peak current mode control.

Fig. 2-14 shows the circuit configuration of an N-phase buck converter with the proposed controller, where a total of \((N+1)\) comparators are used. One comparator is needed for each phase and one comparator is needed for the voltage loop. The inductor current of each phase is sensed.
separately and compared to the peak current reference $I_{\text{ref}}$ produced by the current DAC. The peak current reference $I_{\text{ref}}$ is set to the phase peak current reference. The logic signal of the comparator of each phase is used to turn off its own high side MOSFET and turn on its own low side MOSFET, whereas the high side MOSFET and the low side MOSFET are turned on and off respectively by a signal from the low resolution DPWM. The DPWM is implemented using the counter-comparator method. For an $N$-phase buck converter, the counter bit $n$ is given as

$$ n = \text{int}[\log_2 N], \quad (2.24) $$

where $\text{int}[]$ operates as defined in Equation 2.18.

The operating clock of the target FPGA (or ASIC) will not increase significantly; the only requirement is that it is high enough to generate an $n$-bit resolution DPWM.

The small-signal model of an $n$-channel interleaving buck can be simplified as a single buck converter. The equivalent inductance in the simplified model is $1/N$ of the inductance in each channel. The equivalent switching frequency of the simplified model is $N$ times the switching frequency in each channel. Using this analogy, the small-signal analysis of the interleaved buck is no different from a single buck. [57]

Therefore, the equations or the constraints derived above are still valid for interleaved multiphase buck converters. However, the inductor $L_f$ involved in the calculation should be replaced by the equivalent inductance, which is $1/N$ of the inductance in each channel, and the switching frequency should be replaced by the equivalent switching frequency, which is $N$ times the switching frequency in each channel. The smallest current reference adjustment step $\Delta I_{\text{ref}}$ should be replaced by $N \cdot \Delta I_{\text{ref}}$.

The peak-to-peak inductor current ripple of a single phase buck converter can be expressed as.
\[ \Delta I_{i\phi} = \frac{V_o (1-D)}{f_{sw} \cdot L_f} . \] (2.25)

Because of the ripple cancellation effect in the interleaving topology, the total inductor current ripple of an \( N \)-phase interleaving buck converter can be calculated as

\[ \Delta I_L = \Delta I_{i\phi} \cdot \frac{1-N \cdot D}{1-D} , \] (2.26)

where we assume that \( N \cdot D < 1 \). The total inductor current ripple frequency is \( N \) times the channel switching frequency.

The output voltage ripple due to the charge variation of the capacitors is

\[ \Delta V_{o,r} = \frac{\Delta I_L}{8N \cdot f_{sw} \cdot C} . \] (2.27)

The output voltage ripple due to the ESR of the capacitors is

\[ \Delta V_{o,r,ESR} = \Delta I_L \cdot ESR , \] (2.28)

and the combined output voltage ripple may be estimated to be

\[ \Delta V_{o,r} = \Delta I_L \cdot \sqrt{\frac{1}{(8N \cdot f_{sw} \cdot C)^2 + ESR^2}} . \] (2.29)

The expression in Equation (2.28) does not include the ripple contribution due to the output capacitor effective series inductance (ESL). The ESL depends strongly on the capacitor packaging and circuit layout, and should be reduced as much as possible [58].

### 2.2.7 Small Signal Analysis

The state-space description of dynamic systems is a mainstay of modern control theory, and the state-space averaging method makes use of this description to derive the small-signal...
averaged equations of the PWM switching converters [56]. It is especially suitable for digital control theory.

Fig. 2-15 Typical synchronous buck converter with the digital controller

Fig. 2-15 shows the synchronous buck converter with the proposed controller. The equivalent series resistor $R_L$ models the series combination of the equivalent resistance of the inductor, the losses of the MOSFETs and the losses of the power paths. The equivalent series resistor of the output capacitors is represented by ESR, while the current source $i_o$ models the load. The state-space averaging small signal model of the synchronous buck converter can be expressed as

$$
\begin{bmatrix}
\frac{d i_L}{dt} \\
\frac{d v_c}{dt}
\end{bmatrix} =
\begin{bmatrix}
\frac{-1}{L} & \frac{-1}{L} \\
\frac{1}{C} & 0
\end{bmatrix}
\begin{bmatrix}
\hat{i}_L \\
\hat{v}_c
\end{bmatrix} + \begin{bmatrix}
\frac{ESR}{L} & \frac{D}{L} & \frac{V_{in}}{L} \\
\frac{-1}{C} & 0 & 0
\end{bmatrix}
\begin{bmatrix}
\hat{i}_o \\
\hat{v}_m \\
\frac{d}{dt}
\end{bmatrix}
$$

and

(2.30)
\[
\begin{bmatrix}
\hat{v}_o \\
\hat{i}_L
\end{bmatrix} =
\begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix}
\begin{bmatrix}
\hat{v}_e \\
\hat{v}_c
\end{bmatrix} +
\begin{bmatrix}
-ESR & 0 \\
0 & 0
\end{bmatrix}
\begin{bmatrix}
\hat{i}_o \\
\hat{v}_{in}
\end{bmatrix} - \frac{d}{\omega}
\]

From (2.30) and (2.31), the transfer functions of the buck converter can be derived as follows:

\(Z_o\) represents the open-loop output impedance; \(G_{sv}\) is the open-loop line-to-output transfer function; \(G_{sd}\) is the open-loop control-to-output transfer function; \(G_{si}\) is the open-loop load-to-inductor–current transfer function; \(G_{sv}\) is the open-loop line-to-inductor-current; \(G_{id}\) is the open-loop control-to-inductor-current transfer function.

\[
Z_o(s) = \frac{\hat{v}_o}{\hat{i}_o} = \frac{\hat{v}_o}{-\hat{i}_o} = \frac{ESR \cdot (s + \omega_{ESR})(s + \omega_L)}{s^2 + Q \cdot \omega_r \cdot s + \omega_r^2}
\]

\[
G_{sv}(s) = \frac{\hat{v}_o}{\hat{v}_{in}} = \frac{\hat{v}_o}{\hat{v}_{in}} = \frac{D \cdot ESR}{L} \cdot (s + \omega_{ESR})
\]

\[
G_{sd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{\hat{v}_o}{\hat{d}} = \frac{V_{in} \cdot ESR}{L} \cdot (s + \omega_{ESR})
\]

\[
G_{si}(s) = \frac{\hat{i}_L}{\hat{i}_o} = \frac{\hat{i}_L}{\hat{i}_o} = \frac{ESR}{L} \cdot (s + \omega_{ESR})
\]

\[
G_{iv}(s) = \frac{\hat{i}_L}{\hat{v}_{in}} = \frac{\hat{i}_L}{\hat{v}_{in}} = \frac{D}{L} \cdot \frac{s}{s^2 + Q \cdot \omega_r \cdot s + \omega_r^2}
\]
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\[ G_{ad}(s) = \frac{i_r}{d} = \frac{V_{in}}{L} \frac{s}{s^2 + Q \cdot \omega_r \cdot s + \omega^2}, \]  \hspace{1cm} (2.37)

where \( \omega_{ESR} = \frac{1}{ESR \cdot C}, \omega_L = \frac{R_L}{L}, \omega_r = \sqrt{\frac{1}{L \cdot C}}, \) and \( Q = \frac{R_L + ESR}{\sqrt{L / C}}. \)

Under the peak current mode control, the average inductor current differs from the peak inductor current, which is regulated by the control signal \( i_r. \) Hence, the average inductor current \(<i_L>\) can be represented (from [56]) as

\[ <i_L> = \frac{1}{R_i} \cdot <i_r> - m_a \cdot d \cdot T_s = \frac{m_1 \cdot d^2 \cdot T_s}{2} - \frac{m_2 \cdot (1-d)^2 \cdot T_s}{2}, \]  \hspace{1cm} (2.38)

\[ m_1 = \frac{v_{in} - v_o}{L} \hspace{1cm} m_2 = \frac{v_o}{L} \hspace{1cm} m_1 \cdot D = m_2 \cdot (1-D) \]  \hspace{1cm} (2.39)

where \( m_a \) is the artificial ramp slope for the purpose of stability, which will be equal to 0 if no artificial ramp is added.

The small signal model of the peak current mode controller modulation can be found by perturbation and linearization of (2.38):

\[ \hat{d} = \frac{1}{m_a \cdot T_s \cdot R_i} (i_r - R_i \cdot \hat{i}_L - R_i \cdot \frac{D^2 \cdot T_s}{2} \cdot \hat{m}_1 - R_i \cdot \frac{(1-D)^2 \cdot T_s}{2} \cdot \hat{m}_2). \]  \hspace{1cm} (2.40)

According to the small-signal variations of (2.39), \( \hat{m}_1 \) and \( \hat{m}_2 \) depend on \( \hat{v}_{in} \) and \( \hat{v}_o, \) so we can re-express (2.40) in the following form:

\[ \hat{d} = \frac{1}{m_a \cdot T_s \cdot R_i} (i_r - R_i \cdot \hat{i}_L - R_i \cdot \frac{D^2 \cdot T_s}{2L} \cdot \hat{v}_{in} - R_i \cdot \frac{(1-2D) \cdot T_s}{2L} \cdot \hat{v}_o). \]  \hspace{1cm} (2.41)
According to (2.41), the function block of the peak current mode controller modulation can be constructed as shown in Fig. 2-16.

\[ F_M = \frac{1}{m_a \cdot T_s \cdot R_i}, \quad \text{(2.42)} \]

\[ F_{df} = R_i \cdot \frac{D^2 \cdot T_s}{2L}, \quad \text{and} \quad \text{(2.43)} \]

\[ F_{dv} = R_i \cdot \frac{(1-2D) \cdot T_s}{2L}, \quad \text{(2.44)} \]

where \( F_M \) models the effect of the artificial ramp \( m_a \) on the average inductor current, and the \( F_{df} \) and \( F_{dv} \) gains model the small-signal effects of the inductor current ripple.
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The peak current reference \( i_r \) is generated by the digital-to-analog converter, which is commanded by the digital controller. The outer voltage loop is formed in the discrete-time domain. From the control idea presented in Section 2.2.1, the behavior of the digital controller can be described as follows:

\[
\begin{align*}
V_{\text{ref}}(n+1) &= V_{\text{ref}}(n) + e(n) \\
I_{\text{ref}}(n+1) &= I_{\text{ref}}(n) + R_i \cdot f(z) \cdot e(n)
\end{align*}
\]  
(2.45)

\[
e(n) = \begin{cases} \\
\Delta V_{\text{ref}} & V_{\text{ref}}(n) \leq V_o \\
-\Delta V_{\text{ref}} & V_{\text{ref}}(n) > V_o
\end{cases}
\]

If the simplest control function described in (2.6) is applied, whose behavior is also detailed in Section 2.2.2, the discrete-time transfer function \( C(z) \) of the digital controller is derived approximately as

\[
C(z) = R_i \cdot f(z) \cdot z^{-1} = -\frac{R_i}{R_o} \cdot z^{-1}
\]  
(2.46)

where \( R_o \) is desired output impedance.
Fig. 2-17 shows the small signal model blocks of the synchronous buck converter with the proposed controller under peak current mode control. A ZOH (zero-order hold) is added to model DAC function; the ZOH transfer function is represented as
\[ G_{ZOH}(s) = \frac{1 - e^{-sT}}{s}, \]

where \( T \) is the DAC clock period, which is much smaller than switching period \( T_s \) (normally 4 - 16 times the clock period \( T \)).

In Fig. 2-17, the inner current loop and the power stage are in continuous time; only the voltage loop is in discrete time. Therefore, when the inner current loop is closed and the voltage loop is open, the transfer functions of the power stage and the control loop are modified to be

\[
G_{vvl}(s) = \frac{G_{vvi}(s) \cdot (1 + F_M \cdot R_i \cdot G_{id}) - F_M \cdot (R_i \cdot G_{iv} + F_{df} \cdot G_{vd}) \cdot G_{vd}}{1 + F_M \cdot (F_{dv} \cdot G_{vd} + R_i \cdot G_{id})}, \quad (2.48)
\]

\[
Z_{ol}(s) = \frac{Z_{oi}(s) \cdot (1 + F_M \cdot R_i \cdot G_{id}) + F_M \cdot R_i \cdot G_{ii} \cdot G_{vd}}{1 + F_M \cdot (F_{dv} \cdot G_{vd} + R_i \cdot G_{id})}, \quad \text{and} \quad (2.49)
\]

\[
G_{vcl}(s) = \frac{F_M \cdot G_{vd}}{1 + F_M \cdot (F_{dv} \cdot G_{vd} + R_i \cdot G_{id})}, \quad (2.50)
\]

where \( G_{vvi}, Z_{oi} \) and \( G_{vcl} \) represent the line-to-output transfer function, the output impedance and the control-to-output transfer function respectively when the inner current loop is closed.
Fig. 2-18 The small signal model blocks with the inner current loop closed and the voltage loop open

Fig. 2-18 shows the transfer function blocks of the synchronous buck converter using the proposed controller with the inner current loop closed and the outer voltage loop open.

$H(s)$ is the transfer function of the output voltage sensing network. To obtain purely resistive output impedance, an $R_f\cdot C_f$ low-pass filter is used for this sensing network with a pole at $\omega_{ESR}$, which ideally cancels the capacitor ESR zero. This transfer function is represented as

$$H(s) = \frac{1}{1 + s \cdot R_f \cdot C_f} = \frac{1}{1 + s / \omega_{ESR}}.$$  \hspace{1cm} (2.51)

It should be noted that this sensing network also can be moved into the digital controller and be implemented in digital form.

$G_{DL}(s)$ is added to model the effective delay of the modulator, the gate drivers, and the power switches, and can be represented by
Chapter 2 Digital Adaptive Voltage Positioning Techniques

\[ G_{DL}(s) = e^{-sT_d} \approx \frac{1-s \cdot T_d / 2 + (s \cdot T_d)^2 / 12}{1+s \cdot T_d / 2 + (s \cdot T_d)^2 / 12} \] \quad (2.52)

In Fig. 2-18, the control loop still consists of a discrete control part \( C(z) \), which feeds the peak current reference control signal to the block \( G_{vc} \) through the digital-to-analog converter.

The analysis and design of a digital control system is complicated by the fact that the plant is a continuous-time system while the controller is a discrete-time system. One way of dealing with this problem is to replace the plant with a discrete-time model that specifies its behavior at sampling instants. In this way, the entire control system becomes discrete time, and standard discrete-time system theory can be used to design the controller. Analysis and design using this discrete model is called direct digital design [60][61].

In most cases, approximation methods are used to convert the transfer functions from \( s \)-domain to \( z \)-domain, such as Tustin’s method, the impulse invariant discretization method, and the matched pole-zero (MPZ) method. But the sampled-data (ZOH) model is preferred because it is not an approximation and is thus more accurate. The sampled-data (ZOH) model for the synchronous buck converter exactly describes the behaviors of the buck converter at sampling instants [56] [60-61]. With this method, the discrete form of transfer functions of the power stage can be converted from the continuous time transfer functions using the formula

\[
GH(z) = Z \left\{ G_{ZOH}(s) \cdot G_{DL}(s) \cdot G_{vc}(s) \cdot H(s) \right\} = (1-z^{-1}) \cdot Z \left\{ \frac{G_{vc}(s) \cdot H(s) \cdot G_{DL}(s)}{s} \right\} \cdot \quad (2.53)
\]

Therefore, the system open loop transfer function \( T_{vi} \) can be seen to be

\[
T_{vi}(z) = -C(z) \cdot GH(z) = \frac{R_i}{R_v} \cdot \left( \frac{z-1}{z^2} \right) \cdot Z \left\{ \frac{G_{vc}(s) \cdot H(s) \cdot G_{DL}(s)}{s} \right\} \cdot \quad (2.54)
\]

57
To verify the stability of the designed discrete-time system, the system open loop transfer function $T_{vi}$ can be used for the analysis. In general, the stability analysis techniques applicable to a linear continuous-time system may also be applied to the analysis of a discrete-time system, so long as certain modifications are made. These techniques include the Routh-Hurwitz criterion, root locus procedures, and frequency-response techniques. The July stability test dedicated for discrete systems also can be applied. [60][61]

Fig. 2-19 Nyquist Plot of the discrete-time system open loop transfer function

Fig. 2-19 shows the Nyquist plot of the designed discrete system open loop transfer function. The frequency of interest is valid from $-\pi/T$ to $\pi/T$. In the Nyquist plot, stability, phase margin, bandwidth, and delay margin can be determined. For example, in Fig.2-19 the minimum stability margin point was found, with 56 KHz bandwidth, 88.6 degree phase margin and 70-sample delay margin.
2.2.8 Switching Stability Constraints

In fixed-frequency switching converters with feedback control there is a fundamental limit on the loop-gain bandwidths, which results in stable closed-loop operation. In particular, feedback bandwidth which approaches or exceeds the switching frequency may result in non-linear behaviors such as period-doubling or chaos [62]. This stability constraint can be expressed as

\[ f_c < \alpha \cdot f_s, \quad (2.55) \]

where \( f_c \) is the feedback unity-gain frequency, \( f_s \) is the switching frequency, and \( \alpha \) is a constant.

According to [63-64] the fundamental upper limit for naturally-sampled, triangle carrier PWM is \( \alpha = 1/3 \). In an interleaved \( N \)-phase buck converter the stable bandwidth can potentially be extended by \( N \) times [65]; however, in the presence of parameter mismatches among the phase legs, aliasing effects at the switching frequency may reduce the usable bandwidth [65]. Thus, Equation (2.55) with \( \alpha = 1/6 \) stands as a practical stability guideline, with the understanding that for multi-phase designs it may be on the conservative side.

To simplify the analysis, it is assumed that no artificial ramp \( M_a \) is added and the effects of the inductor current ripple are ignored. Therefore, \( F_M \to \infty \), \( F_{df} \to 0 \) and \( F_{dv} \to 0 \). The control-to-output transfer function \( G_{vci}(s) \) with inner current loop closed will be reduced to a first-order system, given as

\[
G_{vci}(s) = \lim_{F_M \to \infty, F_{df} \to 0, F_{dv} \to 0} G_{vci}(s) = \frac{G_{id}}{R_i \cdot G_{id}} = \frac{s / \omega_{ESR} + 1 \cdot R_i}{s \cdot C \cdot R_i}. \quad (2.56)
\]

In order to obtain a brief expression of crossover frequency, the discrete-time transfer function \( C(z) \) of the digital controller is converted into the continuous-time domain. If the sample frequency \( T \) is much higher than the switching frequency \( T_s \), such a conversion will be quite
accurate and the sampler and zero-order hold ($G_{ZOH}$) may be ignored with very little resulting error [62]. The continuous-time transfer function is

$$C(s) = S\{C(z)\} = -\frac{R_i}{R_o} \cdot e^{-sT}.$$  \hspace{1cm} (2.57)

Therefore, the system open loop transfer function $T_{vis}$ in the continuous-time domain can be shown to be

$$T_{vis}(s) = -C(s) \cdot G_{vis}(s) \cdot H(s) \cdot G_{dl}(s) = \frac{1}{s \cdot C \cdot R_o} \cdot e^{-s(T+T_s)}$$

$$\approx \frac{1}{s \cdot C \cdot R_o},$$  \hspace{1cm} (2.58)

where $(T + T_s) << T_r$.

Obviously, the system crossover frequency $f_c$ can be determined to be

$$f_c = \frac{1}{2\pi \cdot R_o \cdot C}.$$  \hspace{1cm} (2.59)

The bode diagram of the continuous-time system open loop transfer function is plotted in Fig. 2-20. It should be noted that the crossover frequency (56 KHz) found in Fig. 2-20 is same as that (56 KHz) found in Fig.2-19, and the phase margin is also very close (90 deg in Fig 2-20 vs. 88.6 deg in Fig. 2-19). This verifies that the approximation analysis method here to find the system crossover frequency is acceptable.
Hence, in this load-line feedback control, the following constraint can be derived by combining (2.55) and (2.59) to get

\[
\frac{1}{2\pi \cdot R_o \cdot C} = f_c < \alpha \cdot f_s ,
\]  

(2.60)

where \( R_o \) is the desired output impedance (load line), \( C \) is the output filter capacitor, and \( f_s \) is the switching frequency (or the equivalent switching frequency for multi-phase converters).

Fig. 2-21 illustrates the minimum output capacitance requirement for switching stability. For a given switching frequency, the output capacitor should be selected to be sufficiently large to meet the constraint (2.60). Therefore, with this load-line feedback control approach, there is a trade-off between the number of output capacitors required and the switching frequency used.
Fig. 2-21 Minimum output capacitance for switching stability

As an extension, the closed-loop output impedance $Z_{oc}(s)$ is found to be

$$Z_{oc}(s) = \frac{Z_{ois}(s)}{1 + T_{vis}(s)} ,$$

(2.61)

where

$$Z_{ois}(s) = \lim_{F_{id} \to 0} \lim_{F_{id} \to 0} Z_{oi}(s) = Z_{o}(s) + \frac{G_{ii} \cdot G_{id}}{G_{id}} .$$

(2.62)

Fig. 2-22 shows the bode diagram of the closed-loop output impedance. A constant output impedance is realized by the proposed digital controller, which coincides with the result derived by the current source equivalent circuit in Fig. 2-11, whose bode diagram is plotted in Fig. 2-12.
2.3 Simulation Verification

In this section a two-phase interleaved buck converter is designed to verify the theoretical analysis of Section 2.2. A two-phase version of the architecture in Fig.2-14 was designed and simulations were performed in the co-simulation environment consisting of PSIM, ModelSim and Simulink. The power stage was constructed in PSIM, the digital control function was realized by VHDL in ModelSim, and the power circuits and digital controller were linked together in MATLAB/Simulink. Fig. 2-23 shows the co-simulation environment.
The circuit parameters of the two-phase interleaved synchronous buck converter for 12V-1V/40A VRMs are listed in the Table 2-1. The phase switching frequency is 250 KHz, the phase inductor is 400nH and the output capacitors are three 470uF POSCAP capacitors in parallel (ESR: 5mΩ/3, ESL: 1.6nH/3). The desired output impedance is set at 2mΩ.

**Table 2-1 Circuit parameters of the power converter**

<table>
<thead>
<tr>
<th>Number of phases ($N$)</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ($V_{in}$)</td>
<td>12 V</td>
</tr>
<tr>
<td>Output voltage ($V_o$)</td>
<td>1V</td>
</tr>
<tr>
<td>Maximum load current ($I_{omax}$)</td>
<td>40A, 20A/phase</td>
</tr>
<tr>
<td>Maximum load transient ($\Delta I_{omax}$)</td>
<td>27A (13A ↔ 40A)</td>
</tr>
</tbody>
</table>
The design parameters of the digital controller are listed in Table 2-2. The digital-to-analog converters operate at 32MHz with 7-bit resolution. The minimum voltage reference step is set to 0.84mV and the minimum current reference is set to 0.21A.

Design procedure of the multiphase VRM with the proposed digital controller is provided in Appendix A.

<table>
<thead>
<tr>
<th>Parameters of Digital Controller</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Operating Clock</strong> $f_{clk}$</td>
<td>32MHz</td>
</tr>
<tr>
<td><strong>Resolution of Current DAC</strong></td>
<td>7 bits</td>
</tr>
<tr>
<td><strong>Resolution of Voltage DAC</strong></td>
<td>7 bits</td>
</tr>
<tr>
<td><strong>Minimum Voltage Reference Step</strong> $\Delta V_{ref}$</td>
<td>$0.84mV \ (N=1)$</td>
</tr>
<tr>
<td><strong>Minimum Current Reference Step</strong> $\Delta I_{ref}$</td>
<td>$0.21A \ (M=1)$</td>
</tr>
</tbody>
</table>
Chapter 2 Digital Adaptive Voltage Positioning Techniques

Fig. 2-24 shows the simulation results for the load transient response. Fig.2-25 and Fig 2-26 show expended waveforms during load transient-up and load transient-down respectively. Only a very small output voltage ring-back exists after a large load transient; nearly perfect AVP control is achieved with the proposed digital controller.

Fig. 2-24 Load transient response

Fig. 2-25 Expended simulation waveforms during load transient-up
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Fig. 2-26 Expended simulation waveforms during load transient-down

Fig. 2-27 Generated peak current reference and phase inductor current

Fig. 2-27 illustrates the relationship between the generated peak current reference and the phase inductor current. The ripple of the generated peak current reference has an inverse shape of the output voltage ripple. As represented in Equation (2.8), a current error exists between the generated peak current reference and the peak phase current, because of the circuit delay (here about 100ns in total, estimated), including the MOSFET turn-off delay and the computing delay.
Fig. 2-28 shows the shape of the generated voltage reference, which tightly follows the output voltage, verifying the expectation in Section 2.2.5.

![Fig. 2-28 Shapes of generated voltage reference and the output voltage](image)

**Fig. 2-28 Shapes of generated voltage reference and the output voltage**

(voltage scale: 1.25mV/div, time scale: 2µs)

Fig. 2-29 illustrates the active current sharing inherent in the peak current mode control in the multi-phase VRM. Phase #1 inductance is set to 396nH, 10% more than the nominal value (360nH), and phase #2 inductance is set to 324nH, 10% less than the nominal value. The RMS values on the two phase inductors are very close: 20.13A (phase #1) vs. 20.25A (phase #2).

![Fig. 2-29 Active current sharing](image)

**Fig. 2-29 Active current sharing**

(current scale: 2A/div, time scale: 5µs)
2.4 Experimental Results

To verify the theoretical analysis and simulation results, the digital controller was tested on a prototype of a two-phase interleaved synchronous buck converter with FPGA board. Fig. 2-30 shows the block schematic of the prototype power converter with digital controller.

Fig. 2-30 Block schematic of the prototype power converter

The circuit parameters of the prototype power converter are listed in Table 2-3. The phase switching frequency, phase inductor, output capacitors and output impedance are set as they were for the simulations in Section 2.3.
Two digital-to-analog converters (DAC2904 from Texas Instrument, 14 bits) were used to generate the peak current reference and voltage reference. The current DAC operates at 7 bits, and the voltage DAC operates at 10 bits with an effective 7-bit voltage variation range, both at 32MHz.

The digital control algorithm is coded in VHDL and implemented in an FPGA (Stratix II EP2S60 DSP development board from Altera). The FPGA also operates at 16MHz. Design parameters of the digital controller are listed in Table 2-4.
Table 2-4 Parameters of the digital controller

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Clock $f_{clk}$</td>
<td>32MHz</td>
</tr>
<tr>
<td>Resolution of Current DAC</td>
<td>7 bits</td>
</tr>
<tr>
<td>Resolution of Voltage DAC</td>
<td>7 bits</td>
</tr>
<tr>
<td>Minimum Voltage Reference Step $\Delta V_{ref}$</td>
<td>1.07mV ($N=1$)</td>
</tr>
<tr>
<td>Minimum Current Reference Step $\Delta I_{ref}$</td>
<td>0.251A ($M=1$)</td>
</tr>
</tbody>
</table>

Fig. 2-31 shows the steady-state output voltage ripple. The peak-to-peak voltage ripple is about 5mV.

Fig. 2-31 Steady-state output voltage ripple
(voltage scale: 10mV/div, time scale: 2µs/div)

Fig. 3-32 shows the output voltage during load transient up/down. Obviously, the AVP operation is realized as expected.
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Fig. 2-32 Output voltage during load transient up/down

(voltage scale: 20mV/div, time scale: 500µs/div)

Fig. 2-33 shows the tested phase inductor current at half load (20A) and full load (40A). It is found that phase inductor currents are well balanced between two phases because of the inherent active current sharing ability.

Fig. 2-33 Tested phase inductor current at half load (20A) and full load (40A)

(current scale: 10A/div, time scale: 1µs/div)
2.5 Summary

In this chapter, an AVP control unit is generalized to realize AVP control, which generates the voltage reference and the current reference according to the desired output impedance. It is identified by the uniqueness of its dynamic voltage/current references. There are a number of options for constructing such an AVP control model, including decisions about where the analog-to-digital conversion or the digital-to-analog conversion is performed and whether to use peak or average current control.

A digital controller with peak current mode control is used to demonstrate the operation of the AVP control unit. Two digital-to-analog converters are used to generate the required voltage and current references. A straightforward control law is supplied for the AVP control unit; no compensator, and only simple addition computation and control logic are required. The use of low-complexity DACs and a straightforward control law makes the proposed digital controller very suitable for high-volume low-cost low-dissipated-power integrations.

Steady state analysis is performed to demonstrate the digital controller operation. After that, a small signal model is explored to determine system stability. Then, a switching stability constraint is derived to give the minimum output capacitor requirement. At last, a two-phase 12V-to-1V/40A 250 KHz synchronous buck converter with the proposed digital controller is designed to verify the theoretical analysis by simulations and experiments.
Chapter 3

Control Algorithms to Improve Dynamic Performance

3.1 Introduction

As future processors require a tremendous load current with increasingly violent load transients at a low supply voltage, the VRM will need to use a large number of output bulk capacitors to sustain the output voltage, which increases size and cost. Therefore, much research [48-49, 52, 55, 64-84] has delved into VRM transient design: improving VRM transient performance to reduce the number of bulk capacitors and make the VRM meet the even tighter output voltage regulation necessary in recent and future processors. Most of the research cited above attempts to optimize the control loop or the output impedance to improve the transient performance and reduce the number of bulk capacitors. However all are limited by the control bandwidth. Some research [22, 66] has revealed the relationship between the control bandwidth and the transient response in buck converters. The critical inductor revealed that further reducing inductance does not improve the transient response speed [66]. Hence, increasing the switching frequency to push the control bandwidth higher is necessary for these analog controllers to reduce their energy storage capacitor requirement. However, higher switching frequency operation results in higher power losses in power switches and magnetic components.

Digital control techniques offer some advantages over analog control. Some non-linear controls such as operation-state recognition, decision-making, and multi-mode, can break the tight relationship between the control bandwidth and the transient response, thus easily making it possible for a low-frequency low-bandwidth VRM to offer a very fast transient response speed while digital control methods are used.
This chapter investigates relationships between the reference updating frequency $f_{clk}$, the current reference step $\Delta I_{\text{ref}}$ and VRM transient performance when using the proposed digital controller. The output voltage spike is also given in terms of the reference updating frequency $f_{clk}$ and the current reference step $\Delta I_{\text{ref}}$. Then, based on these relationships, several control methods—including dynamic reference step adjustment, non-linear control and transient detection circuits—are introduced to improve transient performance. Finally, the dual-voltage-loop control, which integrates all these control methods, is proposed, offering superior dynamic performance when compared to other control methods.

### 3.2 Voltage Deviation during Load Current Transient

In conventional VRMs, a single-phase synchronous buck converter is used. Due to the steady-state ripple requirements, large inductances must be employed which limit the speed of the transient response. The multi-phase interleaved synchronous buck converter is a commonly-used topology for VRM designs. The interleaved structure greatly reduces the total inductor current ripple and the output voltage ripple, so this structure allows the use of smaller inductances to improve transient response. However, since the interleaved structure does not change the average small signal model, the single-phase synchronous buck converter still can be used to analyze the load transient response. [55][66]

Fig. 3-1 shows the large transient equivalent circuit of the buck converter. For simplicity, the equivalent resistance of the inductor and the average equivalent on-resistance of power switches are ignored, and the equivalent series inductance (ESL) of bulk capacitors is also ignored. The effects of decoupling capacitors and both the interconnection parasitic resistance and inductance are also ignored in order to simplify the analysis.
During load current transient, the inductor current slew rate is determined by the supply rails, which can be expressed,

for load transient-up as \[ V_L = v_i - V_o = V_{in} - V_o, \] (3.1)

and for load transient-down as \[ V_L = v_i - V_o = -V_o. \] (3.2)

Fig. 3-2 shows the inductor current and the output voltage with load transient-up. It is assumed that the load current slew rate is fast enough compared to the inductor current slew rate, the initial output voltage is \( V_{o0} \), the initial inductor current is \( I_{o0} \), the final inductor current is \( I_{o1} \), and the step-up load current is \( \Delta I_o = I_{o1} - I_{o0} \). The capacitor is discharging during the periods \( t_D \) and \( t_r \), with the latter being the time of minimum capacitor charge. However, the minimum output voltage occurs sometime before the end of \( t_r \) due to ESR effects. During load step-down transient, the inductor current, the load current and the output voltage will vary in the opposite direction, with the maximum capacitor charge at time \( t_r \) and the maximum output voltage occurs sometime before the end of \( t_r \) due to ESR effects.
Fig. 3-2 The inductor current $i_L$ and the output voltage $V_o$ while load transient-up

Before the controller reacts ($t<0$), the inductor current remains approximately at the initial current, $I_{o0}$. $t_D$ represents the action delay inherent to the physical implementation, including the turn-on delay of the switches, the gate driver delay and the controller delay. After the controller reacts, the inductor current will continue to increase during load transient-up and continue to decrease during load transient-down if the bandwidth of the controller is high enough or non-linear control is applied to make the duty cycle equal 1 or 0. Therefore, the discharging current of the capacitors is expressed as
The output voltage function over the time after $t=0$ can be derived

\[ v_o(t) = v_{ESR} + v_c = -i_c(t) \cdot ESR - \int_{i_o}^{t} i_c(t) \, dt + v_{o0} \]

\[ = v_{o0} - \frac{\Delta I_o \cdot t_p}{C} - ESR \cdot (\Delta I_o - \frac{V_L}{L_f} t) - \frac{1}{C} \int_0^t (\Delta I_o - \frac{V_L}{L_f} t) \, dt, \]

\[ = v_{o0} - \frac{\Delta I_o \cdot t_p}{C} - ESR \cdot (\Delta I_o - \frac{V_L}{L_f} t) - \frac{\Delta I_o}{C} t + \frac{V_L}{2L_f \cdot C} t^2 \]

where $\Delta I_o t_p$ approximately represents the charge variation of the capacitors.

In order to determine the peak output voltage $V_{opk}$, it is necessary to calculate the derivative of the output voltage with respect to time, given by

\[ \frac{dv_o}{dt} = ESR \cdot \frac{V_L}{L_f} - \frac{\Delta I_o}{C} + \frac{V_L}{L_f \cdot C} t. \]

By setting Equation (3.5) equal to zero and solving for $t$, $T_m$ is calculated as

\[ T_m = \frac{\Delta I_o \cdot L_f}{V_L} - ESR \cdot C. \]

Since it is physically impossible for the peak output voltage to occur before the controller reacts, $T_m$ should be redefined as

\[ T_m = \begin{cases} 0 & L_f < \frac{ESR \cdot C \cdot V_L}{\Delta I_o} = L_{crit} \\ \frac{\Delta I_o \cdot L_f}{V_L} - ESR \cdot C & L_f \geq \frac{ESR \cdot C \cdot V_L}{\Delta I_o} = L_{crit} \end{cases} \]
where \( L_{crit} \) is defined as a critical inductance value, below which the output voltage transient is independent of the inductance.

By substituting Equation (3.7) into Equation (3.4), the peak output voltage \( V_{opk} \) is shown to be

\[
V_{opk} = \begin{cases} 
V_{o0} - \frac{\Delta I_o \cdot t_D}{C} - ESR \cdot \Delta I_o & \text{if } L_f < L_{crit} \\
V_{o0} - \frac{\Delta I_o \cdot t_D}{C} - \frac{ESR \cdot C^2 \cdot V_L^2 + \Delta I_o^2 \cdot L_f^2}{2L_f \cdot C \cdot V_L} & \text{if } L_f \geq L_{crit}
\end{cases}
\]

which leads trivially to an expression of the maximum voltage deviation

\[
\Delta V_{o\text{max}} = V_{o0} - V_{opk} = \begin{cases} 
\frac{\Delta I_o \cdot t_D}{C} + ESR \cdot \Delta I_o & \text{if } L_f < L_{crit} \\
\frac{\Delta I_o \cdot t_D}{C} + \frac{ESR^2 \cdot C^2 \cdot V_L^2 + \Delta I_o^2 \cdot L_f^2}{2L_f \cdot C \cdot V_L} & \text{if } L_f \geq L_{crit}
\end{cases}
\]

During the load transient-up, the maximum voltage deviation at maximum load step-up transient should not exceed the allowed voltage drop, which is normally set within load line specification, \( \Delta I_{o\text{max}} \cdot R_o \), where \( R_o \) is the desired output impedance. This gives the first constraint condition on the size of output capacitors:

\[
\begin{cases} 
\frac{\Delta I_{o\text{max}} \cdot t_D}{C} + ESR \cdot \Delta I_{o\text{max}} \leq \Delta I_{o\text{max}} \cdot R_o & \text{if } L_f < L_{crit} \\
\frac{\Delta I_{o\text{max}} \cdot t_D}{C} + \frac{ESR^2 \cdot C^2 \cdot (V_{in} - V_o)^2 + \Delta I_{o\text{max}}^2 \cdot L_f^2}{2L_f \cdot C \cdot (V_{in} - V_o)} \leq \Delta I_{o\text{max}} \cdot R_o & \text{if } L_f \geq L_{crit}
\end{cases}
\]

During the load transient-down, the maximum voltage deviation at maximum load step-down transient should not exceed the allowed voltage drop. Due to the low conversion ratio (\(<=0.1\)) in modern VR’s, the capacitance required for load transient-down is much larger than that for load...
transient-up. Therefore, the output voltage is allowed to overshoot by some amount \( \Delta V_{os} \) above the defined load line during unloading transients, thus reducing the output capacitor requirement.

This gives the second constraint condition on the size of output capacitors:

\[
\begin{align*}
\frac{\Delta I_{o_{\text{max}}} \cdot t_D}{C} + ESR \cdot \Delta I_{o_{\text{max}}} & \geq \Delta I_{o_{\text{max}}} \cdot R_o - \Delta V_{os} & L_f < L_{crit} \\
\frac{\Delta I_{o_{\text{max}}} \cdot t_D}{C} + \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I_{o_{\text{max}}}^2 \cdot L_f^2}{2L_f \cdot C \cdot (-V_o)} & \geq \Delta I_{o_{\text{max}}} \cdot R_o - \Delta V_{os} & L_f \geq L_{crit}
\end{align*}
\]  

(3.11)

From Equation (3.7), it can be found that the critical inductance depends on the time-constant \( \tau_c = ESR \cdot C \) of the capacitor, the step current amount \( \Delta I_{o_{\text{max}}} \), and the voltage applied to the inductor. A smaller time-constant of the capacitor results in a smaller critical inductance, as shown in Fig. 3-3.

![Fig. 3-3 Critical inductance vs. the time constant of capacitors](image-url)
3.3 Large Transient Operation under Original Control Scheme

The synchronous buck converter with the proposed digital controller was shown earlier in Chapter 2 as Fig. 2-7. The control function \( f(z) \) given in equation (2.6) is implemented, a control law which was described in Section 2.2.2, but which can be summarized as follows:

a) If the output voltage is higher than the reference voltage, then \( V_{\text{ref}} \) increases by \( \Delta V_{\text{ref}} \) and \( I_{\text{ref}} \) decreases by \( \Delta I_{\text{ref}} \). If \( V_{\text{ref}} \) reaches its allowed maximum value, no change is made on \( V_{\text{ref}} \).

b) If the output voltage is smaller than the reference voltage, then \( V_{\text{ref}} \) decreases by \( \Delta V_{\text{ref}} \) and \( I_{\text{ref}} \) increases by \( \Delta I_{\text{ref}} \). If \( V_{\text{ref}} \) reaches its allowed minimum value, no change is made on \( V_{\text{ref}} \).

If a large load current transient occurs, the voltage reference and the current reference should vary quickly to establish a new balance. While load transient-up occurs, the voltage reference decreases consecutively and the current reference increases consecutively until a new steady state is established. While load transient-down occurs, the voltage and current increase and decrease consecutively, respectively, until a new steady state is established. In the subsequent discussion this is referred to as the original control scheme.

3.3.1 Typical Operation during Load Transient

Fig. 3-4 shows the typical operation waveforms during load transient-up. It is assumed that the MOSFET turn-on/off delay is zero. At \( t_5 \), load transient-up occurs, and the output voltage \( v_o \) starts to drop. The output voltage \( v_o \) is smaller than the voltage reference \( V_{\text{ref}} \), and by the control law, \( V_{\text{ref}} \) decreases by a small amount \( \Delta V_{\text{ref}} \) step by step and the peak current reference \( I_{\text{ref}} \) increases by \( \Delta I_{\text{ref}} \) step by step. However, the inductor current \( i_L \) continues to decrease. At \( t_6 \), the switch M1 is turned on and the switch M2 is turned off as scheduled in the DPWM module. Then
the inductor current begins to increase, until $t_7$, when the inductor current reaches the new load current. At $t_8$, the switch M1 is turned off and the switch M2 is turned on by the comparison logic $CI$. After that, a new steady state is established by the control law.

Fig. 3-4 Typical operation waveforms during load transient-up

Fig. 3-5 shows the typical operation waveforms during load transient-down. At $t_9$, load transient-down occurs, and the output voltage $v_o$ begins to rise. The output voltage $v_o$ is larger than the voltage reference $V_{ref}$, so by the control law, $V_{ref}$ increases and $I_{ref}$ decreases, although the inductor current $i_L$ continues to decrease. At $t_{10}$, Switch M1 is turned on and Switch M2 is turned off as scheduled in the DPWM module if the inductor current $i_L$ is smaller than the peak current reference $I_{ref}$, at which point the inductor current begins to increase. At $t_{11}$, the switch M1 is turned off and the switch M2 is turned on because of the comparison logic $CI$, and the inductor
current begins to decrease. At $t_{12}$, the inductor current reaches to the new load current, and a new steady state begins to establish itself.

![Typical operation waveforms during load transient-down](image)

**Fig. 3-5 Typical operation waveforms during load transient-down**

### 3.3.2 Constraints on the Operation Clock

In Fig. 3.6 (a), during load transient-up, if the (averaged) current reference variation slope $(f_{clk} \cdot \Delta I_{ref})$ is larger than the slope of inductor current increase then the duty cycle will be saturated; by acting in this manner the digital controller acts as though the control bandwidth is high enough. Similarly, in Fig. 3.6 (b), during load transient-down, if the (averaged) current
reference variation slope \( f_{\text{clk}} \cdot \Delta I_{\text{ref}} \) is smaller than the inductor current increasing slope, the duty cycle will keep to be 0, indicating that the controller is fast enough.

\[
f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{V_m - V_o}{L_f}
\]

\( I_{\text{ref}} \)

\( I_{\text{ref}} \)

\( i_L \)

\( \Delta I_{\text{ref}} \)

\( i_o \)

(a) transient up

\[
f_{\text{clk}} \cdot \Delta I_{\text{ref}} < \frac{-V_o}{L_f}
\]

\( i_L \)

\( I_{\text{ref}} \)

\( \Delta I_{\text{ref}} \)

\( i_o \)

(b) transient down

**Fig. 3-6 Current reference adjustment during load transient**

Hence, if the operating clock \( f_{\text{clk}} \) of the target FPGA and DACs is high enough or the current reference adjustment step \( \Delta I_{\text{ref}} \) is large, a very fast load transient speed can be achieved. Only the inductance \( L_f \) impacts the inductor current transient speed if the operating clock \( f_{\text{clk}} \) meets the following conditions:

- **Load transient-up:** \( f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{V_m - V_o}{L_f} \), and

\[
(3.12)
\]

- **Load transient-down:** \( f_{\text{clk}} \cdot \Delta I_{\text{ref}} < \frac{-V_o}{L_f} \),

\[
(3.13)
\]
where $\Delta I_{\text{ref}}$ is defined as in equation (2.13), and hence is negative during transient-down. In this control scheme, $M$ in (2.13) is normally set to be 1, to take advantage of the full range of the current DAC.

Fig. 3-7 The minimum operation clock to ensure the controller is fast enough during load transient-up

Fig. 3-8 The minimum operation clock to ensure the controller is fast enough during load transient-down
Fig. 3-7 and Fig. 3-8 show the minimum operation clock for target FPGA and DACs to ensure that the digital controller is fast enough during load transient-up and load transient-down. A faster operation clock is required when there is a smaller current reference step $\Delta I_{\text{ref}}$ or a smaller inductance $L_I$.

Fig. 3-9 and Fig. 3-10 show the load transient responses at different speeds of the operation clock, $f_{\text{clk}}$. Comparing results in Fig. 3-9 and Fig. 3-10, it is concluded that better (faster) transient response can be achieved at higher operation clock of target FPGA and DACs. Due to the low conversion ratio ($\leq 0.1$) in modern VR designs, the required capacitance during load transient-down is much larger than that for load transient-up; the constraint in equation (3.13) is much easier to meet than the constraint in equation (3.12). In a practical design, the operating clock $f_{\text{clk}}$ is usually chosen in a reasonable frequency range to meet constraint (3.13) only. In Fig. 3-9(a), although the constraint in (3.12) is not met, there is still no undershoot.

However, further decreasing the operation clock to 8MHz will impair the transient response speed. As shown in Fig. 3-11, transient response speed is limited by the low operation clock since neither constraint is met; explicit undershoot and overshoot exist during load transient up and down, respectively.

The simulation prototype is same as that used in Section 2.3; circuit parameters of the power converter for simulations are listed in Table 2-1. Controller parameters are given in Table 2-2. As a default, in this chapter, same simulation circuits and the same circuit parameters will be used for the simulations unless a change of circuit parameters is explicitly mentioned.
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**Fig. 3-9 Load transient response while $f_{clk}=32$MHz**

(voltage scale: 50mV/div, current scale: (a) 5A/div (b) 10A/div, time scale: 10µs)

**Fig. 3-10 Load transient response while $f_{clk}$ varies from 32MHz to 8MHz**

(voltage scale: (a) 25mV/div (b) 50mV/div, current scale: 10A/div, time scale: 10µs)

The prototype of the two-phase interleaved synchronous buck converter for 12V-1V/40A VRMs is described in Section 2.4. Circuit parameters of the prototype power converter are listed in Table 2-3. Controller parameters are given in Table 2-4. As default, the same prototype and
same circuit parameters will be used for the experimental tests in this chapter, unless a change of circuit parameters is explicitly mentioned.

Fig. 3-11 shows the tested transient response extended waveforms, further verifying the theoretical analysis and simulation results.

![Fig. 3-11 Experimental load transient response with $f_{clk}$=32MHz](image)

(Voltage scale: 20mV/div, current scale: 10A/div, time scale: 10µs/div)
To keep the dynamic performance within the desired specifications, the minimum current reference step $\Delta I_{\text{ref}}$ should be increased while decreasing the operation clock. Fig. 3-12 shows the transient response while the operation clock frequency is decreased from 32MHz to 8MHz and the minimum current reference step $\Delta I_{\text{ref}}$ is increased by 4 times accordingly. The transient response in this case is similar to that in Fig. 3-9. A big disadvantage of increasing the minimum current reference step $\Delta I_{\text{ref}}$ is that the amplitude of the low frequency dithering ripple becomes larger, because the minimum voltage reference step $\Delta V_{\text{ref}}$ will also increase with $\Delta I_{\text{ref}}$ according to the desired output impedance. And it also results in larger error on the output voltage.

![Transistor](image)

**Fig. 3-12 Load transient response while $f_{\text{clk}}=8$MHz and large reference step**

(voltage scale: 25mV/div, current scale: 5A/div, time scale: 5µs)

Fig. 3-13 shows the tested load transient response waveforms. The operation clock frequency is set to 4MHz. Large overshoot and undershoot occur as expected because of slow transient response speed limited by the low operation clock frequency.
3.3.3 Minimum Output Capacitors

The required minimum output filter capacitors are determined by Equations (2.60), (3.10), and (3.11). However, if the conditions in (3.12)/(3.13) are not met, the inductor current slew rate (transient-up/transient-down) will be limited by the reference current upwards/downwards slew rate, and the constraints in (3.10)/(3.11) will be not valid.

If the conditions in (3.12) or (3.13) are not met, to re-derive the capacitor constraints, the discharging current of the output capacitor (originally defined in equation (3.3)) should be approximately rewritten as

\[
i_c(t) = i_o(t) - i_L(t) = \begin{cases} 
\Delta I_o = I_{o1} - I_{o0} & -t_D \leq t < 0 \\
\Delta I_o - f_{\text{clk}} \cdot \Delta I_{\text{ref}} \cdot t & 0 \leq t \leq t_r 
\end{cases}
\]

(3.14)

Fig. 3-13 The tested load transient response waveforms with \( f_{\text{clk}} = 4 \text{MHz} \)

(voltage scale: 20mV/div, time scale: 500\( \mu \text{s}/\text{div} \))
where to generalize the equations, $\Delta I_{ref}$ is deemed as a positive value during load transient-up and as a negative value during load transient-down.

Similarly, the output voltage over the time after $t=0$ is re-derived as

$$v_{o}(t) = v_{ESR} + v_c = -i_c(t) \cdot ESR - \int_{t_p}^{t} i_c(t) dt + V_{a0}$$

$$= V_{a0} - \frac{\Delta I_o \cdot t}{C} - ESR \cdot (\Delta I_o - f_{clk} \cdot \Delta I_{ref} t) - \frac{1}{C} \int_{0}^{t} (\Delta I_o - f_{clk} \cdot \Delta I_{ref} t) \cdot dt \cdot$$  \hspace{1cm} (3.15)

$$= V_{a0} - \frac{\Delta I_o \cdot t}{C} - ESR \cdot (\Delta I_o - f_{clk} \cdot \Delta I_{ref} t) - \frac{\Delta I_o}{C} t + \frac{f_{clk} \cdot \Delta I_{ref}}{2} t^2$$

In order to find out the peak output voltage $V_{opk}$, it is necessary to calculate the derivative of the output voltage with respect to time:

$$\frac{dv_o}{dt} = ESR \cdot f_{clk} \cdot \Delta I_{ref} - \frac{\Delta I_o}{C} + \frac{f_{clk} \cdot \Delta I_{ref}}{C} t \cdot$$ \hspace{1cm} (3.16)

By setting Equation (3.16) equal to zero and solving for $t$, $T_m$ is calculated as

$$T_m = \frac{\Delta I_o}{f_{clk} \cdot \Delta I_{ref}} - ESR \cdot C \cdot$$ \hspace{1cm} (3.17)

It is physically impossible for the peak output voltage to occur before the controller reacts. Therefore, $T_m$ should be redefined as

$$T_m = \begin{cases} 0 & f_{clk} \cdot \Delta I_{ref} > \frac{\Delta I_o}{ESR \cdot C} \\ \frac{\Delta I_o}{f_{clk} \cdot \Delta I_{ref}} - ESR \cdot C & f_{clk} \cdot \Delta I_{ref} \leq \frac{\Delta I_o}{ESR \cdot C} \end{cases}$$ \hspace{1cm} (3.18)

By substituting (3.18) into (3.15), the peak output voltage $V_{opk}$ is calculated as
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\[
V_{\text{opk}} = \begin{cases} 
V_o - \frac{\Delta I_o \cdot t_D}{C} - ESR \cdot \Delta I_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{\Delta I_o}{ESR \cdot C} \\
V_o - \frac{\Delta I_o \cdot t_D}{C} - \frac{ESR^2 \cdot C \cdot V_L \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}}{2} - \frac{\Delta I_o^2}{2C \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}} & f_{\text{clk}} \cdot \Delta I_{\text{ref}} \leq \frac{\Delta I_o}{ESR \cdot C} 
\end{cases}
\]

(3.19)

The maximum voltage deviation can be solved for:

\[
V_{\text{omax}} = V_o - V_{\text{opk}} = \begin{cases} 
\frac{\Delta I_o \cdot t_D}{C} + ESR \cdot \Delta I_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{\Delta I_o}{ESR \cdot C} \\
\frac{\Delta I_o \cdot t_D}{C} + \frac{ESR^2 \cdot C \cdot V_L \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}}{2} + \frac{\Delta I_o^2}{2C \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}} & f_{\text{clk}} \cdot \Delta I_{\text{ref}} \leq \frac{\Delta I_o}{ESR \cdot C} 
\end{cases}
\]

(3.20)

During load transient-up, a new constraint on the size of output capacitance needs to be derived instead of Equation (3.10) if the condition in (3.12) is not met:

\[
\begin{cases} 
\frac{\Delta I_{\text{omax}} \cdot t_D}{C} + ESR \cdot \Delta I_{\text{omax}} \leq \Delta I_{\text{omax}} \cdot R_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{\Delta I_o}{ESR \cdot C} \\
\frac{\Delta I_{\text{omax}} \cdot t_D}{C} + \frac{ESR^2 \cdot C \cdot V_L \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}}{2} + \frac{\Delta I_{\text{omax}}^2}{2C \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}} \leq \Delta I_{\text{omax}} \cdot R_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} \leq \frac{\Delta I_o}{ESR \cdot C} 
\end{cases}
\]

(3.21)

Similarly, during load transient-down, a new output capacitance size constraint is required to replace Equation 3.11 if the condition in (3.13) is not met:

\[
\begin{cases} 
\frac{\Delta I_{\text{omax}} \cdot t_D}{C} + ESR \cdot \Delta I_{\text{omax}} \geq \Delta I_{\text{omax}} \cdot R_o - \Delta V_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{\Delta I_o}{ESR \cdot C} \\
\frac{\Delta I_{\text{omax}} \cdot t_D}{C} + \frac{ESR^2 \cdot C \cdot V_L \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}}{2} + \frac{\Delta I_{\text{omax}}^2}{2C \cdot f_{\text{clk}} \cdot \Delta I_{\text{ref}}} \leq \Delta I_{\text{omax}} \cdot R_o - \Delta V_o & f_{\text{clk}} \cdot \Delta I_{\text{ref}} \leq \frac{\Delta I_o}{ESR \cdot C} 
\end{cases}
\]

(3.22)

Hence, the required minimum output filter capacitance is determined by (2.60), (3.10) or (3.21), and (3.11) or (3.22), depending on whether or not the constraints (3.12) and (3.13) are met.
The action delay $t_D$ is important to determine the required minimum capacitance. The largest delay in the worst case can be approximated as

\[
\text{Load transient-up: } t_{D,\text{WST}} = \frac{2-D}{2f_{sw}} + t_{dc}, \quad \text{and} \\
\text{Load transient-down: } t_{D,\text{WST}} = \frac{1+D}{2f_{sw}} + t_{dc},
\]

where $t_{dc}$ is the circuit delay, including the turn-on/off delay of the switches and the gate driver delay.

The critical operating clock frequency $f_{clk\_cr}$ can be derived from (3.17):

\[
f_{clk\_cr} = \frac{\Delta I_o}{ESR \cdot C \cdot \Delta I_{ref}}
\]

Setting the operating clock frequency $f_{clk}$ above the critical operating clock frequency $f_{clk\_cr}$ will minimize the output voltage spike. Since the inductor current slew rate is fast enough to follow load current, further increases in the operating clock frequency will not help to reduce the output voltage spike.

### 3.4 Control Methods to Improve Transient Response

#### 3.4.1 Dynamic Reference Step Adjustment

Under the original control scheme, a high operation clock speed is necessary to achieve fast transient response, and to reduce the operation clock frequency $f_{clk}$, the minimum current reference step $\Delta I_{ref}$ should be increased accordingly. Under the desired output impedance AVP control, given in equations (2.6) and (2.15), the minimum voltage reference step $\Delta V_{ref}$ should also increase proportionally, resulting in big errors and a large dithering ripple on the output voltage.
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To reduce the operation clock speed without impairing steady-state performance, a dynamic reference step adjustment method is used. Since constraints (3.12) and (3.13) are necessary only for the load transient operation to achieve fast transient response, a larger current reference adjustment step is used to meet constraints (3.12) and (3.13) during the load transient stage and a smaller current reference adjustment step is used during steady-state stage to achieve good steady-state performance.

![Flow chart of the control unit](image)

**Fig. 3-14 Flow chart of the control unit**

A control unit is implemented to judge whether the power system is in the transient state or not. By observing operation waveforms in Fig. 3-6, it is found that the current reference
continuously increases during load transient-up and the current reference continuously decreases during load transient-down. Therefore, a counter TU is used to count the consecutive increase of the current reference, and another counter TD is used to count the consecutive decrease of the current reference. The counter TU is reset to zero if the current reference decreases and the counter TD is reset to zero if the current reference increases. If the counter TU reaches a limitation value \(LMT_{TU}\), predefined in the digital controller, it will judge that there is a load transient-up. If the counter TD reaches the limitation value \(LMT_{TD}\), predefined in the digital controller, it will judge that there is a load transient-down. When judged to be in a transient state, the adjustment step of the voltage/current reference will increase to a larger amount (predefined) than in the steady state. Hence, the voltage reference and the current reference will reach the new balance value quickly at the same operating clock frequency. Fig. 3-14 shows a flow chart of the control unit.

The typical operation waveforms are the same as those with the original control scheme. The only difference is that the reference adjustment amounts \(\Delta V_{ref}\) and \(\Delta I_{ref}\) in the transient-state stage are larger than those in the steady-state stage. Therefore, the constraints in equations (3.12) and (3.13) can be met in the load transient stage when they matter and be violated in the steady-state stage when these conditions are not important. A relatively low frequency may be chosen for the operation clock.

Choosing the limitation values \(LMT_{TU}\) and \(LMT_{TD}\) is very important to achieve good performance. Limitation values that are too large slow down the transient response and limitation values that are too small affect steady-state operation and impair steady-state performance. By observing the relationship between the voltage reference and the output voltage in Fig. 2-27, appropriate minimum limitation value constraints can be determined to be
\[ LMT_{TU} \geq \min \left\{ \text{int} \left( \frac{f_{\text{sw}}}{2f_{\text{clk}}} \right), \text{int} \left( \frac{\Delta V_{o,r}}{\Delta V_{\text{ref}}} \right) \right\} + 1 \text{, and} \]

\[ LMT_{TD} \geq \min \left\{ \text{int} \left( \frac{f_{\text{sw}}}{2f_{\text{clk}}} \right), \text{int} \left( \frac{\Delta V_{o,r}}{\Delta V_{\text{ref}}} \right) \right\} + 1 \]

where \( D \) is the duty cycle, \( f_{\text{sw}} \) is the switching frequency, \( f_{\text{clk}} \) is the operating clock frequency of the target FPGA and DACs, \( \Delta V_{o,r} \) is the peak-to-peak output ripple voltage, \( \text{int}[x] \) is the function that takes the smallest integer larger than \( x \), and \( \text{min}[x,y] \) is the function that takes the smaller value of \( x \) and \( y \).

It is assumed that \( M \) is always equal to 1 in equation (2.13) in the steady-state stage. \( M \) for the transient-state stage can be selected to achieve good dynamic performance as follows:

Load transient-up: \( M \geq \text{int} \left( \frac{V_{\text{in}} - V_o}{\Delta I_{\text{ref}} \cdot L_f \cdot f_{\text{clk}}} \right) \), and

Load transient-down: \( M \geq \text{int} \left( \frac{V_o}{\Delta I_{\text{ref}} \cdot L_f \cdot f_{\text{clk}}} \right) \).

If \( M \) in (2.13) is chosen according to (3.28) and (3.29) for the transient-state stage and \( \Delta I_{\text{ref}} \) is replaced by \( M \cdot \Delta I_{\text{ref}} \) in the constraints (3.12) and (3.13), then these constraints will be always satisfied during the load transient stage. Therefore, the required minimum output filter capacitors can once again be determined by (2.60), (3.10), and (3.11). The largest action delay \( t_d \) in the worst case can be also approximated by (3.23) and (3.24).
Fig. 3-15 The transient response with $f_{clk}=8$MHz and dynamic reference step adjustment (voltage scale: 25mV/div, current scale: 10A/div, time scale: 10µs)

Fig. 3-15 shows the transient response with a reduced operation clock speed and a dynamic reference step adjustment. When compared with Fig. 3-10, the dynamic performance improvement is apparent without impairing the steady-state performance.

Fig. 3-16 shows the tested load transient response extended waveforms with reduced operation clock speed (8MHz) and a dynamic reference step adjustment. Its transient response performance is comparable to that of a digital controller with 32MHz shown in Fig.3-11.
3.4.2 Non-linear Control

The dynamic reference step adjustment method helps to improve the transient response under a low operation clock speed, but it cannot reduce the transient-assertion-to-action delay, which impairs the transient response. As shown in Fig. 3-17(a), the channel #1 switch action occurs following an elapsed time interval \( t_{dl} \) after the load transient-up is asserted by the control unit,
and the channel #2 switch action delays is represented by $t_{d2}$. This is because the turn-on of the high-side switches is only scheduled by the timing of the DPWM module. The delay $t_{d1}$ is almost half the switching period and the delay $t_{d2}$ is nearly an entire switching period. Such large delays result in slow transient response and a requirement for a large number of bulk capacitors. In Fig.3-17(b), a transient-assertion-to-action delay also exists since the action of turning off the high-side switches is controlled only by the current comparison result.

**Fig. 3-17** The transient-assertion-to-action delay without non-linear control
(voltage scale: (a) 25mV/div (b) 20mV/div, current scale: 10A/div, time scale: 5µs)

Hence, non-linear controls, here including operation-state recognition, decision-making, and multi-mode, are used to reduce the transient-assertion-to-action delay. Under non-linear control, once the control unit asserts load transient-up, the controller will enter transient-up mode and all high-side switches will be turned on to obtain maximum inductor current ascending slew rate; once the control unit asserts load transient-down, the controller will go into transient-down mode and all high-side switches will be turned off to obtain maximum inductor current descending slew rate. Hence, in this manner, the transient-assertion-to-delay is minimized.
Fig. 3-18 Control idea of non-linear control

The control unit for judging the transient state is also implemented. The flow chart of this mode control unit is also illustrated in Fig. 3-14, but non-linear control can be used in the transient state, here named transient mode. Fig. 3-18 shows the block diagram of this non-linear control. In the steady state, peak current mode control (linear control) is applied, named normal operation mode. But in transient mode, the peak current mode control will be disabled and the adjustment step of the voltage/current reference will increase to a (predefined) larger amount than in normal operation mode. This control scheme offers very fast load transient speed, especially in multi-phase VRMs, where during load transient-up all high-side switches will be closed and all low-side switches will be opened, and during load transient-down, all high-side switches will be opened and all low-side switches will be closed or opened.

With this control scheme, the constraints (3.12) and (3.13) are not applied, since in transient mode the turn-on or -off of switches are controlled by decision-making behavior of the digital controller, regardless of the relationship between the current reference and the inductor current.
(peak current mode control is disabled). Therefore, the required minimum output capacitors are safely determined by (2.60) (3.10) (3.11).

The largest action delay \( t_D \) in the worst case, which is important to determine the minimum output bulk capacitors, can be approximated by

\[
\text{Load transient-up: } t_{D_{\text{wST}}} = \min \left[ \frac{(2 - D)}{2 f_{sw}}, \frac{LMT \_ TU}{f_{sw}} \right] + t_{dc} \quad \text{and} \quad \frac{LMT \_ TD}{f_{sw}} + t_{dc} \quad , \quad (3.30)
\]

\[
\text{Load transient-down: } t_{D_{\text{wST}}} = \min \left[ \frac{(1 + D)}{2 f_{sw}}, \frac{LMT \_ TD}{f_{sw}} \right] + t_{dc} \quad , \quad (3.31)
\]

where \( t_{dc} \) is the circuit delay, including the turn-on/off delay of the switches and the gate driver delay.

As mentioned above, the dynamic reference step adjustment is also applied. The selection of the magnitude of the reference adjustment step is important to achieve good dynamic performance, such as small voltage spikes and a reduced voltage ring-back oscillation. During the load transient-up stage, the voltage reference should be larger than the output voltage before the output voltage reaches its minimum, and then it will stay within transient mode and force the inductor current to continue increasing. Referring back to (3.10), the constraint on the reference adjustment amount can be expressed as

\[
M \leq \left\{ \begin{array}{ll}
\frac{\Delta I_{\text{max}} \cdot t_D + ESR \cdot \Delta I_{\text{max}} - \Delta V_{\text{ref}} \cdot LMT \_ TU}{C \cdot \Delta V_{\text{ref}} \cdot \text{int}[t_{dc} + T_m] f_{\text{ck}}} \\
\Delta V_{\text{ref}} \cdot \text{int}[t_{dc} + T_m] f_{\text{ck}} \end{array} \right. \quad \frac{L_f < L_{\text{crit}}}{L_f \geq L_{\text{crit}}} , \quad (3.32)
\]

\[
\left\{ \begin{array}{ll}
\Delta I_{\text{max}} \cdot t_D + \frac{ESR \cdot C \cdot (V_{\text{in}} - V_f) + \Delta I_{\text{max}}^2 \cdot \frac{L_f^2}{2L_f \cdot C \cdot (V_{\text{in}} - V_f)} - \Delta V_{\text{ref}} \cdot LMT \_ TU}{C} \\
\Delta V_{\text{ref}} \cdot \text{int}[t_{dc} + T_m] f_{\text{ck}} \end{array} \right. \quad \frac{L_f < L_{\text{crit}}}{L_f \geq L_{\text{crit}}}
\]

where it is assumed that \( M=1 \) in equation (2.13) in the steady-state stage. \( M \) for the transient-up state stage can be chosen to be the largest integer number that meets constraint (3.32).
Similarly, during the load transient-down stage, the voltage reference will be smaller than the output voltage before the output voltage reaches its maximum, and then it will stay in transient mode and as the inductor current continues to decrease. Referring to (3.11), the constraint on the reference adjustment amount can be expressed as

\[
M \leq \begin{cases} 
\frac{\Delta I_{\text{max}} \cdot t_D + ESR \cdot \Delta I_{\text{max}} - \Delta V_{\text{ref}} \cdot LMT \cdot TD}{\Delta V_{\text{ref}} \cdot \text{int}\left(\frac{t_{\text{dc}} + T_\alpha}{f_{\text{clk}}}\right)} & L_f < L_{\text{crit}}, \\
\frac{\Delta I_{\text{max}} \cdot t_D + ESR^2 \cdot C \cdot V_o^2 + \Delta I_{\text{max}}^2 \cdot L_f^2 - \Delta V_{\text{ref}} \cdot LMT \cdot TD}{2L_f \cdot C \cdot V_o} & L_f \geq L_{\text{crit}}
\end{cases}
\]

(3.33)

where it is assumed that \( M=1 \) in (2.13) in the steady-state stage. \( M \) for the transient-down state stage can be chosen to be the largest integer number that meets the constraint (3.33).

Fig. 3-19 shows the transient response with non-linear control. The transient-assertion-to-action delay is minimized. In Fig. 3-19 (a), once the load transient-up is asserted, all high-side switches are turned on to obtain maximum inductor current slew rate. As a result, a fast transient response speed is achieved and the number of bulk capacitors is reduced from 3 to 2.
Fig. 3-19 The transient response with non-linear control
(voltage scale: 25mV/div, current scale: 5A/div, time scale: (a) 10µs (b) 5µs)

Fig. 3-20 shows the experimental transient response. The number of bulk capacitor (470uF) is reduced from 3 to 2 as expected by simulation with the same performance, compared to the digital controller with dynamic reference step adjustment shown in Fig. 3-16.

Fig. 3-20 The experimental transient response with non-linear control
(voltage scale: 20mV/div, time scale: 500µs/div)
In fact, the number of bulk capacitors can be further reduced to 1. However, in this case the voltage-ring back will be large, which is not acceptable, as shown in Fig. 3-21.

![Fig. 3-21 Enlarging view of the voltage ring-back](image)

(voltage scale: 13.7mV/div, time scale: 3.25µs/div)

### 3.4.3 Transient Detection Circuit

In the dynamic reference step adjustment method and non-linear control described in Sections 3.4.1 and 3.4.2, a control unit is used to assert whether the power system operation status is transient or steady-state. Two counters are implemented to count successive current/voltage reference adjustments. However, due to the output voltage ripple and recalling the limitation values defined in (3.26) and (3.27), normally, several operation clock periods (10 or more) are required to determine the switch to the transient state. Regardless of the transient step amount and transient current slew rate, the time needed to assert the transient state stays nearly the same. This delay becomes worse when the operation clock decreases.
To mitigate this problem, a dedicated transient detection circuit is implemented to detect the load transient, as shown in Fig. 3-22 (a). A voltage limitation gap is formed around the voltage reference, as shown in Fig. 3-22 (b), and always follows the voltage reference.

![Diagram of transient detection circuit and voltage limitation gap](image)

**Fig. 3-22 Dedicated transient detection circuit**

In the steady state, the voltage reference tightly follows the output voltage $v_o$, so the output voltage stays within the voltage limitation gap. Once load transient-up occurs, the output voltage will drop quickly. If it becomes smaller than the bottom limit $V_{LD}$ of the voltage limitation gap, the transient detection circuit will assert a signal indicating load transient-up state. Similarly, once load transient-down occurs, the output voltage will ascend quickly. If it becomes larger than the upper limit $V_{LU}$ of the voltage limitation gap, the transient detection circuit will assert a signal indicating load transient-down state.

Obviously, the larger the load current transient step or the faster the load current transient slew rate, the faster the output voltage drops or ascends, and the earlier the transient detection circuit asserts the transient state status.
3.5 Dual Voltage Loop Control

As described in the previous section, the dynamic reference step adjustment method breaks the constraints on the operation clock and finds a new balance point quickly, the transient detection circuit detects the load transient-up/down in a manner adaptive to the load transient step amount and slew rate, and the non-linear control minimizes the transient-assertion-to-action delay and maximizes the inductor current slew rate. All three of these methods help improve the dynamic performance.

![Synchronous buck converter with dual voltage loop control](image)

**Fig. 3-23 Synchronous buck converter with dual voltage loop control**

The proposed dual voltage loop control integrates these three methods to achieve a fast transient response speed. Fig. 3-23 shows the configuration of a single-phase synchronous buck converter with dual voltage loop control. There are also two digital-to-analog converters implemented in the digital controller, one each to generate the current and voltage references. Two voltage loops are implemented: one a slow voltage loop with a low-pass filter (H), and the
other a fast voltage loop. The purpose of the two voltage loops is to smooth the load transient transition and improve the system stability. A dedicated load transient detection circuit is implemented to detect the transient state.

Similar to the proposed digital controller with one voltage loop control, the AVP control function based on (2.6) is also implemented in the digital control algorithm block. Therefore, the straightforward adjustment control law to achieve AVP is also applied. See Section 2.2.2 for details, but recall that the voltage reference moves stepwise in the direction of the output voltage until its maximum or minimum is reached while the peak current reference is adjusted in the opposite direction.

![Fig. 3-24 Block view of the dual voltage loop control](image-url)
Chapter 3 Control Algorithms to Improve Dynamic Performance

If the slow voltage loop is closed, the voltage reference will follow the sensed output voltage $v_s$ in the slow voltage loop. But, if the fast voltage loop is closed then the voltage reference should follow the sensed output voltage $v_q$ in the fast voltage loop. The control idea of the dual voltage loop control is illustrated in Fig. 3-24.

Fig. 3-25 Control strategy of dual voltage loop control

Fig. 3-25 shows the control strategy of the dual voltage loop control, involving three modes of operation: normal operation mode, transient mode, and link mode. Peak current mode control is utilized in the normal operation mode and link mode. The slow voltage loop is closed in normal operation mode, but the fast voltage loop is closed in link mode. Non-linear control is used in transient mode, while peak current mode control is disabled. The link mode makes the load transient transition smoothly without large voltage ring-back.
Transitions among three types of operation modes are controlled by the mode control unit. The mode control unit accepts transient indication signals ($CV_{qd}$ and $CV_{qu}$) from the dedicated transient detection circuit, and control logic signals ($CV$ and $CV_q$) from the slow/fast voltage loop comparators.

**Fig. 3-26 Voltage limitation gap of the transient detection circuit**

Fig. 3.26 shows the voltage limitation gap for load transient detection. The voltage gap always follows the voltage reference $v_{ref}$. In the steady state, the voltage reference tightly follows the sensed output voltage $v_s$, which is the fed back by the slow voltage loop.

If load transient-down occurs, the output voltage $v_q$, which is fed back by the fast voltage loop, will ascend ahead of the output voltage $v_s$ and the voltage reference $v_{ref}$. When the output voltage $v_q$ reaches and becomes larger than the upper limit $V_{LU}$ of the voltage limitation gap, the transient detection circuit asserts a signal indicating load transient-down state. The controller enters transient-down mode. In transient-down mode, peak current mode control is disabled and non-linear control is applied. All high side switches is turned off to maximize inductor current.
descending slew rate and a large current/voltage reference step is used to track the new balance point. The voltage limitation gap also follows the variation of the voltage reference. When the output voltage \(v_q\) goes back into the voltage limitation gap, the controller enters link mode. In this mode, the fast voltage loop is closed and the slow voltage loop is open. The voltage reference \(v_{\text{ref}}\) follows the output voltage \(v_q\). A medium current/voltage reference step will be used to track the new balance point and peak current mode control is applied. The voltage limitation gap still follows the variation of the voltage reference. When the voltage reference crosses over the output voltage \(v_o\) again, the controller enters normal operation mode. In this mode, the slow voltage loop is closed and the fast voltage loop is open. A small current/voltage reference step is used to achieve good steady-state performance.

Similarly, if load transient-up occurs, the output voltage \(v_q\), which is fed back by the fast voltage loop drops ahead of the output voltage \(v_o\) and the voltage reference \(v_{\text{ref}}\). When the output voltage \(v_q\) reaches and becomes smaller than the bottom limit \(V_{LD}\) of the voltage limitation gap, the transient detection circuit asserts a signal indicating load transient-up state. The controller will enter the transient (up) mode. In the transient-up mode, peak current mode control is disabled and non-linear control is applied. All high side switches is turned on to maximize inductor current ascending slew rate and a large current/voltage reference step is used to track the new balance point. The voltage limitation gap still follows the variation of the voltage reference. When the output voltage \(v_q\) goes back into the voltage limitation gap, the controller enters link mode, where the fast voltage loop is closed and the slow voltage loop is open. The voltage reference \(v_{\text{ref}}\) follows the output voltage \(v_q\). A medium current/voltage reference step is used to track the new balance point, and peak current mode control is applied. When the voltage reference crosses over the output voltage \(v_o\) again, the controller enters normal operation mode. In this mode, the slow
voltage loop is closed and the fast voltage loop is open. A small current/voltage reference step is used while peak current control is also applied.

Note that the higher the load current transient and the higher the load current slew rate, the earlier the controller goes into transient mode. If the load current step amount is low or the load current slew rate is low, the controller may not enter transient mode, since normal operation mode, in which the dynamic reference step adjustment method is embedded, can handle such a load transient.

In applications with a high load current slew rate and a large load current transient step, the dual voltage loop control will exhibit its superiority over other control schemes. In this situation, the output voltage variation caused by ESL and ESR of the output capacitors forces the controller go into the transient mode immediately, as shown in Fig.3-22. The largest action delay \( t_D \) here is the circuit delay \( t_{dc} \), including the comparator delay, the turn-on/off delay of the switches and the gate driver delay.

![Fig. 3-27 Output voltage spike deviation during load transient](image-url)
Therefore, the voltage limitation gap should be chosen carefully. If the gap is too narrow, that is, if $V_{bu}$ and $V_{bd}$ are too small, it may interfere with steady state operation. If the gap is too wide, the dynamic performance of the controller will be degraded and more output capacitors or a smaller power inductor may be needed. The factors to be considered while choosing the gap voltage ($V_{bu}$ and $V_{bd}$) are summarized as follows:

1) the output voltage ripple $\Delta V_{O,R}$;

2) the dithering voltage ripple $\Delta V_{O,d,R}$;

3) the offset voltage between the fast voltage loop and slow voltage loop $V_{offset}$; and

4) the noise $V_{noise}$.

Also, a certain margin should be added to the sum of all of items mentioned above. Typically, the gap voltages ($V_{bu}$ and $V_{bd}$) are chosen to be equal to each other, within the range of 25mV ~ 35mV.

The selection of the reference adjustment steps is another important factor to achieve good dynamic performance, such as small voltage spikes and reduced voltage oscillation. During load transient-up mode, the voltage reference should keep up with the output voltage as quickly as possible. The current reference should also increase to track the new load current. Referring to (3.4), the constraint on the reference adjustment amount can be expressed as

$$M_t \geq \frac{\Delta I_{omax} - \left( t_{dc} + \frac{2}{f_{cik}} \right) + ESR \cdot \Delta I_{omax} - V_{bd} - \left( ESR + \frac{1}{C \cdot f_{cik}} \right) \cdot \frac{2 \cdot (V_{in} - V_o) - \text{in}[t_{dc} \cdot f_{cik}]}{L_f \cdot f_{cik}} - \Delta V_{ref}}{2 \cdot \Delta V_{ref}}, \quad (3.34)$$

where it is assumed that $M=1$ in equation (2.13) in the steady-state stage. $M_t$ for the transient-up state stage can be chosen to be the smallest integer number that meets constraint (3.34).
During link-up mode, the voltage reference should catch up with the output voltage before the output voltage reaches its minimum and the voltage reference deviation rate should be larger than the output voltage deviation rate to avoid entering transient mode again. Therefore, the constraint on the reference adjustment amount can be expressed as

\[
M_z \geq \begin{cases} 
\frac{ESR \cdot C \cdot (V_{in} - V_o) - \Delta I_{\text{max}} \cdot L_f}{\Delta V_{\text{ref}} \cdot f_{\text{clk}} \cdot L_f \cdot C} & L_f < L_{\text{crit}}, \\
\frac{\Delta I_{\text{max}} \cdot t_{\text{ch}} + \frac{ESR \cdot C^2 \cdot (V_{in} - V_o)^2 + \Delta I_{\text{max}}^2 \cdot L_f^2}{2L_f \cdot C \cdot (V_{in} - V_o)} - 2 \cdot \Delta V_{\text{ref}} \cdot M_z \cdot \text{int}[t_{\text{ch}} \cdot f_{\text{clk}}]}{\Delta V_{\text{ref}} \cdot \text{int}[T_{\text{m}} \cdot f_{\text{clk}}]} & L_f \geq L_{\text{crit}}
\end{cases}
\]

\( M_z \) for the link-up mode stage can be chosen to be the smallest integer number that meets the constraint (3.35).

During the load transient-down stage, the inductor slew rate is quite low, so the controller should stay in the transient mode before the output voltage reaches its maximum, and make the inductor current continue decreasing. Referring to (3.11), the constraint on the reference adjustment amount can be expressed as

\[
M_z \leq \begin{cases} 
\frac{\Delta I_{\text{max}} \cdot t_{\text{ch}} + ESR \cdot \Delta I_{\text{max}} - \Delta V_{\text{ba}} - \text{int}[t_{\text{ch}} \cdot f_{\text{clk}}]}{\Delta V_{\text{ref}} \cdot \text{int}[T_{\text{m}} \cdot f_{\text{clk}}]} & L_f < L_{\text{crit}}, \\
\frac{\Delta I_{\text{max}} \cdot t_{\text{ch}} + \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I_{\text{max}}^2 \cdot L_f^2}{2L_f \cdot C \cdot V_o} - \Delta V_{\text{ba}} - \text{int}[t_{\text{ch}} \cdot f_{\text{clk}}]}{\Delta V_{\text{ref}} \cdot \text{int}[T_{\text{m}} \cdot f_{\text{clk}}]} & L_f \geq L_{\text{crit}}
\end{cases}
\]

where it is assumed that \( M = 1 \) in (2.13) in the steady-state stage. \( M \) for the transient-down state stage can be chosen to be the largest integer number that meets the constraint (3.36).
During the link-down mode, the current reference deviation rate should be larger than the inductor current slew rate to keep the inductor current decreasing, and catch up with load current quickly to avoid entering the transient mode again. The constraint on the reference adjustment amount can be expressed as

\[
M_L \geq \text{int} \left[ \frac{V_o}{\Delta I_{\text{ref}} \cdot L_f \cdot f_{\text{clk}}} \right]
\]

\[
M_L \geq \text{int} \left[ \frac{\Delta I_{\text{max}}}{\Delta I_{\text{ref}}} - t \cdot f_{\text{clk}} \cdot M_t \right]
\]

\[
t \cdot f_{\text{clk}} \cdot M_t \cdot \Delta V_{\text{ref}} + V_{\text{bu}} \geq \frac{\Delta I_o \cdot t_{\text{dc}}}{C} + \text{ESR} \cdot (\Delta I_o - \frac{V_i}{L_f} \cdot t) + \frac{\Delta I_o \cdot t^2}{2L_f \cdot C}
\]

\[
t \cdot f_{\text{clk}} \in (1, 2, 3, \ldots)
\]

\[
t \geq T_m
\]

where it is assumed that \( M=1 \) in (2.13) in the steady-state stage. \( M \) for the transient-down state stage can be chosen to be the smallest integer number that meets the constraint (3.37).

Fig. 3-28 The load transient response with dual-voltage-loop control

(voltage scale: (a) 10mV/div (b) 25mV/div, current scale: (a) 5A/div (b) 10A/div, time scale: (a) 5μs (b) 10μs)
Fig. 3-28 shows the transient response with dual-voltage-loop control. The transient-assertion-to-action delay is minimized as non-linear control does. In Fig. 3-28 (a), once the load transient-up is asserted, all high-side switches are turned on to obtain maximum inductor current slew rate. The number of bulk capacitors is reduced from 3 to 1.

Fig. 3-29 shows the tested transient response waveform with dual-voltage-loop control. Because only one bulk capacitor is used, the overshoot (about 20mV) is larger than the overshoot when two bulk capacitors are used (see Fig 3-20 only with non-linear control).

![Output Voltage](image)

**Fig. 3-29 The tested transient response waveform with dual-voltage-loop control**

(voltage scale: 20mV/div, time scale: 500μs/div)

Fig. 3-30 shows the extended transient response waveforms. In Fig. 3-30 (a), all high-side switches are turned on to achieve maximum inductor current increasing slew rate. No large voltage ring-back exists, much better than that shown in Fig. 3-21 which was only with non-linear control. In Fig. 3-30 (b), all high-side switches are turned off to achieve maximum inductor current decreasing slew rate.
3.6 Summary

In this chapter, the relationship between the transient response and the operation clock (or reference updating clock) is first investigated, which gives the critical output capacitor requirement in terms of the operation clock. After that, three control methods are addressed to
improve the dynamic performance. The dynamic reference step adjustment method breaks the constraints on the operation clock and finds a new balance point quickly; the transient detection circuit detects the load transient-up/down in a manner adaptive to the load transient step amount and slew rate; and the non-linear control minimizes the transient-assertion-to-action delay and maximizes the inductor current slew rate. Finally, the dual voltage loop control is proposed, which integrates all these methods to achieve a fast transient response speed. Simulation and experimental results demonstrate dynamic performance improvements using these methods.
Chapter 4

Dynamic Performance under Large-Step Load Oscillation

4.1 Power Delivery Path Impedance Analysis

Since the dedicated voltage regulator needs to supply large current to processors at low voltage, the total voltage tolerance will be much tighter than ever before. With the dynamic power management control in multi-core processors, the high clock frequency induces a very fast current slew rate \( (di/dt) \) when the processor operation changes from sleep state to power state and vice versa or dynamically disables/enables one or multiple cores [4] [10]. The state transition frequency could reach up to hundreds of KHz. Such high dynamic characteristics of the processors impose large-step load oscillations to the voltage regulators, making it more difficult to maintain accurate voltage regulation.

To deliver power successfully to processors, interconnection parasitic resistance and inductance on the power delivery path should be minimized. Therefore, a dedicated VR is placed as close as possible to the processor to reduce the interconnection parasitics of the power delivery path. Fig. 4-1 shows the typical power solution for today’s processors on LGA775 sockets, in which a dedicated VR is placed so as to surround the processor. VR phases are distributed north and east of the processor. A multi-stage decoupling solution with different types of capacitors is used to meet the impedance target across a range of frequencies. High frequency ceramic capacitors are used for mid-frequency decoupling and placed on the motherboard inside the socket cavity; bulk capacitors are placed at the output of the voltage regulator to address low-frequency decoupling needs [42-43].
Chapter 4 Dynamic Performance under Large-step Load Oscillation

Fig. 4-1 Power delivery solution for today’s processor

Fig. 4-2 shows the motherboard and socket model with the proposed digital controller. An N-phase synchronous buck converter is used as the VR, in which \( X \) phases are located north of the processor and \((N-X)\) phases are located east of the processor. The feedback output voltage is sensed at the north point between motherboard and socket and a sensed network \( C_f-R_f \) is used.

\( I_L \) represents the phase inductor current, which is regulated by the digital controller as follows:

\[
\Delta I_L = \Delta I_{\text{ref}} = (N \cdot R_o)^{-\frac{1}{2}} \cdot \Delta V_{\text{ref}} \quad (4.1)
\]

On the other hand, with the outer voltage loop closed, the voltage reference follows the output voltage. Hence, the relationship between variations in the output voltage and the voltage reference is represented as

\[
\Delta V_{\text{ref}} = \Delta V_f = \frac{\Delta V_o}{s \cdot C_f \cdot R_f + 1} \quad (4.2)
\]
With the control loop closed, the following equations can be derived from Fig.4-2:

\[
\begin{align*}
& - (N - X) \cdot v_n = v_e + v_e - v_{oc}, \\
& N \cdot R_o \cdot K_f \frac{Z_E}{Z_{E1}} \frac{Z_N}{Z_{N1}} - X \cdot v_z = v_a + v_a - v_o, \\
& N \cdot R_o \cdot K_f \frac{Z_N}{Z_{N1}} \frac{Z_{E1}}{Z_E}, \\
& i_o = \frac{v_o - v_{cc}}{Z_{S1}} + \frac{v_e - v_{cc}}{Z_{C1}} + \frac{v_{oc} - v_{cc}}{Z_{S2}} + \frac{v_e - v_{cc}}{Z_{S3}}, \\
& v_n - v_o = \frac{v_o - v_e}{Z_{N1}} + \frac{v_e - v_{cc}}{Z_{S1}} + \frac{v_{oc} - v_{cc}}{Z_{S2}} + \frac{v_e - v_{cc}}{Z_{S3}}, \\
& v_e - v_{oc} = \frac{v_o - v_e}{Z_{E1}} + \frac{v_e - v_{cc}}{Z_{E2}} + \frac{v_{oc} - v_{cc}}{Z_{S3}}, \\
& v_c - v_{cc} = \frac{v_o - v_e}{Z_{N2}} + \frac{v_e - v_{cc}}{Z_{E2}} + \frac{v_{oc} - v_{cc}}{Z_{E2}}, \\
& (4.3)
\end{align*}
\]

where \( K_f = s \cdot C_f \cdot R_f + 1 \) and \( Z_f = 1/(s \cdot C_f) + R_f \).
It is assumed that all voltage/current variables \((v_o, v_{oe}, v_e, v_N, v_{ce}, \text{and } i_o)\) in (4.3) are variations on the voltage/current variables \((V_o, V_{oe}, V_e, V_N, V_{ce}, \text{and } I_o)\) respectively.

Hence, the power delivery path impedance \(Z_{op}(s)\) can be derived from (4.3) as follows:

\[
Z_{op}(s) = \frac{v_o}{i_o} = \frac{Y_i(s)}{Y_i(s) \cdot Y_{\text{ac}}(s) + Y_z(s) \cdot Y_{\text{ac}}(s)}
\]  

(4.4)

where

\[
Y_i(s) = K_4 \cdot \left( \frac{1}{Z_{c1} + Z_{s2}} + \frac{1}{Z_{N2}} + \frac{1}{Z_e} \right) - \frac{K_3 + K_2 \cdot K_4}{Z_{s1} \cdot Z_{e2}}
\]

\[
Y_z(s) = \frac{Z_{N2}}{Z_{s1}} \cdot \left( \frac{1}{Z_{c1} + Z_{s2}} + \frac{1}{Z_{N2}} + \frac{1}{Z_e} \right) + \frac{1}{Z_{c1} + Z_{s2}} + \frac{K_3 \cdot Z_{s1} - K_2 \cdot Z_{N2}}{Z_{s1} \cdot Z_{e2}}
\]

\[
Y_{\text{ac}}(s) = \frac{1}{Z_{s1}} + \frac{K_4}{Z_{c1} + Z_{s2}} + \frac{K_3 \cdot Z_{s1} - K_2 \cdot Z_{N2}}{Z_{s1} \cdot Z_{e2}}
\]

\[
K_1 = \frac{- (N - X) \cdot Z_e \cdot Z_{e2} \cdot Z_{s3}}{N \cdot R_o \cdot K_f \cdot \left[ Z_{e2} \cdot (Z_e + Z_{s3}) + Z_{e1} \cdot (Z_{e2} + Z_{s3}) + Z_e \cdot Z_{s3} \right]}
\]

\[
K_2 = \frac{Z_{s3} \cdot (Z_e + Z_{e1})}{Z_{e2} \cdot (Z_e + Z_{s3}) + Z_{e1} \cdot (Z_{e2} + Z_{s3}) + Z_e \cdot Z_{s3}}
\]

\[
K_3 = \frac{Z_{e3} \cdot (Z_e + Z_{e1})}{Z_{e2} \cdot (Z_e + Z_{s3}) + Z_{e1} \cdot (Z_{e2} + Z_{s3}) + Z_e \cdot Z_{s3}}
\]

\[
K_4 = 1 + \frac{Z_{N2}}{Z_{N1}} + \frac{Z_{N2}}{Z_{s1}} + \frac{Z_{N2}}{Z_f} + \frac{Z_N \cdot Z_{N2}}{Z_N + Z_{N1}} \left( \frac{X}{N \cdot R_o \cdot K_f} - \frac{1}{Z_{N1}} \right)
\]
Based on Equation (4.4), Fig. 4-3 shows the power delivery path impedance with proposed digital control loop closed. The power delivery path impedance is largely dependent on the selection of the bulk capacitors, high frequency ceramic capacitors, power plane parasitics and control loop. Within the VR control bandwidth, the power delivery path impedance is regulated by the controller. Above the VR control bandwidth, the power delivery path impedance is dominated by the bulk capacitors, high frequency ceramic capacitor and interconnection parasitic inductance/resistance. Therefore, as required by VR design specifications [42-43], the decoupling capacitor selection needs to be verified to make sure the impedance of the decoupling is below the load line target up to the frequency $F_{\text{break}}$, above which the impedance will be dominated by the processor package decoupling.
4.2 Time Domain Validation by Simulations

When load oscillation frequency approaches or exceeds the VR control bandwidth, the power delivery path impedance is dominated by the bulk capacitors, the filtering capacitors and interconnection resistance/inductance. To ensure that the output voltage not violate the tolerance range under large-step load oscillation over frequencies from DC to $F_{break}$, time domain validations are necessary. One effective way to perform time domain validation is by conducting simulations with the power delivery path model shown in Fig. 4-2.

A two-phase interleaving synchronous buck converter for 12V-1V/40A VRMs is used to conduct simulations. The simulation prototype is same as that used in Section 2.3, with circuit parameters listed in Table 2-1. The phase switching frequency is 250 KHz, the phase inductor is 400nH and the output capacitors are two 330uF capacitors (ESR: 5mΩ/2, ESL: 1.6nH/2). The desired output impedance is set at 2mΩ and the output voltage is set at 1V at no load. The load transient step is 27A (13A→40A) and the current transient slew rate is 2A/ns. Hence, if the output voltage is allowed to overshoot by some amount 50mV above the defined load line during unloading transients, the output voltage tolerance range will be from 0.92V to 1.026V.

Fig. 4-4 through Fig. 4-11 show the load transient response under large-step load oscillation. Some typical frequencies are chosen to demonstrate the time domain validation: 1 kHz, 10 kHz, 50 kHz, 100 kHz, 125 kHz, 250 kHz, 500 kHz, and 1 MHz.

Fig.4-4, Fig.4-5, and Fig.4-6 show the load transient response with 1 kHz, 10k Hz, and 50 kHz load oscillation, respectively. These figures indicate that the output voltage can be sustained within the voltage tolerance range all the time except on the rising/falling edge, which can be ignored since its width is less than 100ns (specified in [42-43]). Obviously, it can be predicted that under all load oscillations with frequencies lower than 50 kHz the output voltage can be
Chapter 4 Dynamic Performance under Large-step Load Oscillation

sustained within the voltage tolerance range, since the output voltage has completely settled down before a new load transient occurs.

Fig. 4-4 The load transient response with 1kHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 250µs)

Fig. 4-5 The load transient response with 10kHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 50µs)
Fig. 4-6 The load transient response with 50kHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 10µs)

Fig. 4-7 The load transient response with 125kHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 5µs)

Fig.4-7 and Fig 4-8 show the load transient response with 125 kHz and 100 kHz load oscillations, respectively. At these load oscillation frequencies, the output voltage has not completely settled down; sometimes the voltage is near the peak of its ring-back and the inductor current also is near its highest level when a new unloading transient occurs, as shown in Fig. 4-7. Therefore, suppressing the voltage ring-back is critical to maintain the output voltage within the
tolerance range. Since the voltage ring-back is quite small (about 10mV) after loading transient, the output voltage can be maintained within the tolerance range at all times.

Fig. 4-8 The load transient response with 100kHz load oscillation  
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 5µs)

Fig.4-9 shows the load transient response with 250 kHz load oscillation frequency, which is equal to the switching frequency. Fig. 4-10 and Fig. 4-11 show the load transient response with 500 kHz and 1 MHz load oscillations, respectively. At such high load oscillation frequencies, the output voltage does not settle down and is still in transient when a new load transient occurs.

As shown in Fig. 4-12, the bulk capacitors and the high frequency filtering capacitors sustain the load current transient; the inductor current only contains the DC (average) component of the load and the operating ripple current. Therefore, characteristics of bulk capacitors and high frequency filtering capacitors, along with the interconnection parasitic inductance/resistance determine the path impedance and thus the output voltage. The amplitude of the voltage ripple becomes smaller with higher load oscillation frequency, which can be expected by the reduced path impedance at higher frequency as shown in Fig. 4-3.
Fig. 4-9 The load transient response with 250kHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 2.5µs)

Fig. 4-10 The load transient response with 500kHz load oscillation
(voltage scale: 25mV/div, current scale: 10A/div, time scale: 51µs)
Chapter 4 Dynamic Performance under Large-step Load Oscillation

Fig. 4-11 The load transient response with 1MHz load oscillation
(voltage scale: 25mV/div, current scale: 5A/div, time scale: 500ns)

Fig. 4-12 Current Distribution when load oscillation frequency is very high
(current scale: (top) 10A/div (bottom) 5A/div, time scale: 1µs)
4.3 Time Domain Validation by Experiments

Checking the voltage violations at some typical load-oscillation frequencies by means of
eperiment is another effective method to ensure that the output voltage does not violate the
tolerance range under large-step load oscillation. Load oscillation testings were performed on a
prototype of a two-phase interleaved synchronous buck converter with FPGA board. Fig. 4-13
shows a prototype board of a four-phase synchronous buck converter, in which two phases were
used as the two-phase interleaving synchronous buck converter. To reduce the interconnection
(layout) parasitic resistance/inductance, the prototype board has six layers, each with 2-ounce
copper. The copper layout area is balanced between core voltage and ground planes to minimize
power path resistance: three core voltage planes and three ground planes. Spacing between core
voltage/ground plane pairs is minimized to achieve the smallest possible inductance.

Fig. 4-13 A prototype board of a four-phase synchronous buck converter

Fig. 4-14 shows the load transient circuit, which was used to generate dynamic load current.
Two power resistors (50mΩ/1W each) in series with two MOSFETs (SD7236DP from Vishay)
are used as the load. A 9A gate driver (UCC37322 from Texas Instrument) is used to drive these
two power MOSFETs. The load oscillation frequency is set by FPGA. Fig.4-15 shows the load
current generated by the load transient circuit. The current step is measured to be about 28A; the loading transient slew rate is measured to be 350A/us and the unloading transient slew rate is measured to be 1.5A/ns.

The circuit parameters of the prototype power converter are listed in Table 2-3. The phase switching frequency is 250 KHz, the phase inductor is 360nH and the output capacitor is two
Chapter 4 Dynamic Performance under Large-step Load Oscillation

470μF capacitors (ESR: 5mΩ/2, ESL: 1.6nH/2). The desired output impedance is set at 2mΩ and the output voltage is set at 1V at no load. The output voltage tolerance range also is same as that of simulation. Load transient oscillations are applied at some typical frequencies to check the voltage violations: 31.25 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, and 1 MHz.

Fig.4-16 shows the output voltage and current reference waveforms with 31.25 kHz load oscillation. It can be found that the output voltage has settled down before a new load transient occurs. The output voltage is always maintained within the voltage tolerance range.

Fig. 4-16 The tested output voltage and current reference waveforms with 31.25 kHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 10µs/div)

Fig. 4-17 and Fig. 4-18 show the output voltage and current reference waveforms with 62.5 kHz and 125 kHz load oscillations, respectively. In Fig. 4-17, the output voltage is near the valley of its ring-back after the unloading transient when a new loading transient occurs; In Fig. 4-18, the output voltage is near the peak of its ring-back after the loading transient when a new unloading transient occurs. In both of these cases the voltage cannot completely settle down before a new load transient occurs, but the output voltage is still within the tolerance range.
Chapter 4 Dynamic Performance under Large-step Load Oscillation

Fig. 4-17 The tested output voltage and current reference waveforms with 62.5 kHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 10μs/div)

Fig. 4-18 The tested output voltage and current reference waveforms with 125 kHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 5μs/div)

Fig. 4-19, Fig.4-20, and Fig. 4-21 show the output voltage and current reference waveforms with 250 kHz, 500 kHz, and 1 MHz load oscillations, respectively. As expected in simulations, the amplitude of the voltage ripple will be reduced when the load oscillation frequency is pushed...
to a higher frequency, and the current reference ripple is reduced since the bulk capacitors and high frequency filtering capacitors supply the load transient current.

Fig. 4-19 The tested output voltage and current reference waveforms with 250 kHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 2µs/div)

Fig. 4-20 The tested output voltage and current reference waveforms with 500 kHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 1µs/div)
Fig. 4-21 The tested output voltage and current reference waveforms with 1 MHz load oscillation (voltage scale: 20mV/div, current scale: 20A/div, time scale: 500ns/div)

4.4 Summary

In this chapter, the power delivery path impedance with the proposed digital control is analyzed. The power path impedance over frequencies is given. When load oscillation frequency approaches or exceeds the VR control bandwidth, the power delivery path impedance will be dominated by the bulk capacitors, the filtering capacitors and interconnection resistance/inductance. To ensure that the output voltage does not violate the tolerance range under large-step load oscillation over frequencies from DC to $F_{break}$, the time domain validations are necessary. Time-domain validations in simulation and experiments prove the operations of the VR with proposed digital controller, without violating the voltage tolerance range under large-step load oscillation over a wide range of frequencies.
Chapter 5

Summary and Future Work

5.1 Summary of Contributions

In this thesis high performance digital control techniques with low system complexity architecture has been proposed. The main contributions of this thesis can be summarized as follows:

i. An AVP control unit has been generalized to realize AVP control, which generates the voltage reference and the current reference according to the desired output impedance. It is identified by the uniqueness of its dynamic voltage/current references. There are a number of options for constructing such an AVP control model, including decisions about where to perform the analog-to-digital conversion or the digital-to-analog conversion and whether to use peak or average current control.

ii. A digital controller with peak current mode control has been used to demonstrate the operation of the AVP control unit. Two digital-to-analog converters are used to generate the required voltage and current references. A straightforward control law is applied for the AVP control unit; no compensator is used in the feedback, and only simple addition computation and control logic are required. The current/voltage reference is updated at every DAC clock, which exhibits the fast transient response. The use of low-complexity DACs and a straightforward control law makes the proposed digital controller very suitable for high-volume low-cost low-dissipated-power integrations.

iii. A small signal model of a synchronous buck converter with the proposed digital controller has been derived. A stability check has been performed both in the discrete-
time domain and the continuous-time domain. Then, a switching stability constraint has
been derived, which gives the minimum output capacitor requirement for specific output
impedance.

iv. The relationship between the reference updating frequency and the transient response has
been investigated and constraints on the reference updating frequency to make the
controller fast enough have been given. A minimum output capacitor requirement then
has been derived for load transients, depending on whether these constraints are met or
not.

v. A dynamic reference step adjustment method has been proposed to break constraints on
the reference updating frequency, which improves the dynamic performance without
degrading steady-state performance at the same reference updating frequency.

vi. Non-linear control has been addressed to minimize the transient-assertion-to-action delay
and achieve maximum inductor current slew rate, which reduces the number of output
capacitors.

vii. Dual-voltage-loop control, which integrates dynamic reference step adjustment and non-
linear control, has been proposed. A dedicated transient detection circuit is also added to
detect the load transient; with this in place, the larger the load current transient step or the
faster the load current transient slew rate, the faster the output voltage drops or ascends,
and the earlier the transient state status is asserted. With dual-voltage-loop control, fast
transient response speed is achieved while the transition is smoothed.

viii. The power delivery path impedance with the proposed digital control has been analyzed.
The power path impedance over frequencies has been given. Time-domain validations in
simulation and experimentations have proven the operations of the VR with proposed
digital controller, without violating the voltage tolerance range under large-step load oscillation over the wide range of frequency.

5.2 Future work

This thesis has developed a new digital control architecture with low-complexity and high performance, thus making it a valuable candidate as a high-volume, low-cost controller for processor voltage regulators. Further research work is necessary to further improve performance.

1) **Breaking switching stability constraint**: minimum output capacitance are needed to make the converter stable, which depends on the switching frequency and specified output impedance. The output capacitance cannot be further reduced when the transient response becomes extremely fast. A control law with a compensator which can break the switching stability constraint should be further explored. If the control law meets equation (2.5), AVP control can also be realized.

2) **Non-AVP control**: the AVP control unit is addressed especially to realize AVP operation. But, in some applications, non-AVP control may be required. If the output impedance $R_o$ is set to be zero in equation (2.5) and necessary theory for designing compensators should be developed.

3) **Investigating performance of other possible configurations**: the AVP control unit can be constructed in a number of ways, using either peak or average current mode control, or using the analog-to-digital conversion or the digital-to-analog conversion. Section 2.2.2 presents four possible configurations, one of which is investigated in this thesis. Performances of other configurations should be further explored.
5.3 Conclusion

In this thesis new digital control techniques are proposed for powering the microprocessors. The proposed digital controller which has a reduced-complexity structure realizes the adaptive voltage positioning control by generating dynamic voltage and current references. Advanced control algorithms have been presented to improve dynamic performance to achieve very fast transient response. Analytical, simulation and experimental results have been presented to prove the proposed digital control techniques.

Compared to the traditional active-droop analog controller presented in [85], the number of output bulk capacitors can be reduced from 3 to 1 with the proposed digital controller. The traditional active-droop analog controller is required to operate at 500 KHz switching frequency and 200nH phase inductance, in order to achieve the similar transient performance as the proposed digital controller operates at 250 KHz and 400nH phase inductance. Lower switching frequency results in higher efficiency.
Bibliography


[10]. Ed Stanford, “Power technology roadmap for microprocessor voltage regulators,”
Presentation at PSMA, Feb. 2003, available at www.apec-conf.org/2004/APEC04_SP1-
1_Intel.pdf


[12]. Alon Naveh, Efrain Rotem, Avi Mendelson, etc., “Power and thermal management in the

[13]. Suresh Subramanyam, Taninder Sijher, Sidharth Krishnama, etc., “Intel 945GMS Express
Chipset for small form factor platform based on Intel Centrino Duo Mobile technology”, Intel

DC/DC modules for next generations of data processing circuits,” in IEEE Transaction on

efficiency and fast transient voltage regulator module ---- push-pull forward converter,” IEEE

“Investigation of candidate VRM topologies for future microprocessors” , IEEE Applied

[17]. Pit-Leong Wong, P. Xu, P. Yang, and F. C. Lee, “Performance improvements of interleaving


[67]. Yuancheng Ren, Kaiwei Yao, Ming Xu, and Fred C. Lee, “Analysis of the Power Delivery Path From the 12-V VR to the Microprocessor”, IEEE Transaction on power electronics, Vol. 19, No. 6, Nov. 2004


[83]. Xin Zhang, Gary Yao, and Alex Q. Huang, “A novel VRM control with direct load current


[94]. “Power Supplies Goes Digital”, white paper, available at

[95]. Stefano Saggini, Massimo Ghioni, and Angelo Geraci, “An Innovative Digital Control
   Architecture for Low-Voltage, High-Current DC–DC Converters With Tight Voltage
   218.
Appendix A

Design Procedure

A two-phase interleaved buck converter for 12V-1V/40A VRM is normally dedicated to notebook CPUs. Design requirements are listed in Table A-1.

### Table A-5-1 Design requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of phases ($N$)</td>
<td>2</td>
</tr>
<tr>
<td>Input voltage ($V_{in}$)</td>
<td>12 V ±10%</td>
</tr>
<tr>
<td>Output voltage ($V_o$)</td>
<td>1V</td>
</tr>
<tr>
<td>Maximum load current ($I_{omax}$)</td>
<td>40A, 20A/phase</td>
</tr>
<tr>
<td>Maximum load transient ($\Delta I_{omax}$)</td>
<td>27A (13A ↔ 40A)</td>
</tr>
<tr>
<td>Phase switching frequency ($f_{sw}$)</td>
<td>250KHz</td>
</tr>
<tr>
<td>Maximum allowed output voltage ripple ($\Delta V_{o,r}$)</td>
<td>10mV</td>
</tr>
<tr>
<td>Maximum peak-to-peak inductor current ripple ($\Delta I_{L,\Phi}$)</td>
<td>50% phase current (10A)</td>
</tr>
<tr>
<td>Desired output impedance ($R_o$)</td>
<td>2mΩ</td>
</tr>
<tr>
<td>Maximum allowed overshoot voltage ($\Delta V_{os}$)</td>
<td>50mV</td>
</tr>
</tbody>
</table>

The design procedure of the multiphase VRM with the proposed digital controller is described as follows:

1) Determine the phase inductor by Equation (2.25).

$$L_f = \frac{V_o(1-D)}{f_{sw} \cdot \Delta I_{L,\Phi}} = 367nH$$  \hspace{1cm} (A. 1)

Choose 400nH for the phase inductor. By (2.25) and (2.26), recalculating the peak-to-peak phase inductor current ripple and the total inductor current ripple as:
2) Determine the minimum output capacitor:

By switching stability constraint (2.60), \( \alpha = 1/6 \):

\[
\frac{1}{2\pi \cdot R_o \cdot C} < \alpha \cdot N \cdot f_{sw} \quad \Leftrightarrow \quad C \geq 960 \mu F
\]

By loading transient constraint (3.10):

\[
t_o = \frac{(2 - D)}{2 f_{sw}} + t_{dc} = 955 n + 150 ns = 1105 ns
\]

\[
L_f < \frac{ESR \cdot C \cdot (V_{in} - V_o)}{\Delta I_o} = L_{crit} = 806 nH
\]

\[
\frac{\Delta I_{o_{\max}} \cdot t_D}{C} + ESR \cdot \Delta I_{o_{\max}} \leq \Delta I_{o_{\max}} \cdot R_o
\]

\[
\Leftrightarrow \quad C \geq 1.5 mF
\]

Assumed: bulk capacitors (330\( \mu \)F, 6m\( \Omega \) ESR) with 1.98\( ns \) time constant \((ESR \cdot C)\) are used and 150\( ns \) is estimated for the circuit delay.

By unloading transient \((40 A \rightarrow 13 A)\) constraint (3.11):

\[
t_o = \frac{(1 + D)}{2 f_{sw}} + t_{dc} = 650 ns + 150 ns = 800 ns
\]

\[
L_f > \frac{ESR \cdot C \cdot V_o}{\Delta I_o} = L_{crit} = 73 nH
\]

\[
\frac{\Delta I_{o_{\max}} \cdot t_D}{C} + \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I_o^2 \cdot L_f^2}{2L_f \cdot C \cdot (-V_o)} \geq \Delta I_{o_{\max}} \cdot R_o - \Delta V_o - I_{o_{\min}} \cdot R_o
\]
Choose 1.6mF for the output capacitor: three 330µF bulk capacitors (ESR=6mΩ/3) + 32 x 22µF ceramic capacitor

3) Voltage reference step and current reference step

7 bit digital-to-analog converter is used for both the voltage and current reference generators. By (2.11):

\[ \Delta I_{\text{ref}} = M \frac{I_{\text{ref max}}}{2^n} = \frac{I_{\text{o max}, \Phi} + \Delta I_{\text{ref}}/2}{2^n} = \frac{20 + 7}{128} = 0.21A \]

\[ \Delta V_{\text{ref}} = R_o \cdot (N \cdot \Delta I_{\text{ref}}) = 0.84mV \]

4) Controller Design

**Control Scheme I (original control scheme):**

Recall condition (3.13):

\[ f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{V_o}{L_f} \quad \Rightarrow \quad f_{\text{clk}} > 12 MHz \]

But condition (3.12) cannot be met. Therefore, constraint (3.21) should be used to determine the capacitor during loading transient. If want to keep the same amount of the output capacitors, the following condition should be satisfied, from (3.21):

\[ f_{\text{clk}} \cdot \Delta I_{\text{ref}} > \frac{\Delta I_o}{ESR \cdot C} \quad \Rightarrow \quad f_{\text{clk}} > 32 MHz \]

Therefore, choose 32 MHz for the operating clock for the target FPGA and DACs.

Voltage reference adjustment step in the steady state and in the transient state are the same:

\[ \Delta V_{\text{ref}} = 0.84mV \]
Current reference adjustment step in the steady state and in the transient state are also same:

\[ \Delta I_{ref} = 0.21A \]

If we want to decrease the operating frequency, the resolution (bit) of DACs must also decrease. If 8 MHz clock is used, the voltage and current reference adjustment step (or 5-bit DACs used) should be increased to four times those in the 32 MHz application, to keep same transient-up performance, see (3.12) (3.13). Now, the voltage and current reference adjustment step will be \( \Delta V_{ref} = 3.36mV \) and \( \Delta I_{ref} = 0.84A \).

**Control Scheme II (Dynamic reference step adjustment):**

Since conditions (3.12) and (3.122) are broken in the steady-state stage, we can choose the operating clock more freely, such as 8MHz. Therefore, the limitation value for counters (for transient judgment) can be determined by (3.26), (3.27):

\[
LMT_{TU} \geq \min \left\{ \text{int} \left( \frac{f_{clk}}{2f_{sw}} \right), \quad \text{int} \left( \frac{\Delta V_{o,r}}{\Delta V_{ref}} \right) \right\} + 1 = 8
\]

\[
LMT_{TD} \geq \min \left\{ \text{int} \left( \frac{f_{clk}}{2f_{sw}} \right), \quad \text{int} \left( \frac{\Delta V_{o,r}}{\Delta V_{ref}} \right) \right\} + 1 = 8
\]

Choose 9 for \( LMT_{TU} \) and \( LMT_{TD} \).

\( M \) for the loading transient-state-stage can be determined by (3.28) (3.29):

Load transient-up:

\[
M \geq \int \left( \frac{V_{in} - V_o}{\Delta I_{ref} \cdot I_f \cdot f_{clk}} \right) = 16
\]

Load transient-down:
\[
M \geq \text{int} \left[ \frac{V_o}{\Delta I_{\text{ref}} \cdot L_f \cdot f_{\text{clk}}} \right] = 2
\]

So during load transient-up, choose \(M=N=16\), the reference adjustment step is

\[
M \cdot \Delta I_{\text{ref}} = 16 \times 0.21A = 3.36A
\]

\[
N \cdot \Delta V_{\text{ref}} = 16 \times 0.84mV = 13.44mV
\]

During load transient-down, choose \(M=N=2\), the reference adjustment step is

\[
M \cdot \Delta I_{\text{ref}} = 2 \times 0.21A = 0.42A
\]

\[
N \cdot \Delta V_{\text{ref}} = 2 \times 0.84mV = 1.68mV
\]

**Control Scheme III (non-linear control):**

Choose 16MHz for the operating clock. The limitation value for counters (for transient judgment) is same.

\[
LMT_{\text{TU}} = 9
\]

\[
LMT_{\text{TD}} = 9
\]

The reference adjustment step during the transient state can be

Load transient-up:

\[
M \leq \frac{\Delta I_{o_{\text{max}}} \cdot t_d + ESR \cdot \Delta I_{o_{\text{max}}} - \Delta V_{\text{ref}} \cdot LMT_{\text{TU}}}{\Delta V_{\text{ref}} \cdot \text{int}[(t_{dc} + T_m) \cdot f_{\text{clk}}]} = 14.2
\]

Choose \(M=N=14\), so,

\[
M \cdot \Delta I_{\text{ref}} = 14 \times 0.21A = 2.94A
\]

\[
N \cdot \Delta V_{\text{ref}} = 14 \times 0.84mV = 11.4mV
\]
Load transient-down:

\[
M \leq \frac{\Delta I_{o_{\text{max}}} \cdot t_D}{C} + \frac{ESR \cdot C \cdot V_o^2 + \Delta I_{o_{\text{max}}}^2 \cdot L_f}{2L_f \cdot C \cdot V_o} - \frac{\Delta V_{\text{ref}} \cdot LMT_{\text{TD}}}{\Delta V_{\text{ref}} \cdot \text{int}\left(\left(\frac{t_d}{t_m} + \frac{T_m}{f_{\text{clk}}}\right)\right)} = 1.9
\]

Choose \(M=N=2\), which are closer to 1.9. Therefore, the reference adjustment step during unloading transient is:

\[
M \cdot \Delta I_{\text{ref}} = 2 \times 0.21A = 0.42A
\]
\[
N \cdot \Delta V_{\text{ref}} = 2 \times 0.84mV = 1.68mV
\]

**Control Scheme IV (dual-voltage-loop control):**

Since the largest delay in the worst case is much smaller than others, the output capacitor should be re-determined as follows:

By loading transient constraint (3.10):

\[
t_D = t_{dc} = 150\text{ ns}
\]
\[
L_f < \frac{ESR \cdot C \cdot (V_{\text{in}} - V_o)}{\Delta I_o} = L_{\text{crit}} = 806\text{ nH}
\]
\[
\frac{\Delta I_{o_{\text{max}}} \cdot t_D}{C} + ESR \cdot \Delta I_{o_{\text{max}}} \leq \Delta I_{o_{\text{max}}} \cdot R_o
\]
\[
\Rightarrow \quad C \geq 1\text{ mF}
\]

Supposed: bulk capacitors (330\text{ uF}, 6m\Omega \text{ ESR}) with 1.98\text{ us} time constant \((ESR \cdot C)\) are used and 150\text{ ns} is estimated for the circuit delay.

By unloading transient \((40A \rightarrow 13A)\) constraint (3.11):

\[
t_D = t_{dc} = 150\text{ ns}
\]
Appendix A Design Procedure

\[ L_f > \frac{ESR \cdot C \cdot V_o}{\Delta I_o} = L_{crit} = 73nH \]

\[ \frac{\Delta I_{o-max} \cdot t_D}{C} + \frac{ESR^2 \cdot C^2 \cdot V_o^2 + \Delta I_o^2 \cdot L_f^2}{2L_f \cdot C \cdot (-V_o)} \geq \Delta I_{o-max} \cdot R_o - \Delta V_{os} - I_{o-min} \cdot R_o \]

\[ \Rightarrow C \geq 620\mu F \]

Choose 1.0mF for the output capacitor: one 330uF bulk capacitors (ESR=6mΩ) + 32 x 22uF ceramic capacitor

Choose 16MHz for the operating clock. The voltage gaps (\(V_{bd}\) and \(V_{bu}\)) are chosen to be 30mV.

The reference adjustment step during the transient mode and the link mode can be

**Transient-up Mode:**

\[
M_t \geq \frac{\Delta I_{o-max} \cdot (t_D + \frac{2}{f_{ck}}) + ESR \cdot \Delta I_{o-max} \cdot V_{bd} - (ESR + \frac{1}{C \cdot f_{ck}}) \cdot \frac{2 \cdot (V_o - V_{in})}{L_f \cdot f_{ck}} \cdot \text{in}[t_{dc} \cdot f_{ck}] \cdot \Delta V_{ref} \cdot 2 \cdot \Delta V_{ref}}{4.7}
\]

Choose \(M_t=N_t=5\), so,

\[ M_t \cdot \Delta I_{ref} = 5 \times 0.21A = 1.05A \]

\[ N_t \cdot \Delta V_{ref} = 5 \times 0.84mV = 4.2mV \]

**Link-up Mode:**

\[
M_L \geq \frac{ESR \cdot C \cdot (V_{in} - V_o) - \Delta I_{o-max} \cdot L_f}{\Delta V_{ref} \cdot f_{ck} \cdot L_f \cdot C} = 1.8
\]

Choose \(M_L=N_L=2\), so,

\[ M_L \cdot \Delta I_{ref} = 2 \times 0.21A = 0.42A \]

\[ N_L \cdot \Delta V_{ref} = 2 \times 0.84mV = 1.68mV \]
Choose $M=N=1$. Therefore, the reference adjustment step during unloading transient is:

$$M_t \cdot \Delta I_{ref} = 1 \times 0.21A = 0.21A$$

$$N_t \cdot \Delta V_{ref} = 1 \times 0.84mV = 0.84mV$$

Link-down Mode:

From the constraint (55), we can get

$$
\begin{align*}
M_L \geq \text{int} \left[ \frac{V_o}{\Delta I_{ref} \cdot L_f \cdot f_{clk}} \right] \\
M_L \geq \text{int} \left[ \frac{\Delta I_{max}}{\Delta I_{ref}} - t \cdot f_{clk} \cdot M_t \right] \\
t \cdot f_{clk} \cdot M_t \cdot \Delta V_{ref} + V_{bu} > \frac{\Delta I_{max} \cdot t_{de}}{C} + \frac{\Delta I_o \cdot t_{de} \cdot L_f}{C} + \frac{\Delta I_o \cdot t}{2L_f \cdot C} - \frac{V_{I_v}}{L_f} \cdot t^2 \\
t \cdot f_{clk} \in (1, 2, 3, \ldots) \\
t \geq T_m
\end{align*}
$$

$\Rightarrow M_L \geq 6$

Choose $M_L=N_L=6$, so,

$$M_L \cdot \Delta I_{ref} = 6 \times 0.21A = 1.26A$$

$$N_L \cdot \Delta V_{ref} = 6 \times 0.84mV = 5.04mV$$
Table A-2 summarizes the parameters calculated above for four control schemes.

<table>
<thead>
<tr>
<th></th>
<th>Control Scheme I</th>
<th>Control Scheme II</th>
<th>Control Scheme III</th>
<th>Control Scheme IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Clock $f_{clk}$</td>
<td>32MHz</td>
<td>8MHz</td>
<td>8MHz</td>
<td>16MHz</td>
</tr>
<tr>
<td>Resolution of Current DAC</td>
<td>7 bits</td>
<td>5 bits</td>
<td>7 bits</td>
<td>7 bits</td>
</tr>
<tr>
<td>Resolution of Voltage DAC</td>
<td>7 bits</td>
<td>5 bits</td>
<td>7 bits</td>
<td>7 bits</td>
</tr>
<tr>
<td>Voltage Reference Step $\Delta V_{ref}$ in the steady state</td>
<td>0.84mV ($N=1$)</td>
<td>3.36mV ($N=1$)</td>
<td>0.84mV ($N=1$)</td>
<td>0.84mV ($N=1$)</td>
</tr>
<tr>
<td>Current Reference Step $\Delta I_{ref}$ in the steady state</td>
<td>0.21A ($M=1$)</td>
<td>0.84A ($M=1$)</td>
<td>0.21A ($M=1$)</td>
<td>0.21A ($M=1$)</td>
</tr>
<tr>
<td>Voltage Reference Step $N\Delta V_{ref}$ in the transient/Link-up state</td>
<td>$N_t=1$</td>
<td>$N_t=1$</td>
<td>$N_t=16$</td>
<td>$N_t=14$</td>
</tr>
<tr>
<td>Current Reference Step $M\Delta I_{ref}$ in the transient/Link-up state</td>
<td>$M_t=1$</td>
<td>$M_t=1$</td>
<td>$M_t=16$</td>
<td>$M_t=14$</td>
</tr>
<tr>
<td>Voltage Reference Step $N\Delta V_{ref}$ in the transient/Link-down state</td>
<td>$N_t=1$</td>
<td>$N_t=1$</td>
<td>$N_t=2$</td>
<td>$N_t=2$</td>
</tr>
<tr>
<td>Current Reference Step $M\Delta I_{ref}$ in the transient/Link-down state</td>
<td>$M_t=1$</td>
<td>$M_t=1$</td>
<td>$M_t=2$</td>
<td>$M_t=2$</td>
</tr>
</tbody>
</table>
Fig. B-5-1 Schematic of power stage used in simulation
Fig. B-5-2 Schematic of power delivery path used in simulation
Appendix C Transient Performance Comparison

To demonstrate transient performance improvement of the proposed digital controller, a traditional analog controller with active droop control presented in [85] is designed for a two-phase VR. Fig. C-1 shows the power circuit of the interleaved synchronous buck converter with active-droop analog controller. The circuit parameters of the two-phase interleaved synchronous buck converter for 12V-1V/40A VR are same as those used in simulations with the proposed digital controller, listed in the Table 2-1. The phase switching frequency is 250 KHz, the phase inductor is 400nH and the output capacitors are three 470uF POSCAP capacitors in parallel (ESR: 5mΩ/3, ESL: 1.6nH/3). The desired output impedance is set at 2mΩ.

Fig. 5-3 the interleaved synchronous buck converter with active-droop analog controller
Appendix C Transient Performance Comparison

Fig. C-1 shows the transient response with the active-droop analog controller. It is found that at least three bulk capacitors (470uF) are needed to sustain the output voltage within the voltage tolerance. As comparison, only one bulk capacitor is needed when the proposed digital controller with dual loop control is used. Table C-1 illustrates the minimum output bulk capacitor requirement comparison between the proposed digital controller and active droop analog controller.

![Analog Controller with Active Droop Control proposed in [65]](image)

![Load current transient step: 13A → 40A @2A/ns 40A→ 13A @2A/ns.](image)

**Fig. 5-4 the transient response with the active-droop analog controller**

(voltage scale: 25mV/div, current scale: 5A/div, time scale: 50µs)

**Table 5-3 Minimum output bulk capacitor requirement comparison**

<table>
<thead>
<tr>
<th></th>
<th>Phase Switching Frequency</th>
<th>Phase Inductance</th>
<th>Minimum number of bulk Capacitors (470uF, 6mΩ)</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed digital controller</td>
<td>250KHz</td>
<td>400nH</td>
<td>1</td>
<td>66%</td>
</tr>
<tr>
<td>Active-droop analog controller</td>
<td>250KHz</td>
<td>400nH</td>
<td>3</td>
<td>0%</td>
</tr>
</tbody>
</table>
When one output bulk capacitor is applied with the active droop analog controller, the switching frequency is required to increase from 250 KHz to 500 KHz and the phase inductance is required to reduce from 400nH to 200nH. Fig. C-3 shows the transient response with the active-droop analog controller at 500 KHz switching frequency and 200nH phase inductance. Table C-2 gives the switching frequency requirement comparison between the proposed digital controller and active droop analog controller.

Fig. 5-5 the transient response with the active-droop analog controller at 500 KHz switching frequency and 200nH inductance
(voltage scale: 20mV/div, current scale: 5A/div, time scale: 20µs)

Table 5-4 Switching frequency requirement comparison

<table>
<thead>
<tr>
<th></th>
<th>Phase Switching Frequency</th>
<th>Phase Inductance</th>
<th>Minimum number of bulk Capacitors (470uF, 6mΩ)</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed digital controller</td>
<td>250KHz</td>
<td>400nH</td>
<td>1</td>
<td>50%</td>
</tr>
<tr>
<td>Active-droop analog controller</td>
<td>500KHz</td>
<td>200nH</td>
<td>1</td>
<td>0%</td>
</tr>
</tbody>
</table>
Appendix D VHDL Codes

VHDL codes for the digital controller with dual-voltage-loop control:

```vhdl
library ieee;
use ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

package mypackPCMMP is
  Constant CounterWidth: integer:=7;
  Constant CounterUpLimit: integer:=127;  --- equal to (2^CounterWidth)-1
  Constant VolCounterWidth: integer:=7;
  Constant DACWidth: integer:=14;
  Subtype CounterType is std_logic_vector(CounterWidth-1 downto 0);
  Subtype VolCounterType is std_logic_vector(VolCounterWidth downto 0);
  Subtype CurCounterType is std_logic_vector(VolCounterWidth downto 0);
  Subtype DACType is std_logic_vector(DACWidth-1 downto 0);

  Constant InitialTurnOnGT1: CounterType:=B"0000000";
  Constant InitialTurnOnGT2: CounterType:=B"1000000";
  Constant InitialTurnOffGT1: CounterType:=B"0001100";
  Constant InitialTurnOffGT2: CounterType:=B"1001100";

  Constant InitialVolMid: VolCounterType:=B"11010000";--B"10110000";
  Constant MaxVolMid: VolCounterType:=B"11010000";--B"10110000";
  Constant MinVolMid: VolCounterType:=B"01000100";--B"00010100";
  Constant MaxPeakCur: CurCounterType:=B"11000000";--B"11000000";
  Constant MinPeakCur: CurCounterType:=B"00110100";--B"00100100";
  Constant InitialPeakCur: CurCounterType:=B"00110100";--B"00100100";

  Constant AdjustStepSteady: CurCounterType:=B"00000001";
  Constant AdjustStepTransUp: CurCounterType:=B"00000110";
  Constant AdjustStepUpLink: CurCounterType:=B"00000010";
  Constant AdjustStepTransDown: CurCounterType:=B"00000001";
  Constant AdjustStepDownLink: CurCounterType:=B"00000110";

  Constant LMT_TU: CurCounterType:=B"00011000";
  Constant LMT_TD: CurCounterType:=B"00001010";
  Constant LMT_TL: CurCounterType:=B"00011001";
end;

package body mypackPCMMP is

end mypackPCMMP;
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE work.mypackPCMMP.all;
ENTITY MPPCMControl IS PORT ( 
  CLK:IN std_logic;
  WRT: IN std_logic;
  resetn: IN std_logic;
  CompV : IN std_logic;
  CompVqu : IN std_logic;
  CompVqd : IN std_logic;
  CompVq : IN std_logic;
  CompI1: IN std_logic;
  CompI2: IN std_logic;
  CompI3: IN std_logic;
  CompI4: IN std_logic;
  PWM1: OUT std_logic:='0';
  PWM2: OUT std_logic:='0';
  PWM3: OUT std_logic:='0';
  PWM4: OUT std_logic:='0';
  EN: OUT std_logic:='0';
  DACV: OUT DACType;
  DACi: OUT DACType;
  TestLed: OUT std_logic;
  DataCatched: OUT CurCounterType;
  OverFlowUpLed: OUT std_logic;
  OverFlowDownLed: OUT std_logic;
  TUCatched: OUT CurCounterType;
  TDCatched: OUT CurCounterType;
  StartReleaseLed: OUT std_logic 
);
END MPPCMControl;

ARCHITECTURE Structure OF MPPCMControl IS
Component ClockManagement
  Port ( resetn: in std_logic;
    CLK:IN std_logic;
    CLK_CTRL:OUT std_logic;
    SystemCount: OUT CounterType
  );
end Component;

Component DPWM
  Port (resetn: IN std_logic;
    CLK: IN std_logic;
Appendix D VHDL Codes

SystemCount: IN CounterType;
CompI1: IN std_logic;
CompI2: IN std_logic;
CompI3: IN std_logic;
CompI4: IN std_logic;
IsTransientUp: IN std_logic;
IsTransientDown: IN std_logic;
SoftStart: IN std_logic;
StartRelease: IN std_logic;
SWCLK: OUT std_logic;
PWM1: OUT std_logic;
PWM2: OUT std_logic;
PWM3: OUT std_logic;
PWM4: OUT std_logic;
EN: OUT std_logic
)

End Component;

Component TransientDetection
Port {
    resetn: IN std_logic;
    clk: IN std_logic;
    CompVqu : IN std_logic;
    CompVqd: IN std_logic;
    IsLinkMode: IN std_logic;
    SoftStart: IN std_logic;
    IstransientUp: Out std_logic;
    IstransientDown: Out std_logic;
    IsLinkUp:Out std_logic;
    IsLinkDown:Out std_logic
}
end Component;

Component ControlUnit
PORT {
    resetn: IN std_logic;
    WRT: IN std_logic;
    CLK_CTRL: IN std_logic;
    CompV: IN std_logic;
    CompVq : IN std_logic;
    SWCLK: IN std_logic;
    IsTransientUp: IN std_logic;
    IsTransientDown: IN std_logic;
    IsLinkUp: IN std_logic;
    IsLinkDown: IN std_logic;
    IsLinkMode: OUT std_logic;
    SoftStart: OUT std_logic;
    StartRelease: OUT std_logic;
    DACV13: OUT std_logic;
    DACV12: OUT std_logic;
    DACV11: OUT std_logic;
    DACV10: OUT std_logic;
}
DACV9: OUT std_logic;
DACV8: OUT std_logic;
DACV7: OUT std_logic;
DACV6: OUT std_logic;
DACV5: OUT std_logic;
DACV4: OUT std_logic;
DACV3: OUT std_logic;
DACV2: OUT std_logic;
DACV1: OUT std_logic;
DACV0: OUT std_logic;
DACI13: OUT std_logic;
DACI12: OUT std_logic;
DACI11: OUT std_logic;
DACI10: OUT std_logic;
DACI9: OUT std_logic;
DACI8: OUT std_logic;
DACI7: OUT std_logic;
DACI6: OUT std_logic;
DACI5: OUT std_logic;
DACI4: OUT std_logic;
DACI3: OUT std_logic;
DACI2: OUT std_logic;
DACI1: OUT std_logic;
DACI0: OUT std_logic;
TestLed: OUT std_logic;
DataCatched: OUT CurCounterType;
OverFlowUpLed: OUT std_logic;
OverFlowDownLed: OUT std_logic;
TUCatched: OUT CurCounterType;
TDCatched: OUT CurCounterType;
StartReleaseLed: OUT std_logic};
END Component;

Signal SGNSystemCount: CounterType;
Signal CLK_CTRL,SWCLK,SGNStartRelease: std_logic;
Signal SoftStart,IsTransientUp,IsTransientDown: std_logic;
signal SGNIsLinkUp: std_logic;
signal SGNIsLinkDown: std_logic;
signal SGNIsLinkMode: std_logic;
BEGIN

U0: ClockManagement
Port map (resetn,CLK,CLK_CTRL,SGNSystemCount);

U1: DPWM
Port map (resetn,CLK,SGNSystemCount,Compl1,Compl2,Compl3,Compl4,IsTransientUp,
IsTransientDown,SoftStart,SGNStartRelease,SWCLK,PWM1,PWM2,PWM3, PWM4,EN);
U2: TransientDetection
   Port map (resetn, clk, CompVqu, CompVqd, SGNIsLinkMode, SoftStart, IstransientUp,
   IstransientDown, SGNIsLinkUp, SGNIsLinkDown);

U3: ControlUnit
   Port map (resetn, WRT, CLK, CompV, CompVq, SWCLK, IsTransientUp, IsTransientDown,
   SGNIsLinkUp, SGNIsLinkDown, SGNIsLinkMode, SoftStart, SGNStartRelease,
   DACV(13), DACV(12), DACV(11), DACV(10), DACV(9), DACV(8), DACV(7),
   DACV(6), DACV(5), DACV(4), DACV(3), DACV(2), DACV(1), DACV(0),
   DACI(13), DACI(12), DACI(11), DACI(10), DACI(9), DACI(8), DACI(7),
   DACI(6), DACI(5), DACI(4), DACI(3), DACI(2), DACI(1), DACI(0), TestLed,
   DataCatched, OverFlowUpLed, OverFlowDownLed, TUCatched, TDCatched,
   StartReleaseLed);

END Structure;

--- Clock Management for the Chip -------

library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE work.mypackPCMMP.all;
ENTITY ClockManagement IS PORT (resetn:IN std_logic;
   CLK: IN std_logic;
   CLK_CTRL:OUT std_logic;
   SystemCount: OUT CounterType
);
END ClockManagement;

ARCHITECTURE behavioral OF ClockManagement IS

BEGIN
   PROCESS (clk,resetn)
   variable count: CounterType;
   BEGIN
      if resetn='0'then
         count:=(others=>'0');
         SystemCount:=(others=>'0');
         CLK_CTRL<='0';
      else
         if rising_edge(clk) then
            if count<CounterUpLimit then
               count:=count+1;
            else
               count:=count;
               SystemCount:=SystemCount+1;
               CLK_CTRL<='1';
               SystemCount<=SystemCount;
            end if;
         else
            count:=count;
            SystemCount:=SystemCount;
         end if;
      end if;
   end PROCESS;
END;

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Appendix D VHDL Codes

--- Digital PWM Generator ---

Library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
use IEEE.std_logic_arith.all;
USE work.mypackPCMMMP.all;

ENTITY DPWM IS PORT (resetn: IN std_logic;
CLK: IN std_logic;
SystemCount: IN CounterType;
CompI1: IN std_logic;
CompI2: IN std_logic;
CompI3: IN std_logic;
CompI4: IN std_logic;
IsTransientUp: IN std_logic;
isTransientDown: IN std_logic;
SoftStart: IN std_logic;
StartRelease: IN std_logic;
SWCLK: OUT std_logic;
PWM1: OUT std_logic:= '0';
PWM2: OUT std_logic:= '0';
PWM3: OUT std_logic:= '0';
PWM4: OUT std_logic:= '0';
EN: OUT std_logic)
);
END DPWM;

ARCHITECTURE behavioral OF DPWM IS
Signal SGNPWM3,SGNPWM4: std_logic;
BEGIN
Process (clk,resetn,CompI3,CompI4,IsTransientUp,IsTransientDown)

begin

END PROCESS;
END behavioral;

count:=(others=>'0');
end if;
CLK_CTRL<=count(0);
SystemCount<=count;
end if;
end if;
END PROCESS;
END behavioral;

--- Digital PWM Generator ---
if resetn='0' then
VarPWM1:='0';
VarPWM2:='0';
EN<='0';
PWM1<='0';
PWM2<='0';
PWM3<='0';
PWM4<='0';
SWCLK<='0';
SGNPWM3<='0';
SGNPWM4<='0';
else
if rising_edge(clk) then
VarAction1:='0';
VarAction2:='0';
if InitialTurnOnGT1=systemCount then
VarPWM1:='1';
VarAction1:='1';
end if;
if InitialTurnOnGT2=systemCount then
VarPWM2:='1';
VarAction2:='1';
end if;
if softstart='1' then
  if InitialTurnOffGT1=systemCount then
    VarPWM1:='0';
    VarAction1:='1';
  end if;
  if InitialTurnOffGT2=systemCount then
    VarPWM2:='0';
    VarAction2:='1';
  end if;
end if;
end if;
if VarAction1='1' then
  PWM3<=VarPWM1;
  SWCLK<=not VarPWM1;--'0';
  SGNPWM3<=VarPWM1;
end if;
if VarAction2='1' then
  PWM4<=VarPWM2;
  SGNPWM4<=VarPWM2;
end if;
if IsTransientUp='1' then
  PWM3<='1';
  PWM4<='1';
else

if CompI3='1' then
  PWM3<='0';
  SGNPWM3<='0';
  SWCLK<='1';
end if;
if CompI4='1' then
  PWM4<='0';
  SGNPWM4<='0';
end if;
end if;

if Istransientdown='1' then
  PWM3<='0';
  PWM4<='0';
  SGNPWM3<='0';
  SGNPWM4<='0';
end if;
PWM1<=IsTransientUp;
PWM2<=IsTransientDown;
end if;
end process;
END behavioral;

----------------------------------
-- Transient Detection
----------------------------------
library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE work.mypackPCMMP.all;
ENTITY TransientDetection IS PORT(
  resetn: IN std_logic;
  clk: IN std_logic;
  CompVqu: IN std_logic;
  CompVqd: IN std_logic;
  IsLinkMode: IN std_logic;
  SoftStart: IN std_logic;
  IsTransientUp: Out std_logic;
  IsTransientDown: Out std_logic;
  IsLinkUp: Out std_logic;
  IsLinkDown: Out std_logic
);
END TransientDetection;

ARCHITECTURE behavioral OF TransientDetection IS
BEGIN
PROCESS(clk,resetn,IsLinkMode,CompVqu,CompVqd)
Variable VarIstransientUp,VarIstransientDown:std_logic;
Variable LastTransientDown,LastTransientUp,VarLinkUp,VarLinkDown:Std_logic;
BEGIN
if resetn='0'then
IsTransientUp<='0';
IsTransientDown<='0';
IsLinkUp<='0';
IsLinkDown<='0';
VarLinkUp:='0';
VarLinkDown:='0';
VarIstransientUp:='0';
VarIstransientDown:='0';
else
if rising_edge(clk) then
if SoftStart='1' then
VarIstransientDown:='0';
VarIsTransientup:='0';
else
if CompVqu='1' then
VarIstransientDown:=VarIsTransientDown;
VarIsTransientDown:=VarIsTransientDown;
end if;
if LastTransientDown='1' then
VarLinkDown:='1';
end if;
end if;
if CompVqd='1' then
VarIsTransientup:='1';
else
LastTransientUp:=VarIsTransientUp;
VarIsTransientUp:=VarIsTransientUp;
end if;
if LastTransientUp='1' then
VarLinkUp:='1';
end if;
end if;
if CompVq==='1'
VarIsTransientUp:=VarIsTransientUp;
else
LastTransientUp:=VarIsTransientUp;
VarIsTransientUp:=VarIsTransientUp;
end if;
if LastTransientUp='1' then
VarLinkUp:='1';
end if;
end if;
IsTransientUp<=VarIsTransientup;
IsTransientDown<=VarIsTransientdown;
IsLinkUp<=VarLinkup;
IsLinkDown<=VarLinkDown;
end}

Appendix D VHDL Codes

BEGIN
PROCESS(clk,resetn,IsLinkMode,CompVqu,CompVqd)
Variable VarIstransientUp,VarIstransientDown:std_logic;
Variable LastTransientDown,LastTransientUp,VarLinkUp,VarLinkDown:Std_logic;
BEGIN
if resetn='0'then
IsTransientUp<='0';
IsTransientDown<='0';
IsLinkUp<='0';
IsLinkDown<='0';
VarLinkUp:='0';
VarLinkDown:='0';
VarIstransientUp:='0';
VarIstransientDown:='0';
else
if rising_edge(clk) then
if SoftStart='1' then
VarIstransientDown:='0';
VarIsTransientup:='0';
else
if CompVqu='1' then
VarIstransientDown:=VarIsTransientDown;
VarIsTransientDown:=VarIsTransientDown;
end if;
if LastTransientDown='1' then
VarLinkDown:='1';
end if;
end if;
if CompVqd='1' then
VarIsTransientup:='1';
else
LastTransientUp:=VarIsTransientUp;
VarIsTransientUp:=VarIsTransientUp;
end if;
if LastTransientUp='1' then
VarLinkUp:='1';
end if;
end if;
end if;
IsTransientUp<=VarIsTransientup;
IsTransientDown<=VarIsTransientdown;
IsLinkUp<=VarLinkup;
IsLinkDown<=VarLinkDown;
end
IsLinkDown<=VarLinkdown;
end if;
end if;
END PROCESS;
END behavioral;

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_misc.and_reduce;
use ieee.std_logic_misc.or_reduce;
use work.mypackPCMMPP.all;

entity ControlUnit is port (resetn: in std_logic;
WRT: in std_logic;
CLK_CTRL: in std_logic;
CompV: in std_logic;
CompVq: in std_logic;
SWCLK: in std_logic;
IsTransientUp: in std_logic;
IsTransientDown: in std_logic;
IsLinkUp: in std_logic;
IsLinkDown: in std_logic;
IsLinkMode: out std_logic;
SoftStart: out std_logic;
StartRelease: out std_logic;
DACV13: out std_logic;
DACV12: out std_logic;
DACV11: out std_logic;
DACV10: out std_logic;
DACV9: out std_logic;
DACV8: out std_logic;
DACV7: out std_logic;
DACV6: out std_logic;
DACV5: out std_logic;
DACV4: out std_logic;
DACV3: out std_logic;
DACV2: out std_logic;
DACV1: out std_logic;
DACV0: out std_logic;
DACI13: out std_logic;
DACI12: out std_logic;
DACI11: out std_logic;
Appendix D VHDL Codes

DACI10: OUT std_logic;
DACI9: OUT std_logic;
DACI8: OUT std_logic;
DACI7: OUT std_logic;
DACI6: OUT std_logic;
DACI5: OUT std_logic;
DACI4: OUT std_logic;
DACI3: OUT std_logic;
DACI2: OUT std_logic;
DACI1: OUT std_logic;
DACI0: OUT std_logic;
TestLed: OUT std_logic;
DataCatched: OUT CurCounterType;
OverFlowUpLed: OUT std_logic;
OverFlowDownLed: OUT std_logic;
TUCatched: OUT CurCounterType;
TDCatched: OUT CurCounterType;
StartReleaseLed: OUT std_logic);
END ControlUnit;

ARCHITECTURE behavioral OF ControlUnit IS
Type StateType is (S0,S1);
Signal CurState,CurStateM: StateType;
Signal SGNVolMid: VolCounterType;
Signal SGNPeakCur,CounterTU,CounterTD: CurCounterType;
BEGIN

process(CLK_CTRL,resetn)
Variable VarDACI,VarPeakCur,AdjAmount,startupCounter: CurCounterType;
Variable VarDACV,VarVolMid: VolCounterType;
Variable NextState: StateType;
Variable VarsIsTransientUp,VarsIsTransientDown,LastTransientUp,LastTransientDown, SoftRelease: std_logic;
Variable VarSmoothTransient,VarOverTransientUp: std_logic;
Variable VarLinkUp,VarLinkDown,VarCompV,VarLinkMode: std_logic;
begin
if resetn='0' then
VarVolMid:=InitialVolMid;
VarPeakCur:=InitialPeakCur;
VarDACV:=InitialVolMid;
VarDACI:=InitialPeakCur;
SGNVolMid<=InitialVolMid;
SGNPeakCur<=InitialPeakCur;
DACV13<='1';
DACV12<='1';
DACV11<=VarDACV(7);
DACV10<=VarDACV(6);
DACV9<=VarDACV(5);
DACV8<=VarDACV(4);
DACV7<=VarDACV(3);
DACV6<=VarDACV(2);
DACV5<=VarDACV(1);
DACV4<=VarDACV(0);
DACV3<='1';
DACV2<='1';
DACV1<='1';
DACV0<='1';
DACI13<=VarDACI(7);
DACI12<=VarDACI(6);
DACI11<=VarDACI(5);
DACI10<=VarDACI(4);
DACI9<=VarDACI(3);
DACI8<=VarDACI(2);
DACI7<=VarDACI(1);
DACI6<=VarDACI(0);
DACI5<='0';
DACI4<='0';
DACI3<='0';
DACI2<='0';
DACI1<='0';
DACI0<='0';

AdjAmount:=AdjustStepSteady;
SoftStart<='1';
SoftRelease<='1';
SGNStartUp<='1';
IsOverFlowUp<='0';
IsOverFlowDown<='0';
OverFlowUpLed<='0';
OverFlowDownLed<='0';
NextState:=S0;
CurStateM<=S0;
SGNCompV<='0';
SGNCompVq<='0';
CounterTU<=(others=>'0');
CounterTD<=(others=>'0');
VarSmoothTransient<='0';
IsLinkMode<='0';
VarLinkUp<='0';
VarLinkDown<='0';
VarCompV<='0';
VarLinkMode<='0';
StartReleaseLed<='0';

else
if rising_edge(CLK_CTRL) then
Case CurStateM is
  when S0 => if CompV='1' then

SGNCompV<='1';
else
    SGNCompV<='0';
end if;

if CompVq='1' then
    SGNCompVq<='1';
else
    SGNCompVq<='0';
end if;

if (SGNPeakCur > MaxPeakCur) then
    IsOverFlowUp<='1';
    OverFlowUpLed<='1';
else
    IsOverFlowUp<='0';
    OverFlowUpLed<='0';
end if;

if (SGNPeakCur < MinPeakCur) then
    IsOverFlowDown<='1';
    OverFlowDownLed<='1';
else
    IsOverFlowDown<='0';
    OverFlowDownLed<='0';
end if;

if IsTransientDown='1' or IsTransientUp='1' then
    IsLinkMode<='0';
    if IsTransientUp='1' then
        AdjAmount:=AdjustStepTransUp;
    end if;
    if IsTransientDown='1' then
        AdjAmount:=AdjustStepTransDown;
    end if;
else
    if IsLinkUp='1' or IsLinkDown='1' or VarLinkUp='1' or VarLinkDown='1' then
        IsLinkMode<='1';
        VarLinkMode<='1';
        if IsLinkUp='1' or VarLinkUp='1' then
            AdjAmount:=AdjustStepUpLink;
            VarLinkUp<='1';
        end if;
        if IsLinkDown='1' or VarLinkDown='1' then
            AdjAmount:=AdjustStepDownLink;
            VarLinkDown<='1';
        end if;
    else
        if VarSmoothTransient='1' then

end if;
AdjAmount:='0' & AdjAmount(VolCounterWidth downto 1);
else
   AdjAmount:=AdjustStepSteady;
end if;
IsLinkMode<='0';
VarLinkMode:='0';
end if;
end if;
NextState:=S1;

when S1 => if SGNCmpV='0' then
   VarLinkUp:='0';
else
   VarLinkDown:='0';
end if;

if AdjAmount>AdjustStepSteady then
   VarSmoothTransient:='1';
else
   VarSmoothTransient:='0';
end if;
if VarLinkMode='0' then
   VarCompV:=SGNCmpV;
else
   VarCompV:=SGNCmpVq;
end if;
case VarCompV is
   when '0' => if IsOverflowUp='1' then
      VarVolMid:=MinVolMid;
      VarPeakCur:=MaxPeakCur;
   else
      VarVolMid:=VarVolMid-AdjAmount;
      VarPeakCur:=VarPeakCur+AdjAmount;
   end if;
   when '1' => if IsOverflowDown='1' then
      VarVolMid:=MaxVolMid;
      VarPeakCur:=MinPeakCur;
   else
      VarVolMid:=VarVolMid+AdjAmount;
      VarPeakCur:=VarPeakCur-AdjAmount;
   end if;
   SoftStart<='0';
   SoftRelease:=0';
   SGNStartUp<='0';
   StartReleaseLed<='1';
   when others => null;
end case;

SGNVolMid<=VarVolMid;
SGNPeakCur<=VarPeakCur;
VarDACV:=VarVolMid;
VarDACI:=VarPeakCur;
DACV11<=VarDACV(7);
DACV10<=VarDACV(6);
DACV9<=VarDACV(5);
DACV8<=VarDACV(4);
DACV7<=VarDACV(3);
DACV6<=VarDACV(2);
DACV5<=VarDACV(1);
DACV4<=VarDACV(0);
DACI13<=VarDACI(7);
DACI12<=VarDACI(6);
DACI11<=VarDACI(5);
DACI10<=VarDACI(4);
DACI9<=VarDACI(3);
DACI8<=VarDACI(2);
DACI7<=VarDACI(1);
DACI6<=VarDACI(0);
NextState:=S0;
when others => null;
end case;
CurStateM<=NextState;

end if;
end if;
end process;

process(CLK_CTRL,resetn)
Variable VarTU,VarTD: CurCounterType;
begin
if resetn='0' then
  TUCatched<=(others=>'0');
  TDCatched<=(others=>'0');
  VarTU:=(others=>'0');
  VarTD:=(others=>'0');
else
  if rising_edge(CLK_CTRL) then
    if SGNStartUp='0' then
      if CounterTU>VarTU then
        TUCatched<=CounterTU;
        VarTU:=CounterTU;
      end if;
      if CounterTD>VarTD then
        TDCatched<=CounterTD;
        VarTD:=CounterTD;
      end if;
    end if;
  end if;
end if;
end if;
end process;
process(SWCLK,resetn)
begin
if resetn='0' then
   DataCatched<=(others=>'0');
else
   if rising_edge(SWCLK) then
      DataCatched<=SGNPeakCur;
   end if;
end if;
end process;

End behavioral;