MOSFET CURRENT SOURCE GATE DRIVERS AND TOPOLOGIES FOR HIGH EFFICIENCY AND HIGH FREQUENCY VOLTAGE REGULATOR MODULES

by

Zhiliang Zhang

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Abstract

With fast development of semiconductor industry, the transistors in microprocessors increase dramatically, which follows the Moore’s law. As a result, the operating voltages of the future microprocessors follow the trend of decreasing (sub 1V) while the demanding currents increase (higher than 100A). Furthermore, the high slew rates during the transient will reach 1200 A/us. All these impose a serious challenge on a Voltage Regulator (VR) or Voltage Regulator Module (VRM). In order to meet requirements of the next generation microprocessors, four new ideas are proposed in this thesis.

The first contribution is an accurate analytical loss model of a power MOSFET with a Current-Source Driver (CSD). The impact of the parasitic components is investigated. Based on the proposed loss model, a general method to optimize the CSD is presented. With the proposed optimization method, the CSD improves the efficiency from 79.4% using the conventional voltage source driver to 83.6% at 12V input, 1.5V/30A output and 1MHz.

The second contribution is a new continuous CSD for a synchronous buck converter. The proposed CSD is able to drive the control and Synchronous Rectifier (SR) MOSFETs independently with different drive currents enabling optimal design. At 12V input, 1.5V/30A output and 1MHz, the proposed CSD improves the efficiency from 79.4% using a conventional voltage source driver to 83.9%.

The third contribution is a new discontinuous CSD. The most important advantage of the new CSD is the small inductance (typically, 20nH at 1MHz switching frequency). A hybrid gate drive scheme for a synchronous buck converter is also proposed. The idea of the hybrid gate driver scheme is to use the CSD to achieve switching loss reduction for the control MOSFET, while use the conventional voltage source driver for the SR. At 12V input, 1.3V/25A output and 1MHz, the proposed CSD improves the efficiency from 80.7% using the voltage source driver to
85.4%.

The final contribution is new self-driven zero-voltage-switching (ZVS) non-isolated full-bridge converters for 12V input VRM applications. The proposed converter achieves the duty cycle extension, ZVS operation and SRs gate energy recovery. At 12V input, 1.3V output and 1MHz, the proposed converter improves the efficiency from 80.7% using the buck converter to 83.6% at 50A.
Acknowledgements

I would like to thank my supervisors, Dr. Yan-Fei Liu and Dr. P. C. Sen for their encouragement, guidance, and support throughout this thesis project. Their eagerness to share their knowledge, expertise and time is greatly appreciated. In addition, I would like to thank all of my past and present colleagues from the Queen’s Power Group. In particular, I would like to thank Wilson Eberle and Zhihua Yang for their insights into current-source drivers (CSDs) and switching loss. Discussions with Eric Meyer, Sheng Ye, Darryl Tschirhart, Kai Xu, Guang Feng, Ping Lin and Jizhen Fu on many topics on Power Electronics were also a great help.

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For My Parents
Jing Li
Shanpei Zhang
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<th>Description</th>
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<tbody>
<tr>
<td>$B_{ac, pk}$</td>
<td>Magnetic core peak AC flux density</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitor</td>
</tr>
<tr>
<td>$C_b$</td>
<td>Bootstrap capacitance</td>
</tr>
<tr>
<td>$C_{dsi}$</td>
<td>MOSFET parasitic drain-to-source capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_f$</td>
<td>Converter powertrain output filter capacitance</td>
</tr>
<tr>
<td>$C_g$</td>
<td>MOSFET total parasitic gate capacitance</td>
</tr>
<tr>
<td>$C_{gdi}$</td>
<td>MOSFET parasitic gate-to-drain capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_{gsi}$</td>
<td>MOSFET parasitic gate-to-source capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_{issi}$</td>
<td>MOSFET parasitic input capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_m$</td>
<td>Magnetic core loss constant</td>
</tr>
<tr>
<td>$C_{ossi}$</td>
<td>MOSFET parasitic output capacitance, where $i$ corresponds to the MOSFET number</td>
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<tr>
<td>$d$</td>
<td>MOSFET drain terminal</td>
</tr>
<tr>
<td>$d_i$</td>
<td>MOSFET drain terminal, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>$D_i$</td>
<td>Diode, where $i$ corresponds to the diode number</td>
</tr>
<tr>
<td>$D_f$</td>
<td>Bootstrap diode</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$g_i$</td>
<td>MOSFET gate terminal, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$g_{fs}$</td>
<td>MOSFET transconductance</td>
</tr>
<tr>
<td>$i_d$</td>
<td>MOSFET drain current</td>
</tr>
<tr>
<td>$i_g$</td>
<td>Gate drive current</td>
</tr>
<tr>
<td>$i_{Li}$</td>
<td>$i$th inductor current, ($i=1,2,3,...$)</td>
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<tr>
<td>$I_o$</td>
<td>Load current</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>Current at turn off</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>Current at turn on</td>
</tr>
<tr>
<td>$M_i$</td>
<td>$i$th power MOSFET, ($i=1,2,3,...$)</td>
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Transformer turns ratio: primary turns over secondary turns

$P_{\text{core}}$ Core loss

$P_{\text{cond}}$ Total conduction loss

$P_g$ MOSFET gate loss

$Q_{rr}$ Reverse recovery charge

$R_i$ $i$th resistor, $(i=1,2,3,\ldots)$

$R_{ac}$ AC resistance

$R_{dc}$ DC resistance

$R_{DS(\text{on})}$ MOSFET on resistance

$R_g$ MOSFET internal gate resistance

$S$ MOSFET source terminal

$S_i$ MOSFET source, where $(i=1,2,3,\ldots)$ is the MOSFET number

$t$ time

$T_s$ Switching period

$v_{ds}$ Drain-to-source-voltage

$v_{gs}$ MOSFET gate-to-source voltage

$v_o$ Output voltage

$V_b$ Blocking capacitor voltage

$V_{cc}$ MOSFET driver supply voltage

$V_{core}$ Volume of the core

$V_{ds}$ Drain-to-source voltage

$V_F$ Diode forward voltage drop

$V_{in}$ Input voltage

$V_o$ Average output voltage

$V_{pl}$ MOSFET plateau voltage

$V_{th}$ MOSFET threshold voltage

$x$ Core loss switching frequency parameter

$y$ Core loss peak flux density parameter

**Abbreviations**

BJT Bipolar Junction Transistor

CSD Current-Source Driver

FB Full Bridge
IC | Integrated Circuits  
MOSFET | Metal Oxide Silicon Field Effect Transistor  
PCB | Printed Circuit Board  
PWM | Pulse Width Modulation  
RMS | Root Mean Square  
SR | Synchronous Rectifier  
VR | Voltage Regulator  
VRM | Voltage Regulator Modulator  
ZCS | Zero Current Switching  
ZVS | Zero Voltage Switching  

**Prefixes for SI Units**

<table>
<thead>
<tr>
<th>Letter</th>
<th>Prefix</th>
<th>Factor</th>
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<tbody>
<tr>
<td>p</td>
<td>Pico</td>
<td>$10^{-12}$</td>
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<tr>
<td>n</td>
<td>Nano</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>μ</td>
<td>Micro</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>m</td>
<td>Milli</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>k</td>
<td>Kilo</td>
<td>$10^3$</td>
</tr>
<tr>
<td>M</td>
<td>Mega</td>
<td>$10^6$</td>
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**SI Units**

<table>
<thead>
<tr>
<th>Symbol</th>
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<tbody>
<tr>
<td>A</td>
<td>Amperes</td>
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<tr>
<td>F</td>
<td>Farads</td>
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<tr>
<td>H</td>
<td>Henries</td>
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<tr>
<td>Hz</td>
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<td>W</td>
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<td>Ω</td>
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Chapter 1
Introduction

1.1 Introduction

This section gives the basic introduction to a Voltage Regulator Module (VRM) or Voltage Regulator (VR) in a computer power system. It lays the groundwork for the material presented in Chapters 2-6, which focus on current source drivers (CSDs), analytic switching loss model and new non-isolated topologies for 12V input VRMs. Then, the recent trends and challenges to VMRs are discussed, which provides the motivation of high switching frequency VRMs for next generation microprocessors.

1.2 Introduction and Requirements of VRMs

The fast development in VLSI (Very Large Scale Integration) technologies imposes an increasing challenge to supply state of the art microprocessors with high quality power. As Moore’s law predicts that the number of transistors per chip will double every 18 months, the number of the transistors has kept increasing steadily in the past decades. Meantime, the clock frequencies of microprocessors have also increased significantly.

The increase in the microprocessor’s speed and transistor number has led to high current demands and fast transient load change requirement since the supply voltage of the microprocessor is decreased to reduce the power consumption of the chip. In the point-of-load regulation system, a dedicated dc/dc converter, a VRM or VR, is used to deliver a highly accurate supply voltage to the microprocessor. VRMs are placed in close proximity to the microprocessor in order to minimize the impact of the parasitic impedance between the VRMs and microprocessor.

According to Intel microprocessor’s road map in [1], the microprocessors operate at
extremely low voltages (<1V) and high currents (>100A) with the continuous increase of the speed and transistors within the chips. Meanwhile, the strict transient requirement [1] of the microprocessors is another serious challenge to VRMs. As an example, for Dual-Core Intel Xeon Processor 7000/7100 series processor, the VRM/EVRD 11.0 is required to support the following: 1) a maximum continuous load current of 130A; b) a maximum load current of 150A peak; 3) a maximum current slew rate of 1200A/\mu s at the lands of the processor.

In order to meet the strict transient requirement, large amount of expensive output capacitors are required to reduce the output voltage deviation during a transient event. As a result, the cost of a VRM will increase while the power density is reduced. However, the real estate on the mother board for VRMs is so limited that the future VMRs should have much higher power density than today’s version. To increase power density, high switching frequency operation is an effective approach. More importantly, high switching frequency leads to high bandwidth and improves the dynamic response. Therefore, high switching frequency (> 1MHz) operation of VRMs is strongly desired and becomes the trend of new generation VRMs. Unfortunately, high frequency operation normally increases the frequency-dependent loss in the power supply system. Therefore, high efficiency is of critical importance to achieve good thermal management and thus high power density. Overall, the challenges for future VRMs are to provide a precisely regulated output with high efficiency, high power density and fast dynamic response.

### 1.3 Power Architecture for Computer Systems

Figure 1.1 shows the power delivery architecture for computer systems such as desktop and notebook computers. The silver box is actually an AC-DC converter to process power from the AC line to provide multiple output DC voltages (3.3V, 5V, 12V etc). The extreme dynamic requirements of the microprocessor make it difficult for the centralized silver box to provide
energy for the microprocessor directly because the silver-box is too far away from the microprocessor. The high parasitic inductances due to the long connection cable prevent the silver-box power supply from delivering transient current quickly. So a VRM is used to meet the strict dynamic requirement. As shown in Figure 1.1, the silver box provides 12V to feed the VRM, which step down the voltage to around 1.2V to power the microprocessor. Since a VRM is placed close to the microprocessor and parasitic inductance is minimized, the transient load current can be handled quickly by the VRM. In particular, for notebook computers, it is important to maintain high light load efficiency to increase battery life.

![Figure 1.1 Power delivery architecture for computer systems](image)

For 12V input voltage VRMs, one of the most popular topologies is a synchronous buck converter as shown in Figure 1.2 because of its simple structure and control. But the problem of a single phase buck converter is the high output filter inductance that limits the transient response. In order to reduce the VRM output capacitance, a fast inductor current slew rate is preferred. Because a smaller inductance gives a larger current slew rate, the inductance should be minimized so that the transient requirement can be met. Nevertheless, small inductances result in large current ripples and high switching loss. In 1997, VPEC (CPES) proposed the interleaving technology to solve large current ripples in quasi-square-wave (QSW) VRMs [2].
Figure 1.2 Single phase synchronous buck converter

Figure 1.3 shows multiphase interleaving buck converters, which are most widely used in today’s VRM industry. The advantages of this topology are: 1) simple and low cost; 2) reduced current ripples to the output capacitors due to the interleaving; 3) small output inductances to improve transient response; 4) better thermal management and package flexibility are also achieved due to the distributed structure of multiphase. The disadvantage of this topology is high switching loss of $Q_1$ and asymmetrical dynamic response due to the extremely low duty cycle of the buck converter.

Figure 1.3 Multiphase interleaving buck converters

1.4 Research Motivation and Objectives

Presently, MHz operation of VRMs includes the following technologies: power MOSFET semiconductor, semiconductor integration, packaging, current-source driver (CSD) technique,
new VR topologies, advanced control technique and magnetic materials.

With fast development of new low voltage power semiconductor devices, it is demanding to propose new technologies to take advantages of these new devices. The scope of this thesis is focusing on techniques to improve efficiency, power density of 12V input VRMs in a cost effective manner. The motivation of research is to propose innovative approaches from perspective of the circuit level to boost the efficiency of VRMs.

This thesis addresses three areas related to high efficiency of MHz 12V input VRMs: 1) a new accurate analytical loss model of a power MOSFET operating at a CSD and a general optimal design method; 2) an improved continuous CSD; 3) a new discontinuous CSD; 4) new soft-switching non-isolated topologies with self-driven Synchronous Rectifier (SR). These new techniques can be used above 1MHz.

1.4.1 Analytical Loss Model of a Power MOSFET with a Continuous CSD

Gate drive loss becomes a penalty at high frequency (>1MHz) when using conventional voltage source gate drivers. In the last fifteen years, resonant gate drivers or soft drivers have originally been proposed with the objective of recovering gate energy lost in conventional voltage gate drivers. Many different resonant gate drivers have been proposed. However, these investigations are generally emphasizing gate energy savings by resonant gate drivers and concentrating on the drive topologies, but ignoring the potential switching loss reduction that are actually much more dominant in a high frequency buck converter.

Recently, CSD technology has been proposed to reduce the switching loss. In order to achieve maximum efficiency improvement of the CSD, a general method for the purpose of optimal design is needed. Therefore, an analytical loss model of the power MOSFET with a CSD should be developed.
The contribution of the work presented in Chapters 3 is to solve the above problems and demonstrate the advantages of the CSD for high frequency VRM applications. A new analytical loss model of the power MOSFET with a CSD is developed. Based on the proposed loss model, a generalized method to optimize the new CSD is proposed and employed in the development of a 12V input and 1MHz synchronous buck converter prototype. Through the optimal design, a significant improvement of the efficiency is achieved.

### 1.4.2 A New Continuous CSD

In Chapter 3, the proposed model are used to optimize the CSD proposed in [3] for a synchronous buck converter to achieve efficiency improvement. However, carefully investigating the equivalent circuits of operation, it is noted that this CSD in [3] suffers from the following disadvantages:

1) In a buck converter, a high gate drive current is desired for the control MOSFET to ensure fast switching speed and reduce switching loss, while a relatively low gate drive current is desired for the synchronous MOSFET to achieve gate energy recovery. Therefore, it is beneficial to have different gate drive currents for optimal design. However, the CSD in [3] can only provide identical drive currents for the two MOSFETs in a buck converter;

2) Due to the reverse recovery of the body diode, the switching node has severe oscillation. This switching node is actually in series with the level-shift capacitor of this CSD, which makes the circuit sensitive to the reverse recovery noise in practical applications. In addition, the input voltage is applied to the current source inductor, which results in high inductance value at high input voltage;

3) The resonant inductor current flows through the control MOSFET and SR, which causes additional conduction loss;
4) To enhance light load efficiency, the switching frequency may be reduced or diode emulation may be used to turn off SRs to allow discontinuous conduction mode. However, it is difficult to achieve these features using the CSDs.

The contribution of Chapter 4 is to propose a new CSD to solve the above problems and improve the CSD performance.

1.4.3 A New Discontinuous CSD

In Chapter 3 and Chapter 4, the CSDs use continuous inductor currents as the gate drive currents. A significant efficiency improvement has been achieved owing to fast switching speed. However, one concern of the continuous CSD is the inductance value is relatively high (typically, around 1μH at the switching frequency of 1MHz). In addition, the switching frequency variation will impact on the inductance value in the continuous CSDs.

The contribution of Chapter 5 is to present a new CSD with a discontinuous inductor current to overcome the disadvantages of the continuous CSDs. Compared to other CSDs proposed in previous work, the most important advantage of the proposed discontinuous CSD is the small inductance (typically, around 20nH at 1MHz switching frequency). Other features of the proposed CSD include: 1) discontinuous inductor current with low circulating loss; 2) fast switching speed and reduced switching loss; 3) wide range of duty cycle and switching frequency; 4) high noise immunity. Compared to the discontinuous CSD in [4], since the actual voltage across the inductor is reduced by half, for the same pre-charge time and gate drive current, the proposed driver can further reduce the inductance value by half.

1.4.4 New ZVS Self-Driven Non-Isolated Full Bridge Topologies for 12V Input VRMs

Multiphase synchronous buck converters are used exclusively in 12V VRMs owing to the simplicity and minimum components. However, they suffer from extremely low duty cycle at
12V input voltage. To make thing worse, the parasitic in the buck converter may result in high switching loss and low conversion efficiency.

The contribution of Chapter 6 is to present new ZVS self-driven non-isolated FB topologies to solve the problems of a buck converter. The proposed topology achieves duty cycle extension and features ZVS, self-driven capability with SR gate energy recovery and reduced voltage stress over the SR MOSFETs. Owing to the duty cycle extension, lower output inductances can be used and the reverse recovery losses of the SR body diodes can also be reduced. All these features improve the efficiency to achieve high switching frequency and fast dynamic response. In addition, the proposed converter can use existing multiphase buck controllers and buck drivers directly.

1.5 Thesis Organization

This thesis consists of seven chapters. Chapter 1 introduces background of VRMs/VRs in a computer power system. This chapter also establishes motivation and sets objectives for the research contributions presented in Chapters 3-6. A literature review on switching loss, gate drivers, CSDs and non-isolated topologies for 12V input VRM applications are presented in Chapter 2. Chapter 3 proposes a new analytical model for the CSD and a general optimal design method. Simulation and experimental results are presented to verify the validity of the modeling analysis. Chapter 4 introduces a new CSD to solve the problems of the CSD in [3]. The driver loss analysis, design with optimization, logic and level shift implementations and experimental results are also presented. In Chapter 5, a new discontinuous CSD is presented to overcome the disadvantages of the continuous CSDs. The experimental results verify the functionality of the proposed circuit. Chapter 6 introduces new ZVS non-isolated self-driven topologies to solve the problems of buck converters for 12V input VRMs. The efficiency improvement has been verified
by the experimental results. Chapter 7 summarizes the contributions of the research presented in this thesis and gives recommendations for future work.
Chapter 2
Literature Review

2.1 Introduction

In this chapter, a critical review of literature relevant to the three main thesis topics is presented, which are all related to high frequency VRMs. They include: 1) MOSFET gate drive including switching and gate driving loss; 2) resonant gate drivers; 3) non-isolated VRMs topologies.

In section 2.2, an overview of VRMs is presented. Loss mechanisms in VRMs are discussed in section 2.3. A review of MOSFET gate drive techniques is presented in section 2.4. A review of non-isolated VRM topologies is presented in section 2.5. The conclusions are presented in section 2.6.

2.2 High Switching Frequency VRMs

High switching frequency shrinks the passive components and leaves more space for power semiconductor devices, thus yields higher power density. Moreover, the reduction of the filter components also makes it possible to increase the bandwidth of the converter and output current slew rate, which improves the dynamic response of VRMs.

In recent years, MHz VRMs show great advantages over the conventional 300KHz VRMs in terms of cost, power density and dynamic response etc [5]-[8]. It is known that the higher the bandwidth of VRMs, the smaller the output capacitance. Unfortunately, an increase in switching frequency will lead to lower efficiency and thermal problems due to excessive frequency-related loss, and result in degradation in overall system performance. Therefore, it is of great importance to understand the loss mechanism in a high frequency VRM and then reduce the loss.
2.3 Frequency-Dependent Loss

The loss of a VRM includes the frequency dependent loss and non-frequency dependent loss. In a high frequency VRM, the efficiency could be greatly degraded due to excessive frequency-dependent loss causing serious thermal problems. Actually, the switching loss, the body diode loss, the reverse recovery loss and the gate charge loss are the major frequency-dependent loss in a VRM. To reduce these losses is critical to achieve high frequency and high power density for new generation VRMs.

2.3.1 Switching Loss

Switching loss is a most important frequency-dependent loss and the dominant loss in a synchronous buck converter. Therefore, the way of calculating switching loss is critical to design a VR. Normally, the piecewise linear approximation of the MOSFET turn-on and turn-off waveforms is usually made for simplifying the switching loss model [9]-[10]. The turn-on transition equivalent circuit and its associated waveforms are illustrated in Figure 2.1.

![Figure 2.1 MOSFET turn-on transition: (a) simplified turn-on equivalent circuit and (b) waveforms](image)
During $T_1$ interval, the MOSFET driver turns on and begins to supply current to the MOSFET gate to charge its input capacitance $C_{gs}$ and $C_{gd}$. There are no switching loss until the gate voltage $v_{gs}$ reaches the threshold voltage $V_{th}$. Entering $T_2$ interval, $v_{gs}$ reaches $V_{TH}$, the input capacitance is being charged and the MOSFET’s drain current $i_{ds}$ is rising linearly until it reaches the load current. During $T_2$, the MOSFET is sustaining the entire input voltage across it. During $T_3$ interval, the load current is flowing through MOSFET, and the drain voltage $v_{ds}$ begins to fall. All of the gate current will be going to charge the capacitance $C_{gd}$ and $v_{gs}$ comes into Miller plateau level. During this interval, $i_{ds}$ is constant as the load current and the drain voltage is falling fairly linearly from the input voltage to zero. During $T_4$ interval, the MOSFET is just fully enhancing the channel to obtain its rated on-resistance $R_{DS(ON)}$ at a rated $V_{gs}$.

Therefore, the turn-on switching loss happens during $T_2$ and $T_3$ intervals and can be calculated based on the linear current and voltage waveforms by (2.1)

$$P_{\text{turn-on}} = \frac{V_{ds} \cdot I_{ds}}{2} \cdot (T_2 + T_3) \cdot f_s$$

where $V_{ds}$ is the block voltage and $I_{ds}$ is the load current and $f_s$ is the switching frequency.

The turn-off transition equivalent circuit and its associated waveforms are illustrated in Figure 2.2.

During $T_5$ interval, the input capacitance $C_{gs}$ and $C_{gd}$ are discharged from the initial value to the Miller plateau level. During this interval, the gate current is supplied by the input capacitance. During $T_6$ interval, the drain voltage $v_{ds}$ begins to rise. All of the gate current will be going to discharge the capacitance $C_{gd}$, which corresponds to the Miller plateau in the waveform. During $T_7$ interval, the gate voltage resumes falling form $V_{pl}$ to $V_{th}$. The MOSFET is in linear operation and the drain current $i_d$ decrease to zero. During $T_8$, the input capacitor is fully discharged and the MOSFET is turned off completely.
Therefore, the turn-off switching loss happens during $T_6$ and $T_7$ intervals and can be calculated based on the linear current and voltage waveforms by (2.2)

$$P_{\text{turn-off}} = \frac{V_{ds} \cdot I_{ds} \cdot (T_6 + T_7) \cdot f_s}{2} \quad (2.2)$$

Unfortunately, this simplifying switching loss model does not consider the common source inductance and the non-linear characteristics of the parasitic capacitors of the MOSFET. The common source inductance $L_{s1}$ of the control MOSFET, as illustrated in Figure 2.3, is the inductance shared by the main current path and the gate driver loop, which has negative impact on switching transition and increases switching loss at high switching frequency (>1MHz).
Figure 2.4 illustrates the equivalent circuit of turn-on transition with the common source inductance. During the turn-on transition, the drain current $i_{ds}$ increases, which will induce a positive voltage across $L_s$. The turn-on gate current is

$$i_{g_{\text{on}}} = \frac{v_{gs} - v_{Cgs} - L_s \frac{d i_{ds}}{dt}}{R_g + R_{hi}}$$

(2.3)

From (2.3), because of $L_s \frac{d i_{ds}}{dt}$, the effective turn-on gate current $i_{g_{\text{on}}}$ is reduced, which increases the turn-on transition time and turn-on loss.

Figure 2.4 Equivalent circuit of turn-on transition with the common source inductance.

Figure 2.5 illustrates that with the conventional voltage source driver, after the common source inductance of 2nH is considered, the turn-on transition time dramatically increases from 7ns to 17ns, which increases the turn-on loss. The circuit parameters are as follows: $V_{in}=12\text{V}$, $V_o=1.2\text{V}$, $I_o=20\text{A}$, control MOSFET: HAT2168, SR: HAT2165 [11]-[12].
Figure 2.5 Turn-on transition comparison: (a) without the common source inductance, (b) with the common source inductance ($L_s = 2\, \text{nH}$)

Figure 2.6 illustrates the equivalent circuit of turn-off transition with the common source inductance. During the turn-off transition, the drain current $i_{ds}$ decreases, which will induce a negative voltage across $L_s$. Therefore, the turn-off gate current is

$$i_{g\_off} = \frac{v_{C_{gs}} - L_s \frac{di_{ds}}{dt}}{R_g + R_{so}} \quad (2.4)$$

From (2.4), because of $L_s \frac{di_{ds}}{dt}$, the effective turn-off gate current $i_{g\_off}$ is reduced, which
increases the turn-off transition time and turn-off loss.

Figure 2.7 illustrates that after the common source inductor of 2nH is considered, the turn-off transition time dramatically increases from 6ns to 23ns, which increases the turn-off loss greatly.

![Diagram of turn-off transition comparison](image)

Figure 2.7 Turn-off transition comparison: (a) without the common source inductance, (b) with the common source inductance ($L_{s1}=2nH$)

In summary, change of the drain-source current will induce a voltage across the common source inductance $L_{s1}$, which always reduces the effective gate drive currents of the control MOFET and prolongs the switching time, and consequently increases the switching loss significantly at high switching frequency. Therefore, the loss calculation based on the piecewise linear model is much lower than the experimental results obtained from synchronous buck converters with MHz switching frequency.

In order to predict the switching loss at high frequency more accurately, the analytical switching loss model was proposed in [11] considering the common source inductance, which is suitable for massive data processing of some applications that need good accuracy and short simulation time. The bus voltage for 12V two-stage VR was optimized based on the above
accurate analytical loss model in [12] and the loss calculation matches the experimental results at the switching frequency of 2MHz well. In [13], the common source inductance and switching loop inductance were modeled simultaneously and the MOSFET switching characteristics is explored based on close-form analytical equations, which provides design criteria for optimizing switching performance of packaged power electronics.

The impact of the common source inductance $L_{c2}$ on SR $Q_2$ was investigated in [14]. The common source inductance could help to reduce power loss because of the reverse current direction in the SR compared to the control MOSFET. In addition, with common source inductance, $Cdv/dt$ immunity and zero dead time switching could be achieved, which could reduce power loss of the SRs.

New packaging technology, such as PowerPAK SO-8 from Vishay and DirectFET from International Rectifier, reduces the parasitic influence to improve the efficiency and provide better thermal characteristics for a high frequency VR [15] [16].

It is observed from (2.1) and (2.2) that for the given current and voltage, it is a possible to reduce switching loss by reducing the switching time. The is the basic idea of the CSDs to reduce the switching loss by driving the MOSFETs faster. Alternatively, soft-switching technique can reduce the switching loss since the voltage across the switch is zero when it turns on (ZVS) or the current is zero when it turns off (ZCS).

2.3.2 Body Diode Conduction Loss

In high current VRM applications, SR technique is widely used to reduce the conduction losses of the diode rectifiers. In a synchronous buck converter, the dead-time is the amount of time that both the control MOSFET and SR are off to prevent “shoot-through”. The body diode conduction loss is
\[ P_{\text{body}} = V_{\text{body}} \cdot I_o \cdot f_s \cdot t_{\text{body}} \] (2.5)

where \( V_{\text{body}} \) is the body diode forward voltage drop and \( t_{\text{body}} \) is the body diode conduction time.

During the dead time, the SR body diode carries the load current, resulting in high conduction loss due to high forward voltage drop of the body diode. At high switching frequency around 1MHz, the body diode conduction loss becomes high due to the relative ratio of the dead time in one switching cycle. In order to achieve high efficiency of a buck converter, it is so important to minimize the conduction time of the body diode.

The driver chips with adaptive control and predictive control to minimize the dead time are available from different companies such as TPS2832 [17] and UCC27222 [18] from Texas Instrument. In [19], a new resonant gate driver with a transformer and Zener diode was proposed to reduce the body diode conduction loss. As long as the crossover level of the gate driver signals of the two MOSFETs is equal to or less than the threshold voltage of the devices, the dead time can be eliminated and the shoot-through can also be avoided. However, the Zener diode will induce additional gate charge loss and the leakage inductance of the gate drive transformer may deteriorate the overall performance at high frequency.

2.3.3 Reverse Recovery Loss

The reverse recovery loss for the SR body diode is,

\[ P_{\text{QRR}} = Q_{\text{RR}} \cdot V_{R} \cdot f_s \] (2.6)

where \( Q_{\text{RR}} \) is the body diode reverse recovery charge and \( V_R \) is the reverse block voltage.

The reverse recovery current introduces voltage oscillation, decreasing efficiency and causing EMI problems. Soft-switching technique may be used to eliminate the reverse recovery when the forward current through the diode decrease to zero before the reverse voltage block
across the diode.

### 2.3.4 Gate Drive Loss

Energy is required to charge and discharge the MOSFET gate capacitance each switching cycle. For the conventional voltage source driver, this energy is dissipated through resistances in series with the gate within the gate drive circuit. The power to charge the gate of MOSFET is

\[
P_{\text{GATE}} = Q_g \cdot V_c \cdot f_s
\]

(2.7)

where \( Q_g \) is the total gate charge and \( V_c \) is the amplitude of the gate drive voltage.

The gate drive loss becomes a concern at switching frequency beyond 1MHz, which decreases the overall efficiency and causes thermal problems on the driver chips.

### 2.4 Review of Resonant Gate Driver Technique

Resonant gate driver technique was originally developed to recover part of MOSFET gate drive loss when operating at high switching frequency (above 1MHz) [20]-[22]. The self-oscillating resonant gate driver with a resonant network was used in the application of radio frequency (RF) power amplifier featuring sinusoidal waveforms generally [23]-[24]. The self-oscillating resonant gate driver (soft gating driver) is also applied to a high frequency (>30 MHz) DC-DC converter to reduce the gate drive loss [25].

Resonant gate drivers were initially developed in using a small inductance to recover part of the gate energy with reduced circulating loss [26]. Figure 2.8 illustrates a typical resonant gate drive circuit and its corresponding waveforms.

The MOSFET \( M \) is charged or discharged by resonant current \( i_L \), which is provided by the resonant inductor \( L \). When the gate is fully charged to \( V_{cc} \), drive transistor \( S_1 \) is turned on so that it provides a low impedance path to the gate voltage source. At the same time, current \( i_L \) in \( L \) rises linearly. The turn-off transition is initiated by turning \( S_2 \) off. When the gate capacitance is fully
discharged, \( S_2 \) is turned on so that it shunts the gate and the source of the power MOSFET. \( S_1 \) and \( S_2 \) are turned on and off at zero voltage.

The major advantage of this approach is simplicity since only one additional inductor and a capacitor are added comparing to a conventional gate drive circuit. However, this circuit can only be used for only low side and ground referenced drive. At the same time, the basic idea of this resonant gate driver is to recover the gate drive loss, not the switching loss. Therefore, the design criteria is different from the CSD.

Resonant topologies based on resonant pulse technique including full resonance and clamped resonance were proposed in [27]-[32] with the advantage of the low conduction loss. Figure 2.9 illustrates the gate driver with the resonant pulse. It consists of two control drive switches (\( S_1 \) and \( S_2 \)) and two diodes (\( D_1 \) and \( D_2 \)).
The major disadvantage of the resonant pulse solution is that both the turn-on period and turn-off period must be longer than half of the resonant period. Therefore, the switching frequency is limited, which makes it difficult be applied at high frequency application. Moreover, due to the diodes, the gate terminals of the power MOSFET is not effectively clamped to drive voltage when on, or ground when off, which has lower noise immunity.

As a conclusion, among the resonant gate drive circuits previously proposed, all of them suffer from at least one of the following driver specific problems:

1) Only low side, ground referenced drive [26]-[30].

2) The leakage inductance of bulky transformer, or coupled inductance [19], [31]-[33].

3) Slow turn-on and/or turn-off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero current [27]-[29] and [31]-[33].

4) The inability to actively clamp the power MOSFET gate to the supply voltage during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e. lack of $C_{dv/dt}$ immunity [27]-[29] and [31]-[33].

A comparison of fundamental gate-driver topologies for high frequency applications was discussed in terms of suitable operating conditions, construction and losses in [34].
assessment of resonant drive techniques for use in low power dc/dc converters was presented in [35] and the mathematical model was built to estimate the power loss of the drive circuit in [36]. The effects of internal parasitic inductance and the parasitic output capacitance of the driver switches were analyzed focusing on their impact on the driver loss and on the SR gate voltage in different non-isolated resonant driver topologies [37].

Unfortunately, all the above investigations are generally emphasizing gate energy savings by the resonant driver and concentrating on the drive topologies, but ignore the potential switching loss savings that are much more dominant in MHz switching power converter.

A dual low side symmetrical CSD was proposed in [38]-[39]. Figure 2.10 illustrates the dual low-side drive circuit. The circuit is a full-bridge topology consisting of four switches $S_1$-$S_4$ and a inductor $L_r$. $V_c$ is the voltage source.

![Dual low side symmetrical CSD](image)

Figure 2.10 Dual low side symmetrical CSD

The advantage of this drive circuit is that the gate of MOSFET is charged and discharged by a constant current source during the switching transition, which ensures the fast switching speed and reduces the switching loss. In addition, this drive circuit has a simple structure since only one inductor is needed to drive two power MOSFETs.

A level-shift version of the above drive circuit for a synchronous buck converter with the same advantages was proposed and in [3]. The dual channel high side and low side CSD is shown.
in Figure 2.11.

This drive circuit can provide two drive signals with duty cycle $D$ and $1-D$ respectively when it operates in a complementary mode. So it can be used for driving two MOSFETs in synchronous buck converters, which are used exclusively as 12V input VRMs to power microprocessors due to its simplicity and low component count.

To reduce the circulating current in the drive circuit, a CSD circuit with discontinuous resonant inductor current to minimize circulating current conduction loss was proposed in [40]-[41]. Figure 2.12 illustrates this drive circuit. This drive circuit consists of $Q_1$-$Q_4$ including their body diodes $D_1$-$D_4$, and a small inductance $L_R$. 

Figure 2.11 Dual channel high side and low side CSD
The key idea of the driver operation is the control of the driver switches and body diodes to generate the discontinuous inductor current waveforms. A portion of the inductor current waveform at its peak is then used to charge the power MOSFET gate as a nearly constant current source. This concept is illustrated in Figure 2.13.

This drive circuit can operate effectively over a wide range of duty cycles with constant peak current, a significant advantage for many applications since turn on and turn off times do not vary with the operating point. It can also recover a portion of the \( CV^2 \) gate energy and achieve quick
turn on and turn off transition times to reduce switching loss. The disadvantage of this driver circuit is that each power MOSFET requires four drive switches.

### 2.5 Review of Non-Isolated Topologies for 12V Input VRMs

As it is known, frequency-dependent loss is one of the major barriers to achieve high switching frequency operation, especially in MHz range. Multiphase buck converters are popular for 12V VRMs. Nevertheless, buck converters suffer from extremely low duty cycle, which increases the switching loss (especially during turn off) and the reverse recovery loss of the body diode. More importantly, it has been noticed that the parasitic inductance, especially the common source inductance, has a serious propagation effect during the turn off transition and thus leads the switching loss to increase even higher. Another important frequency-dependent loss is the excessive gate driver losses of the SR MOSFETs that possess high total gate charge [42] for VRM applications above MHz switching frequency. Furthermore, due to the extremely low duty cycle, buck converters have asymmetrical dynamic response during the load transient events. This increases the number of the expensive output capacitors to meet the voltage deviation requirements by the microprocessors.

#### 2.5.1 Limitation of Multiphase VRMs and Duty Cycle Extension

As shown in Figure 2.14, multiphase VRs use interleaving technology to reduce the large output current ripples and then the output voltage ripples. This makes it possible to use small inductances in buck converters to achieve fast transient response. Furthermore, the distribute structure leads to better thermal dissipation evenly. Multiphase VRs have become the most popular solution for low voltage and high current application in today’s VR industry.

In [2], the quasi-square-wave (QSW) buck converters are proposed using the multiphase interleaving technique to achieve zero-voltage switching (ZVS). Nevertheless, the concern of the
QSW converter is that high inductor current ripples result in high RMS value and high conduction loss and also increase the output voltage ripples.

Figure 2.14 Multiphase buck VRs

Figure 2.15 shows the waveforms of current through the control MOSFET $Q_1$ and the voltage across the SR. A buck converter converts 12V to low output voltage (around 1V), so the duty cycle is only around 10%.

The turn-off loss of the control MOSFET can be estimated approximately as

$$P_{\text{turn-off}} = \frac{1}{2} i_{Q1_{\text{pk}}} \cdot V_{in} \cdot t_{\text{off}} \cdot f_s \tag{2.8}$$

where $i_{Q1_{\text{pk}}}$ is the turn off current of the control MOSFET, $V_{in}$ is the input voltage and $t_{\text{off}}$ is the turn-off time.
As seen from Figure 2.15, the extremely small duty cycle results in high turn-off current \( i_{Q1, pk} \) and high reverse block voltage \( V_S \). According to (2.8), this causes high switching loss and high body diode recovery loss. These losses are frequency related, so they degrade the overall efficiency at switching frequency of MHz dramatically.

Additionally, this extremely narrow duty cycle may cause malfunctions at high switching frequency due to short conduction time for the control MOSFET. Furthermore, the extreme duty cycle degrades the effect of the ripple cancellation. Figure 2.16 illustrates the relationship between the ripple cancellation and duty cycle. It is observed that, for a four-phase VR, the current ripple is about 0.7 p.u. at the duty cycle \( D=0.1 \), which is much higher than current ripple of 0.2 p.u. at the duty cycle=0.3. The low duty cycle also deteriorate the dynamic response, especially when the load currents step down.

![Poor ripple cancellation](image)

Figure 2.16 Ripple cancellation effect versus duty cycle

**2.5.2 Transformer-Based Approach**

In order to extent the extreme low duty cycle, a Tapped Inductor (TI) buck converter was proposed in [43] as shown in Figure 2.17. The voltage gain of a TI buck converter is
where the turn ratio $n=(n_1+n_2)/n_1$ and $D$ is the duty cycle of $Q_1$.

\[
\frac{V_o}{V_{in}} = \frac{D}{D + n \cdot (1 - D)}
\]

where the turn ratio $n=(n_1+n_2)/n_1$ and $D$ is the duty cycle of $Q_1$.

Figure 2.17 Tapped inductor buck converter

The turns ratio $n$ introduces an extra degree of design freedom. From (2.9), by modifying the turns ratio $n$, the small duty cycle existing in a conventional buck converter can be extended. Actually, for example, for 12V input voltage and 1.5V output voltage and $n=2$ ($n_1=1$ and $n_2=1$), the duty-cycle is extended to 22%.

However, there are two major drawbacks of a tapped inductor buck converter. First, there is no simple way to drive the control MOSFET $Q_1$, which has a floating source connection. So the simple bootstrap gate driver can not be applied in the TI buck converter. A transformer-isolated or an opto-isolated gate driver is required, either of which will increase the complexity of the original converter. The second and more serious problem is the leakage energy loss, since it is impossible to achieve a perfect coupling effect. All of the energy stored in the leakage inductance will transfer to the small drain-to-source capacitance of $Q_1$, thus causing a huge voltage spike across $Q_1$ and increasing the switching loss and voltage stress of $Q_1$.

The first problem can be solved by modifying the structure of the TI buck converter as shown in Figure 2.18. In this structure, the control MOSFET $Q_1$ and SR $Q_2$ are connected in the same manner as a conventional buck converter. Therefore, the simple bootstrap can be used. However, the coupling between $n_1$ and $n_2$, which makes the secondary problem mentioned above
even worse.

Figure 2.18 Modified structure of a tapped inductor buck converter

In order to solve the voltage spike problem, a tapped inductor buck converter with a lossless clamp circuit was proposed in [43] as shown in Figure 2.19. When \( Q_1 \) is turned off, the current in the leakage inductance goes through clamp capacitor \( C_s \) and \( D_{s1} \) and the leakage inductance energy is stored in \( C_s \). The voltage stress across \( Q_1 \) is then clamped by \( C_s \), which is large enough and the increased voltage of \( C_s \) is relatively small. When \( Q_1 \) is turned on, the extra energy stored in \( C_s \) will be discharged to the output through \( D_{s2} \) and winding \( n_1 \) so that all the leakage energy is entirely recovered to the output.

Figure 2.19 Lossless clamp circuit for a modified TI buck converter

However, the control MOSFET in the proposed tapped inductor buck converter operates under hard-switching condition, which still limits the further increase of the switching frequency.

A non-isolated half bridge (NHB) converter which extends duty cycle using a transformer was proposed in [44]-[46]. Figure 2.20 illustrates the NHB converter with direct energy transfer capability in [44]. Figure 2.21 illustrates the NHB converter proposed in [45]. Comparing with the
conventional half bridge topology, the major advantage of this NHB converters is that part of the output energy can be transferred from the input to the load directly. Therefore, the secondary winding current and inductor current is reduced.

Figure 2.20 Non-isolated half bridge topology

A family of buck-type dc-dc converters including forward, push-pull and half-bridge topologies as shown in Figure 2.22, which take advantages of autotransformers, were proposed in [46]. Similarly, an autotransformer version converter with input current shaper for VRM applications was proposed in [47]. Unfortunately, in the above mentioned topologies, the control power MOSFETs are still under hard-switching condition, which results in high switching loss at high frequencies (>1MHz).
A soft-switching 12V VR, the phase-shift buck (PSB) converter, was proposed in [48] as shown in Figure 2.23. $Q_1$ to $Q_4$ are the primary control switches while $Q_5$ and $Q_6$ are SRs. $Q_1$ and $Q_3$ are controlled out of phase and $Q_2$ and $Q_4$ are controlled out of phase. $Q_1$ and $Q_3$ are phase-shift controlled according to $Q_2$ and $Q_4$ respectively, so that all the control switches can achieve zero-voltage switching. This topology is able to form an autotransformer structure during the power transfer stages, which can reduce the current stress of the transformer windings. Therefore, the efficiency of the PSB converter can be greatly improved at high frequency. Furthermore, by
introducing the matrix-transformer into the PSB converter, a simplified version of the four-phase PSB named matrix-transformer phase-shift buck (MTPSB) converter was also proposed and the number of the active switches can be reduced.

![Phase-shift buck converter](image)

Figure 2.23 Phase-shift buck converter

However, because more active MOSFETs are used in the PSB converter and all control MOSFETs have floating grounds, the gate drive signals become complex and external level-shift drive circuits must be used. In addition, paralleling more power MOSFETs, such as SRs, results in high gate drive losses and makes the SRs a hot spot in the VRM system.

An improved ZVS self-driven 12V VR was proposed in [49]-[50] as shown in Figure 2.24. The driving loss and SR body diode loss are both reduced by using self-driven technique for the SRs. The magnetic integration technique was used to improve the power density and efficiency of the self-driven topology. Different magnetic integration structures are investigated and compared to reduce the leakage inductance of the power transformer [51]-[52].

![ZVS self-driven non-isolated 12V VRM](image)

Figure 2.24 ZVS self-driven non-isolated 12V VRM
Similar to the PSB converter in Figure 2.23, all the four control MOSFETs have floating grounds in this self-driven VR in Figure 2.24. Though a simple level-shift drive scheme is used, the drive path of the control MOSFETs goes though the SR MOSFET, which increases the parasitic inductance, especially the common source inductance. This may result in high turn off loss. Additionally, the drain-to-source voltage oscillation of the SR MOSFETs, due to the reverse recovery of the body diode, may cause high voltage spikes over the control MOSFETs.

A non-isolated full-bridge (NFB) topology with direct energy transfer capability was proposed in [53]-[54]. The NFB converter is illustrated in Figure 2.25. The two-phase version of the NFB converters with the sharing bridge leg was reported in [55]. Due to direct energy transfer capability, the current stresses of the transformer windings and the power MOSFETs are reduced. In this NFB topology, traditional phase-shift control is applied and auxiliary transformer windings are used to drive the SR MOSFETs. The disadvantage of using the drive transformer self-driven scheme is that the leakage inductance causes the propagation delay of the SR drive signals, which results in a high conduction loss of the body diode.

![Figure 2.25 Non-isolated full bridge topology](image)

Generally, the transformer-based topologies can significantly reduce the switching loss, which is usually dominant loss in a buck converter at MHz switching frequency range. However, high frequency and high current power transformer design is a challenging work.


2.5.3 Two-Stage Approach

Another solution to extend the narrow duty cycle is two-stage approach as illustrated in Figure 2.26 [56]-[57].

![Diagram of Two-stage approach for 12V VRM](image)

Two-stage approach connects two buck converters in cascade. The first-stage buck converter converts 12V to 5V and operates at 500 KHz to achieve simplicity and high efficiency. The point of the two-stage approach is to realize ultra-high frequency for the second stage. The optimized intermediate bus voltage of 5V feed the second-stage multiphase buck converters with 2 MHz switching frequency per phase. Because the input voltage of the second-stage is 5V, the switching loss and the conduction loss can be greatly reduced as compared with 12V input voltage.

The issue of the two-stage approach is how to optimize the conversion efficiency since it is a cascade system. More power switches and passive components in two converters may also lead to an overall cost increase. Also, additional design efforts are required for the control design of the two power stages approach.

2.6 Conclusion

In this chapter, starting from the introduction of the loss distribution of a high frequency VRM, the frequency-depend losses are emphasized since they are one of the major barriers to push the switching frequency of VRMs beyond MHz. In order to achieve high efficiency and high power density, these losses should be minimized.

Gate drive loss becomes a concern when the switching frequency approaches MHz and so
resonant gate driver technique was proposed to recover some of the gate drive loss. However, with the development of power MOSFET technology in recent years, the gate drive loss is reduced. Therefore, the benefit of resonant gate drive circuits is diminishing. On the other hand, at 1MHz operation, the switching loss becomes the dominant one. Therefore, it is important to reduce the switching loss in order to boost the efficiency of VRMs.

Nevertheless, the parasitic inductance, especially, the common source inductance, severely increases the switching transition time and thus switching loss as a result. The conventional voltage drive can hardly provide strong drive current since the induced voltage over the parasitic inductance is always against the drive voltage. Therefore, new drive techniques are desired to solve the problem caused by the parasitic inductance.

The review of these driver circuits provides the basic background information for the analytical loss modeling of a power MOSFET with a CSD in Chapter 3 and new CSD topologies in Chapter 4 and Chapter 5.

Buck converters suffer from extremely low duty-cycle problem when the output voltage is around 1.0V-1.5V, and the problem will become worse when the output voltage is sub 1V. In terms of efficiency, the low duty cycle causes high turn-off loss due to the parasitics. It also degrades the dynamic response of VRMs and increases the number of the output capacitors. In order to extend extremely low duty cycle, different non-isolated topologies are analyzed focusing on the advantages and disadvantages. Unfortunately, these topologies have certain problems and need to be improved for the operation of several MHz switching frequency as mentioned in section 2.5. Therefore, in order to improve the performance of VRMs and meet the strict requirement of future microprocessors, new topologies need to be proposed.

The review of these non-isolated topologies provides the basic background information for focusing on exploring innovative VRM topologies at high switching frequency in Chapter 6.
3.1 Introduction

In the previous chapter, CSD technique is reviewed comprehensively. Unfortunately, most of work done on CSD technique is concentrating on the circuit topology. Several other important issues still need to be explored. Firstly, the impact of the parasitic inductance on the CSDs has not been investigated analytically and the switching behavior of a power MOSFET with a CSD has not been studied. Secondly, the potential switching loss saving by a CSD considering the parasitic inductance at high (≥1MHz) frequency over a conventional voltage driver is not addressed clearly. Thirdly, the optimal design method of a CSD needs to be proposed to achieve maximum efficiency improvement for a synchronous buck converter. The objective of this chapter is to propose a loss model for optimal design.

In section 3.2, the analytical loss model for the CSD is derived in details. In section 3.3, the analytical modeling and simulation results are presented. In section 3.4, the CSD under investigation is introduced. In section 3.5, the proposed optimal design method based on the analytical loss model is presented. In section 3.6, the hardware implementation is presented. Experimental results and efficiency comparison to other state of the art VRM approaches are provided in section 3.7. The conclusions are given in section 3.8.

† The content of this chapter has been published in the following journals:
3.2 Proposed MOSFET Loss Model with CSD

The MOSFET switching loss models can be classified into (1) a physical-based model using physical parameters of the device; (2) a behaviour model provided by device vendor supplies; (3) an analytical model (also called a mathematical model). The physical-based model and the behaviour model are convenient using simulation software, but it is time consuming to use simulation to achieve the optimal design. It should be stressed that the piecewise loss model by linearizing the switching waveforms is no longer valid due to the parasitic inductance at high frequency. Therefore, we need a new analytical MOSFET loss model to predict the optimal design solution for a CSD.

3.2.1 Circuit and Basic Assumption

The circuit with clamped inductive load, as shown in Figure 3.1, is used to illustrate the MOSFET switching behavior. In Figure 3.1, $D_1$ is the anti-parallel diode and $V_D$ is the supply voltage. The equivalent circuit for the switching transition is shown in Figure 3.2, where MOSFET $M_1$ is represented with a typical capacitance model, the clamped inductive load is replaced by a constant current source and the CSD is simplified as a current source ($I_G$) since the charge and discharge current is kept constant during the switching transition. $L_D$ is the switching loop inductance including the packaging inductance and any unclamped portion of the load inductance. $L_S$ is the common source inductance, which is shared by the main current path and the gate driver loop. The critical MOSFET parameters are as follows: 1) the gate-to-source capacitance $C_{GS}$, the gate-to-drain capacitance $C_{GD}$ and the drain-to-source capacitance $C_{DS}$; 2) the gate equivalent series resistance (ESR) $R_G$ (external and internal); 3) the threshold voltage $V_{th}$; 4) transconductance $g_\beta$. 
For purpose of transient analysis, we make the following assumptions:

(1) $i_D=g_f(v_{GS}-V_{th})$ and MOSFET is ACTIVE, provided $v_{GS}>V_{th}$ and $v_{DS}>i_D R_{DS(on)}$;

(2) For $v_{GS}<V_{th}$, $i_D=0$, and MOSFET is OFF;

(3) When $g_f(v_{GS}-V_{th})>v_{DS}/R_{DS(on)}$, the MOSFET is fully ON.

### 3.2.2 Analytical Modeling of Switching Transition

During the switching transition period, the MOSFET enters its active state and the linear transfer characteristics is assumed as given in (3.1) [58], where $i_D(t)$ is the instantaneous switching current and $v_{GS}(t)$ is the instantaneous gate-to-source voltage of the MOSFET:

$$i_D(t) = g_f(v_{GS}(t) - V_{th})$$  \hspace{1cm} (3.1)

According the equivalent circuit in Figure 3.2, the circuit equations take the form

$$I_G = C_{GD} \frac{dv_{GD}}{dt} + C_{GS} \frac{dv_{GS}}{dt}$$  \hspace{1cm} (3.2)

and
\[ v_{GD} = v_{GS} - v_{DS} \]  

(3.3)

So

\[ I_G = (C_{GS} + C_{GD}) \frac{dv_{GS}}{dt} - C_{GD} \frac{dv_{DS}}{dt} \]  

(3.4)

From (3.4), \( \frac{dv_{DS}}{dt} \) is solved as

\[ \frac{dv_{DS}}{dt} = \frac{C_{GS} + C_{GD}}{C_{GD}} \frac{dv_{GS}}{dt} - \frac{I_G}{C_{GD}} \]  

(3.5)

So \( \frac{d^2v_{DS}}{dt^2} \) and \( \frac{d^3v_{DS}}{dt^3} \) are respectively

\[ \frac{d^2v_{DS}}{dt^2} = \frac{C_{GS} + C_{GD}}{C_{GD}} \frac{d^2v_{GS}}{dt^2} \]  

(3.6)

\[ \frac{d^3v_{DS}}{dt^3} = \frac{C_{GS} + C_{GD}}{C_{GD}} \frac{d^3v_{GS}}{dt^3} \]  

(3.7)

During the switching interval, the change of the switching loop current \( i_{DL} \) induces a voltage across the parasitic inductance. The drain-to-source voltage \( v_{DS} \) is given as

\[ v_{DS} = V_D - L_D \frac{di_{DL}}{dt} - L_s \frac{d(i_{DL} + I_G)}{dt} = V_D - (L_D + L_s) \frac{di_{DL}}{dt} \]  

(3.8)

And

\[ i_{DL} = C_{GS} \frac{dv_{GS}}{dt} + C_{DS} \frac{dv_{DS}}{dt} + g \left( v_{GS} - V_{th} \right) - I_G \]  

(3.9)

Substituting (3.9) to (3.8) yields

\[ v_{DS} = V_D - (L_D + L_s)(C_{GS} \frac{d^2v_{GS}}{dt^2} + C_{DS} \frac{d^2v_{DS}}{dt^2} + g \left( v_{GS} - V_{th} \right)) \]  

(3.10)

Substituting (3.6) to (3.10) yields

\[ v_{DS} = V_D - (L_D + L_s)\left( \frac{C_{GS}C_{GD}}{C_{GD}} + C_{DS}C_{GD} + C_{DS}C_{GS} \frac{d^2v_{GS}}{dt^2} + g \frac{dv_{GS}}{dt} \right) \]  

(3.11)

Differentiating (3.11) yields
\[
\frac{dv_{DS}}{dt} = -(L_D + L_s)(C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS}) \cdot \frac{d^3v_{GS}}{dt^3} + g_f \cdot \frac{d^2v_{GS}}{dt^2}
\]  
(3.12)

Substituting (3.5) into (3.12), (3.13) is derived

\[
A \frac{d^3v_{GS}(t)}{dt^3} + B \frac{d^2v_{GS}(t)}{dt^2} + C \frac{dv_{GS}(t)}{dt} = I_G
\]  
(3.13)

where parameters \(A, B\) and \(C\) are represented in terms of the device parameters \((C_{GS}, C_{GD}, C_{DS}, g_f\) and \(R_G)\) and the equivalent circuit parameters \((L_D\) and \(L_S)\) as

\[
A = (L_D + L_s)(C_{GS}C_{GD} + C_{DS}C_{GD} + C_{DS}C_{GS}), \quad B = g_f(L_D + L_s)C_{GD} \quad \text{and} \quad C = C_{GS} + C_{GD}.
\]

For turn-on transition, the initial condition for (3.13) is \(v_{GS}(0) = V_{th}\). Then (3.13) solves to give either sinusoidal or exponential solutions, depending on the relative magnitudes of \(B^2\) and \(AC\).

When \(B^2 - 4AC < 0\), sinusoidal solution occurs and \(v_{GS}(t)\) takes the form:

\[
v_{GS}(t) = \left(\frac{B^2}{2C^2} - \sqrt{\frac{4AC - B^2}{2C^2}}\right)I_G \cdot \exp\left(-\frac{t}{T_1}\right) \cdot \sin(\omega t)
\]  
(3.14)

\[
+ \frac{B}{C^2}I_G \cdot \exp\left(-\frac{t}{T_2}\right) \cdot \cos(\omega t) + \frac{I_G \cdot t}{C} - \frac{B}{C} \cdot I_G + V_{th}
\]

where \(T_1 = \frac{2A}{B}\), \(\omega h = \sqrt{\frac{4AC - B^2}{2A}}\).

When \(B^2 - 4AC > 0\), exponential solution occurs. Then \(v_{GS}(t)\) takes the form

\[
v_{GS}(t) = \frac{(\sqrt{B^2 - 4AC} + B) \cdot I_G \cdot A \cdot \exp\left(-\frac{t}{T_2}\right)}{(\sqrt{B^2 - 4AC} - B) \cdot C \cdot \sqrt{B^2 - 4AC}} + \frac{(\sqrt{B^2 - 4AC} - B) \cdot I_G \cdot A \cdot \exp\left(-\frac{t}{T_3}\right)}{(\sqrt{B^2 - 4AC} + B) \cdot C \cdot \sqrt{B^2 - 4AC}}
\]  
(3.15)

\[
+ \frac{I_G \cdot t}{C} - \frac{B \cdot I_G}{C^2} + V_{th},
\]

where \(T_2 = \frac{2A}{B - \sqrt{B^2 - 4AC}}\) and \(T_3 = \frac{2A}{B + \sqrt{B^2 - 4AC}}\).

Then, by substituting \(v_{GS}(t)\) to (3.1) and (3.11), \(i_D(t)\) and \(v_{DS}(t)\) of the MOSFET can be calculated respectively. Therefore, the turn on loss is
The turn-off transition is similar to the turn-on transition except for the initial condition becomes $v_{GS}(0) = V_{th} + \frac{I_L}{g_{fs}}$. The turn off loss is

$$P_{\text{turn-off}} = \int_{0}^{t_{\text{on}} - t_{\text{off}}} v_{DS}(t) \cdot i_D(t) dt \cdot f_s$$

(3.17)

From (3.16) and (3.17), the switching loss is

$$P_{\text{switching}} = P_{\text{turn-off}} + P_{\text{turn-on}}$$

(3.18)

### 3.3 Analytical Modeling and Simulation Results

The modeling results in section 3.2 are presented in this section. The turn-on and turn-off transition are divided into several intervals, during which the gate-to-source voltage $v_{GS}(t)$, the drain current $i_D(t)$ and the drain voltage $v_{DS}(t)$ can be calculated analytically with corresponding boundary conditions and constraints. Once the instantaneous waveforms of $v_{GS}(t)$, $i_D(t)$ and $v_{DS}(t)$ are solved, the switching transition time and the switching loss can be easily obtained from (3.18).

In the experimental prototype, MOSFET Si7860 from Vishay is used and the circuit specifications and the device parameters are listed in Table 3.1. In this case, since $B^2$ is more than 4AC depending on the above parameters, the exponential solution occurs as (3.15).

**Table 3.1 Circuit Specifications and Device Parameters in Analytical Modeling**

<table>
<thead>
<tr>
<th>$C_{GS}$ (pF)</th>
<th>$C_{GD}$ (pF)</th>
<th>$C_{DS}$ (pF)</th>
<th>$V_{th}$ (V)</th>
<th>$g_{fs}$ (S)</th>
<th>$R_G$: current driven (Ω)</th>
<th>$R_G$: voltage driven (Ω) (include driver resistance)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1600</td>
<td>200</td>
<td>500</td>
<td>1.8</td>
<td>60</td>
<td>1</td>
<td>1.5 ohm</td>
</tr>
</tbody>
</table>

$V_o=12V$, $I_I=20A$, $f_f=1MHz$

Figure 3.3 illustrates the calculated turn-on waveforms and turn-off waveforms. The turn-on and turn-off instantaneous loss are shown in black curves by integrating the drain current $i_D(t)$ and drain voltage $v_{DS}(t)$. 41
Figure 3.3 Calculated waveforms of $v_{GS}$, $v_{DS}$, $i_D$ and $p_{loss}$

Figure 3.4 shows the switching loss comparison between the above model using Mathcad software and the simulation results using Vishay Si7860AD SPICE model. It should be pointed out that the switching loss is related to the equivalent circuit in Figure 3.2 other than the buck converter. It is noted that the modeling results are in good agreement with the simulation results. The advantage of the proposed switching loss model is that it provides the physics and the detailed voltage and current information for the optimal design. However, the SPICE model is convenient for simulation software while it is difficult to use the SPICE model to achieve the optimal design.

Figure 3.4 Switching loss comparison between modeling and simulation

In order to compare the voltage source driver to the CSD with the parasitic inductances,
Figure 3.5 shows the circuit diagram of the power MOFSET with the conventional voltage source gate driver for simulation. Figure 3.6 illustrates the simulation waveforms of turn-on transition comparison between of the CSD and conventional voltage source driver with the same parasitic inductance of $L_s=1\text{nH}$, $L_D=2\text{nH}$ and circuit parameters. It is observed that the turn-on transition time of the CSD is reduced to 2.3ns [see Figure 3.6 (a)] compared to 12.2ns [see Figure 3.6 (b)] of the voltage driver (a reduction of 81%). The turn-on loss is reduced from 0.65W to 0.1W (a reduction of 84.6%).

![Circuit Diagram](image)

**Figure 3.5** The power MOFET with Conventional voltage source gate driver and the parasitic inductance
Figure 3.6 Simulation comparison of turn-on transition between the CSD and voltage source driver: the gate-to-source voltage $v_{GS}$, the drain-to-source voltage $v_{DS}$ and the drain current $i_D$ ($V_{in}=12V$, $I_o=20A$, $f_s=1MHz$, $L_s=1nH$, $L_D=2nH$, $R_G=1.5ohm$ and $V_{cc}=6V$)

Similarly, Figure 3.7 illustrates the simulation waveforms of turn-off transition comparison. The turn-off transition time of the CSD is reduced to 5ns [see Figure 3.7 (a)] compared to 13.4ns [see Figure 3.7 (b)] of the voltage driver (a reduction of 62%). The turn-off loss is reduced 2.1W to 1.16W (a reduction of 44.8%). So the total switching loss saving is 1.49W (a reduction of 54.2%).

Figure 3.7 Simulation comparison of turn-off transition between the CSD and voltage source driver: the gate-to-source voltage $v_{GS}$, the drain-to-source voltage $v_{DS}$ and the drain current $i_D$ ($V_{in}=12V$, $I_o=20A$, $f_s=1MHz$, $L_s=1nH$, $L_D=2nH$, $R_G=1.5ohm$ and $V_{cc}=6V$)
It is noted that the common source inductance has a negative impact on the switching transition of the voltage source driver. Figure 3.8 shows the gate charge current during the turn-on transition and turn-off transition with the voltage source driver respectively when the common source inductance is not zero.

It is observed from Figure 3.8(a) that during turn-on transition, before the actual gate-to-source voltage $v_{GS}$ reaches the miller plateau voltage, the drain current $i_d$ still remain zero and the gate charging current is about 3A. However, as soon as $i_d$ starts to rise, the induced voltage $v_{Ls}$ ($v_{Ls}=L_s \cdot \frac{di_d}{dt}$) over the common source inductance $L_s$ occurs due to the rise of the drain current, which is against the gate drive voltage $v_{GS'}$. Since $v_{GS'}= v_{GS}-L_s \cdot \frac{di_d}{dt}$, the actual gate-to-source voltage $v_{GS}$ is reduced. As a result, the gate charging current $i_G$ is reduced to as low as 10mA, which increases the turn-on transition time and turn-on loss dramatically.
It is observed from Figure 3.8(b) that during turn-off transition, before the actual gate-to-source voltage $v_{GS}$ declines to the miller plateau voltage, the drain current $i_d$ still remains as the load current and the gate discharging current is around 3A. But, as soon as the drain current begins to decrease, the induced voltage $v_{Ls}$ over $L_s$ occurs, which is also against the gate drive voltage. This also results in the reduction of the gate discharging current to as low as 15mA and
thus increases the turn-off transition time and the turn-off loss as a result.

As a conclusion, for both of the turn-on transition and turn-off transition, $v_{Ls}$ induced over the common source inductance is always against the gate drive voltage $v_{GS}$, and thus decreases the actual gate-to-source voltage $v_{GS}$ and the gate charge current $i_G$, which consequently slows down the turn-on speed and turn-off speed of the MOSFET and increases the switching transition time and switching loss dramatically.

However, as for a CSD, the great advantage is that the common source inductance is absorbed by the current-source inductor to ensure the constant gate drive current during the switching transition. Therefore, the propagation impact of the common source inductance on the switching transition is eliminated, which leads to a significant reduction of the switching time and switching loss.

Figure 3.9 illustrates the comparison of the turn-on and turn-off loss as a function of the common source inductance on the basis of the above analytical loss model. With today’s MOSFET packaging and compact PCB layout, the parasitic inductance is usually less than 2nH. It is observed that with the CSD, the common source inductance $L_s$ does not increase the switching loss of the MOSFET. Therefore, the CSD reduces the switching loss compared to the conventional voltage source driver.
3.4 The CSD Under Investigation

Figure 3.10 shows the CSD under investigation, which is proposed in [3]. The design of the CSD is optimized for a 12V input buck converter operating at 1MHz switching frequency using the proposed method.

![Synchronous buck converter with the proposed CSD](image)

Figure 3.10 Synchronous buck converter with the proposed CSD

Figure 3.11 shows the key waveforms. In Figure 3.11, the gate-to-source signals of $Q_1$ and
\( Q_2 \) have a small crossover level, which is less than the threshold voltage of the devices, to minimize the dead time and to reduce the conduction loss and reverse recovery of the body diode. It should also be pointed that an additional margin should be set for this crossover level according to the threshold voltage at high temperature, which reduces with temperature increasing.

![Image of key waveforms]

**Figure 3.11 Key waveforms**

The advantages of this drive circuit are highlighted as follows: 1) fast switching of the power MOSFET, which reduces the switching time and the switching loss greatly; 2) gate energy recovery; 3) reduced dead time; 4) zero-voltage-switching (ZVS) of the drive switches (\( S_1-S_4 \)); 5) high \( Cdv/dt \) immunity.

More importantly, it should be pointed that the CSD is a most cost-effective approach to increase the efficiency at high frequency based on today’s multiphase buck VRMs. The proposed loss model will be used to optimize the design in the following section.

### 3.5 Proposed Optimization Method

As observed from the waveforms in Figure 3.11, the peak current \( I_{Lr.pk} \) of the current-source inductor \( L_r \) is regarded as the current source magnitude \( I_G \). So the higher \( I_{Lr.pk} \) is, the larger
charge/discharge current, the shorter of switching transition is, thus more switching loss can be reduced. On the other hand, higher $I_{Lr_{pk}}$ will result in a larger RMS value of the inductor circulating current $i_{Lr}$ since the waveform of $i_{Lr}$ is triangular, which increases the resistive circulating loss in the drive circuit and decreases the gate energy recovery efficiency. Therefore it is critical to decide $I_{Lr_{pk}}$ (i.e., $I_G$) properly so that the maximum loss saving can be achieved.

The general method proposed here is to find the optimal solution on the basis of the object function that is the sum of the switching loss and CSD circuit loss. The object function should be a U-shape curve as function of the drive current $I_G$, and the optimization solution is simply located at the lowest point of the curve. When the optimal $I_G$ value is decided, the currents-source inductor $L_r$ can be calculated base the switching frequency and duty cycle. It is noted that the analytical loss model proposed in section 3.2 is used to calculate the switching loss since the piecewise loss model is no longer valid due to the parasitic inductance at high frequency. The specifications are: $V_{in}$=12V; $V_o$=1.5V; $I_o$=30A; $V_c$=8V; $f_s$=1MHz; $Q_1$: Si7860DP; $Q_2$: Si7336ADP and $L_f$=300nH.

First, the switching loss of the control MOSFET should be calculated. Using (3.16) for the turn-on loss and (3.17) for the turn-off loss, the total switching loss as function of drive current $I_G$ is

$$P_{switching_{Q1}} = \int_{0}^{t_{sw(on)_{Q1}}} v_{ds(on)_{Q1}} \cdot i_{on}dt \cdot f_s + \int_{0}^{t_{sw(off)_{Q1}}} v_{ds(off)_{Q1}} \cdot i_{off}dt \cdot f_s$$

where $v_{ds(on)_{Q1}}$ and $v_{ds(off)_{Q1}}$ are the drain-to-source voltages during turn-on interval and turn-off interval respectively; $i_{on}_{Q1}$ and $i_{off}_{Q1}$ are the drain currents at turn-on interval and turn-off interval with the inductor current ripples respectively; $t_{sw(on)_{Q1}}$ is the turn-on switching transition time and $t_{sw(off)_{Q1}}$ is the turn-off switching transition time. Figure 3.12 illustrates the switching loss $P_{switching_{Q1}}$ as function of drive current $I_G$. It is observed that the switching loss reduces when
$I_G$ increases.

Secondly, the loss of the CSD circuit should be calculated. The loss of the CSD includes: 1) the resistive loss and gate drive loss of switches $S_1$-$S_4$; 2) the loss of the current-source inductor; 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs.

The inductor current waveform indicated in Figure 3.11 can be regarded as a triangular waveform since the charging/ discharging time $[t_0, t_2]$ and $[t_3, t_5]$ are small and can be neglected. Therefore, the RMS value of the inductor current $I_{Lr,RMS}$ is $I_{Lr, pk} / \sqrt{3}$.

The RMS currents flowing through the switches $S_1$ and $S_4$ are

$$I_{s1,RMS} = I_{s4,RMS} = I_{Lr, pk} \cdot \frac{\sqrt{D}}{3} \quad (3.20)$$

The RMS currents flowing through switches $S_2$ and $S_3$ are

$$I_{s2,RMS} = I_{s3,RMS} = I_{Lr, pk} \cdot \frac{1 - D}{3} \quad (3.21)$$

The conduction loss of $S_1$-$S_4$ are...
\[ P_{\text{cond}_{\text{s1-s4}}} = \frac{2}{3} I_{\text{Lr}_{\text{rms}}}^2 \cdot R_{\text{ds(on)}} + \frac{2}{3} I_{\text{Lr}_{\text{rms}}}^2 \cdot R_{\text{ds(on)}} \tag{3.22} \]

where \( R_{\text{ds(on)}} \) is the on-resistance of \( S_1-S_4 \), assuming \( S_1-S_4 \) are same.

Substituting (3.20) and (3.21) yields

\[ P_{\text{cond}} = \frac{2}{3} I_{\text{Lr}_{\text{pk}}}^2 \cdot R_{\text{ds(on)}} \tag{3.23} \]

which is dependent on inductor peak current only and is independent of duty cycle.

DC resistance of the inductor winding cannot be used here to directly calculate its copper loss because of the high operation frequency. Skin-effect has to be considered. The copper loss of the inductor winding is

\[ P_{\text{copper}} = R_{\text{ac}} \cdot I_{\text{Lr}_{\text{rms}}}^2 \tag{3.24} \]

where \( R_{\text{ac}} \) is the AC resistance of the inductor winding and \( I_{\text{Lr}_{\text{rms}}} \) is the RMS value of the inductor current. Core loss of the inductor is another loss in this CSD circuit. The core loss \( P_{\text{core}} \) depends upon the inductor design. Core materials with high permeability such as 3F5 or PC50 can be used to reduce core loss. The total inductor loss is:

\[ P_{\text{ind}} = P_{\text{copper}} + P_{\text{core}} \tag{3.25} \]

Both the charge and discharge currents flow through the internal gate mesh resistance \( R_G \) of the power MOSFET and cause resistive loss. The charge and discharge current is the peak value of the inductor current. Thus the total loss caused by the internal resistance of two power MOSFETs during turn-on and turn-off is

\[ P_{\text{RG}} = 2R_{\text{G1}}I_{\text{Lr}_{\text{pk}}}^2 \cdot t_{\text{sw1}} \cdot f_s + 2R_{\text{G2}}I_{\text{Lr}_{\text{pk}}}^2 \cdot t_{\text{sw2}} \cdot f_s \tag{3.26} \]

where \( t_{\text{sw1}} \) and \( t_{\text{sw2}} \) are the switching time of MOSFET \( Q_1 \) and \( Q_2 \) respectively; \( R_{\text{G1}} \) and \( R_{\text{G2}} \) are the internal gate resistors of \( Q_1 \) and \( Q_2 \) respectively.

Since the switching frequency of these four switches is the same as the switching frequency of the control MOSFET, the gate drive loss of \( S_1-S_4 \) is

52
\[ P_{\text{gate}} = 4 \cdot Q_{g,s} \cdot V_{gs,s} \cdot f_s \]  
(3.27)

where \( Q_{g,s} \) is the total gate charge of a switch and \( V_{gs,s} \) is the drive voltage of the switch, which is usually 5V.

Therefore, the total loss of the CSD circuit can is

\[ P_{\text{CSD}} = P_{\text{cond}} + P_{\text{gate}} + P_{\text{ind}} + P_{BG} \]  
(3.28)

Using (3.28), Figure 3.13 illustrates the loss of the CSD circuit \( P_{\text{CSD}}(I_G) \) as function of drive current \( I_G \) is given, illustrating that the CSD drive circuit loss increases when \( I_G \) increases.

Figure 3.13 CSD circuit \( P_{\text{CSD}}(I_G) \) as function of gate drive current \( I_G \)

Thirdly, in order to find the optimized gate drive current, the objective function is established by adding the switching loss in (3.19) and the CSD circuit loss in (3.28) as

\[ F(I_G) = P_{\text{CSD}}(I_G) + P_{\text{switching-QI}}(I_G) \]  
(3.29)

Figure 3.14 illustrates the objective function \( F(I_G) \) with the drive current \( I_G \), which is a U-shaped curve. Therefore, the optimization solution can be found at the lowest point of the curve, and accordingly, the gate drive current \( I_G \) is chosen as 1.2A. It is noted that the bottom of the U-shape is flat. In other words, when \( I_G \) changes from 1A to 2A, the power loss does not change.
much.

Finally, from the selected gate drive current, the calculated inductor value from (3.30) is 1.5uH

\[
L_c = \frac{(V_{in} + 2V_c) \cdot D \cdot (1 - D)}{2 \cdot I_G \cdot f_s}
\]  

(3.30)

where \(V_{in}=12\text{V}, f_s=1\text{MHz}, V_o=1.5\text{V}, V_c=8\text{V}\) and \(I_G=1.2\text{A}\).

Figure 3.15 illustrates the loss breakdown comparison based on the analytical loss model between the above optimized CSD and conventional diver. At \(V_o=1.5\text{V}\) and \(I_o=20\text{A}\), the turn-on loss is reduced by 0.55W and the turn-off loss is reduced by 0.94W. The total loss reduction is 1.66W, which is 5.5%, 1.66W/(1.5V×20A), of the output power. This loss saving will translate into a great efficiency improvement of 2.6% over the conventional voltage driver. Furthermore, for five-phase buck VRs to provide 100A, the total loss reduction comes to 8.3W (1.66W×5).
Figure 3.15 Loss breakdown between the CSD and conventional voltage driver ($V_{in}=12V$, $V_o=1.5V$ and $I_o=20A$)

Figure 3.16 shows the loss comparison between the CSD and the voltage source driver as function of the switching frequency based on the above circuit parameters. It is interesting to observe that as long as the switching frequency is above 252KHz, the loss of the CSD is always lower than that of the voltage source driver, which means that the CSD can always achieve loss saving over the voltage source driver. The higher switching frequency, the more loss saving is achieved. However, when the switching frequency is lower than 252KHz, the loss of the CSD is higher than that of the voltage source driver. The reason is that though the frequency-dependent loss is reduced, it is offset by the circulating loss of the CSD circuit itself, which means the CSD can not achieve the loss saving when the switching frequency is below 252KHz.
3.6 Hardware Implementation

3.6.1 Bootstrap and Level-shift Circuit

From the viewpoint of a standard gate driver for a synchronous buck converter, the control PWM signal is the input of the driver and two complimentary gate drive signals with minimum dead time are the output of the driver. Therefore, all the control signals for the four switches (S₁-S₄) in the CSD circuit should be generated based on the input PWM signal. As observed from Figure 3.10, since the switches S₁-S₃ (N-channel) have the floating source and do not share the same ground with switch S₄, the bootstrap gate drive technique need to be used in the control circuit. It should be noted that if switches S₁ and S₃ are P-channel MOSFETs with a little bit higher $R_{DS(on)}$, only one set of level shift circuit is required for the whole drive circuit. In the thesis, N channel MOSFET is used.

A double pulse level shift circuit is used as shown in Figure 3.17. It is noted that in order to maintain high efficiency and to minimize power dissipation; the level shifters should not draw...
any current during the on-time of the control switch.

Figure 3.17 Schematic of the level-shift drive circuit

As indicated in Figure 3.17, the input PWM signal are fed to the CPLD and is translated to ON and OFF commands as two short pulses at the rising and the falling edges with certain delay time. Through the pulse filter, these two pulses drive the level shift transistor pair which interfaces with the level-shifted circuitry. This operation leads to lower power dissipation because of the short duration of the current in the level shifter. Then these two level-shifted signals are fed into an SR latch to generate the level-shifted PWM gate signal. Finally, the level-shifted PWM signal goes to the bipolar totem-pole circuit to drive the switches (S1-S3) in the CSD. In addition to the drive signal level-shifter, the bootstrap circuit also includes a bootstrap diode and bootstrap capacitor to provide the supply voltage for the level-shift circuit.

3.6.2 CPLD Implementation

The four control signals should be generated based on the PWM signal and the delayed circuit should be used to give the proper delay time between two complimentary signals, i.e., S1 and S3, S2 and S4 as seen from Figure 3.11. As the turn-on transition time and turn-off transition time are small, around 10ns, it is important to adjust the dead time precisely. Usually, RC delay circuit is popular to achieve the delay function due to its simplicity, but the drawback of RC delay
is difficult to adjust the time accurately and conveniently due to the tolerance of the resister and
the capacitor. Delay line such as Maxim DS1100 [59] is another option to achieve the delay, but
it is difficult to do the component replacement and modification once the PCB is completed. The
CPLD MAX II from Altera is used to achieve the programmable delay function and generate the
desired the control signals. Therefore, the delay time of the control signals can be adjusted
precisely and conveniently.

Figure 3.18 shows the schematic of the digital circuit in Quartus II software. The basic idea
is presented as follows. First, the rising edge of the input PWM signal is used to enable one
counter chain. The falling edge of the input PWM signal is used to enable the other counter chain.
When the first chain times out, a single pulse is generated to set an SR latch and reset that chain
meanwhile. When the second chain times out, a single pulse is generated to set an SR latch and
reset that chain. Then, the output of the latch will be the delayed version of the input PWM signal
if the two counter chains have the same delay. On the other hand, by setting the different delay
time of the two counters, the output of the latch will be the PWM signal with the desired width
and delay time. In the implementation, the delayed rising/ falling pulses are directly sent to the
level-shift circuit because the SR latch has been included in the level-shift circuit as shown in
Figure 3.17.
The asynchronous counter clock based on a ring oscillator is used here as shown in Figure 3.19. The PWM rising edge is used to trigger the asynchronous counter to generate the counter clock signal. The clock period in the experimental hardware is set to 3ns, which equals the resolution of the dead time.

3.7 Experimental Verification and Discussion

A 1MHz synchronous buck converter with the CSD was built to verify the modeling results and demonstrate the advantages. The specifications are as follows: input voltage $V_{in}=12V$; output
voltage $V_o = 1.5V$; output current $I_o = 30A$; switching frequency $f_s = 1MHz$; CSD voltage $V_c = 8V$. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows:

Control MOSFET $Q_1$: Si7860DP (30V N-channel, $R_{DS(on)} = 11m\Omega @ V_{GS} = 4.5V$, Vishay)

SR $Q_2$: Si7336ADP (30V N-channel, $R_{DS(on)} = 4m\Omega @ V_{GS} = 4.5V$, Vishay)

Drive switches $S_1-S_4$: FDN335N (20V N-channel, $R_{DS(on)} = 70m\Omega @ V_{GS} = 4.5V$, Fairchild)

Output filter inductance: $L_f = 330nH$ (R = 1.3mohm, IHLP-5050CE-01, Vishay)

Current source inductor: $L_r = 1.5uH$.

Figure 3.20 shows the gate drive signal $v_{gsQ_1}$ of $Q_1$ and $v_{gsQ_2}$ of $Q_2$. The crossover level of these two gate signals is less than the threshold voltage of the switches so that the dead time can be minimized and the shoot-through can be avoided. It is observed that $v_{gsQ_1}$ is smooth and the miller plateau is less than 5ns due to the constant charging current. Moreover, the rise time and fall time of $v_{gsQ_1}$ is less than 15ns, which indicates the gate charging time is significantly reduced compare to the conventional voltage driver.

![Figure 3.20 Waveforms of the gate signals $v_{gsQ_1}$(control MOSFET) and $v_{gsQ_2}$(SR)
Figure 3.21 shows the drain-source voltage $v_{ds,Q2}$ and the gate signal $v_{gs,Q2}$ of the SR. It can be seen from $v_{ds,Q2}$ that the body diode conduction time is small, which reduces the conduction loss and the reverse recovery loss of the body diode.

Figure 3.21 Waveforms of the drain-source voltage $v_{ds,Q2}$ and the gate signal $v_{gs,Q2}$ (SR)

Figure 3.22 shows the gate drive current $i_g$ and the gate signal $v_{gs,Q2}$ of the SR MOSFET. It is noted that the gate drive current keeps constant during the switching interval disregarding the current oscillations. Because the extra wire length is used to allow the insertion of a current probe to measure the current waveforms, this introduces higher stray inductances, which causes the parasitic oscillations of the current waveform at high frequency.

Figure 3.23 shows the current-source inductor current $i_{Lr}$ and its peak current value is 1.2A, which is the optimized value of the drive current.
In order to illustrate efficiency improvement by the CSD, a benchmark of a synchronous buck converter with the conventional gate driver was built. A Predictive Gate Drive UCC 27222 from Texas Instruments [18] was used as the conventional voltage driver.

In the efficiency measurement, a DC power supply (Agilent 6552A) fed the buck converter with 12V input voltage. Through measuring the input voltage and input current, the input power $P_{in}$ is obtained. The buck converter output fed a DC electronic load (Agilent N330/A). Through
measuring the output current and voltage, the output power $P_o$ is obtained. The CSD drive voltage was fed by another DC power supply (Agilent 6655A). The drive loss $P_{Drive}$ is obtained through this DC voltage and current. Therefore, the efficiency is $P_o/(P_{in}+P_{Drive})$. The losses of the CPLD and other logic circuits are negligible here.

Figure 3.24 shows the measured efficiency comparison for the CSD and conventional gate driver at 1.5V output. It is observed that at 20A, the efficiency is improved from 84.0% to 86.6% (an improvement of 2.6%) and at 30A, the efficiency is improved from 79.4% to 83.6% (an improvement of 4.2%).

![Figure 3.24 Efficiency comparison at 1.5V/30A condition: top, CSD; bottom: voltage source driver (Conv.)](image)

Figure 3.25 illustrates the loss reduction for the CSD over the voltage source driver with different load currents. It can be observed that 18.8% loss reduction is achieved for load current at 20A and 24.4% loss reduction is achieved at 30A.
Vin = 12V, Vo = 1.5V, Fs = 1MHz

Figure 3.25 Loss reduction at 1.5V/30A condition: top: CSD, bottom: Conventional voltage source driver (Conv.)

Figure 3.26 shows the power loss comparison for the CSD and the voltage source driver. It shows that at 20A, the total loss is reduced from 5.71W to 4.64W, a reduction of 18.8%. At 30A output current, the total loss is reduced from 11.68W to 8.83W, a reduction of 24.4%.

Figure 3.26 Power loss comparison at 1.5V/30A condition: Top: CSD, bottom: conventional voltage source driver (Conv.)
Another interesting observation from Figure 3.26 is that for same power loss of 6.4W, the buck converter with the conventional voltage driver can only provide 21A output current, while the buck converter with the CSD can provide 25A (an improvement of 20%). In other words, if the total VRM output current is 100A, we need 5 phases buck converters if the conventional voltage driver is used, while we only need to use 4 phases if the CSD is used. This will be a lot cost saving. Similarly, if the power loss is limited at 8.8W, the buck converter with the voltage source driver can only provide about 26A while with the CSD the converter will be able to provide 30A (an improvement of 15%). In other words, if the total load current is 150A, we will need 6 (150/24) phases for the conventional voltage driver while we only need 5 (150/30 = 5) phases for the CSD.

Figure 3.27 shows the measured efficiency for the CSD at different output voltages and load currents. It is observed that at 1.0V/20A, the efficiency is 83.5% and it is almost the same as 84.0% (see Figure 3.24) of the voltage source driver at 1.5V/20A, which means that we can reduce the output voltage from 1.5V to 1.0V by the CSD without penalizing the efficiency. This is important because that the VRM output voltage keeps reducing and will be less than 1V in the near future.
The efficiency comparison of different approaches of 12V VRMs at the switching frequency of 1MHz is listed in Table 3.2. Compared to the tapped-inductor (TI) buck converter in [43], the CSD improves the efficiency from 84% to 87% (an improvement of 3%). Compared to the soft-switching phase-shift buck (PSB) converter in [48], the CSD improves the efficiency from 82% to 86% (an improvement of 4%). The CSD achieves almost the same efficiency as the self-driven soft-switching buck-derived multiphase converter in [49]. Furthermore, it should be noted that the CSD does not change the multiphase buck architecture of today’s VRMs featuring lower cost and simple control while improving the efficiency in a cost-effective manner. In particular, it should also be mentioned that an efficiency improvement of 1.6% at 1.5V/20A is also achieved over the Toshiba synchronous buck Multi Chip Module using semiconductor integration approach to minimize the parasitic inductances [60].
<table>
<thead>
<tr>
<th>VRM Topologies</th>
<th>Conversion Efficiency</th>
<th>Output current/Phase</th>
<th>Output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tapped-inductor (TI) buck converter [43]</td>
<td>84%</td>
<td>12.5A</td>
<td>1.5V</td>
</tr>
<tr>
<td>Toshiba synchronous buck Multi Chip Module (TB7001FL) [60]</td>
<td>85%</td>
<td>20A</td>
<td>1.5V</td>
</tr>
<tr>
<td>Proposed CSD (Figure 3.27)</td>
<td>87%</td>
<td>12.5A</td>
<td>1.5V</td>
</tr>
<tr>
<td></td>
<td>86.6%</td>
<td>20A</td>
<td>1.5V</td>
</tr>
<tr>
<td>Soft-switching phase-shift buck (PSB) converter [48]</td>
<td>82%</td>
<td>17.5A</td>
<td>1.3V</td>
</tr>
<tr>
<td>Self-driven soft-switching buck-derived multiphase converter [49]</td>
<td>84.7%</td>
<td>25A</td>
<td>1.3V</td>
</tr>
<tr>
<td>Proposed CSD (Figure 3.27)</td>
<td>86%</td>
<td>17.5A</td>
<td>1.3V</td>
</tr>
<tr>
<td></td>
<td>84.3%</td>
<td>25A</td>
<td>1.3V</td>
</tr>
</tbody>
</table>

Figure 3.28 gives the total loss breakdown of the buck converter with the CSD. Figure 3.29 shows the measured efficiency and the analytical efficiency based on the loss model. It can be observed that the modeling results matches the experimental result well. The calculated efficiency is slightly higher than the measured one since there are some additional losses are not included such as PCB trace conduction loss and via loss etc.

![Figure 3.28 Loss breakdown](image)

Vin=12V, Vo=1.5V, Io=20A, Fs=1MHz
3.8 Conclusion

In this chapter, an accurate analytical loss model of a power MOSFET with the CSD is developed and the impact of the parasitic inductance is investigated. The advantages of the CSD are verified thoroughly by the analytical analysis, simulation and experimental results. Compared to a voltage source driver, the CSD uses a current source to turn on and turn off the MOSFET and therefore, absorbs the parasitic common source inductance. As a result, the switching transition time can be greatly reduced, which leads to a reduction of the switching loss. Based on the proposed loss model, a general method to optimize the CSD is proposed. A 12V synchronous buck converter with the CSD operating at 1 MHz was built to verify the analysis and prove the significant loss saving. The level-shift circuit of the CSD and the CPLD implementation are also presented. The analytical results of the loss model match the simulation results and the experimental results well. The loss model can be used to optimize a CSD at high frequency.

The CSD achieves an efficiency improvement over the voltage source driver, improving from 79.4% to 83.6% for 12V input, 1.5V/30A output and 1MHz buck converter. More
importantly, compared to other state of the art VR approaches, the CSD approach is promising from the standpoints of both performance and cost-effectiveness.
Chapter 4
A New Continuous CSD for a Buck Converter with Different Gate Drive Currents

4.1 Introduction

In the previous chapter, it has been noted that CSDs can reduce the switching transition time and the switching loss due to high gate drive currents. The CSD in [3] under investigation is illustrated in Figure 4.1 again. Through the optimal design method proposed in the previous chapter, this CSD can achieve an efficiency improvement over the conventional voltage driver at the switching frequency of 1MHz.

Figure 4.1 Synchronous buck converter with the CSD

However, with carefully investigating the equivalent circuits of operation in [3], it should be noted that this CSD has several drawbacks:

*The content of this chapter has been filed as a U.S. provisional patent, and has been published the following journal:
1) In a buck converter, high turn-on and turn-off gate currents are desired for the control MOSFET to ensure fast switching speed to reduce switching loss, while relatively low turn-on and turn-off gate currents (and therefore low drive circuit loss) are desired for the SR to achieve gate energy recovery. Therefore, it is beneficial to have different gate drive currents for optimal design. However, this CSD only provides identical drive currents for the control and SR MOSFETs;

2) Due to the reverse recovery of the body diode, the switching node has severe oscillation. Figure 4.2 illustrates the equivalent circuit. This switching node \( V_s \) is actually in series with the level-shift capacitor \( (C_1) \), which makes the CSD sensitive to the reverse recovery noise in practical applications. Moreover, the input voltage is applied to the current source inductor, which results in high inductance value at high input voltage;

![Figure 4.2 Equivalent circuit during switching transition](image)

3) The current-source inductor current flows through the control MOSFET and SR, which causes additional conduction loss;

4) To enhance light load efficiency, the switching frequency can be reduced or diode emulation can be used to turn off SRs to allow discontinuous conduction mode by detecting when the inductor current reaches zero. However, it is difficult to achieve these advanced features using this CSD.
In order to solve the above problems and improve the CSD performance, an improved CSD is proposed in this chapter. In section 4.2, the proposed CSD is presented. An improved version of the new circuit with magnetic integration is presented in section 4.3. The experimental results are reported in section 4.4. Finally, the conclusions and discussions are given in section 4.5.

4.2 Proposed CSD

One objective of the proposed CSD is to achieve independent gate drive currents for the control and SR MOSFET to achieve optimal performance. For the control MOSFET, the optimal design involves a tradeoff between switching loss and drive circuit loss; while for the SR, optimal design involves a tradeoff between body diode conduction loss and drive circuit loss (gate energy recovery). Moreover, the drive currents should not go through the main power MOSFETs.

All the above features can be achieved by the proposed CSD as shown in the dotted area in Figure 4.3. In Figure 4.3, Q1 is the control MOSFET and Q2 is the SR in a buck converter. Figure 4.4 gives the key waveforms.

4.2.1 Principle of Operation

In Figure 4.3, there are two sets of the CSDs (CSD #1 and CSD #2) and each of them has the structure of the half-bridge topology, consisting of drive MOSFETs S1&S2 and S3 &S4 respectively. CSD #1 can also be regarded as a level-shift version of CSD #2. Vc1 and Vc2 are the drive voltages and they could use the same, or different drive voltages if desired. The diode Df provides the path to charge Cf to the voltage of the drive voltage Vc2. Cb1 and Cb2 are the blocking capacitors. It is noted that the drive MOSFETs (S1-S4) are similar to those in a voltage source driver integrated circuit (driver IC), which means S1-S4 can also be implemented in a driver IC. The new CSD is analyzed with discrete components and the timing is tuned using digital complex programmable logic device (CPLD).
Figure 4.3 Buck converter with proposed CSD

Figure 4.4 Key waveforms of the proposed CSD
As illustrated in Figure 4.4, $S_1$ and $S_2$ are switched out of phase with complimentary control to drive $Q_1$, while $S_3$ and $S_4$ are switched out of phase with complimentary control to drive $Q_2$. With complimentary control, all the drive switches can achieve ZVS.

Figure 4.5 illustrates the equivalent circuits accordingly. There are six switching modes in one switching period. $D_1$-$D_4$ are the body diodes and $C_1$-$C_4$ are the intrinsic drain-to-source capacitors of $S_1$-$S_4$ respectively. $C_{gs1}$ and $C_{gs2}$ are intrinsic gate-to-source capacitors of $Q_1$ and $Q_2$ respectively. The switching transitions of charging and discharging $C_{gs1}$ and $C_{gs2}$ are during the interval of $[t_0, t_2]$ and $[t_3, t_5]$. The peak currents $i_{G_{Q1}}$ and $i_{G_{Q2}}$ during $[t_0, t_2]$ and $[t_3, t_5]$ are constant during switching transition, which ensures fast charging and discharging of the MOSFET gate capacitors including the miller capacitors.

1) Mode 1 [$t_0, t_1$] [Figure 4.5 (a)]: Prior to $t_0$, $S_2$ and $S_3$ conduct and the inductor current $i_{Lr1}$ increases in the positive direction, while $i_{Lr2}$ increases in the negative direction. $Q_2$ is on. At $t_0$, $S_3$ turns off. $i_{Lr2}$ charges $C_3$ and discharges $C_4$ plus $C_{gs2}$ simultaneously. Due to $C_3$ and $C_4$, $S_3$ achieves zero-voltage turn-off. The voltage of $C_3$ rises linearly and the voltage of $C_4$ decays linearly.

2) Mode 2 [$t_1, t_2$] [Figure 4.5 (b)]: At $t_1$, $v_{c3}$ rises to $V_{c1}$ and $v_{c4}$ decays to zero. The body diode $D_4$ conducts and $S_1$ turns on with zero-voltage condition. The gate-to-source voltage of $Q_2$ is clamped to ground through $S_4$. At $t_1$, $S_2$ turns off. $i_{Lr1}$ charges $C_2$ plus the input capacitor $C_{gs1}$ and discharges $C_1$ simultaneously. Due to $C_1$ and $C_2$, $S_2$ is zero-voltage turn-off. The voltage of $C_2$ rises linearly and the voltage of $C_1$ decays linearly.

3) Mode 3 [$t_2, t_3$] [Figure 4.5 (c)]: At $t_2$, $v_{c2}$ rises to $V_{c2}$ and $v_{c1}$ decays to zero. The body diode $D_1$ conducts and $S_1$ turns on under zero-voltage condition. The gate-to-source voltage of $Q_1$ is clamped to $V_{c2}$ through $S_1$. $i_{Lr1}$ and $i_{Lr2}$ both decrease.
4) Mode 4 \([t_3, t_4]\) [Figure 4.5 (d)]: Before \(t_3\), \(i_{L1}\) and \(i_{L2}\) changes each polarity and increases in opposite directions respectively. At \(t_3\), \(S_4\) and \(S_1\) turns off. \(i_{L2}\) charges \(C_4\) plus \(C_{gs2}\) and discharges \(C_3\). Due to \(C_3\) and \(C_4\), \(S_4\) achieves zero-voltage turn-off. The voltage of \(C_4\) rises linearly and the voltage of \(C_3\) decays linearly. \(i_{L1}\) charges \(C_1\) and discharges \(C_2\) plus \(C_{gs1}\) simultaneously. Due to \(C_1\) and \(C_2\), \(S_1\) achieves zero-voltage turn-off.

5) Mode 5 \([t_4, t_5]\) [Figure 4.5 (e)]: At \(t_4\), \(v_{c1}\) rises to \(Vc_2\) and \(v_{c2}\) decays to zero. The body diode \(D_2\) conducts and \(S_2\) turns on with zero-voltage. The gate-to-source voltage of \(Q_1\) is clamped to zero through \(S_2\).

6) Mode 6 \([t_5, t_6]\) [Figure 4.5 (f)]: At \(t_5\), \(v_{c4}\) rises to \(Vc_1\) and \(v_{c3}\) decays to zero. The body diode \(D_3\) conducts and \(S_3\) turns on with zero-voltage. The gate-to-source voltage of \(Q_2\) is clamped to \(Vc_1\) through \(S_3\). After \(t_6\), the next switching cycle starts.
4.2.2 Advantages of Proposed CSD

The advantages of the proposed CSD are highlighted as follows:

1) Significant reduction of the switching transition time and switching loss

During the switching transition \([t_1, t_2]\) and \([t_3, t_4]\) (see Figure 4.4), the proposed CSD uses the peak portion of the inductor current to drive the control MOSFET and absorbs the common source inductance. This reduces the propagation impact of the parasitics during the switching transition, which leads to a reduction of the switching transition time and switching loss.
2) Gate energy recovery

The proposed CSD, using an inductor as a current source, store energy in the inductance, which can be recovered to the driver supply voltage source. In the proposed CSD, the inductor returns its stored energy to the line during intervals \([t_0, t_2]\) for SR \(Q_2\). Energy is also returned to the driver supply during the corresponding time intervals for the control MOSFET, \(Q_1\). Owing to gate energy recovery, high gate drive voltage can be used to further reduce \(R_{DS(on)}\) conduction loss.

3) Reduced SR body diode conduction

Quick switching is also beneficial to minimize the dead time between the control and SR MOSFETs. As the gate-source voltage rises from the plateau voltage to \(V_{cc}\), the \(R_{DS(on)}\) of SR is decreasing. Quick switching enables a fast transition to the minimum value of \(R_{DS(on)}\) at \(v_{gs}=V_{cc}\). This results in conduction loss savings and reverse recovery loss in the SR body diode.

4) ZVS of the drive switches

Through the analysis, it is noted that all of the drive switches (\(S_1\)-\(S_4\)) are able to achieve ZVS, which is beneficial for high frequency (i.e. >1 MHz) operation.

5) High noise immunity

In the proposed CSD, the gate terminals of the MOSFETs (\(Q_1\) and \(Q_2\)) are clamped to either the drive voltage source via a low impedance path (\(S_1\) and \(S_3\) with fairly small \(R_{DS(on)}\)) or their source terminals (\(S_2\) and \(S_4\)). This offers high noise immunity and leads to the alleviation of \(dv/dt\) effect to prevent \(Cdvdv/dt\) induced turn-on of the SR.

4.2.3 Drive Circuit Loss Analysis

CSD #1 and CSD #2 have similar driver losses, except each operates with different peak inductor currents. In CSD #1, the drive loss includes: 1) the resistive loss and gate drive loss of drive switches \(S_1\)-\(S_2\); 2) the loss of the inductor \(L_{r1}\); 3) the resistive loss caused by the internal gate
mesh resistance of the power MOSFETs.

Using volt-second balance across the inductor, the DC voltage, \( v_{cb1} \), across the blocking capacitor, \( C_{b1} \), is given by

\[
v_{cb1} = (1 - D) \cdot V_{c2}
\]  

(4.1)

where \( D \) is the duty cycle of \( S_1 \) and \( V_{c2} \) is the drive voltage.

The blocking capacitor value is found using

\[
C_{b1} = \frac{I_{Lr1\_pk}}{4 \cdot k \cdot V_{c1} \cdot f_s}
\]  

(4.2)

where \( k \) is the percent ripple on \( C_{b1} \) and \( f_s \) is the switching frequency. For example, for \( V_{c1}=7 \) V, \( I_{Lr1\_pk}=1.5 \) A, \( k=5\% \) and \( f_s=1 \) MHz, then \( C_{b1}=1.0 \) \( \mu F \) should be used.

The relationship of the inductor value \( L_{r1} \) and the peak inductor current \( I_{Lr1\_pk} \) is

\[
L_{r1} = \frac{V_{c1} \cdot D \cdot (1 - D)}{2 \cdot I_{Lr1\_pk} \cdot f_s}
\]  

(4.3)

By choosing the proper peak inductor current (i.e. gate drive current for the power MOSFET), the inductor value can be obtained using (4.3).

As observed from the principle of operation in Figure 4.4, the peak current, \( I_{Lr1\_pk} \), of the inductor, \( L_{r1} \), is actual gate drive current for the power MOSFET and can be regarded as a constant current source. Therefore, the higher \( I_{Lr1\_pk} \) is, the shorter the switching transition time is, and thus more switching loss can be reduced. On the other hand, higher \( I_{Lr1\_pk} \) results in a larger RMS value of the inductor circulating current, \( i_{Lr1} \), which increases the circulating current conduction loss in the drive circuit, and therefore, decreases the gate energy recovery. Therefore, it is critical to decide \( I_{Lr1\_pk} \) properly so that the maximum loss savings can be achieved. The optimal design to choose \( I_{Lr1\_pk} \) will be given in section 4.2.4.

The inductor current waveform in Figure 4.4 can be regarded as a triangular waveform since
the charging/discharging time \([t_0, t_2]\) and \([t_3, t_5]\) are small and can be neglected. Therefore, the RMS value of the inductor current, \(I_{L_{r1,RMS}}\), is \(I_{L_{r1,pk}}/\sqrt{3}\).

The RMS current flowing through \(S_1\) is given by:

\[
I_{s_{1\_RMS}} = I_{L_{r1,pk}} \cdot \frac{D}{3}
\]  

(4.4)

The RMS current flowing through \(S_2\) is given by:

\[
I_{s_{2\_RMS}} = I_{L_{r1,pk}} \cdot \frac{1-D}{3}
\]  

(4.5)

Assuming the same MOSFETs are used for \(S_1\) and \(S_2\), the conduction loss in \(S_1\) and \(S_2\) is

\[
P_{\text{cond}} = I_{s_{1\_RMS}}^2 \cdot R_{ds(on)} + I_{s_{2\_RMS}}^2 \cdot R_{ds(on)}
\]  

(4.6)

Substituting (4.4) and (4.5) into (4.6) yields

\[
P_{\text{cond}} = \frac{1}{3} \cdot I_{L_{r1,pk}}^2 \cdot R_{ds(on)}
\]  

(4.7)

The copper loss in the inductor is

\[
P_{\text{copper}} = R_{ac} \cdot I_{L_{r1,RMS}}^2
\]  

(4.8)

where \(R_{ac}\) is the AC resistance of the inductor winding and \(I_{L_{r1,RMS}}\) is the RMS value of the inductor current.

The loss \(P_{\text{core}}\) can be calculated using (4.9)

\[
P_{\text{core}} = K_1 \cdot f^\times \cdot B^y \cdot V_e
\]  

(4.9)

where \(K_1\) is constant for core material, \(f\) is the frequency, \(B\) is peak flux density, \(x\) is frequency exponent, \(y\) is flux density exponent, and \(V_e\) is effective core volume [61]. These parameters are unique to each core material, which are usually provided by the inductor suppliers.

In our case, since the inductor used in the experiment is the DK1608C series from Coilcraft, \(P_{\text{core}}\) can be estimated as 0.08 W through the web-based inductor core calculator [62].
The total inductor loss is

\[ P_{\text{ind}} = P_{\text{copper}} + P_{\text{core}} \]  

Both the charge and discharge currents flow through the internal gate mesh resistance, \( R_G \), of the power MOSFET and therefore, cause resistive loss.

The total loss dissipated in internal resistance of \( Q_1 \) during turn-on (\( t_{\text{on1}} \)) and turn-off (\( t_{\text{off1}} \)) is

\[ P_{RG} = R_{G1} \cdot I_r \cdot \left(t_{\text{on1}} + t_{\text{off1}} \right) \cdot f_s \]  

where \( R_{G1} \) is the internal gate resistors of \( Q_1 \).

The gate loss in \( S_1 \) and \( S_2 \) is

\[ P_{\text{gate}} = 2 \cdot Q_{g,s} \cdot V_{gs,s} \cdot f_s \]  

where \( Q_{g,s} \) is the total gate charge of a drive switch and \( V_{gs,s} \) is the drive voltage, which is typically 5 V.

Therefore, the total loss in CSD #1 is

\[ P_{\text{Drive}} = P_{\text{cond}} + P_{\text{ind}} + P_{RG} + P_{\text{gate}} \]  

4.2.4 Optimal Design

One advantage of the proposed CSD is that it can drive the control and SR MOSFET independently with different gate currents to achieve an optimized design.

For the control MOSFET, \( Q_1 \), optimal design involves a trade off between the switching loss and drive circuit loss. Following the optimal design procedure using the analytical loss model in chapter 3, the gate drive current can be decided. The sum of the switching loss and drive circuit loss can be plotted as \( P_{Q1,\text{Optimal}} \) and the optimal gate current, \( I_{G,Q1} \) can be determined from the graph (at the minimum point of \( P_{Q1,\text{Optimal}} \)). For \( V_{in}=12 \text{ V}, V_o=1.5 \text{ V}, I_o=30 \text{ A}, f_s=1 \text{ MHz}, \) gate driver voltage \( V_{c1}=8 \text{ V} \) and \( Q_1: \text{Si7860DP}, \) the curves are illustrated in Figure 4.6. In Figure 4.6, the optimal gate current is 1.5A and the required current-source inductor value is 1.0\( \mu \)H using
In this example, $P_{Q_1 \_switching} = 2.3\, \text{W}$ and $P_{\text{Drive}} = 0.5\, \text{W}$.

Figure 4.6 Optimization curves for the control MOSFET $Q_1$: power loss vs. gate current

SR $Q_2$ operates with ZVS since its output capacitance is discharged to zero before it turns on. Therefore, for the SR, optimal design involves a tradeoff between body diode conduction loss and gate drive loss.

The SR body diode conduction loss is

$$P_{\text{body} \_Q_2} = V_{\text{body} \_Q_2} \cdot I_o \cdot f_s \cdot t_{\text{body}} \quad (4.14)$$

where $t_{\text{body}}$ is body diode conduction time, which can be estimated using (4.15). In (4.15), it is assumed that the body diode conducts during the interval when the gate voltage is between the threshold and until the gate voltage is large enough so that the SR $R_{DS(on)}$ is less than about 20mOhms, which means the voltage drop across the channel is less than the body diode drop. The values for $Q_{g \_Q_2}(V_{20\, \text{mohm}})$ and $Q_{g \_Q_2}(V_{\text{th}\_Q_2})$ can be estimated using the MOSFET manufacturer datasheets.

$$t_{\text{body}} = 2 \left[ \frac{Q_{g\_Q_2}(V_{20\, \text{mohm}}) - Q_{g\_Q_2}(V_{\text{th}\_Q_2})}{I_g\_Q_2} \right] \quad (4.15)$$

Using $P_{\text{Drive}}$ given in (4.13) and $P_{\text{body} \_Q_2}$ given in (4.14), the sum of the two loss components
can be plotted as $P_{Q2_{Optimal}}$. The optimal gate current, $I_{G,Q2}$ can be determined from the graph (at the minimum point of $P_{Q2_{Optimal}}$). For $V_{in}=12\text{V}$, $V_o=1.5\text{V}$, $I_o=30\text{A}$, $f_s=1\text{MHz}$, gate driver voltage $V_{c2}=8\text{V}$ and $Q_1$: Si7336ADP, the curves are illustrated in Figure 4.7. In Figure 4.7, the optimal gate current is 1.1A and the inductor value is 1.2µH by using (4.3). In this example, $P_{Drive}=0.33\text{W}$, $P_{body,Q2}=0.58\text{W}$, $t_{body}=12\text{ns}$.

Figure 4.7 Optimization curves for the SR MOSFET $Q_2$: power loss vs. gate current

Figure 4.8 illustrates the loss breakdown comparison between the CSD with the optimal design and the conventional voltage source driver. At $V_o=1.5\text{ V}$, $I_o=20\text{ A}$ and $f_s=1\text{ MHz}$, the most loss reduction is the switching loss. The turn-on loss is reduced by 0.5 W and the turn-off loss is reduced by 0.7 W. The conduction loss and the body diode loss are also reduced by 0.05 W and 0.2 W respectively. The total loss reduction is 1.45W.
Figure 4.8 Loss breakdown between the CSD and conventional voltage driver (Conv.)

4.2.5 Application Extension

Half-bridge (HB) converters and full-bridge (FB) converters can achieve ZVS using complimentary control and phase-shift control respectively. However, turn-off loss still exits and could be high due to the parasitics of the main power MOSFETs. There, the turn-off loss becomes a concern at MHz switching frequencies.

It is noted that the proposed CSD can also be used to drive two MOSFETs in one leg of the HB or FB topologies to achieve switching loss reduction and gate energy recovery at high switching frequencies (>1 MHz), as shown in Figure 4.9.
4.3 New CSD with Integrated Magnetics

In Figure 4.4, it is interesting to observe that $i_{Lr1}$ is nearly a mirror image about the time axis of $i_{Lr2}$. This provides good ripple cancellation effect of the magnetic flux enabling potential inductors integration. Figure 4.10 shows the proposed CSD with integrated magnetics.

Figure 4.10 Proposed CSD with integrated inductors

Figure 4.11 illustrates an integrated inductor structure for the CSD. The two inductors ($L_{r1}$ and $L_{r2}$) are built on the two outer legs of one E-I core with different air gaps, $g_1$ and $g_2$, respectively. The fluxes $\Phi_1$ and $\Phi_2$ in the two outer legs generated by the two windings flow.
through the center leg, which is a low-reluctance magnetic path with no air gap. Though $L_{r1}$ and $L_{r2}$ are built on the same E-I core, there is no interaction between two flux loops of $\Phi_1$ and $\Phi_2$ and there is no coupling effect between $L_{r1}$ and $L_{r2}$. Therefore, the operation of the CSD with the integrated inductors does not change, however, the core number is reduced from two to one.

Another benefit of using integrated inductors is that the flux $\Phi$ ($\Phi=\Phi_1+\Phi_2$) in the center leg has smaller ripple owing to the flux ripple cancellation effect of the current $i_{Lr1}$ and $i_{Lr2}$ as shown in Figure 4.12. The smaller flux ripple helps to reduce the core losses in the center leg.

![Figure 4.11 Integrated inductor structure](image1)

![Figure 4.12 Flux ripple cancellation effect](image2)

**4.4 Experimental Results and Discussion**

In order to verify the advantages of the new CSD, a synchronous buck converter was built. The specifications are as follows: input voltage $V_{in}=12\text{V}$; output voltage $V_o=1.5\text{V}$; output current $I_o=30\text{A}$; switching frequency $f_s=1\text{MHz}$; gate driver voltage $V_{c1}=V_{c2}=8\text{V}$. The PCB uses six-layer 2 oz copper. The components used in the circuit are listed as follows:

Control MOSFET $Q_1$: Si7860DP (30 V N-channel, $R_{DS(on)}=11\ \text{m}\Omega@V_{GS}=4.5\ \text{V}$)

SR $Q_2$: Si7336ADP (30 V N-channel, $R_{DS(on)}=4\ \text{m}\Omega@V_{GS}=4.5\ \text{V}$)
Drive MOSFETs $S_1$-$S_4$: FDN335N (20 V N-channel, $R_{DS(on)}=70$ mΩ at $V_{GS}=4.5$ V)

Output filter inductance: $L_f=330$ nH ($R_{dc}=1.3$ mohm, IHLP-5050CE-01, Vishay)

Current-source inductors: $L_{r1}=1 \, \mu$H ($I_{pk1}=1.5$ A) and $L_{r2}=1.2 \, \mu$H ($I_{pk2}=1.1$ A), DO1608C series from Coilcraft.

The bootstrap and level-shift circuit in session 3.6.1 were used for the non-ground referenced switches. Altera Max II EPM240 CPLD was used to generate the driver gating signals. Surface mount (SMT) power inductors (DO1608C series) from Coilcraft are used for the inductors. The integrated inductors were also implemented with a grounded magnetic core in the experimental test.

Waveforms of the gate drive signals $v_{gs,Q1}$ (control MOSFET) and $v_{gs,Q2}$ (SR) are provided in Figure 4.13. The zoomed waveforms are shown in Figure 4.14. It is observed that the dead time between two gate signals is minimized to reduce the body diode conduction. It is noted that additional fixed dead time can be set to account for the threshold voltage variation at high temperature.

It is also observed that $v_{gs,Q1}$ is smooth since the miller charge is removed fast due to the constant charging/discharging current. It is also noted that due to gate energy recovery, 8V drive voltage is used to reduce $R_{DS(on)}$ by 25% compared to 5V drive voltage. This translates into a reduction of the conduction loss by 25%.
Figure 4.13 The gate signals $v_{gs. Q_1}$ (control MOSFET) and $v_{gs. Q_2}$ (SR)

Figure 4.14 Zoomed gate signals $v_{gs. Q_1}$ (control MOSFET) and $v_{gs. Q_2}$ (SR)

Waveforms of the inductor currents, $i_{Lr1}$ and $i_{Lr2}$, are given in Figure 4.15 for the CSD with discrete inductors. It is observed that for the control MOSFET, the drive current $i_{Lr1}$ is the optimal value, 1.5 A, while for the SR MOSFET, the drive current $i_{Lr2}$ is the optimal value, 1.1 A.
Waveforms of the inductor currents, $i_{Lr1}$ and $i_{Lr2}$, are illustrated in Figure 4.16 for the CSD with integrated inductors. It is observed that the mirror relationship between $i_{Lr1}$ and $i_{Lr2}$ leads to the feasibility of inductor integration and lower core loss due to the magnetic flux cancellation effect. In addition, the integrated inductor does not change the operation of the drive circuits.

A benchmark synchronous buck converter using the UCC27222 voltage source driver with predictive dead time control was built. The same parameters are used as the CSD. Figure 4.17
illustrates the measured efficiency comparison for the CSD and the conventional gate driver at 1.5V output. It is observed that at 20A, the efficiency is improved from 84% to 87.3% (an improvement of 3.3%) and at 30A, the efficiency is improved from 79.4% to 83.9% (an improvement of 4.5%). The CSD with one integrated inductor achieves similar efficiency as the driver with two discrete inductors.

Figure 4.17 Efficiency comparison at 1.5V/30A/1MHz

Figure 4.18 shows the converter power loss comparison between the CSD and voltage source driver. It is noted that 30A load, the proposed CSD saves approximately 3.0W (a reduction of 26%) compared to the voltage source driver. This loss reduction turns to be as much as 15W for a five phase VRs.

Another interesting observation is that if the power loss per phase is limited to 8.6W, the buck converter with the conventional gate driver can only provide 26A output current, while the buck converter with the CSD can provide 30A (an improvement of 15%). In other words, if the total output current is 120A, we need 5 phases (120A/26 A per phase) for the conventional gate
driver and only 4 phases (120A/30A per phase) for the CSD. This yields a potential cost savings and space savings enabling high power density.

Figure 4.18 Power loss comparison at 1.5V/30A condition; Top: Conventional voltage source driver (Conv), bottom: CSD

Figure 4.19 shows the measured efficiency for the CSD at different output voltages as a function of load currents.

Figure 4.19 Efficiency at different output voltages
4.5 Conclusion

In this chapter, a new continuous CSD is proposed for a synchronous buck converter. The proposed CSD is able to drive the control MOSFET and SR independently with different drive currents enabling optimal design.

The proposed CSD maintains the following advantages: 1) significant switching loss reduction; 2) gate energy recovery; 3) reduced conduction loss and reverse recovery loss of the body diode; 4) ZVS for the driver switches. The improved CSD using integrated inductors is also presented to reduce the magnetic core count and the core loss due to magnetic flux cancellation.

The proposed CSD can also be used to drive the two MOSFETs in one leg of a HB converter or a FB converter to further reduce the turn-off loss at MHz switching frequencies.

Experimental results demonstrate the advantages of the CSD. At 1.5V output, the CSD improves the efficiency from 84% using the voltage source driver to 87.3% (an improvement of 3.3%) at 20 A, and at 30 A, from 79.4% using the voltage source driver to 83.9% (an improvement of 4.5%).
Chapter 5
A New Discontinuous CSD for High Frequency Power MOSFETs ‡

5.1 Introduction

In Chapter 3 and Chapter 4, continuous CSDs have been investigated in details. The greatest benefit of CSDs for the control MOSFET in a high frequency (>1MHz) buck converter is high switching loss reduction.

However, one concern of continuous CSDs is the gate drive current vary with the duty cycle and switching frequency. Moreover, the inductance value is high (typically, around 1μH at the switching frequency of 1MHz). This value of the inductor can not be integrated into a driver IC chip. Also the continuous CSDs have high circulating loss in the drive switches, which may reduce the efficiency of the gate energy recovery. In addition, the switching frequency variation will impact on the inductance value of the continuous CSDs.

In order to solve the problems of the continuous CSDs, a new CSD with discontinuous inductor current is proposed in this chapter. Compared to other CSDs proposed in previous work, the most important advantage of the proposed discontinuous CSD is the small inductance (typically, around 20nH at 1MHz switching frequency). Other features of the proposed CSD include: 1) discontinuous inductor current with low circulating loss; 2) fast switching speed and reduced switching loss; 3) wide operation range of duty cycle and switching frequency; 4) high noise immunity. Compared to the discontinuous CSD proposed in [4], since the actual voltage over the inductor is reduced by half, for the same pre-charge time and gate drive current, the proposed CSD can reduce the inductance value by half.

‡ The content of this chapter has been submitted to the following conference:
Section 5.2 presents the proposed CSD and its principle of operation. Section 5.3 introduces the proposed isolated discontinuous CSD. Section 5.4 presents the loss analysis and design procedure. Section 5.5 gives the experimental results and discussion. Section 5.6 provides a conclusion.

5.2 Proposed CSD and Its Principle of Operation

The proposed CSD is illustrated in Figure 5.1. It consists of four drive switches, \( S_1-S_4 \), a small inductor \( L_r \) and a series capacitor \( C_s \). \( V_D \) is the gate drive voltage. In the analysis, it is assumed that the same MOSFETs (n-channel) are used for \( S_1-S_4 \). \( S_1-S_4 \) are controlled to allow the inductor current to be discontinuous and the power MOSFET can be turned on or off beginning from a non-zero pre-charge current. Flowing charging, or discharging of the power MOSFET, the excess stored energy in the inductor is allowed to return to the series capacitor \( C_s \) and drive voltage source.

Figure 5.1 The proposed discontinuous CSD

Figure 5.2 illustrates the control gating signals, inductor current \( i_{L_r} \), gate current \( i_G \) and power MOSFET gate-to-source voltage \( v_{GS} \). The key waveforms to note are: 1) \( S_1 \) and \( S_2 \) are switched out of phase with complimentary control to drive \( Q \); 2) the inductor current \( i_{L_r} \) is discontinuous to minimize conduction loss compared to the continuous circulating current as shown in dotted line; 3) the gate drive current \( i_G \) is relative constant during turn on and turn off transition, which
achieves fast switching speed of the power MOSFET.

Figure 5.2 Key waveforms of the proposed CSD

5.2.1 Principle of Operation

There are eight switching modes in one switching period. The operation of the circuit is explained in the following paragraphs. The equivalent circuits of turn on transition are illustrated in Figure 5.3 (a)-(d). $D_1$-$D_4$ are the body diodes of $S_1$-$S_4$. $C_1$-$C_2$ are the intrinsic drain-to-source capacitors of $S_1$ and $S_2$. $C_{gs}$ is the intrinsic gate-to-source capacitor of the main power MOSFET $Q$. The switching transitions of charging and discharging $C_{gs}$ are during the intervals of $[t_1, t_2]$ and $[t_5, t_6]$ respectively. The peak current $i_G$ during $[t_1, t_2]$ and $[t_5, t_6]$ are constant during the switching transition, which ensures fast charging and discharging of $Q$ gate capacitor including the miller capacitor. Initially, it is assumed that the power MOSFET is in the off state before time $t_0$.

1) Mode 1 $[t_0, t_1]$ [Figure 5.3 (a)]: Prior to $t_0$, $S_2$ is on and the gate of $Q$ is clamped to ground.
At $t_0$, $S_1$ turns on (with ZCS) allowing the inductor current $i_{Lr}$ to ramp up through $D_4$. The current path during this interval is $C_{gs}-L_r-S_3-D_4-S_2$. This interval is the inductor current pre-charge interval and it ends at time $t_1$, which is a pre-determined time set by the user. Since $S_2$ is in the on state, the gate of $Q$ is always clamped low.

2) Mode 2 [$t_1$, $t_2$] [Figure 5.3 (b)]: At $t_1$, $S_2$ is turned off, which allows the inductor current to begin to charge the gate capacitor $C_{gs}$. $i_{Lr}$ charges $C_2$ plus the input capacitor $C_{gs}$ and discharges $C_1$ simultaneously. Due to $C_1$ and $C_2$, $S_2$ is zero-voltage turn off. The inductor current continues to ramp up from the pre-charged level.

3) Mode 3 [$t_2$, $t_3$] [Figure 5.3 (c)]: At $t_2$, $v_{c2}$ rises to $V_D$ and $v_{c1}$ decays to zero. The body diode $D_1$ conducts and $S_1$ turns on under zero-voltage condition. The inductor current continues to conduct through the path $C_{gs}-L_r-S_1-D_4$. This interval continues for a short duration until $t_3$. During this interval, the gate of $Q$ is clamped to the drive voltage $V_D$. This interval ends when the inductor current reaches zero at $t_3$. It is noted that it is during this interval when the stored energy in the inductor is returned to $C_3$. Also during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero.

4) Mode 4 [$t_3$, $t_4$] [Figure 5.3 (d)]: At $t_3$, $D_4$ turns off (with ZCS) and the inductor current is zero. During this interval, the gate of $Q$ remains clamped high. This interval ends at $t_4$ when the pre-charged interval for the turn off cycle begins as dictated by the PWM control signals.
Figure 5.3 Equivalent circuits: turn on intervals

The equivalent circuits of turn off intervals are illustrated in Figure 5.4 (a)-(d).

5) Mode 5 \([t_4, t_5]\) [Figure 5.4 (a)]: At \(t_4\), \(S_4\) turns on (with ZCS). Since \(S_1\) was previously on, the inductor current \(i_{Lr}\) begins to ramp negative through the path \(C_s, S_1, S_4, D_3, L_r\). The energy charge the inductor is provided by \(C_s\). During this interval, the gate of \(Q\) remains clamped to \(V_D\). This interval ends at \(t_5\).

6) Mode 6 \([t_5, t_6]\) [Figure 5.4 (b)]: At \(t_5\), \(S_1\) is turned off, which allows the inductor current to begin to discharge the gate capacitor \(C_{gs}\). \(i_{Lr}\) discharges \(C_2\) plus the input capacitor \(C_{gs}\) and charges \(C_1\) simultaneously. Due to \(C_1\) and \(C_2\), \(S_1\) is zero-voltage turn off. The inductor current continues to ramp negative from the pre-charged level.

7) Mode 7 \([t_6, t_7]\) [Figure 5.4 (c)]: At \(t_6\), \(v_{c1}\) rises to \(V_D\) and \(v_{c2}\) decays to zero. The body diode \(D_2\) conducts and \(S_2\) turns on under zero-voltage condition. The inductor current continues to conduct through the path \(C_s, L_r, D_3, S_4, S_2\). This interval continues for a short duration until \(t_7\). During this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. It is noted that it is during this interval when the stored energy in the inductor is returned to the drive voltage source. During this interval, the gate of \(Q\) is clamped low. This interval ends when the inductor current reaches zero at \(t_7\).

8) Mode 8 \([t_7, t_8]\) [Figure 5.4 (d)]: At \(t_7\), \(D_3\) turns off (with ZCS) and the inductor current is
zero. During this interval, the gate of $Q_1$ remains clamped low. This interval ends at $t_8$ when the pre-charged interval for the turn on cycle begins and the entire process repeats as dictated by the PWM control signal.

![Diagram of equivalent circuits](image)

Figure 5.4 Equivalent circuits: turn off intervals

### 5.2.2 Gate Drive Current of The Power MOSFET

The pre-charge current to turn on and turn off the power MOSFET is decided by the voltage to charge the current-source inductor and the pre-charge time. For the turn on current, the voltage to charge the inductor is $(V_D - V_{CS})$ and the pre-charge time from $t_0$ to $t_1$ ($t_{10}$). For the turn off current, the voltage to charge the inductor is $V_{CS}$ and the pre-charge time from $t_4$ to $t_5$ ($t_{54}$).

From the volt-second balance condition across the inductor, (5.1) should be satisfied

$$ (V_D - V_{CS}) \cdot t_{10} = V_{CS} \cdot t_{32} \quad (5.1) $$

where $V_D$ is the drive voltage and $V_{CS}$ is the DC voltage across the capacitor.
From (5.1), assuming $t_{10}=t_{32}$, the DC voltage across the series capacitor is

$$V_{Cs} = \frac{V_D}{2} \quad (5.2)$$

The pre-charge current to turn on the power MOSFET is

$$I_{G_{on}} = \frac{V_D - V_{Cs}}{L_r} \cdot t_{10} \quad (5.3)$$

From (5.2) and (5.3), the turn on current is

$$I_{G_{on}} = \frac{V_D}{2L_r} \cdot t_{10} \quad (5.4)$$

From (5.2), the pre-charge current to turn off the power MOSFET is

$$i_{G_{off}} = \frac{V_{Cs}}{L_r} \cdot t_{54} = \frac{V_D}{2L_r} \cdot t_{54} \quad (5.5)$$

From (5.3) and (5.4), by changing pre-charge time, the turn-on gate current and turn-off gate current can be decided. It is also noted that compared to the discontinuous CSD in [4], since the actual voltage over the inductor is reduced by half as $V_D/2$, for the same pre-charge time and gate drive current, the proposed driver can reduce the inductance value by half.

### 5.2.3 Benefits of The Proposed CSD

The advantages of the new CSD are highlighted as follows:

1) Significant reduction of the switching transition time and switching loss

The key idea of the proposed CSD is to control the four drive switches to create a constant current source to drive the main power MOSFETs. During the switching transition $[t_1, t_2]$ and $[t_5, t_6]$ (see Figure 5.2), the proposed CSD uses the pre-charge inductor current to drive the control MOSFET and absorbs the parasitic inductance. This reduces the propagation impact of the parasitics during the switching transition, which leads to a reduction of the switching transition time and switching loss. At the same time, the discontinuous current does not increase the
circulating loss compared to other continuous CSDs.

2) Gate energy recovery

The stored energy in the inductor is returned to the series capacitor $C_s$ during $[t_2, t_3]$ and is returned to the drive voltage source during $[t_6, t_7]$ (see Figure 5.2). One benefit of the gate energy recovery capability is that high gate drive voltage can be used to further reduce $R_{DS(on)}$ conduction loss.

3) Small current-source inductance

One of the most important advantages of the proposed CSD is the small inductance. Compared to the continuous CSDs proposed in [3] and [38], which have the inductance value around 1uH at the switching frequency of 1MHz, the inductance of the proposed circuit is only about 10nH~20nH. This is a significant reduction of the inductance value.

4) Wide range of duty cycle and switching frequency

In a high frequency buck converter, the duty cycle is required to response fast during a transient event. At the same time, in order to improve the efficiency in a wide load range, the switching frequency of a buck converter may need to vary according to the load condition. The proposed CSD operates correctly for duty cycles ranging from 0%-100%. The gate drive current (current-source inductor current) only depends on the pre-charge time and is independent of duty cycle and switching frequency, so it is suitable for different types of control and wide operating conditions.

5) High noise immunity

With the new CSD, the gate terminal of the power MOSFETs are clamped to either the drive voltage source via a low impedance path ($S_1$ fairly small $R_{DS(on)}$) or the source terminal ($S_2$). This offers high noise immunity and leads to the alleviation of $dv/dt$ effect.
5.3 Proposed High Side CSD and Hybrid Gate Drive Scheme

Figure 5.5 illustrates the proposed high side CSD for non-ground referenced power MOSFET. It uses a bootstrap circuit consisting of a diode $D_f$ and a bootstrap capacitor $C_f$. This CSD can be used to control the MOSFET in a buck converter to achieve fast switching and reduced switching loss.

![Figure 5.5 Proposed high side CSD](image)

Figure 5.6 illustrates another version of the high side CSD using $C_{s1}$ and $C_{s2}$ in series as the bootstrap capacitor, where $C_{s1}$ and $C_{s2}$ also serve as the bootstrap capacitors.

![Figure 5.6 Proposed high side CSD using series capacitors](image)

Figure 5.7 shows the loss breakdown of buck converter with the conventional voltage gate driver. Carefully investigating the switching behavior of the MOSFETs in a synchronous buck converter, it is interesting to observe that the switching loss of the control MOSFET is dominant.
among the total loss breakdown as shown in Figure 5.7. For the control MOSFET, the common source inductance results in high switching loss, especially, turn-off loss, which makes the fast turn-off transition more desirable. However, on the other hand, for the SR, it almost has no switching loss since its output capacitor has been discharged to zero voltage before it turns on, which can be regarded to achieve ZVS. Moreover, due to the ZVS condition, no miller charge is present and the gate charge is saved by around 30%. Also, the common-source inductance could help to improve the \( \frac{dv}{dt} \) immunity of the SR MOSFET [14]. So the conclusion is that control MOSFET and the SR MOSFET have different switching behavior as far as the parasitics are concerned.

![Figure 5.7 Loss breakdown of the buck converter with the conventional voltage gate driver](image)

Figure 5.7 Loss breakdown of the buck converter with the conventional voltage gate driver \((L_s=1nH, L_D=2nH, \text{control MOSFET: Si7860DP and SR: Si7336ADP})\)

Therefore, in order to reduce the dominant loss (the switching loss) in the buck converter in a low cost manner, a new hybrid gate drive scheme as shown in Figure 5.8 is proposed for a buck converter. For the control MOSFET \( Q_1 \), the proposed high side CSD is used to achieve the switching loss reduction. For the SR \( Q_2 \), the conventional voltage source driver is used for low cost and simplicity, which is the bipolar totem-pole drive structure. PWM\_SR is the signal fed into the bipolar totem-pole pair.
5.4 Loss Analysis and Design Procedure

Based on the principle of operation, the loss analysis is presented in this section. This provides design guideline for the proposed CSD.

5.4.1 Loss Analysis

1) Conduction Loss

Figure 5.9 illustrates the power MOSFET gate voltage and gate drive current waveforms during the turn on interval. The current paths are also listed under the waveforms.
Figure 5.9 Detailed inductor current and power MOSFET gate voltage waveforms during the turn on interval

Interval \([t_0, t_1]\) [see Figure 5.3(a)]: The inductor current path is \(S_3-D_4-S_2\).

The RMS current is

\[
I_{RMS} = I_{G_{on}} \cdot \sqrt{\frac{t_{10} \cdot f_s}{3}}
\]  \hspace{1cm} (5.6)

where \(I_{G_{on}}\) is the pre-charge turn on current from (5.3).

The average value is

\[
I_{aver} = I_{G_{on}} \cdot t_{10} \cdot f_s
\]  \hspace{1cm} (5.7)

The total conduction loss is

\[
P_{t10} = 2I_{RMS}^2 \cdot R_{DS(on)} + I_{aver} \cdot V_F
\]  \hspace{1cm} (5.8)

From (5.6), (5.7) and (5.8), \(P_{t10}\) becomes

\[
P_{t10} = \frac{2}{3} I_{G_{on}}^2 t_{10} f_s R_{DS(on)} + \frac{1}{2} I_{G_{on}} V_F t_{10} f_s
\]  \hspace{1cm} (5.9)

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where \( R_{DS(on)} \) is the on-resistance of \( S_1\)-\( S_4 \), assuming \( S_1\)-\( S_4 \) are same and \( V_F \) is the diode forward voltage.

Interval \([t_1, t_2]\) [see Figure 5.3(b)]: The inductor current path is \( S_3\)-\( R_g\)-\( D_4\) to charge gate capacitor \( C_{gs} \).

The RMS current is

\[
I_{\text{RMS, } t21} = I_{G\rightarrow \text{on}} \sqrt{t_{21} f_s} \quad (5.10)
\]

The average value is

\[
I_{\text{Aver, } t21} = I_{G\rightarrow \text{on}} t_{21} f_s \quad (5.11)
\]

The total conduction loss is

\[
P_{t21} = I_{\text{RMS, } t21}^2 R_{DS(on)} + I_{\text{RMS, } t21}^2 R_g + I_{\text{Aver, } t21} V_F \quad (5.12)
\]

From (5.10), (5.11) and (5.12), (5.13) is obtained

\[
P_{t21} = I_{G\rightarrow \text{on}}^2 t_{21} f_s (R_{DS(on)} + R_g) + I_{G\rightarrow \text{on}} V_F t_{21} f_s \quad (5.13)
\]

where \( R_{DS(on)} \) is the on-resistance of \( S_1\)-\( S_4 \), assuming \( S_1\)-\( S_4 \) are same, \( R_g \) is the gate mesh resistance and \( V_F \) is the diode forward voltage.

Interval \([t_2, t_3]\) [see Figure 5.3(c)]: The inductor current path is \( S_3\)-\( D_4\)-\( S_1 \).

The RMS current is

\[
I_{\text{RMS, } t32} = I_{G\rightarrow \text{on}} \sqrt{\frac{t_{32} f_s}{3}} \quad (5.14)
\]

The average value is

\[
I_{\text{Aver, } t32} = I_{G\rightarrow \text{on}} \frac{t_{32} f_s}{2} \quad (5.15)
\]

The total conduction loss is

\[
P_{t32} = 2I_{\text{RMS, } t32}^2 R_{DS(on)} + I_{\text{Aver, } t32} V_F \quad (5.16)
\]

From (5.14), (5.15) and (5.16), (5.17) is obtained
To simplify the analysis, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed CSD is two times the sum of $P_{110}$ plus $P_{21}$ plus $P_{32}$ as given by (5.18).

\[ P_{\text{cond}} = P_{110} + P_{21} + P_{32} \]  
   \[ (5.18) \]

2) Current-Source Inductor Loss

The copper loss of the inductor winding is

\[ P_{\text{copper}} = R_{ac} \cdot I_{L_{RMS}}^2 \]  
   \[ (5.19) \]

where $R_{ac}$ is the AC resistance of the inductor winding and $I_{L_{RMS}}$ is the RMS value of the inductor current.

Core loss of the inductor should be also included. The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components. If air core inductors are used, the core loss is zero.

3) Gate Drive Loss

The gate drive loss of $S_1$-$S_4$ is

\[ P_{\text{gate}} = 4 \cdot Q_{g_{s,s}} \cdot V_{gs_{s,s}} \cdot f_s \]  
   \[ (5.20) \]

where $Q_{g_{s,s}}$ is the total gate charge of a drive switch and $V_{gs_{s,s}}$ is the drive voltage, which is typically 5V.

5.4.2 Design Example

For the given application, in order to achieve fast switching speed, the gate drive current (pre-charge current) should be chosen by the designer properly. The design tradeoff is between switching speed, which translates into reduced switching loss or reduced body diode conduction, and gate drive loss. Higher gate charge current results greater conduction loss in the CSD. Once
the gate charge current is chosen, we could decide the pre-charge time. In order to minimize the delay in the control loop, the pre-charge time $t_{10}$ should be smaller. For 1MHz switching frequency, the pre-charge time $t_{10}$ is typically 15ns (2% of the switching period). For the continuous CSD in Chapter 3, the optimal drive current for the control MOFET in the buck converter is 1.5A as discussed in section 4.2.4. Since the inductor current is discontinuous in the CSD proposed here, the circulating loss is small, and thus the drive current can be increased to about 2A. However, to increase the drive current further over 2A will result in too much drive loss and reduce the overall efficiency.

From (5.4), (5.21) is obtained to calculate the required inductor value

$$L_r = \frac{t_{10} V_D}{2 i_G}$$  \hspace{1cm} (5.21)

For $t_{10}=15$ns, $V_D=5V$ and $i_G=2.2A$, the required inductor value is 17nH.

The CSD parameters and components are given in Table 5.1. Using (5.18)-(5.20) and the parameters in Table 5.1, Figure 5.10 shows the loss breakdown of the proposed CSD. It is noted that compared to the voltage source driver, the total gate drive loss is reduced by 67.8% with the proposed CSD.

<table>
<thead>
<tr>
<th>Table 5.1 CSD design parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Circuit Parameters</strong></td>
</tr>
<tr>
<td>Switching Frequency, $f_s$</td>
</tr>
<tr>
<td>Gate Drive Voltage, $V_D$</td>
</tr>
<tr>
<td><strong>MOSFET</strong></td>
</tr>
<tr>
<td>Total Gate Charge@$V_{gs}=5V$</td>
</tr>
<tr>
<td>Internal Gate Resistance, $R_g$</td>
</tr>
<tr>
<td><strong>Driver Switches $S_1-S_2$</strong></td>
</tr>
<tr>
<td>Diode Forward Voltage, $V_F$</td>
</tr>
<tr>
<td>On Resistance $R_{DS(on)}$</td>
</tr>
<tr>
<td>Total Gate Charge@$V_{gs}=5V$:</td>
</tr>
<tr>
<td><strong>Driver Inductor $L_r$</strong></td>
</tr>
<tr>
<td>Inductor Value $L_r$</td>
</tr>
<tr>
<td>Driver Inductor Resistance</td>
</tr>
</tbody>
</table>

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5.5 Experimental Results and Discussion

5.5.1 Switching Loss Reduction with The Proposed High Side CSD

The first experiment is to verify the switching loss reduction with the high side CSD for a 12V input buck converter. The circuit diagram of the experimental prototype is shown in Figure 5.11.

The idea to use the proposed CSD is to achieve fast switching speed and reduce the switching loss of the control MOSFET in a buck converter. Conventional voltage source driver is used for the SR MOSFET for its simplicity, good immunity and alleviation of $dv/dt$ effect as the switching loss for SR is minimum.
Figure 5.11 The proposed discontinuous CSD diagram in the experiment

The specifications of the buck converter prototype are as follows: input voltage $V_{in}=12\,\text{V}$; output voltage $V_o=1.0\text{V}-1.5\text{V}$; output current $I_o=25\,\text{A}$; switching frequency $f_s=1\,\text{MHz}$; gate driver voltage $V_c=5\,\text{V}$. The PCB is six-layer with 4 oz copper. The components used in the circuit are listed as follows: $Q_1$: Si7860DP; $Q_2$: irf6691; output filter inductance: $L_f=300\,\text{nH}$ (IHLP-5050CE-01, Vishay); current-source inductors: $L_r=18\,\text{nH}$ (SMT 1812SMS-22N, Coilcraft); drive switches $S_1-S_4$: FDN335.

A photo of the prototype is illustrated in Figure 5.12. The driver was built using discrete components and an Altera Max II EPM240 CPLD was used to generate the driver gate signals as illustrated in Figure 5.12 (a). Surface mount (SMT) air core was used for the inductor as illustrated in Figure 5.12 (b).
Figure 5.12 Photo of the synchronous buck prototype with the hybrid gate driver

Figure 5.13 shows the gate drive signal for the four drive MOSFETs $S_1$-$S_4$ from the CPLD. All waveforms agree with the theory in Figure 5.2. Most notably, the pre-charge intervals are indicated as 20ns.

Figure 5.13 Gate signals of drive MOSFETs $S_1$-$S_4$

Figure 5.14 shows the inductor current $i_{Lr}$ and gate drive signals $v_{gS,Q1}$ (control MOSFET). Its peak current value is 2.0A, which is the optimized value of the CSD drive current. The inductor current is discontinuous as expected. During the pre-charge time, the current ramps up linearly. After the pre-charge time, the inductor current continues to ramp up while charging the gate capacitance of the Si7860DP power MOSFET during the turn on interval. During this interval the average drive current is approximately 2.0A and the power MOSFET voltage charges
from 0V to $V_D=5V$. After the power MOSFET turns on, the inductor current ramps back down to zero while the inductor energy is returned to drive voltage source.

![Figure 5.14 Inductor current and the gate-to-source voltage at 1MHz](image)

Figure 5.14 Inductor current and the gate-to-source voltage at 1MHz

Figure 5.15 shows the gate drive signals $v_{gs\_Q1}$ (control MOSFET) and $v_{gs\_Q2}$ (SR). It is observed that $v_{gs\_Q1}$ is smooth since the miller charge is removed fast by the constant inductor drive current. Moreover, the total rise time and fall time of $v_{gs\_Q1}$ is less than 15ns, which means fast switching speed. The dead time between two drive voltages is fixed to avoid shoot-through and is minimized to reduce the SR body diode conduction loss.

![Figure 5.15 Gate signals $v_{gs\_Q1}$ (control MOSFET) and $v_{gs\_Q2}$(SR)](image)
Figure 5.16 shows the drain-to-source voltage \( v_{ds,Q2} \) of the SR at the load current of 25A. It can be seen from \( v_{ds,Q2} \) that the body diode conduction time is small, which reduces the conduction loss and the reverse recovery loss of the body diode. It should be also noted that adaptive control or predictive of the voltage source driver can also be applied to the hybrid gate driver.

A benchmark of a synchronous buck converter with the conventional gate driver was built. The Predictive Gate Drive UCC 27222 from Texas Instruments was used as the conventional voltage driver. Figure 5.17 shows the measured efficiency comparison for the hybrid gate driver and the conventional gate driver at 1.3 V output. It is observed that at 25A, the efficiency is improved from 80.7% to 85.4% (an improvement of 4.7%) and at 30A, the efficiency is improved from 77.9% to 83.9% (an improvement of 6%).
Vin = 12V, Vo = 1.3V, Fs = 1MHz

Figure 5.17 Efficiency comparison: top: hybrid CSD; bottom: conventional voltage driver (Conv.)

Figure 5.18, Figure 5.19 and Figure 5.20 show the measured efficiencies for the CSD with different output voltages and load currents at 1MHz, 750KHz and 500KHz respectively. It is pointed that the same power train and parameters were used for efficiency measurement with different switching frequencies.

Figure 5.18 Efficiency with different output voltages and currents at 1MHz

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Figure 5.19 Efficiency with different output voltages and currents at 750KHz

Figure 5.20 Efficiency with different output voltages and currents at 500KHz

Figure 5.21 shows the measured efficiency for the CSD at different load currents and $V_o=1.3V$ when the switching frequency changes. It is observed that at the load current of 30A, when the switching frequency changes from 1MHz to 500KHz, the efficiency is improved from
83.9% to 87%.

![Efficiency graph](image)

Figure 5.21 Efficiency with different currents and switching frequencies at $V_o=1.3V$

### 5.5.2 Gate Energy Recovery with The Proposed Low Side CSD for SRs

The second experiment is to verify the gate energy recovery of the proposed CSD. Typically, high gate drive voltage helps to reduce the MOSFET $R_{DS(on)}$ and conduction loss. The SR MOSFET usually has high total gate charge. However, it also increases the gate drive loss. Typically, the gate drive voltage of 6V-7V gives a good tradeoff between the conduction loss and the gate drive loss. In addition, in high current application, more SR MOSFETs are often paralleled to reduce $R_{DS(on)}$ and thus the conduction loss. In this experimental test, the proposed low side CSD is used to drive two paralleled IRF6691 as SRs. The CSD with the same components and parameters is tested. The conventional gate driver chip ISL6208 [63] from Intersil is used for the same SR MOSFETs for comparison.

Figure 5.22 and Figure 5.23 illustrate the gate drive voltages of the SR with the proposed CSD at 1MHz and 2MHz respectively. In both Figures, it is observed that the turn on and turn off transition time is less 20ns, which means that the proposed CSD achieves fast turn on and turn off speed of the SR MOSFET.
The measured losses are listed in Table 5.2. Three different drive voltages of 5V, 6V and 7V are tested under different switching frequency condition. It is observed that when the gate driver voltage increases, the loss difference (Δ loss) increases, which means the CSD is more effective with high drive gate drive voltages to reduce $R_{DS(on)}$ conduction loss. For example, $R_{DS(on)}$ of IRF6691 [64] is reduced from 2.5Ω @ $V_{GS}=5V$ drive voltage to 1.9Ω @ $V_{GS}=7V$ (a reduction of 24%). In Table 5.2, it is noted that with $V_D=7V$ and the switching frequency of 2MHz, the gate loss reduction with the CSD is as much as 2.24W, a reduction of 63% with the voltage source.
Table 5.2 Measured loss comparison of proposed CSD and conventional (Conv.) voltage driver

<table>
<thead>
<tr>
<th>Switching Frequency</th>
<th>$V_d=5V$</th>
<th>$V_d=6V$</th>
<th>$V_d=7V$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CSD (W)</td>
<td>Conv. (W)</td>
<td>Δ Loss (W)</td>
</tr>
<tr>
<td>800kHz</td>
<td>0.28</td>
<td>1.07</td>
<td>0.79</td>
</tr>
<tr>
<td>1.0MHz</td>
<td>0.35</td>
<td>1.10</td>
<td>0.75</td>
</tr>
<tr>
<td>1.2MHz</td>
<td>0.41</td>
<td>1.30</td>
<td>0.89</td>
</tr>
<tr>
<td>1.5MHz</td>
<td>0.52</td>
<td>1.40</td>
<td>0.88</td>
</tr>
<tr>
<td>1.8MHz</td>
<td>0.60</td>
<td>1.50</td>
<td>0.90</td>
</tr>
<tr>
<td>2.0MHz</td>
<td>0.65</td>
<td>1.62</td>
<td>0.97</td>
</tr>
</tbody>
</table>

5.5.3 Wide Operation Range of Duty Cycle and Switching Frequency of The Proposed CSD

The third experiment is to verify the wide operation range of duty cycle and switching frequency of the proposed CSD.

For the switching frequency variation, Figure 5.24 and Figure 5.25 illustrate the proposed drive circuit operates with the switching frequency of 300kHz and 500kHz. It is observed that the CSD can operate with different switching frequencies. Because the drive circuit operate with discontinuous inductor current, the inductor current is only decided by the pre-charge time even if the switching frequency changes. Therefore, the small inductance can be used in a wide switching frequency range. This is also a great advantage for VRM application, in which the switching frequency may be reduced to achieve high light load efficiency.
Figure 5.24 Inductor current and the gate-to-source voltage at 300kHz

Figure 5.25 Inductor current and the gate-to-source voltage at 500kHz

For the step change of the duty cycle, Figure 5.26 and Figure 5.27 illustrate the duty cycle changes from $D=0.1$ to $D=0.8$ and from $D=0.8$ to $D=0.1$ respectively. It is observed that the proposed CSD can respond fast when duty cycle has a step change. This is of great benefit for the VRM application with fast dynamic response requirement.
Figure 5.26 Gate signals $v_{gs_{Q1}}$ (control MOSFET) from $D=0.1$ to $D=0.8$

Figure 5.27 Gate signals $v_{gs_{Q1}}$ (control MOSFET) from $D=0.8$ to $D=0.1$

5.6 Conclusions

In this chapter, a new discontinuous CSD is proposed. Compared to other CSDs proposed in previous work, the most important advantage of the new CSD is the small inductance (typically, 20nH at 1MHz switching frequency). Other features of the proposed discontinuous CSD include: 1) discontinuous inductor current with low circulating loss; 2) fast switching speed and reduced switching loss; 3) wide range of duty cycle and switching frequency; 4) high noise immunity.
A hybrid gate drive scheme for a synchronous buck converter is also proposed in this chapter to take advantage of the new CSD. The key idea of the hybrid gate driver scheme is to achieve switching loss reduction using the CSD. A 12V input, 1.3V output synchronous buck converter with the switching frequency of 1MHz was built to verify the advantages of the proposed CSD. At 1.3V output, the proposed CSD improves the efficiency from 80.7% using a voltage source driver to 85.4% (an improvement of 4.7%) at 25 A, and at 30A, from 77.9% to 83.9% (an improvement of 6%).

In additional, the proposed CSD can also achieve gate energy recovery. Two paralleled SR MOSFETs (IRF6691x2) are used to verify gate energy recovery with different switching frequencies and gate driver voltages. At $V_d=7\text{V}$ and the switching frequency of 2MHz, the gate loss reduction with the CSD is as much as 2.24W, a reduction of 63% with the voltage source driver. The wide operation range of duty cycle and switching frequency is also verified by the experiment results.
Chapter 6
New ZVS Non-Isolated Full Bridge Topologies with Gate Energy Recovery

6.1 Introduction

In section 2.5, the state of the art solutions for 12V input VRMs are analyzed in details. Multiphase synchronous buck converters are almost used exclusively in 12V VRMs due to the simplicity and minimum components. However, buck converters suffer from extremely low duty cycle problem with the output voltage is around 1.0V-1.5V, and the problem will become even worse when the output voltage is sub 1V. In terms of efficiency, the low duty cycle causes high turn-off loss due to the parasitics as the control MOFET is turned off at load currents. It also degrades the dynamic response of VRMs.

In order to solve the above problems, desired topologies should feature the following advantages: 1) soft-switching capability; 2) self-driven capability with the gate energy recovery; 3) good dynamic response.

The objective of this chapter is to present a new ZVS self-driven non-isolated FB converter. The proposed topology achieves duty cycle extension and features ZVS, self-driven capability with SR gate energy recovery and reduced voltage stress over the SRs. Owing to the duty cycle extension, lower output inductors can be used and the reverse recovery loss of the body diodes can also be reduced. In addition, existing multiphase buck controllers and buck drivers can be used directly for the proposed converter and no special control is needed. All these features improve the efficiency greatly to achieve high switching frequency and fast dynamic response.

**The content of this chapter is subject to U.S. patent pending, and is in press in the following conference:
This chapter is organized as follows: section 6.2 presents the derivation of the proposed converter and its principle of operation; section 6.3 presents the analysis of duty cycle loss; section 6.4 presents ZVS condition; section 6.5 presents loss comparison; section 6.6 demonstrates the advantages; section 6.7 presents the experimental results. Section 6.8 gives the conclusion.

6.2 Proposed ZVS Self-Driven Non-Isolated FB VRM

In this section, the derivation of the proposed non-isolated topology and its operation will be described in detail. The objective of this chapter is to propose a new topology so that the high switching loss is reduced significantly and the narrow duty cycle is extended in a buck converter. At the same time, the exiting drivers and controllers can be directly used with low cost and design efforts. The basic idea is to combine the two bridge legs of the isolated FB converter as the drive switches for the SRs. This driver serves as a CSD for the SRs and it eliminates any external SR drivers or auxiliary driver winding. Furthermore, due to the CSD structure, the gate energy of the SR MOSFETs can also be recovered. This will help to apply high gate drive voltage to the SRs for lower $R_{DS(on)}$ and lower conduction loss.

6.2.1 Derivation of Proposed ZVS Non-Isolated FB VRM

Figure 6.1 illustrates the derivation of the proposed ZVS self-driven converter. Figure 6.1 (a) shows the conventional isolated FB converter with current doubler rectifier for high current applications. $V_{in}$ is the input voltage, $Q_1$-$Q_4$ are the control MOSFETs, $T_i$ is the power transformer ($n$ is the turns ratio), $L_k$ is the leakage of the transformer, $Q_5$-$Q_6$ are the SR MOSFETs, $L_1$ and $L_2$ are the output filter inductors and $C_o$ is the output filter capacitor. The derivation of the proposed converter includes the following steps:

1) In order to achieve fast switching and gate energy recovery, the dual low side CSD proposed in [38], is used to drive SR $Q_5$ and $Q_6$, as shown in Figure 6.1 (b). In the CSD, $S_1$-$S_4$ are
the gate drive switches, $L_r$ is the current-source inductor and $V_c$ is the drive voltage. According to the operation in [38], in order to achieve the desired drive waveforms for $Q_5$ and $Q_6$, asymmetrical control is used for $S_1$-$S_4$.

2) It should be observed that for 12V input VRM applications, there is no requirement for isolation between the primary side and secondary side. So it is possible to have the primary side of the transformer share the same ground of the secondary side as indicated in Figure 6.1 (b).

3) It is interesting to note that the dual low side CSD is also a full-bridge structure. Though phase-shift control is generally used for the conventional FB converter, the asymmetrical control featuring ZVS capability can also be applied to two bridge legs of the FB converter respectively, while the voltage applied to the primary side of the transformer is still symmetrical. The other benefit of the asymmetrical control is that existing buck drivers can be directly used to drive the upper and lower MOSFETs in one bridge leg. Therefore, the drive switch pairs ($S_1$&$S_2$ and $S_3$&$S_4$) can merge with the control MOSFETs ($Q_1$&$Q_2$ and $Q_3$&$Q_4$) of the primary side, respectively, as indicated in Figure 6.1 (c). At the same time, the inductor $L_r$ can merge with the leakage inductance $L_k$. The primary side of the transformer shares the same ground as the second side, which can provide the gate drive currents a path for the SRs $Q_5$ and $Q_6$. Therefore, by connecting the bridge leg midpoints of $A$ and $B$ to the gate terminals of $Q_5$ and $Q_6$, as shown in Figure 6.1 (d), the proposed FB converter can be derived. Thus $V_{in}$ becomes the SR gate drive voltage.

Since the drive switches in the CSD emerge with the main power MOSFETs in the proposed converter, there is no additional control required for the SRs. In addition, the inductor is not required anymore, which helps to reduce the size of the converter and increase the power density. Meanwhile, owing to the gate energy recovery of the CSD, high gate drive voltage can be applied to SR $Q_5$ and $Q_6$ to reduce the conduction losses further.
Figure 6.1 Proposed ZVS self-driven non-isolated FB converter
6.2.2 Principle of Operation

The key waveforms of the proposed topology are shown in Figure 6.2. The inductor currents \( i_{L1} = i_{L2} = I_o / 2 \), where \( I_o \) is the total output current neglecting the current ripples of the output inductors. The output inductors are large enough to be regarded as current sources.

For each leg, the purpose of the asymmetrical control is that \( Q_1 \) and \( Q_2 \), and \( Q_3 \) and \( Q_4 \) are controlled complementarily with the dead time to achieve ZVS. It is noted that the primary voltage \( v_{AB} \) is still a symmetrical waveform. In this case, \( Q_1 \) and \( Q_3 \) are the upper control MOSFETs; \( Q_2 \) and \( Q_4 \) are the lower control MOSFETs.

![Figure 6.2 Key waveforms of the proposed topology](image_url)
The duty cycle $D$ of the new converter is defined as

$$D = \frac{T_{on\_Q2}}{T_s} \tag{6.1}$$

where $T_{on\_Q2}$ is the on time of $Q_2$ and $T_s$ is the switching period.

There are twelve switching modes in a switching period. The equivalent circuits in half of a switching cycle are shown in Figure 6.3 accordingly. $D_1$-$D_4$ are the body diodes and $C_1$-$C_4$ are the intrinsic output capacitors of $Q_1$-$Q_4$ respectively, assuming $C_1=C_2=C_3=C_4=C_{oss}$. $D_5$ and $D_6$ are the body diodes and $C_{gs\_Q5}$ and $C_{gs\_Q6}$ are the input capacitors of SR $Q_5$ and $Q_6$ respectively, assuming $C_{gs\_Q5}=C_{gs\_Q6}=C_{gs}\_\text{Q}$. 

1) Mode 1 $[t_0, t_1]$ [Figure 6.3 (a)]: Prior to $t_0$, $Q_1$ and $Q_3$ are on, the voltages over the primary side and the secondary side of the transformer are zero. The gate drive voltages of the SR $Q_5$ and $Q_6$ are all clamped high to the input voltage. At $t_0$, $Q_1$ turns off, the primary current $i_p$ charges $C_1$ and discharges $C_2$ and $C_{gs\_Q6}$ at the same time. As $C_1$ and $C_2$ and $C_{gs\_Q6}$ limit the slew rate of the voltage of $C_1$, $Q_1$ is under zero-voltage turn-off condition. It should be noted that the gate drive energy of the SR capacitance $C_{gs\_Q6}$ is returned to the input voltage source so that the high gate drive losses of SRs can be reduced.

During this stage, the energy to discharge $C_2$ and $C_{gs\_Q6}$ is provided by the leakage inductance of the transformer. $i_p$ decreases resonantly as

$$i_p(t) = \frac{I_o}{2n} \cdot \cos \omega_r (t-t_0) \tag{6.2}$$

$$v_{c2} = v_{gs\_Q6} = V_{in} - Z_r \cdot \frac{I_o}{2n} \cdot \sin \omega_r (t-t_0) \tag{6.3}$$

where $\omega_r = 1/\sqrt{L_k (2C_{oss} + C_{gs})}$ and $Z_r = \sqrt{L_k / (2C_{oss} + C_{gs})}$.

At $t_1$, $v_{c1}=V_{in}$ and $v_{c2}=0$, $D_2$ conducts, which provide a zero-voltage turn-on condition for $Q_2$. The interval of $[t_0, t_1]$ and the value of $i_p$ at $t_1$ are
\[ t_{1,0} = \frac{1}{\omega_r} \sin^{-1} \left( \frac{2nV_{in}}{Z_r \cdot I_o} \right) \]  

(6.4)

\[ I_p(t_1) = \frac{I_o}{2n} \sqrt{1 - \left( \frac{2nV_{in}}{Z_r \cdot I_o} \right)^2} \]  

(6.5)

2) Mode 2 \([t_1, t_3]\) [Figure 6.3 (b)]: During this stage, \(i_p\) decreases and is not enough to power the load. \(i_{L1}\) freewheels through the body diode \(D_6\) and \(i_{L2}\) freewheels through \(Q_5\). At \(t_2\), \(i_p\) increases inversely but is still not large enough to power the load.

3) Mode 3 \([t_3, t_4]\) [Figure 6.3 (c)]: At \(t_3\), \(i_p\) rises to the reflected load current causing \(D_6\) to turn off. During this stage, the voltage over the transformer is the input voltage and the energy transfers from the primary side of the transformer to the load.

4) Mode 4 \([t_4, t_5]\) [Figure 6.3 (d)]: At \(t_4\), \(Q_2\) turns off, the primary current \(i_p\) charges \(C_2\) and \(C_{gsQ6}\) and discharges \(C_1\). As \(C_1\) and \(C_2\) and \(C_{gsQ6}\) limit the slew rate of the voltage of \(C_2\), \(Q_2\) is under zero-voltage turn-off condition. During this stage, the energy to discharge \(C_1\) is provided by the leakage inductance and \(L_1\). \(L_1\) is large enough to be regarded as a constant current source so that the primary current \(i_p\) keeps the value \(I_{p2} = I_o/2n\). The voltage \(C_2\) rises linearly and the voltage of \(C_2\) decays linearly.

\[ t_{5,4} = \frac{2nV_{in}(2C_{oss} + C_{gs})}{I_o} \]  

(6.6)

5) Mode 5 \([t_5, t_6]\) [Figure 6.3 (e)]: At \(t_5\), \(D_1\) conducts, which provides a zero-voltage turn-on condition for \(Q_1\). The voltage over the primary side is zero. The gate drive voltages of the SR \(Q_5\) and \(Q_6\) are all clamped high to the input voltage again. At \(t_6\), the other half of switching cycle starts and the principle of operation is similar except for polarity changes.
(a) $[t_0, t_1]$

(b) $[t_1, t_3]$

(c) $[t_3, t_4]$
6.2.3 Multiphase Interleaving Non-Isolated ZVS Self-Driven Converters

With the increasing high current demanding of the microprocessors, the output current of the VRMs for desktop and server is beyond 100A and will reach 150A in the near future. In order to meet this high current requirement, multiphase buck converters are widely used as the solution of today’s VRM architecture. However, as mentioned before, the buck converter has low efficiency due to the high turn-off loss at high frequency (>1MHz).

To provide high output current (>100A), two proposed non-isolated ZVS self-driven FB converters can be paralleled as shown in Figure 6.4. The gate drive control signals for each bridge can be interleaved to achieve ripple cancellation effect. All the advantages of the proposed non-
isolated ZVS self-driven FB converter are maintained in this structure. Additionally, commercial available multiphase buck converter controller can be directly used for the control of the converter.

![Figure 6.4 Non-isolated ZVS self-driven FB converters with parallel configuration](image)

6.2.4 Three Phase Non-Isolated ZVS Self-Driven FB Converter with Current Tripler Rectifier

Since the switching losses are much reduced owing to ZVS, the SR conduction losses become dominant losses in the new topology. A three phase self-driven non-isolated topologies are proposed to reduce the SR conduction loss, while all the advantages of the original converter as shown in Figure 6.1(d) are maintained.

Figure 6.5 shows the proposed three phase non-isolated ZVS self-driven FB converter with current tripler rectifier. In Figure 6.5, $Q_1$-$Q_6$ are the control MOSFETs, $S_1$-$S_3$ are the SR MOSFETs, $L_1$, $L_2$ and $L_3$ are the output filter inductors and $C_o$ is the output filter capacitor. In this configuration, three transformers $T_1$, $T_2$ and $T_3$ (turn ration $n$) are organized with a delta ($\triangle$) connection. The midpoints $(a, b, c)$ of each bridge leg are connected to the gate terminals of $S_1$-$S_3$.
to drive the SRs respectively.

Figure 6.5 Proposed three phase non-isolated ZVS self-driven FB converter with current tripler rectifier

Figure 6.6 illustrates the key waveforms of the proposed converter. Similar to Figure 6.2, $Q_1$ and $Q_2$, $Q_3$ and $Q_4$ as well as $Q_5$ and $Q_6$ are three bridge legs, which are controlled complementarily with the dead time set to achieve ZVS. It is noted that the control MOSFETs $Q_1$, $Q_2$ and $Q_3$ are phase-shifted 120 degrees to achieve interleaving. Due to the interleaving control of control MOSFETs, the primary-side currents $i_{ab}$, $i_{bc}$ and $i_{ca}$ are 120 degrees phase-shifted as seen from Figure 6.6. Therefore, the magnetic field in each core is 120 degrees phase shifted, which allows for a magnetic flux cancellation effect. Therefore, these three transformers ($T_1$, $T_2$ and $T_3$) can be integrated into one magnetic core, which is similar to an AC three-phase transformer.
Figure 6.6 Key waveforms of the three phase non-isolated ZVS self-driven FB converters
From the waveform of $i_{S1}$ in Figure 6.6, the RMS current of SR $S_1$ with current tripler is

$$I_{S1\_RMS} = \sqrt{\frac{1}{3} \left( \frac{I_o}{3} \right)^2 + \frac{1}{3} \left( \frac{2I_o}{9} \right)^2} = \frac{\sqrt{15}}{9} I_o \approx 0.43I_o \quad (6.7)$$

The RMS value of the secondary winding current with current tripler is

$$I_{Sec\_RMS} = \sqrt{\frac{1}{3} \left( \frac{2I_o}{9} \right)^2 + \frac{2}{3} \left( \frac{I_o}{9} \right)^2} = \frac{\sqrt{2}}{9} I_o \approx 0.16I_o \quad (6.8)$$

The RMS current of SR MOSFET $S_1$ of the current doubler as shown in Figure 6.2 is

$$I_{S1\_RMS} = \sqrt{\frac{1}{2} I_o} \approx 0.71I_o \quad (6.9)$$

The RMS value of the secondary winding current with the current doubler is

$$I_{Sec\_RMS} = \frac{I_o}{2} = 0.5I_o \quad (6.10)$$

For example, $V_{in}=12V$, $V_o=1.0V$ and total load current 120A, in order to do the fair comparison, each phase is assumed to proved 20A. So we can use three ZVS self-driven FB VR converters to parallel and each of them provides $I_o=40A$. According to (6.9), the RMS current of each SR MOSFET is 28.4A. Assuming $R_{DS(on)}$ of each SR is 1.6mΩ and 6 SRs are used, the total SR conduction loss is 7.7W ($6I_{RMS}^2 R_{DS(on)}=6\times28.4^2\times1.6mΩ$). However, for the three-phase non-isolated ZVS self-driven FB converter with current tripler as shown in Figure 6.5, we need two converters to parallel and each of them provides $I_o=60A$. According to (6.7), the RMS current of each SR MOSFET is 25.8A and 6 SRs are used. So the total conduction loss of SR MOSFETs is 6.4W ($6I_{RMS}^2 R_{DS(on)}=6\times25.8^2\times1.6mΩ$). This leads to a SR conduction loss reduction of 1.3W (7.7W-6.4W), which is a reduction of 17% (1.3W/7.7W) of the total SR conduction loss and 1.1% of the output power, 1.3W/(1.0V×120A).

Similarly, for the high current secondary winding loss, the RMS current with current tripler is 9.6A from (6.8) and $P_{winding\_tripler}=9.6^2\times6R_{dc}$ since there are 6 secondary windings. However, for
the current doubler, the RMS current of the secondary winding is 20A from (6.10) and 
\[ P_{winding\_doubler} = 20^2 \times 3R_{ac} \]  
since there are 3 secondary windings. Therefore, the total secondary winding loss reduction is 55.8% \((1 - P_{winding\_tripler} / P_{winding\_doubler})\), assuming the same secondary winding AC resistance \(R_{ac}\).

6.2.5 ZVS Self-Driven Non-Isolated FB Converter with Reduced Gate Drive Voltage

From the analysis in section 6.2, the proposed self-driven non-isolated full-bridge converter has advantages over the conventional buck converter. However, the gate drive voltage of SR MOSFETs reaches the input voltage (usually 12V), which might not be the optimized gate drive voltage of SRs since the \(R_{DS(on)}\) of SRs usually does not decrease a lot when the gate drive voltage over about 7V. In the near future, the low voltage rating SRs with round 12V can only sustain less than 10V gate drive voltage. Therefore, the input voltage 12V will not be suitable to drive these low voltage rating SRs anymore. In this section, an improved ZVS self-driven FB topology with reduced the gate drive voltage is proposed to solve the above mentioned problems.

Figure 6.7 illustrates the proposed converter with reduced gate drive voltage using the voltage divider. \(C_{gs\_Q5}\) and \(C_{gs\_Q6}\) are the internal gate capacitance of SR \(Q5\) and \(Q6\). \(C_s, C_{s2}, R_1, R_2, R_3\) and \(R_4\) with \(C_{gs\_Q5}\) and \(C_{gs\_Q6}\) form voltage dividers.

![Figure 6.7 Proposed ZVS self-driven FB VRM with reduced gate drive voltage using voltage dividers](image)
Assuming $R_1=R_2=R_s$, $R_3=R_4=R_p$ and $C_{s1}=C_{s2}=C_s$, the gate drive voltage across of the SRs is

$$V_{\text{gs-Q5}} = V_{\text{gs-Q5}} = \frac{C_s \cdot V_{\text{in}}}{C_s + C_{\text{gs}}},$$

(6.11)

At the same time, in order to make the simultaneous gate drive voltage has the same phase with the voltage $v_A$ and $v_B$, (6.12) should be satisfied

$$C_s R_s = C_{\text{gs}} R_p$$

(6.12)

The most important advantage of the proposed circuits is that the gate voltage can be chosen for optimal design and safe operation when the input voltage value is not suitable to drive SRs directly due to either low gate voltage ratings of SRs. Figure 6.8 illustrate one example waveforms using the voltage driver. It is observed that the gate drive voltage $v_{\text{GS-Q5}}$ is in the same phase of $v_A$ and the gate voltage is reduced from 12V to 8V.

Figure 6.8 Waveforms of $v_A$ and reduced gate drive voltage $v_{\text{GS-Q5}}$ using voltage dividers: $V_{\text{in}}=12V$, $f_s=1\text{MHz}$, $R_1=R_2=21\text{K}\Omega$, $R_3=R_4=12\text{K}\Omega$, $C_{s1}=C_{s2}=3.3\text{nF}$ and $C_{\text{GS-Q5}}=C_{\text{GS-Q6}}=5.7\text{nF}$

6.3 Duty Cycle Loss

As shown in Figure 6.2, during $[t_0, t_3]$ and $[t_6, t_9]$, the leakage inductance of the transformer limits the rise (or decay) slope of $i_p$. Finite time is required for $i_p$ to make the transition from the
positive direction to the negative direction (or vice versa). During this transition time, \( v_{AB} \) is \(+V_{in}\) or \(-V_{in}\), \( i_p \) is lower than the reflected load current and all the SR diodes conduct. This makes the secondary rectified voltage \( v_A \) and \( v_B \) zero, thus \( v_{AB} \) loses the voltage in \([t_0, t_3]\) and \([t_6, t_9]\) respectively.

The duty cycle loss \( D_{loss} \) during \([t_0, t_3]\) and \([t_6, t_9]\) is

\[
D_{loss} = \frac{I_o \cdot L_k}{n \cdot T_s \cdot V_{in}} \quad (6.13)
\]

where \( I_o \) is the output current, \( L_k \) is the leakage inductance and \( n \) is the transformer turns ratio. It is noted that the leakage inductance of the transformer should be minimized to reduce the duty cycle loss.

### 6.4 Condition of ZVS

From Figure 6.3 (d), for the upper control MOSFETs \( (Q_1, Q_3) \), the energy to achieve ZVS is provided by the output inductors, so (6.14) should be satisfied

\[
\frac{1}{2} \cdot L_f \cdot \left(\frac{I_o}{2 \cdot n}\right)^2 \geq \frac{1}{2} \cdot C_1 \cdot V_{in}^2 + \frac{1}{2} \cdot (C_2 + C_{gs, Q_5}) \cdot V_{in}^2 = C_{oss} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{gs, Q_5} \cdot V_{in}^2 \quad (6.14)
\]

where \( L_f \) is the output filter inductance, \( C_1=C_2=C_{oss} \) (output capacitances of \( Q_2 \) and \( Q_4 \)) and \( C_{gs, Q_5} \) is the gate capacitance of \( Q_5 \). Since \( L_f \) is usually large enough to provide the energy, \( Q_1 \) and \( Q_3 \) can achieve ZVS in a wide load range.

From Figure 6.3 (a), for the lower control MOSFETs \( (Q_2, Q_4) \), the energy to realize ZVS is provided by the leakage inductance of the transformer, so (6.15) should be satisfied

\[
\frac{1}{2} \cdot L_k \cdot \left(\frac{I_o}{2 \cdot n}\right)^2 \geq \frac{1}{2} \cdot C_1 \cdot V_{in}^2 + \frac{1}{2} \cdot (C_2 + C_{gs, Q_5}) \cdot V_{in}^2 = C_{oss} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{gs, Q_5} \cdot V_{in}^2 \quad (6.15)
\]

where \( L_k \) is the leakage inductance of the transformer. It is noted that the larger leakage inductance, the easier to achieve ZVS. However, the larger leakage inductance results in higher duty cycle loss. The leakage inductance \( L_k \) can be chosen based on (6.16) depending on ZVS
\[ L_k \geq \frac{2C_{oss} \cdot V_{in}^2 + C_{gs-Q5} \cdot V_{in}}{\left( \frac{I_{o-ZVS}}{2n} \right)^2} \]  

(6.16)

As an example, for \( V_{in} = 12 \text{V}, V_o = 1.3 \text{V}, n = 3, C_{oss} = 0.65 \text{nF} \) and \( C_{gs-Q5} = 6.6 \text{nF} \), in order to achieve ZVS at \( I_{o-ZVS} = 40 \text{A} \), from (6.16), the leakage inductance can be calculated as 25nH.

### 6.5 Loss Analysis

A detailed loss analysis of the proposed converter in Figure 6.1(d) is given in this section. These losses include: 1) switching loss; 2) gate drive loss and conduction loss of control MOSFETs; 3) body diode conduction loss and reverse recovery loss; 4) gate drive loss and conduction loss of SRs; 5) loss of planar transformer; 6) conduction loss of output inductors.

#### 6.5.1 Switching Loss

Due to ZVS, there is no turn on losses for the control MOSFETs. The total turn off losses are

\[
P_{\text{turn-off}} = \frac{2}{n} \cdot V_{in} \cdot I_{(off)} \cdot t_{\text{sw-off}} \cdot f_s
\]

(6.17)

Where \( I_{(off)} \) is the turn off current and \( t_{\text{sw-off}} \) is the turn off transition time.

#### 6.5.2 Conduction Loss of Control MOSFETs

The RMS current flowing through \( Q_1 \) and \( Q_3 \) is

\[
I_{RMS1} = \frac{1}{2n} \cdot I_o \cdot \sqrt{1-D}
\]

(6.18)

where \( D \) is the duty cycle and the current ripples are neglected.

The RMS current flowing through \( Q_2 \) and \( Q_4 \) is

\[
I_{RMS2} = \frac{1}{2n} \cdot I_o \cdot \sqrt{D}
\]

(6.19)

From (6.18) and (6.19), the total conduction losses of \( Q_1-Q_4 \) is
where \( R_{DS_{\text{controlFET}}} \) is the on-resistance of \( Q_1-Q_4 \), assuming \( Q_1-Q_4 \) are the same.

From (6.20), it is also noted that though the asymmetrical control is applied, the total conduction loss of \( Q_1-Q_4 \) is independent of the duty cycle and is the same as the symmetrical control.

### 6.5.3 Gate Drive Loss of Control MOSFETs

The gate drive loss of \( Q_1-Q_4 \) is

\[
P_{\text{controlFET}} = 4 \cdot Q_g \cdot V_{gs} \cdot f_s
\]

(6.21)

where \( Q_g \) is the total gate charge of \( Q_1-Q_4 \), assuming \( Q_1-Q_4 \) are the same. \( V_{gs} \) is the gate drive voltage and is usually 5V. It should be pointed that the gate drive loss can be reduced since the \( Q_{gd} \) charge is eliminated due to the zero-voltage turn-on condition of the control MOSFETs. For example, for Vishay Si7368DP with \( Q_{gd}=4.5nC \) and \( Q_g=17nC \) at \( V_{gs}=5V \), the gate drive loss can be reduced by 26% for the primary control MOSFETs owing to ZVS.

### 6.5.4 Body Diode Conduction Loss and Reverse Recovery Loss

SR \( Q_6 \) is used to illustrate the calculating of the body diode conduction loss. Figure 6.9 illustrates the waveforms of SR \( Q_6 \) turn-on transition of and its corresponding equivalent circuit.
For the turn on transition \([t_4, t_5]\) of SR \(Q_6\), the primary current \(i_p\) is the reflected current from the load and charges \(C_2\) and \(C_{gs,Q6}\) linearly until \(v_{gs,Q6}\) reaches the input voltage at \(t_5\) causing SR \(Q_6\) to turn on. Then the primary side of the transformer is clamped at zero-state and \(i_p\) equals \(I_o/2n\). Though SR \(Q_6\) turns on before \(t_6\), the drain current of \(Q_6\) remains zero during the zero-state. Therefore, there is no body-diode conduction for the turn on transition of SR \(Q_6\), as shown in Figure 6.9 (a).

Figure 6.10 illustrates the waveforms of the turn-off transition of SR \(Q_6\) and its corresponding equivalent circuit. For the turn off transition \([t_0, t_1]\), at \(t_0\), \(Q_1\) turns off and the leakage inductance \(L_k\) starts to resonate with the capacitance \(C_2\) and \(C_{gs,Q6}\) until \(v_{gs,Q6}\) reaches zero at \(t_1\), which means SR \(Q_6\) turns off. The current through \(Q_6\) then transfers to the body diode \(D_6\) until \(i_p\) changes its polarity and reaches the load current of \(I_o/2n\) at \(t_3\). Therefore, from \(t_1\) to \(t_3\) as shown in the shaded area, the body diode conducts as shown in Figure 6.10 (b).
From (6.5), at $t_1$, the current of the body diode $I_{d,Q6}(t_1)$ is

$$I_{d,Q6}(t_1) = \frac{I_o}{2} \left[ 1 + \sqrt{1 - \left( \frac{2n V_{in}}{Z_r \cdot I_o} \right)^2} \right]$$

(6.22)

where $Z_r = \sqrt{L_k / (2C_{oss} + C_{gs})}$.

At $t_3$, $i_{d,Q6}$ reaches zero, so the conduction time of the body diode is

$$t_{13} = \frac{L_k \cdot I_o}{2n V_{in}} \left[ 1 + \sqrt{1 - \left( \frac{2n V_{in}}{Z_r \cdot I_o} \right)^2} \right]$$

(6.23)

From (6.22) and (6.23), the total conduction losses of the body diodes of the two SRs is

$$P_{body\_diode} = \frac{1}{2} I_{d,Q6}(t_1) \cdot V_F \cdot t_{13} \cdot f_s \cdot 2 = \frac{L_k \cdot I_o^2 \cdot V_F \cdot f_s}{4n V_{in}} \left[ 1 + \sqrt{1 - \left( \frac{2n V_{in}}{Z_r \cdot I_o} \right)^2} \right]^2$$

(6.24)

where $V_F$ is the forward voltage drop of the body diode. It is noted that the conduction loss of the body diode is proportional to the leakage inductance of the transformer. A larger leakage inductance results in a longer time required $[t_1, t_3]$, as shown in Figure 6.10 (b), for the primary
current to change its polarity, thus resulting in higher body diode conduction loss.

The parameters for the loss analysis and comparison are given in Table 6.1.

<table>
<thead>
<tr>
<th>Table 6.1 Parameters and components for loss analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage $V_{in}$/ Output Voltage $V_o$</td>
</tr>
<tr>
<td>Output Current $I_o$ (two phases)</td>
</tr>
<tr>
<td>Switching Frequency $f_s$</td>
</tr>
<tr>
<td><strong>Control MOSFET</strong></td>
</tr>
<tr>
<td>$Q_g@V_{GS}=5V$</td>
</tr>
<tr>
<td>$R_{DS(on)}@V_{GS}=5V$</td>
</tr>
<tr>
<td>$R_g$</td>
</tr>
<tr>
<td><strong>SR MOSFET</strong></td>
</tr>
<tr>
<td>$R_{DS(on)}@V_{GS}=12V$</td>
</tr>
<tr>
<td>$Q_g@V_{GS}=12V$</td>
</tr>
<tr>
<td>$V_f/ R_g/ Q_{rr}$</td>
</tr>
<tr>
<td><strong>Power Transformer</strong></td>
</tr>
<tr>
<td>Turns ratio</td>
</tr>
<tr>
<td>Core materials</td>
</tr>
<tr>
<td><strong>Output Inductor</strong></td>
</tr>
<tr>
<td>Inductance/ DCR</td>
</tr>
</tbody>
</table>

The leakage inductance of the power transformer has a direct impact on the body diode and ZVS range. The effect of the leakage on the body diode conduction loss from (6.24) is given in Figure 6.11. In order to reduce the body diode conduction loss, the leakage inductance needs to be minimized using the PCB planar transformer technique. At the same time, the lower leakage inductance will also help to reduce the duty cycle loss as seen from (6.13). However, this will reduce the range of ZVS operation. According to (6.16), if the range of ZVS operation is 2/3 of the load current ($I_o=60A$), the leakage inductance should be chosen as 25nH using the parameters.
in Table 6.1.

Figure 6.11 Body diode conduction loss as a function of output current (two phases) with different leakage inductances

The reverse recovery loss of the body diode is \( P_{rr} = Q_{rr} \cdot V_s \cdot f_s \), where \( V_s = V_{in}/n \), which is the block voltage of the SR body diode. For the buck converter, the switching node voltage \( V_s \) is 12V. For the proposed non-isolated FB converter with \( n=3 \), \( V_s \) is 4V. Therefore, the reverse recovery loss can be reduced by 67%.

**6.5.5 Conduction Loss of SRs**

From Figure 6.2, the RMS current of the SR is

\[
I_{SR\_RMS} = I_o \cdot \sqrt{(1 - D)}
\]  

(6.25)

So the conduction loss of the SRs is

\[
P_{\text{cond} \_SR} = 2I_{SR\_RMS}^2 \cdot R_{DS(on)\_SR} = 2 \cdot I_o^2 \cdot (1 - D) \cdot R_{DS(on)\_SR}
\]  

(6.26)

where \( R_{DS(on)\_SR} \) is the on resistance of the SR MOSFETs.

**6.5.6 Gate Drive Loss of SRs**

As discussed in section 6.2.1, the gate driver for the SR MOSFETs is actually a CSD, which can achieve gate energy recovery. The efficiency of the gate energy recovery depends on the gate
mesh resistance $R_g$. The equivalent circuits of the turn on transition and turn off transition of the SRs are given in Figure 6.12, assuming the output capacitance $C_{oss,Q3}=C_{oss,Q4}=C_{oss}$, gate capacitance $C_{gs,Q5}=C_{gs,Q6}=C_{gs}$ and $R_{g,Q5}=R_{g,Q6}=R_g$. As seen from Figure 6.12, the gate drive current goes through the MOSFET internal mesh resistance and causes resistive loss at $R_g$.

During the charging transition $[t_4, t_5]$, the primary current $i_p$ is the reflected load current, which means it can be regarded as a constant current source. The resistive loss through $R_g$ is

$$P_{R_{\text{on}}} = 2 \cdot \left( \frac{C_{gs}}{2C_{oss} + C_{gs}} \cdot \frac{I_o}{2n} \right)^2 R_g \cdot t_{5,4} \cdot f_s$$  \hspace{1cm} (6.27)

where $t_{5,4} = \frac{2nV_{in}(2C_{oss} + C_{gs})}{I_o}$ from (6.6).

During the discharging transition $[t_0, t_1]$, the primary current $i_p$ resonates with $C_{oss}$ and $C_{gs}$.

The resistive loss over $R_g$ is

$$P_{R_{\text{off}}} = 2 \cdot \int_0^{t_{1,0}} \left( \frac{C_{gs}}{2C_{oss} + C_{gs}} \cdot \frac{I_o}{2n} \cdot \cos \omega_t \cdot t \right)^2 R_g \cdot dt \cdot f_s$$  \hspace{1cm} (6.28)

where $t_{1,0} = \frac{1}{\omega_r} \cdot \sin^{-1} \left( \frac{2nV_{in}}{Z_r \cdot I_o} \right)$ from (6.4).

![Figure 6.12 Key waveforms of turn on transition and turn off transition of SR $Q_6$](image)

Figure 6.12 Key waveforms of turn on transition and turn off transition of SR $Q_6$
Using the parameters given in Table 6.1, a curve of the self-driven gate drive loss as a function of $R_g$ is given in Figure 6.13 to demonstrate the potential benefits of using MOSFETs with lower $R_g$.

![Graph showing the relationship between gate drive loss and internal gate resistance $R_g$.](image)

Figure 6.13 SR gate drive loss as function of MOSFET internal mesh resistance $R_g$

### 6.5.7 Loss of Planar Transformer

The loss of the power transformer includes the copper loss and the core loss.

The copper loss of the inductor winding is

$$ P_{copper} = R_{ac} \left( \frac{I}{2n} \right)^2 \quad (6.29) $$

where $R_{ac}$ is the AC resistance of the primary winding and $n$ is the turns ratio.

For the core loss, RM50 (TDK 3F5) is used for the experimental prototype. The loss $P_{core}$ can be calculated using (6.30) and (6.31),

$$ P_{core} = K_1 f_s x^{y} B_{pk}^{x} V_e \quad (6.30) $$

$$ B_{pk} = \frac{D V_{in}}{2 n A_e f_s} \quad (6.31) $$

For RM50 (TDK 3F5), with $K_1=0.0087$, $x=2.045$, $y=2.98$, $A_e=23.7 \text{ mm}^2$ and $V_e=530 \text{ mm}^3$, $P_{core}=0.2 \text{W}$. 

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6.5.8 Conduction Loss of Output Inductors

The conduction loss of the output inductor is

$$P_{\text{ind}} = \frac{I_o^2}{2} \cdot \left[1 + \left(\frac{\Delta i}{I_o/2}\right)^2\right] \cdot R_{dc}$$ (6.32)

where $\Delta i$ is the current ripple of the output inductor and $R_{dc}$ is the DC resistance of the output inductor. As compared with the buck converter, in order to maintain same inductor current ripple, due to the duty cycle extension, the output inductor value of the proposed converter is reduced from 300nH to 190nH (a reduction of 35%). This gives a reduction of $R_{dc}$ from 1.2Ω to 1.0Ω (a reduction of 20%), which means a reduction of 20% of the conduction loss.

6.5.9 Loss Comparison

Based on the loss analysis using the parameters in Table 6.1, Figure 6.14 illustrates the loss breakdown of the proposed converter. For comparison, Figure 6.14 also illustrates the loss breakdown of the two phase buck converter with $V_{in}=12\,\text{V}$, $V_o=1.3\,\text{V}$, $I_o=30\times2\,\text{A}$ and $f_s=1\,\text{MHz}$. The loss model in [11] is used to calculate the loss in a buck converter. ZVS feature of the proposed topology reduces the switching loss, especially the turn off loss (9.6W, 12.3% of the output power), in the buck converter. ZVS achievement also helps to reduce the EMI of the switching power converter. Thus, smaller EMI filters can be used. Other frequency dependent losses including body diode conduction loss, reverse recovery loss and gate drive loss are all reduced. In additional, the output inductor conduction loss is also reduced since lower value inductors can be used owing to the duty cycle extension. However, the SR conduction loss is increased due to the circulating currents in the FB structure topology and an additional transformer winding loss has to be taken into account. But The overall loss reduction is 4.2W, which translates into a reduction of 5.4% of the total output power, $4.2\,\text{W}/(1.3\,\text{V}\times60\,\text{A})$. 

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Figure 6.14 Loss breakdown comparison between the buck converter and self-driven ZVS FB converter

6.6 Advantages of Proposed ZVS Self-Driven FB VRM

Based on the principle of operation and analysis, the advantages of the proposed non-isolated converter are highlighted as follows:

6.6.1 Duty Cycle Extension

The voltage gain of the proposed converter is

\[ V_o = \frac{V_{in}}{n} \cdot D \]  

(6.33)

As an example, in order to achieve \( V_{in}=12V \), and \( V_o=1.3V \), \( n=3 \), the required duty cycle is \( D=0.33 \). However, for the same output voltage and input voltage, the duty cycle of a buck converter is only 0.11. Therefore, the duty cycle is extended by three times. For \( V_{in}=12V \), \( V_o=1.3V \), \( I_o=60A \) and \( f_s=1MHz \), with the current ripple of 4A, the output inductor of the proposed converter is 190nH compared to 300nH of the buck converter, which leads to better current ripple
cancellation so that smaller output inductors with lower conduction loss can be used. The lower inductance value also helps to improve the dynamic response of the converter and reduces the number of the output capacitors during step load transient.

**6.6.2 ZVS of Control MOSFETs with Low Voltage Stress**

For a buck converter, the switching loss of the control MOSFET is

\[
P_{Q1} = \frac{1}{2} V_{in} \cdot I_{(on)\_Q1} \cdot t_{sw(on)\_Q1} \cdot f_s + \frac{1}{2} V_{in} \cdot I_{(off)\_Q1} \cdot t_{sw(off)\_Q1} \cdot f_s
\]  

(6.34)

where \(I_{(on)\_Q1}\) is the turn on current and \(I_{(off)\_Q1}\) is the turn off current, \(t_{sw(on)\_Q1}\) is the turn on time and \(t_{sw(off)\_Q1}\) is the turn off time.

For the proposed converter, owing to asymmetrical control used to achieve ZVS, there is no turn on losses. The turn off losses are

\[
P_{\text{turn off}} = 4P_{Q1} = \frac{2}{n} V_{in} \cdot I_{(off)} \cdot t_{sw(off)} \cdot f_s
\]  

(6.35)

In a practical design, for instance, for \(V_{in}=12V, V_o=1.3V, n=3\), switching frequency 1MHz, output inductance \(L_f=300\)nH and total output current \(I_o=60A\), for two phase buck converters, the turn off current of each control MOSFETs is 35A and the total turn off current is 70A. However, for the new converter, the turn off current of the control MOSFETs is only 10A and the total turn off current is 40A (a reduction of 43%). This results in a high reduction of turn off loss due to the duty cycle extension.

For a conventional buck converter, due to the reverse recovery of the body diode, the peak voltage of the switching node with the ringing will become higher than 20V. So a 30V MOSFET is generally used for the control MOSFETs. However, in the proposed converter, the voltage stress of the control MOSFETs is the input voltage (12V, usually), so a 20V MOSFETs with lower on-resistance \(R_{DS(on)}\) can be used to reduce the conduction loss.
6.6.3 Gate Energy Recovery of SRs and Reduced Body Diode Conduction

One of the most important advantages of the proposed topology is the self-driven capability so that no drive ICs are needed, which reduces the cost of the converter. In addition, it is an inherent adaptive drive control for SR MOSFETs. Therefore, no additional dead time control circuit is needed anymore.

With the self-driven control, the dead time is minimized to reduce the body diode conduction loss. For the turn on transition, there is no body diode conduction. For the turn off transition, the body diode conduction is minimized. More importantly, the self-driven topology actually forms a CSD using the leakage inductance of the transformer to achieve gate energy recovery of SRs. This is beneficial at high switching frequency operation (>1MHz) and allows for high drive voltages (input voltage, usually 12V) for SRs to achieve lower \( R_{DS(on)} \) and reduce the conduction loss further. Compared to 5V drive voltage for the SR MOSFETs, the \( R_{DS(on)} \) value with 12V drive voltage is reduced by 20% [64]. This translates into a 20% reduction of the SR conduction loss.

6.6.4 Reduced Conduction Losses and Reverse Recovery Losses of SR MOSFETs

Because of the voltage spikes due to the parasitics in a buck converter, 30V rated MOSFETs are generally used as SRs in 12V input buck converters due to the parasitics. Due to the transformer, the voltage stress of the SRs (including the ringing) are reduced to 8V \( (V_{in}/n) \) when \( n=3 \). Thus lower voltage rating MOSFETs with lower \( R_{DS(on)} \) can be chosen to reduce the conduction further. New low-voltage devices, with extremely low \( R_{DS(on)} \) (sub 1 m\( \Omega \)), will be in production in the near future. This provides the new topology with potential to achieve an even greater efficiency improvement. For example, if the 7V lateral power MOSFETs using CSP concept with 0.9 m\( \Omega \) at \( V_{GS}=6V \) is chosen as SR MOSFETs [65], the SR conduction loss can be further reduced from 8.1W to 4.3W. This turns to be loss reduction of 4.9% of the output power.
(3.8W/1.3V/60A).

The reverse recovery loss of the body diode is $P_{rr} = Q_{rr} \cdot V_{s} \cdot f_{s}$, where $V_{s} = V_{in}/n$, is the blocking voltage over the diode. For the proposed converter, this voltage is 8V compared to 20V in a buck converter. Therefore, the reverse recovery loss is also reduced by as much as 60%.

**6.6.5 Design Compatibility with Existing VRM Technology**

Another important advantage mentioned here is that since the control MOSFETs are located in the legs of the FB structure, low cost commercial buck drivers can be directly used to drive these control MOSFETs without additional auxiliary circuitry. The SR MOSFETs can be driven directly without extra drivers nor auxiliary windings. Exiting multiphase buck controllers can be used for the feedback control. In addition, the design procedure of the new topology is quite straightforward and similar to a traditional FB converter, which is familiar to most design engineers. Therefore, less design efforts are required.

Overall, the proposed ZVS self-driven non-isolated FB converter reduces the frequency-dependent losses including switching loss, reverse recovery loss and gate drive loss of SRs in a cost-effectively manner. It also reduces the voltage stress of the control MOSFETs as well as SRs, and reduces the output filter inductance for better dynamic response.

**6.7 Experimental Verification and Discussion**

A 1MHz self-driven ZVS FB VRM was built to verify the operation of principle and demonstrate the advantages of the proposed topology. The specifications are as follows: input voltage $V_{in}=12V$; output voltage $V_{o}=1.3V$; output current up to 60A; switching frequency $f_{s}=1MHz$, transformer turns ratio $n=3:1$. The PCB uses six-layers of 2 oz copper. The components used in the circuit are listed as follows:

Control MOSFET $Q_{1}$-$Q_{4}$: Si7368DP (20V N-channel, $R_{DS(on)}=8.5m\Omega@V_{GS}=4.5V$, Vishay)
SR MOSFET \(Q_5\) and \(Q_6\): IRF6691 (20V N-channel, \(R_{DS(on)}=1.8\,\text{m}\Omega\)@\(V_{GS}=10\,\text{V}\), International Rectifier)

Power transformer: RM5 (core materials 3F5)

Output filter inductors: \(L_1=L_2=190\,\text{nH}\) (Ice components LP02-191-5)

Output capacitance: \(C_o=22\mu\text{F} \times 10=220\mu\text{F}\)

Figure 6.15 gives the circuit diagram of the test prototype. Two Intersil ISL6208A buck drivers are used to drive four control MOSFETs in the primary side of the transformer. A four phase buck controller LM2639 is used to generate two PWM control signals for driver ISL6208A. It is noted that only two buck drivers and a multiphase phase buck controller are needed for the proposed converter. Figure 6.16 shows a photograph of the prototype.

![Figure 6.15 Schematic of the non-isolated self-driven FB converter](image-url)
Figure 6.16 Photograph of the prototype

Figure 6.17 shows the gate drive signal $v_{GS}$ and drain-to-source $v_{DS}$ of the upper control MOSFET $Q_1$ at full load (60A), which indicates that ZVS has been achieved for $Q_1$. Similarly, Figure 6.18 demonstrates ZVS achievement of the lower control MOSFET $Q_2$.

Figure 6.17 Drain-to-source voltage $v_{DS}$ and gate drive signals $v_{GS}$ of upper control MOSFET $Q_1$ @ $V_{in}=12V$, $V_o=1.3V$ and $I_o=60A$
Figure 6.18 Drain-to-source voltage $v_{DS}$ and gate drive signals $v_{GS}$ of lower control MOSFET $Q_2 @ V_n=12V, V_o=1.3V$ and $I_o=60A$

Figure 6.19 shows the gate drive signal $v_{GS}$ and drain-to-source voltage $v_{DS}$ of the SR $Q_6$. The 20MHz bandwidth limit is used for the waveform $v_{DS}$. It is noted that the gate drive voltage is 12V, which means the $R_{DS(on)}$ of SRs is only 1.6 m$\Omega$ compared to 2.2 m$\Omega$ with 5V gate drive voltage (a reduction of 20%). This reduces the conduction loss by 2.2W (30% of the output power). Moreover, there is no body diode conduction time for the turn on transition of $Q_6$ since the gate voltage has been applied before $v_{DS}$ reaches zero.

Figure 6.19 Gate drive signal and drain-to-source voltage of $Q_6 @ V_n=12V, V_o=1.3V$ and $I_o=60A$

Figure 6.20 shows the voltage $v_{AB}$ across the primary side of the transformer, the rectified
voltages $v_C$ and $v_D$ over the output filter inductors. It is observed that the voltage applied to the primary side is symmetrical though asymmetrical control is applied to the control MOSFETs in the full-bridge structure. It is also noted that the peak rectified voltages $v_C$ and $v_D$ (i.e. drain-to-source voltage of the SRs) is only 5V, which means a reduction of the reverse recovery loss. It should be noted that 20V DirectFET with $R_{DS(on)}=1.8\text{m}\Omega@V_{GS}=10\text{V}$ is used in this experiment. With the fast development of low voltage rating MOSFETs, it is expected that 8V or 10V MOSFETs with $R_{DS(on)}$ less than 1 mΩ will be available commercially in the near future. The emerging low voltage devices will reduce the conduction losses of the SR MOSFETs by approximately 50% (i.e. 4.2W, 5.4% of the total output power at $V_o=1.3\text{V}$ and $I_o=60\text{A}$, and an efficiency improvement of around 4%). It should be noted that 12V input buck converters are not able to take advantage of these future new low-voltage rating device with extremely low $R_{DS(on)}$.

Figure 6.20 Waveforms of primary voltage $v_{AB}$, the rectified voltages $v_C$ and $v_D$ @ $V_{in}=12\text{V}$, $V_o=1.3\text{V}$ and $I_o=60\text{A}$

Figure 6.21 gives the measured efficiency comparison between the proposed topology and the conventional buck converter at 1.3V output. It is observed that at 50A, the efficiency is improved from 80.7% to 83.6% (an improvement of 2.9%) and at 60A, the efficiency is improved from 77.9% to 80.5% (an improvement of 2.6%). The efficiency improvement is due to the
reduction of the frequency dependent losses. It is also pointed that at no load condition, there is some circulating loss in the main power MOSFETs and transformer windings because the output inductor currents are kept in continuous mode since the SRs are self-driven.

Figure 6.21 Efficiency comparison: top: self-driven FB VRM; bottom: two-phase buck converters

Figure 6.22 gives the measured efficiency comparison between the self-driven FB converter with two parallel SRs and the conventional buck converter at 1.3V output. It is observed that at 50A, the efficiency is further improved from 80.7% to 84.7% (an improvement of 4%) and at 60A, the efficiency is improved from 77.9% to 83.2% (an improvement of 5.3%). The efficiency improvement is due to the SR conduction loss reduction at high load currents. It is noted that the efficiency can be further improved using low rating SR MOSFETs to reduce the conduction loss.
Figure 6.22 Efficiency comparison: top: self-driven FB VRM with two parallel SRs; bottom: two-phase buck converters

Figure 6.23 illustrates the output voltage during the load step-up from no load to full load. Figure 6.24 illustrates the output voltage during the load step-up from full load to no load. It is observed that from no load to full load, the voltage deviation is 160mV, and from the full load to no load, the voltage deviation is 150mV. The converter is stable and is able to response fast during the load transient events.

Figure 6.23 Output voltage and the load current step-up: from no-load to full load
A new self-driven ZVS non-isolated FB converter is proposed for 12V input VRM applications in this chapter. Existing multiphase buck controllers and buck drivers can be directly used in the proposed converter. The advantages are highlighted as follows: 1) duty cycle extension; 2) switching loss reduction owing to ZVS of all the control MOSFETs; 3) reduced reverse recovery loss and lower voltage stress of the SRs; 4) high drive voltage to reduce $R_{DS(on)}$ and the conduction loss of SRs owing to gate energy recovery capability; 5) reduced body diode conduction; 6) no external drive IC chips with dead time control needed due to the inherent CSD structure. The multiphase self-driven ZVS non-isolated FB converter and three phase non-isolated ZVS self-driven FB converter with current tripler rectifier are also presented.

A 12V input, 1.3V output and 1MHz prototype of the proposed converter was built to verify the operation and demonstrates the loss reduction. At 50A, the proposed converter improves the efficiency from 80.7% using the buck converter to 83.6%, and at 60A, from 77.9% using the buck converter to 80.5%. With two paralleled SRs, the efficiency is further improved from 83.6% (single SR) to 84.7% (two SRs) and at 60A, the efficiency is improved from 80.5% (signle SR) to 83.2%
(two SRs). During the load transient events, the proposed converter can also response fast.
Chapter 7
Conclusions and Future Work

7.1 Conclusions

In the future, VRMs for next generation microprocessors will operate at switching frequencies in the 1-5MHz range in order to achieve greater power density and better transient response. To meet the next generation requirements of these applications, four new ideas have been proposed in this thesis.

7.1.1 A New Analytical Loss Model for Optimal Design of the CSD with a Buck Converter

The first contribution is a new accurate analytical loss model of a power MOSFET with a CSD. The impact of the parasitic components is investigated. Based on the proposed loss model, a general method to optimize the CSD is proposed. Compared to a voltage source driver, the CSD uses a constant current source to charge and discharge the MOSFET gate capacitor, and therefore, absorbs the parasitic common source inductance. As a result, the switching transition time can be greatly reduced, which leads to a high reduction of the switching loss. A 12V synchronous buck prototype with the CSD operating at 1 MHz was built to verify the analytical modeling. The analytical results of the loss model match the simulation results and the experimental results well. The loss model can be used to optimize a CSD at high frequency.

This body of this chapter has been published in the following publications:

A New Continuous CSD for a Buck Converter with Different Gate Drive Currents

The second contribution is a new CSD for a synchronous buck converter. The improved CSD using integrated inductors is also proposed to reduce the magnetic core count and the core loss due to magnetic flux cancellation. The proposed gate driver is able to drive the control and the SR MOSFET independently with different drive currents enabling optimal design.

The new CSD maintains the following advantages: 1) significant switching loss reduction; 2) gate energy recovery; 3) reduced conduction loss and reverse recovery loss of the body diode; 4) ZVS for the driver switches. The proposed CSD can also be used to drive the two MOSFETs in one leg of a HB converter or a FB converter to further reduce the turn-off loss at MHz switching frequencies.

Experimental results demonstrate the advantages of the new CSD. At 1.5 V output, the new CSD improves the efficiency from 84% using a voltage source driver to 87.3% (an improvement of 3.3%) at 20 A, and at 30 A, from 79.4% to 83.9% (an improvement of 4.5%).

The content of this chapter has been filed as a provisional U.S patent. This body of this chapter has been published in the following publications:


7.1.3 A New Discontinuous CSD for High Frequency Power MOSFETs

The third contribution is a new discontinuous CSD. Compared to other CSDs proposed in previous work, the most important advantage of the new CSD is the small inductance (typically, around 20nH at 1MHz switching frequency). Other features of the proposed discontinuous CSD includes: 1) discontinuous inductor current with low circulating current; 2) fast switching speed and reduced switching loss; 3) wide range of duty cycle and switching frequency; 4) high noise immunity.

A hybrid gate drive scheme for a synchronous buck converter is also proposed. A 12V input, 1.3V output synchronous buck converter with the switching frequency of 1MHz was built to verify the advantages of the proposed CSD. At 1.3 V output, the proposed driver improves the efficiency from 80.7% using a voltage source driver to 85.4% (an improvement of 4.7%) at 25A, and at 30 A, from 77.9% to 83.9% (an improvement of 6%).

In additional, the proposed CSD can also achieve gate energy recovery. Two paralleled SR MOSFETs (IRF6691x2) are used to verify gate energy recovery with different switching frequencies and gate driver voltages. At $V_D=7V$ and the switching frequency of 2MHz, the gate loss reduction with the CSD is as much as 2.24W, a reduction of 63% with the voltage source driver.
7.1.4 New ZVS Non-Isolated Full-Bridge VRMs with Gate Energy Recovery

The final contribution is a new self-driven ZVS non-isolated FB converter for 12V input VRM applications in this paper. The advantages are highlighted as follows: 1) duty cycle extension; 2) significant switching loss reduction due to ZVS of all the control MOSFETs; 3) reduced reverse recovery loss and lower voltage rating SRs with lower $R_{DS(on)}$ owing to reduced voltage stress; 4) high drive voltage to reduce $R_{DS(on)}$ and the conduction losses of SRs due to gate energy recovery capability; 5) reduced body diode conduction; 6) no external drive IC chips with dead time control needed due to the inherent CSD structure. Based on the similar idea, some extended non-isolated topologies are also introduced. In addition, existing multiphase buck controllers and drivers can be directly used.

A 12V input prototype of the proposed converter with a switching frequency of 1 MHz was built to verify the operation and to demonstrate the loss reduction. The new power converter achieves a significant efficiency improvement over the conventional buck converter. At 12V input and 1.3V output voltage, the proposed converter improves the efficiency from 80.7% using the buck converter to 83.6% at 50A, and from 77.9% using the buck converter to 80.5% at 60A.

This body of this chapter is pending U.S patent has been accepted in the following publications:


7.1.5 Summary of Proposed Approaches

In Chapter 3 and Chapter 4, the continuous CSDs are proposed. Compared to the discontinuous CSD proposed in Chapter 5, the advantages of the continuous CSDs are less driver
switches are needed and the control for the drive switches is relative simple. The disadvantages of the continuous CSDs are that the gate drive currents change with the duty cycle and switching frequency as well as high circulating loss in the driver circuit.

On the other hand, the discontinuous CSDs have much smaller inductance values and can use smaller footprint to save board area and improve the power density. Although the discontinuous CSDs need more drive switches, because of the discontinuous inductor current, the driver MOSFET switches do not need $R_{DS(on)}$ as low as the continuous CSDs. Therefore, the chip size of the driver switches can be similar for these two types of CSDs. For 12V input buck converters with 1MHz switching frequency, the discontinuous CSDs offer better performance over the continuous CSDs in terms of power density, duty cycle and switching frequency range. However, for higher switching frequency (>2MHz), the continuous CSDs are the better solution since the discontinuous CSDs need to have enough pre-charge time for the current source inductors, which is normally around 70ns including the switching transition time.

The most important advantage of the CSDs is that the significant switching loss reduction in the buck converter with low cost. When the CSDs are integrated as drive ICs, they can replace the conventional voltage source drivers in a pin-to-pin compatible manner. Therefore, the customers simply replace voltage source drivers with the CSD drivers to improve the efficiency and performance. Nevertheless, the narrow duty cycle problem of the buck converter still exits.

For 12V input voltage and 0.8V output voltage VRM application with the switching frequency of 2MHz, the ZVS non-isolated FB converter proposed in Chapter 5 is the better solution over the buck converter since its duty cycle is only 0.07. In addition, the proposed converter can use future low voltage rating SR MOSFET to reduce the condition losses, which the buck converter can not take advantage of. Integrated magnetic technique can be used to further reduce winding conduction loss and high current joint loss.
7.2 Future Work

This sub-section outlines the possible future work for the thesis topics.

7.2.1 CSDs

In the experimental verification, the proposed CSDs in Chapters 4 and 5 have been implemented discretely. In order to increase the power density and application capability of CSD technique, the drivers will need to be integrated into single discrete driver chip or even with a PWM controller. It will be also beneficial to integrate the CSD and the power MOSFETs in one package as a Power System in Package to further improve the high frequency performance of the power circuits. This involves power circuit and control circuit integration. Methods of integrating a chip inductor and hybrid circuit integration could be an interesting topic. Another interesting topic to improve the CSDs performance is to achieve adaptive gate drive currents depending on the load condition.

7.2.2 ZVS Non-Isolated Self-Driven FB Converters

Currently, the proposed converter is using the discreet power transformer and the output filter inductors. In order to improves the power density and reduce magnetic components of the proposed converter, Integrated Magnetics (IM) technology can be explored to improve the efficiency and power density. Also, advanced control techniques such linear-non-linear control, charge balance control, adaptive voltage positioning (AVP) control etc can be applied to the proposed converter to improve the dynamic performance and reduce the output capacitances.
References


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