MHZ RESONANT DC-DC CONVERTERS WITH FIRST CYCLE CONTROL

by

Hossein Mousavian

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Abstract

Faster dynamic response and higher power density are the major achievements obtained by increasing the switching frequency of power supplies. However, switching frequencies are limited by topology, control, semiconductor materials, and packaging methods. This thesis proposes control and topology solutions for high-frequency resonant converters with wide voltage and load range.

To address these issues, the thesis first proposes a new quasi-resonant converter topology that with no additional cost or use of bulky additional components reduces the switching components’ voltage stress to half, and nearly eliminates the switching losses in quasi-resonant converters specifically under on-off control strategy. This topology improvement authenticates the use of lower voltage diodes in quasi-resonant converters.

The second major thesis achievement is the introduction of the first cycle control method that enhances the performance of the so-called ‘on-off’ control method. This method is quite popular for the high-frequency converters. The on-off control method benefits from its attractive characteristics such as simplicity, robust stability and excellent light-load efficiency. However, the conventional method suffers from overvoltage stress and the hard-switching power losses in on-off transients. The proposed first cycle control method drives a predetermined gate signal at the beginning of each power pulse that substantially alleviates the voltage stress and switching losses, and thus improves the transient behavior of the converter. This achievement makes better use of the switches, and paves the way to further increase the on-off rate.

Another significant contribution of the thesis is the proposed new zero voltage transient (ZVT) cell that is introduced to have a fully zero voltage switching on-off control in a non-isolated quasi-resonant converter. In fact, this ZVT cell enhances the performance of the first cycle control method proposed earlier for every semiconductor under any circumstances. Simple structure, low number of components, and avoidance of inductive components in the cell are advantages of the circuit. Higher modulation frequency, lower input and output filter sizes, and faster dynamic responses are the benefits of this method. The zero voltage
switching operation of all semiconductor components allows the designer to increase the modulation frequency without any significant drop in the overall efficiency.
Acknowledgements

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My heartfelt thanks go to my parents, Ozra and Mehdi for their unconditional love and support. Without them, I wouldn't exist or be where I am.

With the deepest love, I would like to thank my wife and colleague, Somayeh Abnavi, for all her support and encouragement through all the good and the bad times (both professionally and personally). With her support and friendship, my years at Queen’s University, Kingston, and Canada have been full of joy.
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<th>Description</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>APWM</td>
<td>Asymmetrical Pulse Width Modulation</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>AWG</td>
<td>American Wire Gauge</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent Series Inductance</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>HB</td>
<td>Harmonic Balance</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction Field Effect Transistor</td>
</tr>
<tr>
<td>MLCC</td>
<td>Multi-layer ceramic capacitor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semi-Conductor Field Effect Transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-Channel MOSFET (See MOSFET)</td>
</tr>
<tr>
<td>PASIC</td>
<td>Power Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PDM</td>
<td>Pulse Density Modulation</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-Channel MOSFET (see MOSFET)</td>
</tr>
<tr>
<td>PRC</td>
<td>Parallel Resonant Converter</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>QRC</td>
<td>Quasi-Resonant Converters</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>SMT</td>
<td>Surface Mount Technology</td>
</tr>
<tr>
<td>SPICE</td>
<td>Simulation Program With Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>SSOC</td>
<td>Self-Sustained Oscillation Controller</td>
</tr>
<tr>
<td>VF</td>
<td>Variable Frequency</td>
</tr>
<tr>
<td>VTH</td>
<td>High Threshold Voltage Of A Comparator</td>
</tr>
<tr>
<td>VTL</td>
<td>Low Threshold Voltage Of A Comparator</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero Current Switching</td>
</tr>
<tr>
<td>ZDS</td>
<td>Zero Derivative Switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero Voltage Switching</td>
</tr>
<tr>
<td>ZVT</td>
<td>Zero Voltage Transient</td>
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Chapter 1

Introduction

1.1 Introduction

A dramatic increase in switching frequencies is required to improve the dynamic tarnation performance and achieve high power density. The operating frequency of a converter plays the main role in component selection. As a rule of thumb, higher the switching frequency, lower the size of components. By decreasing the period of switching, a lower amount of energy is required to be stored in components to meet converter specifications. Therefore, faster response to the load changes and to the input variations as well as improved transient performance are more feasible at higher frequencies. In addition, traditional transformers and inductors can be replaced by coreless transformers and inductors at high switching frequencies. Operating power converters at higher switching frequencies, however, needs reconsideration of the design criteria and availability of compatible circuit components.

In a practical power electronics circuitry, switching frequency not only influences the converter size but also affects the efficiency and power losses of the system. Copper and magnetic losses, as well as switching losses, are increased by increasing the switching frequency. Parasitic components introduced by the device itself and its packaging and structural interconnections are other important factors that must be considered in high-frequency converters. In many high-frequency circuits, values of some intrinsic parasitic components are comparable to the value of designed components. In addition, the maximum junction temperature of semiconductors and maximum temperature rise of magnetic components play a significant role in the design procedure. The capability of active and passive switches to operate at higher frequency is another issue. Turn on and turn off time,
switching delays, and reverse recovery time limit the operating frequency of a semiconductor switch. All above-mentioned issues should be considered in the converter design.

With the existing semiconductor switches, the number of practical topologies for high-frequency circuits is limited. Resonant converters are legitimate choices for high power MHz circuits since they utilize intrinsic parasitic components in the resonant circuit and eliminate the switching losses. Besides choosing a proper topology, an appropriate control scheme is required to achieve superior characteristics of MHz converters. Effective control strategies are restricted for high-frequency converters due to the timing accuracy, components delay and resonant characteristics of the MHz converters. For instance, the switching period becomes comparable with transient characteristics of a MOSFET. As a result, the duty cycle control becomes more difficult and less accurate. Moreover, the resonant nature of MHz circuits limits their high-performance operation to a narrow frequency, voltage and load ranges. Hence, the demand for compatible topology and suitable control strategy must be addressed properly in a high-frequency converter design.

1.2 Components Selection

1.2.1 Reactive Components

In a converter, passive components such as capacitors and inductors are sized to bound voltage and current ripples below a certain level and/or to achieve a predetermined impedance. Frequency-dependent components such as transformers, capacitors, and inductors are normally sized inversely proportional to the switching frequency. For example, if the switching frequency is increased to 10 times more, a 10-times smaller capacitor is sufficient to get the same voltage ripple. The same scenario is valid for the inductor and transformer design. Equations (1.1)-(1.3) define voltage ripple ($\Delta v$), current ripple ($\Delta i$), and maximum flux density ($B_{\text{max}}$) as functions of switching frequency
\( f_{SW} \), capacitive filter size \((C_f)\), inductive filter size \((L_f)\), winding turns \((n)\), and core cross section area \((\text{Area})\).

\[
\Delta v = k_1 \frac{1}{C_f \times f_{SW}} \quad (1.1)
\]

\[
\Delta i = k_2 \frac{1}{L_f \times f_{SW}} \quad (1.2)
\]

\[
B_{max} = k_3 \frac{1}{n \times \text{Area} \times f_{SW}} \quad (1.3)
\]

Equation (1.4) shows the magnetic power loss as a function of frequency \((f)\), core size \((V_{core})\), material constant \((Cm)\), and flux density \((B_{ac})\), using “Steinmetz” model [1]. For ferrite cores \(\alpha\) varies from 1.4 to 2 and \(\beta\) changes from 2.4 to 3.

\[
P_{core} = V_{core} \times Cm \times f^{\alpha} \times B_{ac}^{\beta} \quad (1.4)
\]

Skin and proximity effects are frequency dependent phenomena and influence the conduction power losses. By increasing the switching frequency, skin depth decreases resulting in an increase in the effective resistance of windings, called as Skin effect. In multi-layer windings, if skin depth is lower than the thickness of the conductor, effective resistance decreases drastically, called as Proximity effect.

Numerous research has been reported on the relation between the switching frequency and magnetic components parameters such as quality factor, dimensions, winding types and temperature rises [2]-[6]. A high-frequency magnetic structure design must consider available magnetic material, winding methods, and thermal considerations. Despite its importance, this topic is out of the scope of this thesis.

1.2.2 Active Components

At higher frequencies, parasitic inductances, capacitances, and the intrinsic body diode may interfere with the switches operation. Figure 1-1 shows a simple MOSFET model for high-frequency applications. Conduction losses of a MOSFET are proportional to its drain-source
resistance which is almost independent of the switching frequency, and thus remain constant for various frequencies. In contrast to the switch conduction losses, gating power losses are increased at high-frequency operations. In addition, power loss associated with the output capacitor ESR is also increased by the square of the switching frequency [7].

Diodes turn on almost simultaneously, but reverse recovery charge affects the diode turn-off procedure and increases the diode losses. At a higher frequency, Schottky diodes and SiC diodes are more suitable according to their theoretical zero reverse recovery charge. Similar to power switches, the intrinsic parallel capacitor in a diode structure should be considered in a design to avoid unwanted current flow and voltage spike.

![Diagram of a high-frequency model for a MOSFET](image)

**Figure 1-1: A high-frequency model for a MOSFET**

Due to the superior performance of Gallium Nitride (GaN) and Silicon Carbide (SiC) semiconductors over the Silicon (Si), these advanced materials had become more popular in high-frequency, high-power applications. GaN and SiC devices are of a much smaller size for the same voltage and current ratings when compared to the Si switches [8]. Today, there are GaN and SiC transistors that are 5-10 times superior to the theoretical limit of silicon, and with the anticipated progress, much higher performance is expected from GaN and SiC over the next few years. GaN switches are more popular for applications requiring 600V and below, while SiC components have
made their way in over 600V applications [8]. The thesis hires SiC components to build the proposed high-frequency power converters.

1.3 High-Frequency Power Structures and Control Methods

1.3.1 High-Frequency Topologies

Zero voltage switching (ZVS) is required to achieve a high efficiency in high-power MHz converters. In addition, a proper topology must be compatible with the inevitable parasitic components such as stray inductors and capacitor. Negligible switching losses in resonant converters, make these types of converters a practical choice for MHz applications. Single-ended resonant topologies are much more popular in MHz converters because of the simplicity of the gate drive systems in these circuits since generating proper gate-drive signals is less problematic in single-ended grounded-reference structures. Since 70’s, switching amplifiers have employed resonant and quasi-resonant circuits to achieve zero voltage switching operation. A DC-DC converter, for instance, can be realized by adding a rectifier to these switching circuits. High-frequency converters are extensively reviewed in Chapter 2.

1.3.2 High-Frequency Converters Control

In high-frequency power converters various control variables such as duty cycle, on-time, and off-time, switching frequency, current, and phase shift, have been used to regulate the output power. By increasing the operation frequency, many practical challenges like the system bandwidth, delay, and time jitter limit the integrity of the conventional control methods. Therefore, control schemes for high-frequency converters must be: (i) very simple and fast enough to keep the aforementioned issues at acceptable levels, and (ii) capable of providing high efficiency and good performance over the full load variations. While (i) has been addressed in conventional resonant converters, (ii) has remained a major challenge in the design of very high-frequency resonant converters, and as
illustrated in [7], [9] and [10] it is difficult to maintain high efficiency over a wide load range according to the gate-drive power losses and significant circulating current during light-load operation. In a method called on-off control, the converter is turned “on” and “off” at a rate much lower than the switching frequency to regulate the power flow. When “on”, the converter delivers the nominal power to the load, and when “off”, the converter delivers no power to the load. The load power, therefore, is determined by the “on” time interval in one period of the on-off cycle [7] and [11]. In this technique, higher efficiency can be obtained across a wide load range since the converter is operating at nominal efficiency or it is off. Despite the fact that the converter operates at high efficiency over a wide range of load power demand, the transient behavior of the converter is critical in this method. Power losses and voltage stress associated with the converter’s startup and shutdown decrease the overall efficiency and increase the switch ratings, respectively. As a conclusion, complexity, voltage stress, and hard switching operation in on-off transients are the major shortcoming of MHz DC-DC converter using on-off control method. The on-off control technique and other control strategies are discussed in detail in Chapter 2.

1.4 Thesis Motivation

As mentioned above, high-frequency power converters offer many benefits to the power conversion process. Therefore, there are remarkable research motivations to resolve the shortcomings of these converters by introducing newer topologies and control schemes that allow higher switching frequencies, improve the converter’s performance, and integrate the newer semiconductor switches into their structure. This thesis’s motivation is to look for such advanced converter topologies and control schemes.

1.5 Thesis Objective

The objective of this thesis is to develop and implement a solution to improve the performance of high-frequency converters in a wide range of loads. It can be detailed as:
(i) Development of an improved single-ended quasi-resonant DC-DC converter to reduce the maximum voltage stress across the rectifier.

(ii) Development of first cycle control method to improve the converter efficiency.

(iii) Development of an auxiliary circuit to eliminate switching losses in a wide load range operation.

1.6 Thesis Outline

The outline of this thesis is as follows:

Chapter 2 presents a comprehensive review on high-frequency converter topologies, modeling, and control methods. Advantages and disadvantages of current high-frequency topologies are studied and discussed. Furthermore, popular control and modeling methods for high-frequency DC-DC converters are presented.

Chapter 3 proposes a topology solution to reduce the rectifier voltage stress and unwanted voltage oscillations in the circuit. Thus, a new quasi-resonant converter topology that reduces the switching components’ voltage stress to half, and nearly eliminates the unwanted oscillations in quasi-resonant rectifier is introduced. This topology improvement authenticates the use of lower voltage diodes in quasi-resonant converters for a certain output voltage level when compared to the existing converter topologies.

Chapter 4 proposes a control solution to reduce the voltage stress and switching power losses in the so-called ‘on-off control’. The major achievement of this chapter is a novel first cycle control method that enhances the performance of the on-off control, which is a popular control method for the high-frequency converters. The proposed first cycle control method drives a predetermined gate signal at the beginning of each power that substantially alleviates the voltage stress and switching losses at the beginning of each power pulse, which then improves the transient behavior of the
converter. This achievement results in a better utilization of switches and paves the road to further increase in on-off rate.

Chapter 5 proposes an auxiliary zero voltage transient circuit to elevate the performance of the first cycle control method and to have a fully zero voltage switching operation while using on-off control method. Simple structure, low number of components, and avoidance of inductive components in the cell are advantages of the circuit. Higher modulation frequency, lower input, and output filter sizes, and faster dynamic response are the benefits of this method. The zero voltage switching operation of all semiconductor components allows designers to increase the modulation frequency without any significant drop in the overall efficiency.

In Chapter 6, conclusions and contributions are summarized, and suggestions for the future works are presented.
Chapter 2

Literature Review

2.1 Introduction

This chapter reviews the existing topologists, modeling and control methods for high-frequency switching systems. To achieve a high-performance switching power supply, a multidimensional challenge requiring a combination of advanced topology, control, semiconductor, and packaging methods must be accomplished. Any obstacle will set an upper bound on achievable switching frequency. This chapter will discuss these issues and present the base for subsequent chapters of this thesis.

2.2 High-Frequency Topologies

Opportunities and challenges of the high-frequency operation were discussed in the first chapter. To achieve high-frequency and high-efficiency operation in switching converters, the zero voltage switching operation is demanded. In this section, major radio switching structures including class E, class F, and class DE as well as quasi-resonant converters are discussed. Advantages and disadvantages of each topology are presented in detail.

2.2.1 High-Frequency Inverters

Tuned switched mode inverters such as classes E, F, and DE employ resonant networks to achieve efficient operation at high frequencies and meet other requirements. These inverters deliver sinusoidal waveforms to their load while keeping switching losses minimized [12] - [14]. A variety of switching inverters has been proposed and modified since 1970’s. Classes E and DE circuits have been more popular due to their high performance and simplicity.
2.2.2 Class E Inverter

The class E inverter is the basis of a family of high-frequency converters. Figure 2-1 (a) shows the class E power amplifier which was proposed in 1970’s [12]. As shown in Figure 2-1 (b), this converter integrates the drain-source parallel capacitor into the circuit. So, this parasitic component does not affect the performance of the inverter. In addition, as already stated, the source terminal of the transistor is grounded, so that switch driving is much easier when compared to other topologies. A switch with grounded source, a capacitor in parallel with the switch, an inductor in series with the input voltage source, a series band-pass filter, and zero voltage switching operation are main specifications of this type of converter. These circuits are modified to operate at very high frequencies.

(a) A simple class E inverter

(b) Class E inverter cell

**Figure 2-1 Class E inverter circuit**

In a classic circuit, $L_{in}$ is an infinite choke providing a pure DC input current. A class E inverter utilizes resonant circuit ($L_r$ and $C_r$) to provide a pure sinusoidal waveform to the load. With a proper selection of circuit parameters, Zero Voltage Switching (ZVS) and Zero Derivative Switching (ZDS) can be guaranteed. Although a class E inverter has many advantages, it has some
limitations like high voltage stress imposed on the switch. The peak voltage stress across the switch in an ideal class E circuit is about 3.6 times the input voltage for a duty cycle of 50% [12]. A class E inverter suffers from a bulky input inductor which results in relatively large stored energy in the converter that reduces the converter’s speed response (e.g., during start-up or shutdown).

To simplify the analysis, all components are assumed to be ideal, the input current is constant, and the output current is a pure sinusoidal waveform. The operation of the converter can be divided into two states. First, the switch is on, $v_{sw}$ is zero, and input inductor is charging while $L_r$ and $C_r$ are resonating. Second, the switch is off and $C_s$ is involved in the resonant circuit. In a well-designed circuit, the parallel capacitor is fully discharged at the turn-on instant. Therefore, the switch turns on at zero voltage condition. As a result, switching loss is eliminated in this circuit. Figure 2-2 (a) and (b) show the circuit in both states. Besides the zero-voltage condition, body diode is not acting any rule in the circuit. So, the slow anti-parallel body diode does not degrade the operation of the circuit. Figure 2-2 (c) shows the waveforms of a class E converter. Equations (2.1)-(2.4) explain the relationship between voltage and current in above-mentioned modes of operation.
(a) Class E equivalent circuit in on state

(b) Class E equivalent circuit in off state

(c) The switching waveform

Figure 2-2: Class E inverter operation

\[ v_i = L_{in} \frac{di_{in}}{dt}, \quad (2.1) \]

\[ \frac{1}{C_r} i_{out} + R_{load} \frac{di_{out}}{dt} + L_{in} \frac{d^2i_{out}}{dt^2} = 0 \quad (2.2) \]

\[ v_{in} - v_{sw} = L_{in} \frac{di_{in}}{dt}, \quad (2.3) \]

\[ \frac{1}{C_r} i_{out} + R_{load} \frac{di_{out}}{dt} + L_{r} \frac{d^2i_{out}}{dt^2} - \frac{1}{C_s} (i_{in} - i_{out}) = 0 \quad (2.4) \]
Different modeling and solutions are proposed for class E inverters. Analytical derivations of design equations in [15] are valid by assuming that the resonant tank current is sinusoidal. This assumption is true only if the quality factor $\frac{\omega L_r}{r_{load}}$ of the network is very high, and becomes less accurate for lower quality factor circuits. [12] claims that a minimum $Q$ of 1.7879 is required to achieve the nominal waveforms of class E converters. In this study, the system was analyzed for a duty cycle of 50%. [12] also provides Table 2-1, including normalized exact numerical solutions for output power. $R_{load}$, $C_r$, and $C_s$ are arranged for eight values of $Q_L$ over the entire possible range. The relevance of power, load, maximum voltage and values of components are lined up.

<table>
<thead>
<tr>
<th>$Q_L$</th>
<th>$PR/(V_{CC} - V_o)2$</th>
<th>$C_s2\pi fR$</th>
<th>$C_r2\pi fR$</th>
</tr>
</thead>
<tbody>
<tr>
<td>infinite</td>
<td>0.576801</td>
<td>0.18360</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>0.56402</td>
<td>0.19111</td>
<td>0.05313</td>
</tr>
<tr>
<td>10</td>
<td>0.54974</td>
<td>0.19790</td>
<td>0.11375</td>
</tr>
<tr>
<td>5</td>
<td>0.51659</td>
<td>0.20907</td>
<td>0.26924</td>
</tr>
<tr>
<td>3</td>
<td>0.46453</td>
<td>0.21834</td>
<td>0.63467</td>
</tr>
<tr>
<td>2.5</td>
<td>0.43550</td>
<td>0.22036</td>
<td>1.01219</td>
</tr>
<tr>
<td>2</td>
<td>0.38888</td>
<td>0.21994</td>
<td>3.05212</td>
</tr>
<tr>
<td>1.7879</td>
<td>0.35969</td>
<td>0.21770</td>
<td>infinite</td>
</tr>
</tbody>
</table>

### 2.2.3 Class F Inverter

Another high-frequency inverter, shown in Figure 2-3, uses additional resonant circuits in series with the load to manipulate the circuit impedance at odd harmonics. As a result, the voltage waveform becomes a square wave as the odd harmonics will change the waveform. This flattening decreases the voltage and current overlap [16] and [17], thus a higher efficiency is achievable. The higher the number of tuned harmonics, the better the efficiency. However, even with using complex high order harmonic circuits, class F inverter operates with significant overlap of device voltage
and current. In fact, class F circuits are not working fully in switched mode, thus providing unacceptably low efficiency for many power electronics applications [18].

![Class F inverter circuit](image1)

(a) Class F inverter circuit

![Switch waveforms](image2)

(b) Switch waveforms

**Figure 2-3: Class F inverter**

### 2.2.4 Class DE Inverter

A class DE inverter, shown in Figure 2-4, consists of a series resonant circuit, two semiconductor devices, and two capacitors [19]-[21]. In fact, a class DE inverter is a series resonant inverter when switches’ parallel capacitors are significant and switching dead time is comparable with switching period. A high-quality factor filter forces the inverter’s output current waveform to be almost sinusoidal. A class DE inverter is a topology which takes characteristics of both series resonant and class E inverters. Therefore, ZVS/ZDS condition is achieved and the switch voltage stress is considerably reduced due to the direct connection to the input source. In fact, the maximum voltage across the switching devices is limited to the input voltage. This circuit has only a single inductor
and carries lower reactive energy. However, the implementation of a class DE converter requires a high side gate drive circuit and a precise switching timing which make it difficult to implement the circuit for high-power and high-frequency applications.

Figure 2-4: Class DE inverter

2.2.5 High-Frequency Rectifiers

Most high-frequency resonant DC-DC converters consist of an inverter, a rectifier, a filter and a transformer for isolation if required. The inverter creates a high-frequency waveform which is rectified and then filtered to produce a DC output voltage. Applications for high-frequency rectifiers include DC-DC converters [22], wireless power transfer systems [23], and energy recovery circuits for radio-frequency systems [24] and [25].

The key difference between conventional and soft switch rectifiers are the role of parasitic components in the diodes. The intrinsic capacitance of the diode can be absorbed in the resonance
circuit and decrease $dv/dt$ of the rectifier and consequently the reverse recovery loss. A variety of rectifiers is proposed for high-frequency applications [22] and [25]. In quasi-resonant and multi-resonant converters, rectifier and inverter stages are analyzed together [26]. In this method, according to the number of reactive components, the solution can be complicated. So, this method is usually useful for circuits with a lower order of differential equations.

In many high-frequency converters, rectifier stage is designed independently and it is desirable for the rectifier to appear as a resistive load at its AC input port. For example, in some VHF DC-DC converters, proper operation of the inverter can depend upon maintaining resistive (but possibly variable) loading in the rectifier stage [27]. In some other applications, it is desired to have a constant input impedance across the operating conditions [25] and [28]. The resistance compression network is a useful circuit to stabilize the input impedance of a resonant rectifier [28] - [30]. Resonant rectifiers are proposed and analyzed in a variety of applications [30] and [31].

2.2.6 Class DE Rectifier

A half bridge class DE rectifier is shown in Figure 2-5 (a) [32]- [34]. This rectifier can be also implemented in full bridge configurations (shown in Figure 2-5(b)) [35]. In this rectifier, diodes are connected directly to the output capacitor and the voltage across them is limited to the output voltage. Furthermore, the class DE rectifier does not require any additional inductor and hence offers a much higher power density as the inductor is normally the biggest component.

To analyze the rectifier, it is assumed that the rectifier is fed by a sinusoidal current, diodes $D_1$ and $D_2$ are ideal, and two output capacitances $C_{out1}$ and $C_{out2}$ are considered as voltage sources. By symmetry, an equal voltage is applied to each output capacitance.
According to the waveforms of the rectifier shown in Figure 2-5(c), at $t = 0$, the input current $i_2$ becomes positive and $D_2$ which was previously conducting, turns off under zero voltage switching condition. Therefore, the current $i_2$ charges the total diode capacitance $2C_d$. At the same time, $dv/dt$ is zero which satisfies the class E switching conditions. Thus, diode capacitances and reverse-recovery charge do not have a deleterious effect. The input voltage, rises from the negative
output rail to the positive one, and reaches to $V_o/2$. Then $D_1$ starts to conduct and keeps conducting until the rectifier current is positive. The other half cycle is symmetrical.

Both diodes are turned off at the instant when the diode current is zero, which makes the diode reverse recovery currents to be very small. Moreover, the maximum value of the diode reverse voltages is equal to the output voltage.

2.2.7 Class E Rectifier

A class E rectifier consists of a diode, a shunt capacitor, and an inductor. The capacitor is placed in parallel with the diode and represents the intrinsic capacitance of the diode or any additional capacitance. As shown in Figure 2-6 and 2-7, this rectifier is proposed in the series inductor and parallel diode capacitor [27] and [36] and in the series capacitor and parallel inductor [10]. The circuit is driven by a nearly sinusoidal current according to the high-quality factor of the series resonance tank. Assuming a large inductance of the output filter L, the output current is constant. When the diode is on, the difference between input current and output current flows through the diode. When the diode is off, the same current runs through the capacitor. Connection to two current sources limits the di/dt of the diode and parallel capacitor limits $dv/dt$ of the diode. Hence, turn off transition of the diode is smooth and almost lossless.

In [27], output inductor is not bulky and therefore carries a considerable AC current ripple. Such a design results in wider resistive characteristics. [37] and [38] use the same idea to design class E inverters for variable-load operation.
The basic circuit of a class E rectifier with a parallel inductor is shown in Figure 2-7 (a). It consists of a rectifier diode D, an inductor L. In [39] and [40], diode parallel capacitor is not considered which makes the analysis less accurate. Inductance L is relatively small so the inductor carries the output average current and significant AC ripple. Similar to the other class E circuits, the input current is assumed to be sinusoidal. The principle of the operation is explained by the current and voltage waveforms, shown in Figure 2-7 (b). When the diode is on, $V_O$ is applied to the inductor. Thus, current $i_L$ increases linearly. The current through the diode increases slowly when it turns on. This current is increasing until $i_L$ reaches zero. Then, the inductor absorbs input current and finally, the diode turns off. When the diode is off, $i_L$ is equal to the input sinusoidal current and the inductor voltage will be sinusoidal. The reverse diode voltage $v_{DR}$ is equal to the difference between $V_O$ and $v_L$. 

**Figure 2-6: Class E rectifier with parallel capacitor waveforms**
This circuit matches the applications includes a transformer with a small magnetizing inductor. So, the magnetizing inductance can be absorbed in the circuit. However, as the intrinsic parallel capacitor of the diode is not considered in the circuit, high-frequency ringing caused by this capacitor increases the voltage stress of the diode up to two times.

![Class E rectifier with parallel inductor](image)

(a) Class E rectifier with parallel inductor

![Class E rectifier with parallel inductor waveforms](image)

(b) Class E rectifier with parallel inductor waveforms

**Figure 2-7: Class E rectifier with parallel inductor**

In [41], as shown in Figure 2-8 (a), the parallel capacitor is considered in the design. In addition, the rectifier is fed by a current source. In this circuit, the parallel capacitor limits the $dv/dt$ of the diode and eliminate the ringing voltage across the diode. As shown in Figure 2-8 (b), the diode waveforms are similar to the rectifiers with a parallel capacitor.
2.2.8 Other High-Frequency Rectifiers

Resonant rectifiers are not limited to class E or class DE circuits. Any high-performance circuit which provides low $dv/dt$ and/or $di/dt$ for the diode and considers the high-frequency limitations is applicable at higher frequencies.

Figure 2-9 (a) shows the proposed rectifier in [42]. It consists of a diode, a capacitor in parallel with it, an inductor connected in series and a large output filter capacitor. This circuit is supplied with a sinusoidal voltage source. This is a useful circuit when the rectifier is placed after a transformer. Important parasitic components are included in the main circuit, such as diode’s intrinsic capacitance and transformer leakage inductance in the inductor L. Consequently, circuit
modeling is accurate and the calculated values of the high-frequency operation parameters are close to the measured ones. Ideal waveforms of the steady-state currents and voltages of the diode are shown in Figure 2-9 (b).

![High-frequency rectifier with series inductor and parallel capacitor](image1.png)

(a) High-frequency rectifier with series inductor and parallel capacitor

![High-frequency rectifier with series inductor and parallel capacitor waveforms](image2.png)

(b) High-frequency rectifier with series inductor and parallel capacitor waveforms

**Figure 2-9: A high-frequency rectifier with series inductor and parallel capacitor**

Similar rectifier structure is used in [43]. In contrast with the proposed circuit in [42], the rectifier is not fed with a sinusoidal waveform. Instead, a single-ended inverter is used in the circuit. According to the nonzero average DC value of the rectifier input voltage, power is delivered in DC and AC form which increases the efficiency of the circuit. Figure 2-10 shows the rectifier structure and waveforms.
2.2.9 Harmonic Manipulation

To decrease the switch voltage stress in class E converters, harmonic elimination is proposed in [7], [44] and [45]. As shown in Figure 2-11, $v_{sw}$ contains a significant amount of the second harmonic which increases the peak of the voltage waveform. Elimination of this harmonic causes lower peak value for $v_{sw}$. A series LC tank tuned at the second harmonic can short out this harmonic to the ground. Figure 2-12 (a) and (b) show two converters using the second harmonic eliminator. This modification is able to decrease the voltage peak down to 2.2 times of input voltage [7]. However, complex circuit design and narrow band frequency operation are the drawbacks of this configuration.
2.2.10 Review of High-Frequency Converters

A class E circuit converts a DC voltage into an AC form. As mentioned before, this voltage can be converted to a DC voltage by using a rectifier. In a class E circuit, a transformer can be utilized to shift the voltage to a higher or lower level. Class E inverters and rectifiers can be designed independently. Therefore, a variety of inverter and rectifier combinations are possible. Figure 2-13 (a) to (g) show a set of different combination of inverters and converters.
Figure 2-13: Miscellaneous class E DC-DC converters

In [46], a 22 MHz converter, shown in Figure 2-13 (a), is proposed based on a class E circuit. A transformer is used to isolate the input/output terminals and the output voltage is controlled by changing the frequency in a narrow range. The input voltage ranges from 40V to 60V, and the converted output voltage was 5V with a 1% tolerance. The efficiency of the converter reaches a maximum of 78% at 35W.

The proposed converter in [48] uses both class E inverter and rectifier. In addition, a second harmonic parallel filter blocks the second harmonic current. This circuit does not require an RF choke for proper operation. However, second harmonic filter increases the design complexity and
reduces the operating frequency range. Maximum efficiency of 82% was achieved at 1 MHz switching frequency. The proposed converter in [49] uses a balanced pair of single diode rectifiers. Therefore, the load appears resistive in a wide range of operation. The circuit achieves 75% efficiency over its operating range at 100 MHz. A 10 MHz isolated synchronous converter is proposed in [50]. This circuit used class E inverter with second harmonic filter and class E rectifier with a parallel capacitor. The synchronous operation of the converter increases the maximum efficiency from 80% to 82%. The proposed circuit in [51] uses class DE inverter and Class E rectifier to gain the benefits of both circuits. The complexity of the gate drive limits the application of this circuit to lower voltage applications. Maximum efficiency of 80% was reported at 1 MHz switching frequency and 1V output.

2.2.11 Quasi-Resonant Converters

One way to achieve zero voltage at turn-on is to employ the Class E or DE inverters. Another alternative is the zero-voltage switching (ZVS) quasi-resonant technique [43], [52] and [53]. This technique introduces a large family of converters capable of high-frequency high-efficiency operation. Figure 2-14 shows a boost quasi-resonant converter. In the ZVS quasi-resonant converters (QRC’s), zero-voltage turn-on is achieved by applying the resonant switch concept where the resonant capacitance is placed in parallel with the switch. The term “quasi-resonant” describes the way the resonant switch operates [52]. In fact, the resonance occurs only when the switch is off. The resonant capacitor voltage initially increases and then decreases in a resonant mode, finally reaching zero. A variety of topologies is introduced in this family [54]. In all cases, the switch is turned on at zero voltage.

According to the lower number of reactive components, the operation frequency of quasi-resonant converters is wider. In addition, this family of converters transfers power in DC form as well as AC which results in lower conduction losses for similar output power. In ideal operation point, both $v_{SW}$ and $dv_{SW}/dt$ are zero at turn-on time. Hence, switch current and voltage oscillations are
minimized. Effect of the rectifier diode intrinsic capacitor the design is considered in [55] to form multi-resonant converters.

(a) A boost quasi-resonant converter

(b) The switch waveforms in a boost quasi-resonant converter

Figure 2-14: A boost quasi-resonant converter

2.2.12 Summary of High-Frequency Topologies

Zero voltage switching operation and absorbing parasitic components in the circuit are the common specifications of high-frequency converters. While the conventional class E inverter provides these specifications, it also has some important limitations such as the high voltage stress imposed on the switch. Class DE inverters solve the voltage stress problem by replacing the input inductor with a switch. However, this modification requires a floating gate and an ultrafast gate drive circuit which is not easy to implement in high frequency and high voltage applications. The second harmonic filters decrease the switch voltage stress at the cost of complexity of the circuit. Operation and specifications of high-frequency rectifiers are similar to their dual inverters. The performance of
the quasi-resonant boost converter is close to class E converters while this circuit takes the advantage of DC power flow to improve its performance. Based on above-mentioned issues, there is a need for proper topologies that fit high-frequency operation, provide low-stress waveforms and require less number of reactive components.

2.3 Converter Modeling

In the previous section, the operation of high-frequency resonant inverters and rectifiers were discussed. In order to design an efficient converter, an accurate model for the converter is required. A variety of methods has been proposed to design high-frequency switching circuits. Generally, in terms of the design methodology, they can be classified into three groups.

2.1.1 Analytical Approaches

In an analytical approach, the steady-state waveforms are presumed and all calculations are based on steady waveforms [50], [56] and [57]. Differential equations are solved for pre-assumed initial values. In many cases, to simplify the equations, all components are considered to be ideal and lossless. In addition, inverters and rectifiers are studied separately. According to the high order of the system, a closed form solution is hard to be achieved and numerical techniques are required. In this type of analysis, the designer must update all of the equations for any changes in the circuit. Consequently, the new solution should be obtained for each topology. Basically, this method is more effective for nonlinear circuits. Driven equations and graphs are valid for a specific range of operation points.

2.3.1 Time-domain Numerical Methods

Time-domain numerical software such as Pspice and PSIM provide a precise result for any circuit. However, this approach is much time consuming and system optimization is slow. Specific time-domain solutions are developed for the Class-E circuit in the steady-state analysis [58] and [59], and optimization [60] and [61]. Several fast time-domain simulation algorithms are proposed for
general switching converters accelerate the procedure. Averaging the high order harmonics in [62], approximating the state transition matrices in [63] and using the waveform relaxation technique in [64] are examples of these methods. However, simulation and optimization based on these methods are still slow [61].

2.3.2 Frequency Domain Solutions

Frequency-domain analysis can be utilized to analyze periodically switched linear circuits [65]. Harmonic balance (HB) technique is a useful method for nonlinear circuits such as class E family [66]. In this method, Kirchhoff's laws are satisfied with a limited number of harmonics [67]. Several iterations are required for an accurate solution. Based on the nonlinearity of the system and required accuracy, the solution could be slow or divergent.

The generalized averaging method is useful for modeling power converters and periodic switching circuits [68]. This method approximates a signal in a period of switching with a time-dependent Fourier series representation and transforms time-varying state-space equations into time-invariant ones. By increasing the number of harmonics in the model, more accurate results are achieved. The complexity of the solution depends on the number of harmonics and level of nonlinearity of the circuit. State-space averaging method, explained in [54], is the simplified form of this technique.

In [58] and [69], the active switch is often modeled as a time-dependent resistance. As previously mentioned, the body diode of the switch is not supposed to conduct in the optimal operation of a class E inverter. So, we can consider the switch as a time-variant resistor. When the switch is on, the equivalent resistor is $R_{on}$ and when the switch is off, the equivalent resistor is $R_{off}$. In steady-state operation, the time-varying resistor is presented by a constant matrix in the frequency domain and Kirchhoff laws are applied to the circuit. Similar to the generalized method, a higher number of harmonics in the model results in a more accurate but complex solution.
2.3.3 Summary of Modeling Methods

Usually, a high-frequency converter is a combination of time-variant components such as switches, nonlinear components such as rectifiers, and linear components such as inductors. Depends on the complexity of the circuit and required accuracy, some assumption is applied to model a circuit. Numerical methods are able to predict the behavior of a circuit with the highest accuracy and minimal simplifications. However, these methods are time-consuming. Using analytical methods provides an insight view of the circuit. But any small modification in the circuit changes the solution. Frequency-domain solutions can be utilized to analyze switching power converters. However, the solution becomes more complex for circuits with a higher order of complexity. All of the reviewed methods have specific advantages and limitations. The circuit designer chooses the proper tool for the modeling problem.

2.4 Converter Control

In this section, the different methods of the output voltage control for resonant converters are reviewed, and their merits/demerits are discussed.

2.4.1 Variable Frequency

Frequency control is the traditional method to control a resonant converter [70] - [73]. Figure 2-15 shows an LCC resonant converter circuit and a frequency control scheme for this converter. The converter gain is a function of switching frequency and by adjusting the frequency, the output voltage is controlled properly. This method is applicable for class E and DE converters. By choosing a proper range of switching frequency, zero voltage switching and power regulation are achieved [46] and [74]. In this method, the voltage error is fed to a compensator to generate the switching frequency.
Figure 2-15: Variable frequency control for LCC resonant converter

A major disadvantage of this control method is the required wide range of operating frequencies to regulate the output. Wide operating range complicates the magnetic design and gate signal generation. Thus, efficiency and performance are degraded. Therefore, with variable frequency control, high performance and zero voltage switching operation are not guaranteed for a wide operating range.
2.4.2 Self-sustained Oscillation Controller

One kind of a variable frequency control is the self-sustained oscillation controller [75], which operates in a smaller frequency range. Figure 2-16 shows a simple SSOC method block diagram. The controller changes the delay between the inverter current zero crossing and the switching voltage. However, SSOC has its own disadvantages. First, current sensing is a part of the structure which makes the system larger and more expensive. Second, measuring the current introduces a significant delay in MHz operation. Another drawback is related to the design requirements. To achieve ZVS for a wide load range, the lower limit of switching frequency should be far above the resonant frequency [76]. This increases reactive power and conduction losses. Also, the high-quality factor is required to reduce the operating frequency range.

![SSOC method block diagram](image)

**Figure 2-16: SSOC method block diagram**

2.4.3 Constant OFF-time Method

Figure 2-17 (a) and (b) show a ZVS quasi-resonant circuit and its waveforms [52]. Achieving zero voltage switching operation while regulating the output for quasi-resonant converters, requires a constant OFF-time control method. This technique is a variable frequency method but switch OFF-time is constant during operation. For ZVS converters, the controller decreases the on-time of the switch at light-load to reduce the power flow. Figure 2-17 (c) shows the block diagram of this control method. To keep the volt-second of the input inductor balance, voltage stress of the switch can be up to 10 times of the input voltage [77].
2.4.4 Constant Frequency

As mentioned before, constant frequency makes the magnetic design more efficient. Also, in some applications, constant frequency operation is required for synchronization between the subsystems. There are a few ways of achieving constant frequency control of resonant converters. For bridge type converters, power flow and gain can be controlled by changing the duty cycle. In this method, instead of applying full square wave and achieving the maximum fundamental harmonic,
harmonics content of the input voltage is manipulated to control power flow. In some circuits, power flow is controlled by disconnecting the load in some switching periods. Finally, some methods turn the converter on and off to regulate the power.

2.4.5 Asymmetrical PWM Control

The method’s name is referred to the asymmetrical inverter voltage [78] and [79]. The idea is to change the fundamental harmonic by changing the duty cycle of the inverter. This method can be implemented by a conventional sawtooth PWM generator. To reduce the power flow, duty cycle decreases from 50% (maximum) to reduce the fundamental harmonics. Equation 2-5 explains the harmonic contents of the input voltage. Figure 2-18 shows the control block diagram of this method. Application of this method is limited to converters with a bridge inverter. In addition, the zero voltage switching operation is not guaranteed for a full range operation.

![Asymmetrical PWM Control control method](image)

Figure 2-18: Asymmetrical PWM Control control method

\[
V_s = \frac{\sqrt{2}V_{in}\sqrt{(1 - \cos(2n\pi D))}}{n\pi} \sin(2n\pi f + \phi_n) \tag{2-5}
\]

where:

\[
\phi_n = \tan^{-1}\left(\frac{\sin(2n\pi D)}{1 - \cos(2n\pi D)}\right) \tag{2-6}
\]
2.4.6 ‘on-off’ Control

In conventional control methods, switching waveforms of the converter are adjusted to change the
converter’s gain and regulate the output. Another approach is to operate the converter at full load
or turn it off to control the average output power and regulate the output voltage. In this method,
we can separate the converter operation and voltage regulation. By increasing the switching
frequency, resonant components become smaller and converter response time becomes shorter.
Therefore, we can turn on and off the converter with lower startup and shutdown losses. This
technique offers efficiency improvements at light load by reducing some of the power losses
mechanisms when the converter is off.

One of the applications for on-off control methods is induction heating [80]. In this case, the quality
factor of the resonant tank is high. So, the resonant current does not fall off during the off-time.
Thus, the converter starts under zero voltage switching condition next time.

On-off control method has been successfully applied to DC-DC converters [50], [76], [81] and [82].
The converter on-off command circuit can be implemented by a conventional PWM controller or
a hysteresis controller. In the first method, when the compensated error is greater than the sawtooth,
the converter is on. Otherwise, the converter is off. In hysteresis control, the converter turns ON,
when the output voltage reaches the lower threshold value and turns off when the voltage reaches
the higher threshold value. Figure 2-19 shows the control block diagram and waveforms in
hysteresis control method.
Despite the high efficiency of on-off control, there are a number of drawbacks related to this method. First, the on-off duty cycle resolution is limited by the ratio of on-off frequency \( f_M \) and the switching frequency \( f_{SW} \). Second, on-off frequency determines the size of the input and output filter capacitors. Third, as the converter is turned on and off frequently, startup and shutdown transients affect the overall performance and efficiency of the system.

### 2.4.7 Thinned-Out Method

This method regulates the output voltage or power with eliminating the voltage pulse of the rectifier at a constant rate [51]. This method is specified for class E rectifiers. Both inverter and rectifier operate under zero-voltage-switching condition. In this method, the rectifier is turned on and off
while the inverter is switching continuously. So, circulating resonant current and gate power losses reduce the efficiency of the converter at light loads. Figure 2-20 shows the schematic and waveforms of a class E rectifier used in this method.

![Block diagram of a class E rectifier with a shunt switch](image)

(a) Class E rectifier with a shunt switch

![Block diagram of a Thinned-Out control method](image)

(b) Thinned-Out control method block diagram

![Waveform of rectifier voltage in Thinned-Out control method](image)

(c) Rectifier voltage in Thinned-Out control method

**Figure 2-20: Thinned-Out control method**

2.4.8 **Summary of Resonant Converter Control Methods**

A verity of control methods was reviewed in this section. To choose a proper control method for a resonant converter, practical considerations such as the implementation of the control method, gate drive circuit, conduction losses, and full range performance should be considered. Inefficient magnetic design, significant circulating current and low efficiency at light load are the main
disadvantages of variable frequency control methods. SSOC and asymmetrical PWM methods are useful for specific converters. In addition, timing requirement of these methods is hard to be implemented in MHz frequency range. Variable ON-time control is suitable for quasi-resonant converters but introduces a high voltage stress on the switch. Constant frequency operation can solve the problems of variable frequency methods, but cannot guarantee zero voltage switching operation for a full operating range. Although on-off or bang-bang control methods improve the converter performance in light-load conditions, their superior performance is achievable for very low on-off rate compared to the switching frequency which makes the converter slow and bulky.

2.5 Conclusion

Considerable reduction in switching losses makes zero voltage switching converters a practical candidate for MHz power conversion. In theory, there is no maximum switching for resonant converters. However, in practical applications, there are constrained imposed by gate drive circuits losses and growth of conduction and magnetic losses at higher frequencies. A proper converter shall be selected based on nearly optimized switching frequency for a specific voltage and power rating. In this regard, a suitable topology for each specific operation range and frequency should be selected. An appropriate and practical control method is also required to achieve a high-performance for a wide range of operation. Time delay, duty cycle resolution, processing time, and converter topology limit the number of practical control methods in MHz range. The on-off based control method is a popular method for high-frequency converters. Although this method improves the converter performance in light-load conditions, its superior performance is achievable only for very low on-off rate compared to the switching frequency.
Chapter 3

New Quasi-Resonant Boost Converters with Reduced Voltage Stress and Switching Losses

3.1 Introduction

In order to develop a high-frequency high-performance switching power supply, a combination of appropriate converter topology and control method must be addressed. Switching losses can be eliminated by using zero voltage switching (ZVS) converters. However, other frequency dependent losses such as conduction losses, magnetic losses, and gate drive losses increase with the switching frequency, and thus negatively impact efficiency. Therefore, a high-frequency high-performance DC-DC converter requires a ZVS topology that avoids/reduces extra frequency-dependent losses while eliminating switching losses.

Since the 1970s, switching converters operating in the MHz frequency range have employed resonant and quasi-resonant circuits to achieve high efficiency [83]-[86]. These topologies utilize single-ended resonant circuits to improve their compatibility at high frequencies. Due to the resonant nature of these circuits, proper performance of the converter is generally limited to a narrow load range. Therefore, achieving high performance across a wide load range is still a challenging topic.

In this chapter, a new quasi-resonant converter topology and a novel approach to analyze and design these types of converters are proposed. The modified rectifier circuit reduces the output diode voltage stress without introducing significant conduction losses. Furthermore, a new approach in synthesizing the converter’s equations provides better insight into the operation of the circuit and the converter’s design. The analysis and design based on the resonant input inductor add more
flexibility to the component selection. These overall developments improve the performance of quasi-resonant converters for MHz DC-DC applications.

3.2 Non-Isolated Quasi-Resonant Converter

Figure 3-1 shows our modified quasi-resonant converter that combines the wide input voltage range of quasi-resonant converters and the low voltage stress of class DE rectifiers. The basic version of this quasi-resonant boost converter was proposed in [86]. The boost nature of the circuit offers a wide input voltage range, and lower number of components provides a wide operating frequency range. Single ground reference switch, parasitic components absorption in the topology, and a low number of reactive components make this topology attractive for MHz operation. In conventional quasi-resonant converters, a bulky input inductor is employed to provide a DC input current. However, a large input inductor costs more and increases the response time of the converter as well as the switching losses during start-up and shut down. As discussed in Chapter 2, on-off control method is an effective technique to control a high-frequency converter (The implementation of this technique on the proposed converter is discussed in Chapter 4). Start-up and shut down power losses influence the overall efficiency in this method. To make the converter compatible with on-off control method, a finite resonant inductor is used as the input inductor. Although the input high-frequency current ripple is amplified, faster dynamic response and lower switching losses during system start-up are gained due to using smaller components.
As shown in Figure 3-1, MOSFET and diodes turn on and off under zero voltage switching condition. The switch parallel capacitor \((C)\) limits \(dv/dt\) of the switch, and the resonant circuit discharges this capacitor just before the gate drive circuit turns the switch on.

In conventional quasi-resonant converters, stored energy in the intrinsic capacitance of the rectifier is dissipated via an unwanted high-frequency oscillation with \(L_r\) that increases the rectifier voltage stress up to 2 times [86]. In [55], an additional parallel capacitor with the rectifier transforms the circuit into a multi-resonant converter and absorbs the unwanted oscillation energy. However, charging and discharging this additional capacitor increase the total conduction losses due to an increase in the circulating current. By introducing a low current rating diode, \(D_2\), in the proposed rectifier, a short circuit path to preserve the stored energy in the rectifier into \(L_r\) is provided that avoids the extra resonant current and voltage stress. In this circuit, \(D_2\) clamps the rectifier maximum reverse voltage to \(V_o\) and reduces the unwanted oscillation. The series inductor \((L_r)\) and intrinsic parallel capacitors \((C_{D1,2})\) of the rectifier reduce \(di/dt\) and \(dv/dt\) of the rectifier and related power losses. Although the rectifier stage looks like a class DE circuit, its operation and waveforms are different. In a class DE rectifier, both diodes carry the same current and the input current is sinusoidal. But in the proposed circuit, \(D_2\) carries much less current compared to \(D_1\).
The switch voltage stress in steady-state is close to class E inverters (about 3.5 times larger than the input voltage for 50% duty-cycle). Although switch voltage stress is higher than converters with a second harmonic filter, availability of high-voltage SiC switches, simplicity, and wide operating range make this converter suitable for high-frequency applications.

Figure 3-2: Key waveforms of the converter in steady-state.
3.2.1 Converter Operation

A switch mode amplifier or a switching power supply is a nonlinear time variant circuit. Therefore, a proper analysis is required to study this type of circuit. Although some exact solutions are proposed for resonant circuits [87], these solutions are complex and difficult to modify. Many simplified solutions are accurate enough for design purposes [83]. In some solutions, valid simplifications are applied to convert the circuit to a linear time-invariant system [69]. In this type of analysis, parasitic components can be considered in state-space equations. In addition, modification of the model can be done with a minor change in the equations. Extracted model is useful to optimize the circuit. However, these method does not provide a good understanding of the circuit operation. In some analysis, the operation of the converter is divided into some specified intervals in each the circuit behaves linearly [77]. The final results of each interval can be considered as initial conditions for the next successive interval. Employing this approach, a circuit can be analyzed, and extracted results normally provide a good insight into the operation of the circuit. In this section, distinct stages of the circuit are explained for better understanding of the converter operation. Moreover, associated state-space equations are provided for each stage. Approximate components stress and the power flow equation are also provided.

To analyze the steady-state operation of the converter, the state-space variables of the circuit are selected. $i_{Lin}$ ($L_{in}$ current), $v_{Q1}$ ($Q_1$ drain-source voltage), and $i_{Lr}$ ($L_r$ current) are the state-space variables of the converter. Other parameters are described in Figure 3-1. The operation of the system is described in 5 stages. To study the circuit behavior, the following assumptions are made: all components are ideal; rectifier’s intrinsic capacitor is small compared to the switch parallel capacitor; and MOSFET switching time is zero.

**Stage 1** ($t_0 - t_1$): Before this interval, the switch is off, $D_1$ is ON, $D_2$ is off, $L_{in}$ and $L_r$ carry $i_{Lino}$ and $i_{Lr0}$ respectively. At $t_0$, the voltage across the switch reaches zero, and $Q_1$ turns on under zero
voltage condition. As shown in Figure 3-3(a), the input inductor $L_{in}$ is charged by the input voltage and $L_r$ is discharged into the output. This interval continues until $L_r$ is fully discharged and $D_1$ turns off. Equations (3.1)-(3.8) illustrate the operation of the system in this interval. Key waveforms of the converter are given in Figure 3-2.

\[ v_{Q1} = 0 \]  
\[ i_{Lin} = \frac{V_i}{L_{in}}(t - t_0) + I_{Lin0} \]  
\[ i_{Lr} = -\frac{V_o}{L_r}(t - t_0) + I_{Lr0} \]  
\[ I_{lr1} = I_{lr1}(t_1) = I_{lr0} - \frac{V_o}{L_{in}}(t_1 - t_0) = 0 \]  
\[ t_1 - t_0 = \frac{I_{lr0} \times L_r}{V_o} \]  
\[ I_{Lin1} = I_{Lin}(t_1 - t_0) = I_{Lin0} + \frac{V_i}{L_{in}}(t_1 - t_0) \]  
\[ v_{Crect1} = V_o \]  
\[ C_{rect} = C_{D1}||C_{D2} \]

**Stage 2** ($t_1 - t_2$): When $L_r$ is fully discharged into the output, the second interval starts. $L_r$ limits $dv/dt$ of the rectifier and equivalent rectifier’s capacitor ($C_{rect}$) limits $dv/dt$ of the diodes. Hence, $D_1$ turns off with the minimum switching loss. The equivalent circuit of the converter in this interval is shown in Figure 3-3(b). As $Q_1$ is still on, input inductor is being charged while $L_r$ resonates with $C_{rect}$. This interval continues until $C_{rect}$ is fully discharged by $L_r$ at $t_2$. In fact, the stored energy into the rectifier capacitance is transferred into $L_r$. When rectifier voltage reaches zero, $D_2$ turns on.
and clamps the rectifier voltage to zero. Equations (3-9)-(3-17) illustrate the operation of the system in this interval.

\[ v_{Q1} = 0 \quad (3.9) \]
\[ i_{Lin} = \frac{V_i}{L_{in}}(t - t_1) + i_{Lin1} \quad (3.10) \]
\[ i_{lr} = -\frac{V_o}{Z_{rect}} \sin(\omega_{rect}(t - t_1)) \quad (3.11) \]
\[ v_{Crect} = V_o \cos(\omega_{rect}(t - t_1)) \quad (3.12) \]
\[ t_2 - t_1 = \frac{\pi}{2} \sqrt{L_R C_{rect}} \quad (3.13) \]
\[ i_{Lin2} = \frac{V_i}{L_{in}}(t_2 - t_1) + i_{Lin1} \quad (3.14) \]
\[ i_{lr2} = -\frac{V_o}{Z_{rect}} \quad (3.15) \]
\[ v_{Crect2} = 0 \quad (3.16) \]

where:

\[ Z_{rect} = \sqrt{\frac{L_R}{C_{rect}}}, \quad \omega_{rect} = \frac{1}{\sqrt{L_R C_{rect}}} \quad (3.17) \]

Stage 3 \((t_2 - t_3)\): By discharging \(C_{rect}\) at \(t_2\), \(D_2\) turns on and connects the output terminal of \(L_r\) to ground. As \(Q_1\) is still on, the voltage across \(L_r\) is zero, and its current stays constant during this mode. In addition, the input voltage is still charging \(L_{in}\). Figure 3-3(c) shows the equivalent circuit in this interval. The operation of the converter in the following stages are dependent on \(i_{Lin}\) at \(t_3\), and hence, the \(Q_1\) stays on until \(L_{in}\) gains enough current to guarantee the proper operation of the system. Equations (3.18)-(3.25) illustrate the operation of the system in this interval.
\[ v_{Q1} = 0 \]  
(3.18)

\[ i_{Lin} = \frac{V_i}{L_{in}} (t - t_2) + l_{Lin2} \]  
(3.19)

\[ i_{Lr} = -\frac{V_o}{Z_{rect}} \]  
(3.20)

\[ v_{Crect} = 0 \]  
(3.21)

\[ t_3 - t_2 = \text{controller ends this mode} \]  
(3.22)

\[ i_{Lin3} = \frac{V_i}{L_{in}} (t_3 - t_2) + l_{Lin1} \]  
(3.23)

\[ i_{Lr3} = -\frac{V_o}{Z_{rect}} \]  
(3.24)

\[ v_{Crect2} = 0 \]  
(3.25)

**Stage 4** \((t_3 - t_4)\): Stage 4 starts when \(Q_1\) turns off. The parallel capacitor \(C\) plays the role of a snubber capacitor and limits \(dv/dt\) of the switch. Therefore, the switch turns on under ZVS condition. By turning \(Q_1\) off, \(L_{in}, L_r\) and \(C\) resonate and the voltage across \(Q_1\) rises. This mode continues until \(i_{Lr}\) reaches zero and \(D_2\) turns off. Figure 3-3(d) shows the equivalent circuit in this mode. Equations (3.26)-(3.32) illustrate the operation of the system in this interval.

\[ v_{Q1}(t) = \frac{(V_i \times L_R)}{L_R + L_{in}} (1 - \cos(\omega_2 (t - t_3))) + I_4 Z_2 \sin(\omega_2 (t - t_3)) \]  
(3.26)

\[ v_{Q1}(t_4) = \frac{(V_i \times L_R)}{L_R + L_{in}} (1 - \cos(\omega_2 (t_4 - t_3))) + I_4 Z_2 \sin(\omega_2 (t_4 - t_3)) \]  
(3.27)

\[ i_{Lin}(t) = i_{Lin3} + \frac{(V_i)}{(L_R + L_{in})} (t - t_3) + \frac{I_4 Z_2}{L_{in} \omega_2} \left(1 - \cos(\omega_2 (t - t_3))\right) \]  
(3.28)

\[ \quad + \frac{(V_i) L_r}{(L_R + L_{in}) L_{in} \omega_2} \sin(\omega_2 (t - t_3)) \]
\[ i_{Lin4} = I_{Lin3} + \frac{(V_i)}{(L_R + L_{in})}(t_4 - t_3) + \frac{I_4Z_2}{L_{in} \omega_2} \left(1 - \cos(\omega_2(t_4 - t_3))\right) \]

\[ + \frac{(V_i)L_r}{(L_R + L_{in})L_{in} \omega_2} \sin(\omega_2(t_4 - t_3)) \]

\[ i_{LR}(t) = I_{LR3} + \frac{(V_i)}{(L_r + L_{in})}(t - t_3) + \frac{I_4Z_2}{L_R \omega_2} \left(1 - \cos(\omega_2(t - t_3))\right) \]

\[ - \frac{(V_i)}{(L_R + L_{in})\omega_2} \sin(\omega_2(t - t_3)) \]

\[ i_{LR4} = I_{LR3} + \frac{(V_i)}{(L_r + L_{in})}(t_4 - t_3) + \frac{I_4Z_2}{L_R \omega_2} \left(1 - \cos(\omega_2(t_4 - t_3))\right) \]

\[ - \frac{(V_i)}{(L_R + L_{in})\omega_2} \sin(\omega_2(t_4 - t_3)) \]  

Where:

\[ Z_2 = \sqrt{\frac{L_{eq}}{C}}, \omega_2 = \frac{1}{\sqrt{L_{eq} C}}, L_{eq} = \frac{L_{eq} L_{in}}{(L_R + L_{in})}, I_4 = I_{Lin3} - I_{LR3} \]

**Stage 5** (\(t_4 - t_5\)): When \(D_1\) turns off, rectifier equivalent capacitor joins the resonant circuit. As shown in Figure 3-3(e), the equivalent circuit is more complicated in this interval. The dynamic of the series combination of \(C_{rect}\) and \(L_r\) is faster than the rest of circuit, the length of this interval is estimated by a fourth of the resonant frequency of \(C_{rect}L_r\) tank. In addition, the effect of rectifier voltage on the rest of the circuit is ignored. At the end of this interval, \(C_{rect}\) is charged to \(V_0\) and \(D_1\) turns on. Equations (3.33)-(3.41) illustrate the operation of the system in this interval.

\[ v_{Q1}(t) = \frac{(V_i \times L_R)}{L_R + L_{in}} \left(1 - \cos(\omega_2(t - t_3))\right) + I_4Z_2 \sin(\omega_2(t - t_3)) \]

\[ v_{Q1}(t_5) = \frac{(V_i \times L_R)}{L_R + L_{in}} \left(1 - \cos(\omega_2(t_5 - t_3))\right) + I_4Z_2 \sin(\omega_2(t_5 - t_3)) \]
\[ i_{Lin}(t) = I_{Lin3} + \frac{(V_i)}{(L_R + L_{in})} (t - t_3) + \frac{I_4Z_2}{L_{in} \omega_2} (1 - \cos(\omega_2(t - t_3))) \]
\[ + \frac{(V_i)L_r}{(L_R + L_{in})L_{in} \omega_2} \sin(\omega_2(t - t_3)) \]
\[ i_{lr} \approx \frac{V_{Q1(t4)}}{Z_{rect}} \sin(\omega_{rect}(t - t_4)) \]
\[ v_{Crect} \approx V_{Q1(t4)} \cos(\omega_{rect}(t - t_4)) \]
\[ (t_5 - t_4) \approx \frac{\pi}{2} \sqrt{L_R C_{rect}} \]
\[ I_{Lin5} = I_{Lin3} + \frac{(V_i)}{(L_R + L_{in})} (t_5 - t_3) + \frac{I_4Z_2}{L_{in} \omega_2} (1 - \cos(\omega_2(t_5 - t_3))) \]
\[ + \frac{(V_i)L_r}{(L_R + L_{in})L_{in} \omega_2} \sin(\omega_2(t_5 - t_3)) \]
\[ i_{lr5} \approx V_{Q1(t_4)} \sqrt{\frac{C_{rect}}{L_R}} \]
\[ V_{Crect5} = V_O \]

**Stage 6** \((t_5 - t_0)\): Stage 6 starts when the rectifier voltage reaches \(V_O\). Figure 3-3(f) shows the equivalent resonant circuit in this mode. During this interval, inductors \(L_{in}, L_r\) and \(C\) resonate until the capacitor voltage reaches zero or the controller turns \(Q_1\) on at \(t_0\). In a proper timing scheme, the capacitor voltage is close to zero when the switch is turned on. Consequently, \(Q_1\) turns on under zero voltage condition in the next cycle. State-space variables are given by (3.42)-(3.45).
\[ v_{Q1}(t) = \left( \frac{V_i \times L_R + V_o \times L_{in}}{L_R + L_{in}} \right) (1 - \cos(\omega_2(t - t_5))) + I_6 Z_2 \sin(\omega_2(t - t_5)) \]  
\[ + V_{Q1}(t_5) \times \cos(\omega_2(t - t_5)) \]  
(3.42)

\[ i_{Lin}(t) = I_{Lin5} + \left( \frac{V_i - V_o}{L_R + L_{in}} \right) (t - t_3) + \frac{I_6 Z_2}{L_{in} \omega_2} (1 - \cos(\omega_2(t - t_3))) + \left( \frac{V_i L_R}{(L_R + L_{in}) L_{in} \omega_2} \right) \]  
\[ + \left( \frac{V_o}{L_R + L_{in} \omega_2} \right) - \frac{v_{Q1}(t_5)}{L_{in} \omega_2} \sin(\omega_2(t - t_3)) \]  
(3.43)

\[ i_{Lr}(t) = I_{Lr5} + \left( \frac{V_i - V_o}{L_R + L_{in}} \right) (t - t_5) + \frac{I_6 Z_2}{L_R \omega_2} (1 - \cos(\omega_2(t - t_5))) + \left( \frac{V_i}{L_R + L_{in} \omega_2} \right) \]  
\[ - \left( \frac{V_o L_{in}}{(L_R + L_{in}) L_R \omega_2} \right) - \frac{v_{Q1}(t_5)}{L_{in} \omega_2} \sin(\omega_2(t - t_5)) \]  
(3.44)

where:

\[ I_6 = I_{Lin5} - I_{Lr5} \]  
(3.45)
The first interval starts right after the sixth. Therefore, final values of the sixth stage are the initial values of the first one. To compute the steady-state operation, we can start with any arbitrary stage.

A stage with minimum unknown initial state values is desired as the initial operating point. At \( t_3 \) the switch voltage is zero, and the initial value of the \( i_{Lr} \) is known as a function of the output voltage. Therefore, \( t_3 \) is a proper moment as the origin of time. A numerical approach is used to find the required frequency and duty cycle for different values of \( i_{L\text{in}}(t_3) \) in the steady-state condition.

**Figure 3-3: The converter equivalent circuits in every stage**
Next, operating parameters such as switch peak voltage, average input current and power are determined for each operating frequency.

### 3.2.2 Converter Design

Proper selection of components is required to achieve ZVS and a high-performance operation. For a nominal frequency and input/output voltage ratings, many combinations of $L_r$, $L_{in}$, and $C$ are available to satisfy ZVS condition. However, the nominal power rating is significantly dependent on resonant inductor $L_r$. In fact, $L_r$ not only plays a critical role in the resonant circuit but also controls the power flow in the converter. Hence, $L_r$ is the first component to be selected.

To determine the value of $L_r$, we assume the voltage across the switch is a half sinusoidal wave and the switch duty cycle is 50% at nominal voltage and power. Furthermore, we assume that rectifier capacitor is negligible and rectifier voltage is rectangular. To achieve volt-second balance of the input inductor, the switch peak voltage is about $\pi$ times the input voltage. Figure 3-4 represents the equivalent circuit for power flow calculations. As shown in (3.56), power flow is a function of input/output voltage, frequency, and $L_r$.

\[
i_{L_r}(t) = 0, \quad 0 < t < t_0
\]

where:

\[
t_0 = \frac{1}{\omega} \sin^{-1}\left(\frac{V_o}{\pi V_{in}}\right)
\]

\[
i_{L_r}(t) = \int_{t_0}^{t} \frac{\pi V_{in}}{L_r} \sin(\omega t) - \frac{V_o}{L_r} \, dt, \quad t_0 < t < \frac{\pi}{\omega}
\]

\[
i_{L_r}(t) = \frac{\pi V_{in}}{L_r} (\cos(\omega t_0) - \cos(\omega t)) - \frac{V_o}{L_r} t
\]

\[
i_{L_r}\left(t = \frac{\pi}{\omega}\right) = \frac{\pi V_{in}}{L_r} (\cos(\omega t_0) + 1) - \frac{\pi V_o}{\omega L_r}
\]

\[
i_{L_r}(t) = i_{L_r}\left(\frac{\pi}{\omega}\right) + \int_{t_0}^{t} - \frac{V_o}{L_r} \, dt, \quad \frac{\pi}{\omega} < t < t_1
\]
\[ i_{L_r}(t) = i_{L_r} \left( \frac{\pi}{\omega} \right) - \frac{V_0}{L_r} t \]  

(3.52)

where:

\[ t_1 = \frac{L_r i_{L_r} \left( \frac{\pi}{\omega} \right)}{V_0} + \frac{\pi}{\omega} \]  

(3.53)

\[ i_{L_r}(t) = 0, \quad t_1 < t < \frac{2\pi}{\omega} \]  

(3.54)

\[ i_{L_r,AVG} = \frac{1}{T} \int_0^T i_{L_r}(t) \, dt, \]  

(3.55)

\[ P_{out} = V_0 \left( \frac{\omega}{2\pi L_r} \left[ \frac{\pi V_{in}}{\omega^2} \sin(\omega t_0) + \frac{\pi V_{in}}{\omega} \cos(\omega t_0) \left( \frac{\pi}{\omega} - t_0 \right) - \frac{V_0}{2} \left( \frac{\pi^2}{\omega^2} - t_0^2 \right) \right] + \frac{\omega}{2\pi} i_{L_r} \left( \frac{\pi}{\omega} \right)^2 L_r \right) \]  

(3.56)

\[ i_{L_r,AVG} = \frac{K_p}{L_r} + \frac{K_q}{L_r} \]  

(3.57)

where:

\[ K_p = \frac{\omega}{2\pi} \left[ \frac{\pi V_{in}}{\omega^2} \sin(\omega t_0) + \frac{\pi V_{in}}{\omega} \cos(\omega t_0) \left( \frac{\pi}{\omega} - t_0 \right) - \frac{V_0}{2} \left( \frac{\pi^2}{\omega^2} - t_0^2 \right) \right] \]  

(3.58)

\[ K_q = \frac{\omega}{2\pi} \left( \frac{\pi^2 V_{in}^2}{2V_0} \cos(\omega t_0) + 1 \right)^2 - \frac{\pi^2 V_0^2}{2\omega^2} \]  

(3.59)

\[ \frac{V_{peak} \sin(\omega t) \times (\text{sgn}(\sin(\omega t)) + 1)}{2} \]

\[ \text{Figure 3-4: Simplified equivalent circuit for power analysis} \]
There is a trade-off between the size of $L_{in}$ and $C$. By using a larger parallel capacitor, a smaller input inductor is required. However, there are limits forced by the theoretical and practical subjects. The lower limit for capacitor value is achieved when input inductor value is infinity. Another constrain is applied by the switch intrinsic capacitance. In other words, the total resonant capacitor cannot be smaller than the switch intrinsic capacitance. For a proper design, power loss, converter size, and dynamic of the converter should considered in selecting component values.

Semiconductor components are selected based on required voltage and current ratings. Equations (3.60)-(3.76) describe the required ratings for $Q_1$, $D_1$, and $D_2$ when operating at the nominal frequency, input/output voltage, and power.

\[
V_{\text{peak}}(Q_1) \approx \pi V_{in} \quad (3.60)
\]
\[
V_{\text{peak}}(D_1) = V_o \quad (3.61)
\]
\[
V_{\text{peak}}(D_2) = V_o \quad (3.62)
\]
\[
l_0(L_r) \approx \frac{\pi}{\omega L_r}(2V_{in} - V_o) \quad (3.63)
\]
\[
t_1 \approx \frac{l_{LR} L_r}{V_o}, t_2 = \frac{T}{2} - t_1 \quad (3.64)
\]
\[
I_{lin0} = \frac{P_{in}}{V_{in}} - \frac{TV_{in}}{4L_{in}} \quad (3.65)
\]
\[
during t_1: I_{Q1} = I_{LR} - \frac{V_o}{L_r} t + I_{lin0} + \frac{V_{in}}{L_{lin}} t \quad (3.66)
\]
\[
t_1: I_{Q1} = a + bt \quad (3.67)
\]
\[
t_2: I_{Q1} = c + dt \quad (3.68)
\]
\[
a = I_{LR} + I_{lin0} \quad (3.69)
\]
\[
b = \frac{V_{in}}{L_{lin}} - \frac{V_o}{L_r} \quad (3.70)
\]
To make the control circuit simple and small, the operating switching frequency is kept constant in a number of bang-bang control applications for high-frequency converters [50] and [81]. Still, fixed frequency switching operation decreases the performance of the system in a wide operating range. To maintain the performance of the converter in a wider voltage range, switching frequency and duty cycle should be controlled according to the input and output conditions. However, it should be noted that changing the switching and duty cycle requires more complicated control and drive circuits when compared to a simple on-off comparator and an oscillator. Then, cost, size, and availability of the control and drive circuits determine the complexity of the control circuit.

3.2.3 Simulation

This section presents LTPICE simulations of the steady-state condition of the 1kW prototype with detailed SPICE models of the system given in Figure 3-5. The component values from design are shown in this figure. The converter was simulated for 1kW output power, nominal input and output voltages of 300V/400V, and a nominal efficiency of 98%. The basic converter waveforms as
simulated for nominal input and output voltage are presented in Figure 3-6. The switch peak voltage is 930 volt which is close to the calculated peak voltage in section 3. As it can be seen in Figure 3-6 (a), $dv/dt$ of the switch is limited when the switch turns off. Hence, gate drive has enough time to turn the switch off under ZVS condition. In addition, the voltage across the switch reaches zero just before the switch turns on.

Figure 3-5: The simulated converter schematic

Figure 3-6(b) illustrates the voltage and current waveforms of the rectifier. Series inductor, $L_r$ limits $di/dt$ of the rectifier. Restricted derivative of the currents gives the diodes enough time to turn off with minimum losses. In addition, the parasitic capacitance of the rectifier, $C_{rect}$ smooths voltage waveform of the rectifier and decreases high-frequency oscillation (ringing) of the circuit. In the conventional quasi-resonance converters, the resonance between $C_{rect}$ and $L_r$ creates a high-frequency ringing at the terminals of $D_1$ (about twice the output voltage). This ringing dissipates the stored energy in the rectifier capacitance and creates electromagnetic interference. In this
circuit, $D_2$ prepares a short circuit path for negative $i_{Lr}$ produced by stored energy in $C_{rect}$ and limits the main diode voltage stress to the output level. In addition, the stored energy in the rectifier capacitance is preserved in $L_r$ until the next cycle. Figures 3-7 and 3-8 show zero voltage switching operation at 200V and 100V input voltages.

Figure 3-6: Simulation results for 3 MHz non-isolated converter at 300V input voltage
(a) Main switch Drain-Source Voltage  
(b) Rectifier voltage  
(c) Inductors currents. Blue: $i_{\text{Lin}}$, Green: $i_{\text{LR}}$

Figure 3-7: Simulation results for non-isolated converter at 200V input voltage
3.2.4 Experimental Results

An experimental prototype design was completed using the procedures outlined above. The basic characteristics are similar to the simulated converter in the previous section. The component values from design are given in table 3-1. Shown in Figure 3-9, 1kW converter operating at 3MHz was designed for the input voltage range of 100V to 300V and 400V output voltage.
Key waveforms of the converter are shown in Figure 3-10. The switch peak voltage demonstrated in Figure 3-10 (a) is about 900V at 100V input voltage. The conventional rectangular waveform is used to drive the MOSFET. According to the low input capacitance of the SiC MOSFET, total gate power loss is less than a watt which is neglectable for a 1kW converter. The switch turns on just after drain-source reaches zero. Also, the drain-source voltage rises slowly after the switch turns off. Figure 3-10(b) shows the switch waveforms at 200V input voltage. The rectifier voltage, shown in Figure 3-10(c), is clamped by the output voltage which makes the use of 650V SiC Schottky diodes safe and reliable. Smooth transient of the rectifier voltage and its minimal voltage ringing, verify the proper operation of the circuit. Maximum efficiency of 96% was achieved at 260V input voltage.
(a) Experimental results for 100V input voltage. Yellow: $v_{GS(Q1)}(10V/Div)$, Green: $v_{Q1}(350V/Div)$, Time: (200n/Div)

(b) Experimental results for 200V input voltage. Yellow: $v_{GS(Q1)}(10V/Div)$, Green: $v_{Q1}(350V/Div)$, Time: (100n/Div)

(c) Rectifier voltage for 260V input voltage. Blue: $v_{D1}(100V/Div)$, Time: (100n/Div)

Figure 3-10: Experimental results for non-isolated converter
Table 3-1: Component’s values in the non-isolated prototype converter

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{in}$</td>
<td>26.5μH, AWG# 14,25 turns M3 1090 core</td>
</tr>
<tr>
<td>$L_r$</td>
<td>6.5μH, AWG# 14,13 turn, M3 1090core</td>
</tr>
<tr>
<td>$C$</td>
<td>200 pF, Ceramic 1500 V</td>
</tr>
<tr>
<td>$Q_1$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$D_1$</td>
<td>C3D04060A</td>
</tr>
<tr>
<td>$D_2$</td>
<td>CSD01060A</td>
</tr>
</tbody>
</table>

3.3 Isolated Converter

In many applications, isolation between the converter input and output terminals are mandatory. In numerous DC-DC converters, isolation between terminals is required due to the different ground references. In addition, a transformer is useful in applications with a wide gap between input and output voltage range such as battery chargers.

By adding a transformer to the circuit, transformer parasitic components such as magnetizing and leakage inductance as well as winding capacitance are involved in the circuit and make the system more complicated. Also, additional power loss will decrease the efficiency of the system. Therefore, design is more complex compared to the non-isolated converter. Then, absorbing the parasitic component in the circuit and avoiding extra component is vital in the design.

Figure 3-11 shows a modified isolated push-pull resonant converter. Using a different approach, this converter has also introduced as an isolated boost push-pull resonant converter with a large DC input inductor [88]. Boost nature of the circuit offers a wide input voltage range. The lower number of components makes it suitable for a wide operating frequency range. In the conventional converter, a bulky input inductor is used to minimize input current. Using a large DC input inductor
costs more and decreases the response time of the converter and increases switches voltage stress during start-up and shut down. Therefore, to make converter compatible with on-off control method, resonant inductors are used as input inductors. Therefore, input high-frequency current ripple is increased but, faster dynamic response and lower voltage stress during system start-up and shutdown are gained. By using a transformer, galvanic isolation and arbitrary converter gain are achieved. Transformer’s leakage inductance is also absorbed in the resonant inductor ($L_r$).

![Figure 3-11: Modified isolated converter](image)

In this section, distinct stages of the circuit are explained for better understanding of the converter operation. Moreover, associated state-space equations are provided for each stage. Approximate components stress and power flow equation are provided in the next section. The same method is applied to analyze the circuit with infinite input inductors in [88]. To explain the operation of the converter using small input inductors, the following assumptions are made. Switching times are negligible. Parasitic capacitors and resistors of diodes and MOSFET are zero. Transformer turn ratio is unity. Magnetizing current of the transformer is zero.
3.3.1 CCM Operation

In class E converters, switching duty cycle can be varied to compensate the load or input voltage variations. However, many class E converters and amplifiers are operating with a constant duty cycle of 50% due to the higher efficiency, simple gate drive circuit and optimal operation of the circuit [7]. Modeling and analysis of the converter also easier when the duty cycle is 50%.

In this mode, the duty cycle of the switches is 50% and complementary. While \( SW_1 \) is on, \( SW_2 \) is off and vice versa. The operation of the converter can be divided into four distinct intervals. As the converter waveforms are half cycle symmetric, only interval 1 and 2 describe the operation of the converter.

**Interval 1 (\( t_0 - t_1 \)):** At the beginning of this interval, \( SW_2 \) turns on and \( SW_1 \) turns off. Proper resonance between \( C_2, L_r \) and \( L_r \) discharges \( C_2 \) at \( t_0 \), so \( SW_2 \) is turned on with minimum power loss.

At the same time, parallel capacitor \( C_1 \) limits \( dv/dt \) of \( SW_1 \) then this switch turns off under zero voltage switching condition. During this interval \( i_{L_r} \) is negative and \( D_1 \) and \( D_3 \) are conducting.

Therefore, the output current and voltage across \( L_r \) is positive. Consequently, \( i_{L_r} \) decreases slowly to zero at \( t_1 \). Limited \( di/dt \) of \( L_r \), makes the rectification of the system smooth and lossless. Figure 3-12 shows the main waveforms of the converter in CCM mode. The equivalent circuit in this interval is shown in Figure 3-13(a). State-space equations in this interval are given by (3.77) - (3.79).

Voltage across \( C_2 \) remains zero and \( L_{in2} \) is charged because \( SW_2 \) is on during this mode

\[
v_{SW1}(t) = \frac{(V_i \times L_R - V_o \times L_{in})}{L_R + L_{in}} (1 - \cos(\omega_2(t - t_0))) + I_1 Z_2 \sin(\omega_2(t - t_0)) \tag{3.77}
\]

\[
v_{SW2}(t) = 0
\]
\[ i_{\text{Lin1}}(t) = I_{\text{Lin1}-0} + \frac{(V_i+V_O)}{(L_R+L_{\text{in}})}(t-t_0) + \frac{I_1Z_2}{L_{\text{in1}}\omega_2}(1-\cos(\omega_2(t-t_0))) + \frac{(V_i)I_r}{(L_R+L_{\text{in1}})L_{\text{in1}}\omega_2} + \frac{(V_O)}{(L_R+L_{\text{in1}})\omega_2}\sin(\omega_2(t-t_0)) \]

\[ i_{\text{Lin2}}(t) = I_{\text{Lin2}-0} + \frac{(V_i)}{(L_{\text{in2}})}(t-t_0) \]

\[ i_{Lr}(t) = I_{Lr0} + \frac{(V_i-V_O)}{(L_R+L_{\text{in1}})}(t-t_0) + \frac{I_1Z_2}{L_{\text{R}}\omega_2}(1-\cos(\omega_2(t-t_0))) + \left(-\frac{(V_i)}{(L_R+L_{\text{in1}})\omega_2}\right) + \frac{(V_O)L_{\text{in1}}}{(L_R+L_{\text{in1}})L_{\text{R}}\omega_2}\sin(\omega_2(t-t_0)) \]

where:

\[ I_{\text{Lin1}-0} = L_{\text{in1}} \text{ initial current at } t_0 \]

\[ I_{\text{Lin2}-0} = L_{\text{in2}} \text{ initial current at } t_0 \]

\[ I_{Lr0} = L_{\text{R}} \text{ initial current at } t_0 \]

\[ I_1 = I_{\text{Lin1}-0} - I_{\text{Lr0}} \]

**Interval 2** \((t_1 - t_2)\): This interval starts when \(i_{Lr}\) reaches zero at \(t_1\). At this time, if \(v_{SW1}\) is greater than \(V_O\), \(D_2\) and \(D_4\) turn on and output voltage \((V_O)\) appears across the transformer. As shown in Figure 3-13(b), \(D_2\) and \(D_4\) are on and the polarity of output voltage source is reversed.

The equivalent circuit consists of \(C_1, L_{\text{in1}}, \text{ and } L_{\text{R}}\). Similar to the first interval, \(L_{\text{in2}}\) is charged and the voltage across \(C_2\) remains zero. At the end of this interval, the voltage across \(SW_1\) and \(C_1\) reaches zero. Therefore, the \(SW_1\) can be turned on under zero voltage switching condition. Equation (3.81) and (3.84) explain the state-space parameters in this interval. At the end of the second interval, a half cycle operation of the converter is finished. Intervals three and four are similar to interval one and two with 180-degree phase shift.
\[ v_{SW1}(t) = \frac{(V_i \times L_R - V_o \times L_{in})}{L_R + L_{in}} \left(1 - \cos(\omega_2(t - t_1))\right) + I_1 Z_2 \sin(\omega_2(t - t_1)) \]  

(3.81)

\[ v_{SW2}(t) = 0 \]

\[ i_{Lin1}(t) = i_{Lin1-1} + \frac{(V_i - V_o)}{(L_R + L_{in})} (t - t_1) + \frac{I_2 Z_2}{L_{in1} \omega_2} (1 - \cos(\omega_2(t - t_1))) \]

\[ + \frac{(V_i) L_T}{(L_R + L_{in1}) L_{in1} \omega_2} - \frac{(V_o)}{(L_R + L_{in1}) \omega_2} - \frac{v_{SW1}(t_1)}{L_{in1} \omega_2} \sin(\omega_2(t - t_0)) \]

\[ i_{Lin2}(t) = i_{Lin2-0} + \frac{(V_i)}{(L_{lin2})} (t - t_0) \]  

(3.82)

\[ i_{lr}(t) = i_{lr1} + \frac{(V_i - V_o)}{(L_R + L_{in1})} (t - t_1) + \frac{I_2 Z_2}{L_R \omega_2} (1 - \cos(\omega_2(t - t_1))) + \left( - \frac{(V_{in})}{(L_R + L_{in1}) \omega_2} \right) \]

\[ - \frac{(V_o) L_{in1}}{(L_R + L_{in1}) L_R \omega_2} - \frac{v_{SW1}(t_1)}{L_{in1} \omega_2} \sin(\omega_2(t - t_1)) \]

(3.83)

\[ i_{Lin2}(t) = i_{Lin2-0} + \frac{(V_i)}{(L_{lin2})} (t - t_0) \]  

(3.84)

\[ i_{lr}(t) = i_{lr1} + \frac{(V_i - V_o)}{(L_R + L_{in1})} (t - t_1) + \frac{I_2 Z_2}{L_R \omega_2} (1 - \cos(\omega_2(t - t_1))) + \left( - \frac{(V_{in})}{(L_R + L_{in1}) \omega_2} \right) \]

(3.85)

where:

\[ i_{Lin1-1} = i_{Lin1}(t_1) \]

\[ i_{Lin2-1} = i_{Lin2}(t_1) \]

\[ i_{lr1} = i_{lr}(t_1) \]

\[ I_2 = I_{Lin1-1} - I_{lr1} \]
Figure 3-12: Key waveforms of the isolated resonant converter in CCM mode.

(a) Stage 1
(b) Stage 2
(c) Stage 3
(d) Stage 4

Figure 3-13: The isolated resonant converter equivalent circuits in CCM mode
3.3.2 DCM Operation

To operate at a lower input voltage, the duty cycle of the switches should be increased symmetrically. By increasing the duty cycle, the discharge time of the $L_r$ is increased. Consequently, $i_{Lr}$ reaches zero and system starts working in DCM mode. Intervals of operation in DCM mode are similar to the operation of the single-ended converter in section 3. In fact, the operation of each half cycle is independent of the other half. However, the symmetric operation is required to achieve transformer volt-second balance.

3.3.3 Converter Power Flow

In this section, ZVS condition and 50% duty cycle are assumed for the converter. Ignoring rectifier’s intrinsic capacitors in CCM mode, $(v_{SW1} - v_{SW2})$ is approximately sinusoidal and the output voltage is a square waveform. In addition, rectifier voltage and current are in phase. Equation (3.86) estimate switches peak voltage as a function of input voltage. Equation (3.87) gives transformer current as a function of the input, output, and $L_r$ where $\omega$ is the switching frequency. Equation (3.89) defines the converter power flow. The volt-second balance of the input inductors is used to estimate the switches voltage.

\begin{equation}
V_{peak} \approx \pi V_{in}
\end{equation}

\begin{equation}
i_{Lr} = \frac{\pi V_{in}}{L_r \omega} \left( \cos \varphi_0 - \cos(\omega t) - \frac{V_o}{L_r} \left( t - \frac{\varphi_0}{\omega} \right) \right)
\end{equation}

\begin{equation}
\varphi_0 = \cos^{-1} \left( \frac{V_o}{2V_{in}} \right)
\end{equation}

\begin{equation}
P_{flow}(CCM) = \left( \frac{\pi V_{in} V_o \cos \varphi_0}{L_r \omega} + \frac{2V_{in} V_o \sin \varphi_0}{L_r \omega} + \frac{-V_o^2}{2L_r} \left( \frac{\pi + 2\varphi_0}{\omega} \right) + \frac{V_o^2 \varphi_0}{L_r \omega} \right)
\end{equation}
3.3.4 Component Design

From the above discussions, switching frequency and $L_r$ value have the most significant influence on the power flow. So, after choosing the switching frequency, the value of $L_r$ is to define the maximum power flow. The design of the input inductor and parallel capacitor is a trade-off between the parallel capacitor value and the input inductor value. In fact, for a larger input inductor, a smaller capacitor is required. Larger capacitor value means a higher circulating current and consequently higher conduction loss. The lower limit for the capacitor is defined by the intrinsic parasitic capacitor of the switches. For given values of the $C_1$ and $L_r$, input inductor selected based on switching frequency. The strategy of the design is similar to single ended converter.

3.3.5 Simulation Results

3.3.5.1 Operating in CCM Condition

This high-frequency converter can be implemented for a variety of voltage and current ratings. In this section, the converter is simulated for a nominal input voltage of 300V and output voltage of 400 V. According to the switch peak voltage in this converter, the breakdown voltage of $SW_1$ and $SW_2$ must be higher than 1000 volts. In addition, output rectifier must stand the output voltage. Figure 3-14(a) shows the drain-source voltage waveforms of $SW_1$ and $SW_2$. As demonstrated, the voltages of switches are half sinusoidal and symmetrical. As shown in Figure 3-14(b), $v_{SW_1}$ is zero when the switch is turned on, so small mismatch timing is acceptable. As shown in Figure 3-14(c), the rectifier voltage is clamped by the output voltage (400 V) without the unwanted oscillation between parasitic inductance and capacitance of the bridge.
3.3.5.2 Operating in DCM Condition

Figure 3-15(a)-(c) show the voltage waveforms of the converter under low input voltage condition. In this simulation, the input voltage is 100V and output is 400V. To keep the peak switch voltage under the nominal value, duty cycle should be limited by 85%. Similar to CCM operation, ZVS is achieved and rectifier turns on and off under low \( \frac{dv}{dt} \) and \( \frac{di}{dt} \). By turning the rectifier off in DCM mode, \( C_{rect} \) and \( L_r \) start to oscillate and a high frequency ringing voltage appears on the rectifier terminals.
Figure 3.15: Simulation results for 3 MHz isolated converter at 300V input voltage in DCM mode.
3.3.6 Experimental Results

The basic characteristics and component values are included in Table 3-2. As shown in Figure 3-16, 1000W converter operating at 3MHz was designed for 100-300V input and 400V output.

![Figure 3-16: The 3MHz prototype converter](image)

**Table 3-2: Component’s values in the isolated prototype converter**

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{in1,2}$</td>
<td>8µH, AWG# 14,15 turns M3 1090 core</td>
</tr>
<tr>
<td>$L_r$</td>
<td>6.5µH, AWG# 14,13 turn, M3 1090core</td>
</tr>
<tr>
<td>$C_{1,2}$</td>
<td>200 pF, Ceramic 1500 V</td>
</tr>
<tr>
<td>$SW_{1,2}$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$D_{1,2,3,4}$</td>
<td>C3D04060A</td>
</tr>
<tr>
<td>Transformer</td>
<td>3F4, E58/11/38</td>
</tr>
</tbody>
</table>

First switch ($SW_1$) Drain-Source and Gate-Source voltages are shown in Figure 3-17. The switch peak voltage is about 900V at nominal input voltage condition. As it can be seen, the drain-source voltage rises slowly after the switch turns off then falls to zero before switch turns on. According
to the low input capacitance of the SiC MOSFET, total gate power loss is less than 2 watts which is neglectable for a 1kW converter. A maximum efficiency of 93% was achieved at 200V input voltage. The efficiency of the isolated converter is reduced compared to the non-isolated one, according to the additional losses such as transformer core losses.

![Figure 3-17: Experimental results for 3MHz isolated converter at 300V input voltage.](image)

Red: $v_{GS(SW1)}(10V/Div)$, Blue: $v_{SW1}(200V/Div)$, Time: (100n/Div)

### 3.4 Conclusion

In this chapter, modified isolated and non-isolated quasi-resonant converters were proposed, and designed to fit MHz DC-DC applications requirements. A simple structure, a low number of components, ground reference switches, and low rectifier voltage stress are advantages of the converters. Simulation results from LTspice have been presented to verify the analysis. Experimental prototypes were built and tested to validate the design. An additional low current rating diode reduced the rectifier diodes voltage stress and unwanted oscillation in the in the non-isolated converter. Also, analysis and design based on resonant input inductor add more flexibility to the component selection. In addition, utilizing finite input inductance enhances the dynamic response of the system which makes the converter compatible with on-off control methods. The non-isolated converter can achieve more than 96% power efficiency at nominal operating condition while the isolated converter reaches an efficiency of more than 93%.
Chapter 4
A Novel First Cycle Control Method for Isolated and Non-Isolated Quasi-Resonant Converters

4.1 Introduction
In Chapter 3, an isolated and non-isolated quasi-resonant converter were analyzed and designed. Based on the resonant nature of these converters, it is difficult to maintain both ZVS and high-efficiency operation over a wide load range. The on-off control method is commonly used for DC-DC converters operating in the MHz frequency range in order to achieve proper performance across a wide range in voltage and load. This method eliminates many loss mechanisms such as switch gate power losses and circulating resonant currents when the converter is operating in a light-load condition. However, the superior performance of this method is limited due to the turn-on and turn-off transients of the converter within on-off control cycles. Because during this transients, the converter may not have zero voltage and/or zero current switching.

In this chapter, a ‘first cycle control method’ is proposed to reduce the effect of startup transient on the operation of the isolated and non-isolated quasi-resonant converters proposed in Chapter 3. By applying a predetermined gate signal in the first cycle of each power pulse, the proposed method minimizes voltage overshoot and transient power losses of the system at the beginning of each power pulse.

4.2 First cycle control method
On-off control methods such as pulse-density-modulation [76] and bang-bang control [82] overcome the limitations of conventional control techniques, such as duty cycle or frequency
control to hold the high efficiency at light loads while maintaining the benefits of resonant converters. Simplicity, stability, and high efficiency are the benefits of these methods.

With an on-off control strategy, high efficiency can be obtained across a wide load range by the simple fact that the converter is operating at nominal efficiency point or it is off [89], [90] and [91]. In a simple structure, the output voltage is kept between two thresholds. When the output voltage falls below the low predefined value, the converter is turned on and delivers nominal power to the load. The difference of the delivered and the consumed power increases the output voltage gradually. When the output rises above the high predefined value, the converter is turned off, and the output voltage will be decreased. Effectively, the output voltage is kept between predefined thresholds and, load power is controlled by changing the duty ratio in which the converter is modulated on and off. When the converter is enabled, it operates at a fixed high-efficiency point. When the converter is disabled, most of its loss mechanisms are removed. Hence, operation over a much wider load range can be achieved with this strategy. Figure 4-1 shows the block diagram and waveforms of this control method.
In ideal on-off control scheme, converter is working in nominal steady-state condition or remaining idle, so the efficiency of the converter is constant for any load. However, startup and shutdown transients affect the superior performance of the on-off control method. Figure 4-2(a) and (b) show start-up transients for two quasi-resonant converters with different component designs. Hard switching events or higher voltage stress are observed during the startup transient which influences the efficiency and switches utilization factor of the converter. In addition, when the controller disables the converter, voltage and current oscillation appear in the circuit. This ringing causes conduction power loss in the system. The effect of transient power loss on the total efficiency is described in (4.1) where $W_{\text{transient}}$ is the dissipated energy during each power pulse and $f_M$ is the modulation frequency. As given by (4.2), the output filter size ($C_{\text{filter}}$) is a function of modulation frequency. Therefore, lower modulation frequency results in a higher overall efficiency but larger
filter capacitors. Hence, to keep the efficiency high and the filters small, we need to minimize the transient power loss. In some converters, start-up transient can double the voltage stress of the converter’s switch [81]. The converter is subjected to this high voltage stress in every on-off pulse. Hence, start-up transient should be managed even if the modulation frequency is very low.

\[
\text{Efficiency} = \frac{P_{out}}{P_{out} + P_{loss} + f_M W_{transient}} \tag{4.1}
\]

\[
C_{filter} = \frac{1}{f_M V_{out} V_{ripple} \left( \frac{1}{P_{Nominal} - P_{out}} + \frac{1}{P_{out}} \right)} \tag{4.2}
\]

![Diagram of startup transient example 1](image1)

(a) Startup transient example 1

![Diagram of startup transient example 2](image2)

(b) Startup transient example 2.

**Figure 4-2: Startup transient of quasi-resonant converters.**

**4.3 First Cycle Control for Single Ended Quasi-Resonant Converter**

To control the transient behavior of the converter, the state-space parameters of the circuit are studied. Nonlinear and time-variant nature of the circuit makes the dynamic modeling of the circuit...
complicated. State space averaging is a popular method to model the dynamics of DC-DC converters. However, this method is useful when the dynamic of the system is slow with respect to the switching frequency [54]. In such case, only the envelope of the signal is modeled in this technique, and zero voltage switching operation cannot be carried out by using this method. The generalized averaging method is a more advanced technique for modeling non-LTI systems. In this method, a signal is approximated in one switching cycle by Fourier series [68]. The accuracy of the model is dependent on the number of utilized harmonics in the series. Increasing the number of harmonics to achieve a better accuracy makes the solution complicated. In fact, this method is very effective for converters such as series or LLC resonant converters where the signals are semi-sinusoidal and inverter section can be replaced by a voltage source [68]. Therefore, the rectifier is the only non-LTI part of the circuit to deal with. Another application of this method is found in switch mode amplifiers modeling where the main switch is modeled as a linear-time-variant component [69]. Although this method is useful for simple circuits, the complexity of the solution drastically increases by the complexity of the circuit. In a class E DC-DC or quasi-resonant converter, both nonlinear rectifier and time-varying switch are present. In this situation, the complexity of the circuit makes this method less effective. In this section, the converter operation is divided into several subintervals where the converter is acting like an LTI circuit.

4.3.1 Single-ended Converter Start-up Operation

To analyze the start-up behavior, the operation of the converter is divided into some specified intervals which the circuit behaves linearly. The final results of each interval can be considered as initial conditions for the next successive interval.

\[ i_{L_{in}} (L_{in} \text{ current}), v_{Q1} (Q1 \text{ drain-source voltage}), \text{ and } i_{L_{r}} (L_{r} \text{ current}) \]

are the state space parameters of the converter. Because the rectifier intrinsic diodes are significantly smaller compared to the resonant capacitor, dynamic of the rectifier is neglected. State-space variables are analyzed as a
function of the first switching period’s ON-time. A proper timing in the first cycle limits the switch’s peak voltage to nominal voltage and guarantees zero voltage switching condition for the next cycle. The operation of the system is described in 3 stages.

**Stage 1** ($t_0 - t_1$): this interval starts, when the controller commands to turn the converter on. At the beginning of this interval, input current ($i_{Lin}$) and resonant current ($i_{LR}$) are zero and the parallel capacitor ($C$) holds input voltage. The operation of the converter starts by turning $Q_1$ on at $t_0$. The first turn-on event dissipates the stored energy in parallel capacitor ($C$). As shown in Figure 4-3(a), the input inductor $L_{in}$ is charged by input source while $i_{LR}$ remains zero and both diodes stay off. The operation of the converter in the following stages are dependent on $i_{Lin}$, and hence, the controller keeps $Q_1$ on until $L_{in}$ gains enough current to guaranty the proper operation of the system. Equations (4.3)-(4.6) illustrate the operation of the system in this interval. Key waveforms of the converter are given in Figure 4-4.

\[
\begin{align*}
v_{Q1}(t) & = 0 \quad \text{(4.3)} \\
i_{Lin}(t) & = \frac{V_i}{L_{in}}(t - t_0) \quad \text{(4.4)} \\
i_{LR}(t) & = 0 \quad \text{(4.5)} \\
I_0 & = i_{Lin}(t_1) = \frac{V_i}{L_{in}}(t_1 - t_0) \quad \text{(4.6)}
\end{align*}
\]

**Stage 2** ($t_1 - t_2$): When $Q_1$ turns off at $t_1$, rectifier diodes are still off, resonant inductor carries no current, and the input inductor carries $I_0$. In this stage, the input inductor and the parallel capacitor resonate until $v_{C1}$ reaches the output voltage. Equations (4.7)-(4.11) give the state’s space variables and Figure 4-3(b) shows the equivalent circuit of the converter.

\[
v_{Q1}(t) = V_i(1 - \cos(\omega_1(t - t_1))) + I_0Z_1 \sin(\omega_1(t - t_1)) \quad \text{(4.7)}
\]
\[ i_{\text{Lin}}(t) = \frac{V_i}{Z_1} \sin(\omega_1(t - t_1)) + I_0 \cos(\omega_1(t - t_1)) \]  

(4.8)

\[ i_{L_r} = 0 \]  

(4.9)

\[ (t_2 - t_1) = \frac{1}{\omega_1} \left( \sin^{-1} \left( \frac{N_1}{M_1} \right) + \varphi_1 \right) \]  

(4.10)

\[ I_1 = i_{\text{Lin}}(t_2) \]  

(4.11)

where:

\[ Z_1 = \sqrt{\frac{L\text{in}}{C_1}}, \quad \omega_1 = 1\sqrt{\frac{L\text{in}}{C_1}}, \quad N_1 = V_o - V_i, \quad M_1 = \sqrt{V_i^2 + (I_0Z_1)^2}, \quad \varphi_1 = \tan^{-1} \left( \frac{V_i}{I_0Z_1} \right) \]

**Stage 3** \((t_2 - t_3)\): Stage 3 starts when the voltage across \(Q_1\) reaches the converter output voltage \(V_O\). At this moment, \(D_2\) turns on and connects \(L_r\) to the output. As shown in Figure 4-3(c), the resonant inductor \(L_r\) and output voltage source \((V_O)\) are added to the resonant circuit. During this interval, inductors \(L\text{in}, L_r\), and \(C\) resonate until the capacitor voltage reaches its peak and then falls to zero or the controller turns \(Q_1\) on at \(t_3\). In a proper timing scheme, the capacitor voltage is zero when the switch is turned on. Consequently, \(Q_2\) turns on under zero voltage condition at the beginning of the second cycle. The peak voltage across the switch and the required time to turn the switch on under ZVS condition are given by (4.12)-(4.18).

\[ v_{Q_1}(t) = V_o + \frac{(V_i-V_o)LR}{L_r+L_{\text{in}}}(1 - \cos(\omega_2(t - t_2))) + I_1Z_2 \sin(\omega_2(t - t_2)) \]  

(4.12)

\[ i_{\text{Lin}}(t) = I_1 + \frac{(V_i-V_o)}{(L_r+L_{\text{in}})}(t - t_2) + \frac{I_1Z_2}{L_{\text{in}}} \left( 1 - \cos(\omega_2(t - t_2)) \right) + \]  

\[ \frac{(V_i-V_o)L_r}{(L_r+L_{\text{in}})L_{\text{in}}\omega_2} \sin(\omega(t - t_2)) \]  

(4.13)

\[ i_{L_r}(t) = \frac{(V_i-V_o)}{(L_r+L_{\text{in}})}(t - t_2) + \frac{I_1Z_2}{L_{\text{in}}\omega_2} \left( 1 - \cos(\omega_2(t - t_2)) \right) - \frac{(V_i-V_o)L_R}{(L_r+L_{\text{in}})L_R\omega_2} \sin(\omega(t - t_2)) \]  

(4.14)
\begin{align}
V_{peak} &= \frac{V_o L_{in} + L_R V_i}{L_R + L_{in}} + \sqrt{I_1 Z_2^2 + \left(\frac{V_i - V_o}{L_R + L_{in}}\right)^2} \\
&= \frac{V_o L_{in} + L_R V_i}{L_R + L_{in}} + \sqrt{I_1 Z_2^2 + \left(\frac{V_i - V_o}{L_R + L_{in}}\right)^2}
\end{align}

(4.15)

\begin{align}
t_3 &= t_2 + \frac{1}{\omega_1} \left(\sin^{-1}\left(\frac{N_1}{M_1}\right) + \varphi_1\right)
\end{align}

(4.16)

\begin{align}
T_{on} &= t_1 - t_0, T_{off} = t_3 - t_1
\end{align}

(4.17)

where:

\begin{equation}
Z_2 = \frac{L_{eq}}{C}, \omega_2 = \frac{1}{\sqrt{L_{eq}C}}, L_{eq} = \frac{L_{R_{in}}}{L_R + L_{in}}
\end{equation}

(a) Stage 1

(b) Stage 2.

(b) Stage 3.

Figure 4-3: Startup intervals

Figure 4-4: Startup intervals key waveforms.
The switch’s peak voltage and required time to discharge the capacitor ($T_{off}$) are plotted in Figure 4-5 and 4-6 as functions of the first cycle $T_{on}$, respectively. By using (4.3)-(4.18), proper $T_{on}$ and $T_{off}$ are calculated to start the converter with a restricted voltage stress and zero voltage switching in the next cycle. As mentioned before, rectifier output capacitors are ignored to simplify the equations. However, calculated peak voltage and $T_{off}$ values accuracy are dependent on these capacitors. Figure 4-7 plots the calculated peak voltage error related to the rectifier intrinsic capacitance. As it can be seen, peak voltage error is less than 5% in the proposed converter. $T_{off}$ error according to the rectifier intrinsic capacitance is less than 2.5 nsec when the rectifier capacitor is less than 50 pF. This time is less than 1% of the switching period. While the rectifier capacitance is smaller than 50 pF, less than 2.5 nsec error is observed in the calculation of $T_{off}$.

**Figure 4-5:** $Q_1$ peak voltage as a function of $T_{on}$.

**Figure 4-6:** Required $T_{off}$ to achieve ZVS as a function of $T_{on}$. 
4.3.2 Controller

By choosing a proper value for the first switching cycle in each pulse, the peak voltage and switching losses in the first cycle are reduced. To implement the technique, a pre-calculated first cycle ON-time and OFF-time are stored in a memory as a function of input and output voltages and applied at the beginning of each power pulse. Then, the steady-state gate signal is applied to the MOSFET after the first cycle. The controller applies predetermined waveform based on the detected input voltage. However, a constant waveform can be applied for a range of input voltage without imposing significant voltage stress to the switch. To reduce the look-up table size and analog to digital conversion rate, the input voltage range is divided into a number of distinct sections. The value of $T_{on}$ for each section is kept constant. So, the switch peak voltage is slightly different in each section. In addition, for the boundary values of each section, the $T_{on}$ value of the following section might be applied due to the input voltage noise or digital to analog quantization. The size of the look-up table is defined by the maximum acceptable voltage stress and behavior of the converter at boundary values. In the designed system, the input range voltage is divided into 10 equal sections. The maximum peak voltage difference for the boundary values is less than 60V.
which occurs at 280V input voltage. In the hysteresis control mode, the converter immediately responds to a step load change and output voltage remains in the hysteresis gap. The converter behavior during input voltage transient depends on on-off frequency and input voltage sampling rate. The controller reacts to any input voltage change by altering the gate driver signal pattern to the predetermined values. When input voltage is sampled in every on-off cycle, it takes less than one on-off cycle to set the proper gate driver signal pattern.

This technique can be implemented with digital controller ICs such as FPGA or DSP. In addition, for a limited input voltage range, the controller can be implemented with a couple of logic gate circuits.

After the first cycle, the converter is driven by a constant duty cycle and frequency signal. The behavior of the converter in the rest of the pulse depends on the operation in the first cycle. As long as the switching gate signal is fixed, a switching power supply is a stable nonlinear system [92]. Therefore, the converter enters the steady state operation after a finite number of cycles. But initial state-space values at the beginning of the second cycle determines the severity of the transient response. The closer the initial values to the steady-state ones, the better the transient response. By choosing the right timing in the first cycle, the transient waveform voltage is close to the steady-state waveform. Then, not only ZVS operation is achieved, but also transient response of the converter is minimized.

This improved controller can be implemented for hysteresis, constant modulation frequency or any other on-off control method. The first \( T_{\text{ON}} \) is highly dependent on the value of \( L_{\text{in}} \). As a rule of thumb, the larger the \( L_{\text{in}} \), the higher the \( T_{\text{on}} \) of the first cycle. During the first on-time, the power delivery to output is zero. Then, the output voltage is being decreased even after the on command is applied to the converter. In addition, when the controller turns the converter off, output power delivery continues until the input inductor is discharged. So actual high and low threshold values
\((V_{THA} \text{ and } V_{TLA})\) are slightly different from the set points \((V_{TH} \text{ and } V_{TL})\). Approximate values of \(V_{THA}\) and \(V_{TLA}\) are given in (4.19) and (4.20).

\[
V_{THA} = V_{TH}(set) + \frac{L_{in}}{2C_{out}(V_{O} - V_{I})} \left( \frac{P_{\text{max}}}{V_{I}} - \frac{P_{O}}{V_{O}} \right) \tag{4.19}
\]

\[
V_{TLA} = V_{TL}(set) - \frac{P_{\text{out}}r_{on}}{V_{OL_{out}}} \tag{4.20}
\]

Figure 4-8 shows the block diagram of the implemented control circuit. The output voltage, input current, and gate command waveforms are illustrated in Figure 4-9.

\[\text{Figure 4-8: Output voltage regulation block diagram.}\]
4.3.2 Simulation

To verify the operation of the improved method, simulation results are provided in this section. PSIM simulated 1kW prototype is shown in Figure 4-10. Table 4-1 gives the simulated circuit components. Figure 4-11 illustrates the behavior of the converter when the conventional on-off control method is used. The main switch voltage ($v_{SW}$) and the sampled turn-on voltage ($v_{C0}$) are shown in Figure 4-11-a. As we can see, the switch turns on under non-ZVS condition in the first five cycles which causes in power dissipation. The start-up power loss becomes more important when the total number of cycles is small in this each power pulse. In addition, it takes about five cycles for the input current to reach the steady-state waveform. To improve the converter efficiency, the first cycle timing of the switch is applied to achieve ZVS in the second cycle by using (4.15)-(4.17). As shown in Figure 4-12, the converter enters the steady-state condition in the

![Figure 4-9: Converter key waveform in on-off control mode.](image-url)
second cycle. Therefore, the hard switching loss of the converter is limited to the first cycle and switch voltage stress is bound to the steady state value.

Figure 4-10: Simulated prototype circuit.

Table 4-1: Component’s values in the simulated non-isolated converter

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{in}$</td>
<td>27µH</td>
</tr>
<tr>
<td>$L_r$</td>
<td>6.5µH</td>
</tr>
<tr>
<td>$C$</td>
<td>270 pF</td>
</tr>
<tr>
<td>$C_{rect}$</td>
<td>20pF</td>
</tr>
</tbody>
</table>
(a) Switch voltage waveform and sampled switching voltage in each cycle.

(b) Input current during startup

(c) Rectifier voltage during startup

Figure 4-11: Behavior of the converter when the conventional on-off control method is used.
(a) Switch voltage waveform and sampled switching voltage in each cycle

(c): Input current during startup

(d) : Rectifier voltage during startup

Figure 4-12: Behavior of the converter when the improved on-off control method is used.
4.3.3 Experimental results

The improved method is applied to the non-isolated quasi-resonant converter designed in Chapter 3. The basic characteristics and component values are similar to the simulated converter in the previous section. The 1kW prototype and controller circuits are shown in Figure 4-13. TMS320F28335 Experimenter Kit is utilized for generating gate signals. As mentioned before, one benefit of the converter is the ground reference switch. Hence, no isolation is required between the controller board and the converter. However, an isolation board is used to protect the TMS320F28335 board during tests. Table 4-2 gives the components value in the prototype circuit.

![Prototype Converter Image](image-url)

**Figure 4-13: The 3MHz prototype converter**
Table 4-2: Component’s values in the non-isolated prototype circuit

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{in}$</td>
<td>26.5(\mu)H, AWG# 14,25 turns M3 1090 core</td>
</tr>
<tr>
<td>$L_r$</td>
<td>6.5(\mu)H, AWG# 14,13 turn, M3 1090 core</td>
</tr>
<tr>
<td>$C$</td>
<td>200 pF, Ceramic 1500 V</td>
</tr>
<tr>
<td>$Q_1$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$D_1$</td>
<td>C3D04060A</td>
</tr>
<tr>
<td>$D_2$</td>
<td>CSD01060A</td>
</tr>
</tbody>
</table>

Figure 4-14 shows the converter key waveforms in conventional on-off control method. Hard switching operation in the first three cycles of a power pulse is observed in Figure 4-13. Drain-source voltage of the switch is nonzero when the switch is turned on. This hard switching operation not only boosts the power losses but also increases EMI in the circuit. As we can see, it takes about three cycles for the converter to reach the steady-state operation.

![Hard Switching Waveforms](image)

**Figure 4-14:** Experimental results for 3MHz non-isolated converter using conventional on-off.
To solve the converter hard switching operation in the few first cycles and to enter the steady-state operation in the second cycle, first cycle control is implemented in the system. As we can see in Figure 4-14, the converter enters the steady-state operation in the second cycle. In fact, the controller keeps the switch on, until the input inductor gains enough current to resonant properly and then, keeps the switch off until the resonant capacitor is fully discharged. In the following cycles, the steady-state gate signal is applied to the switch. The converter operation continues until the output voltage reaches the upper threshold voltage and the controller turns the converter off to regulate the output. Figure 4-15 shows a full on-off operation interval.

![Graph](image)

**Figure 4-15: Experimental results for 3MHz non-isolated converter using first cycle control.**

When controller disables the converter, the oscillation continues until the stored energy in the input inductor is transferred to the output. Then, a high-frequency ringing dissipates the stored energy in
the rectifier parasitic capacitance. Using a semiconductor component with lower parasitic capacitance is helpful to reduce this power loss.

Figure 4-16: Experimental results for 3MHz non-isolated converter (full on-off operation).

A maximum efficiency of 96% is achieved at 260-volt input voltage and 923W output power. Figure 4-17 compares the efficiency of the converter using the first cycle control and conventional on-off methods. About 2% efficiency improvement is obtained by using the proposed control method. The modulation frequency varies between 25kHz to 250kHz for the load range of 5% to full load. To increase the comparison accuracy, efficiency is measured at the same modulation frequency and duty cycle for both methods. Efficiency drops about 2% for light load conditions according to the startup and shutdown power losses. Lower power loss in the improved method startup is more significant at lighter loads. In addition, decreased number of hard switching in each power pulse reduces EMI energy of the converter and makes the filter design easier.
4.4 First Cycle Control for Double-Ended Quasi Resonant Converter

In the previous section, the first cycle control was applied to the single-ended quasi-resonant converter. This method was able to minimize the switching loss in the first few cycles in each power pulse. Similar to the single-ended circuit, start-up behavior of double-ended converter should be studied to prevent any stress or power losses.

Figure 4-18 shows the start-up behavior of a double-ended quasi-resonant converter in conventional on-off control method. Switches peak voltage in the first switching cycles is up to 25% higher compared to the steady state peak voltages. To stand this voltage stress in every power pulse, a switch with a higher breakdown voltage is required. Therefore, switch utilization factor of the converter will be decreased. To reduce this voltage stress, the analysis in the previous section is used to study the transient behavior of the double-ended converter designed in Chapter 3.
4.4.1 Double-ended Converter Start-up Operation

Similar to the single-ended converter, to reduce the transient voltage stress and switching losses the state-space parameters of the converter are analyzed and proper switching scheme is selected. The intrinsic parallel capacitances of rectifier diodes are small; thus, the rectifier intrinsic capacitors are ignored to avoid complex equations. $C_{1,2}, L_{in1,2},$ and $L_r$ are reactive components of the circuit. $v_{SW_{1,2}}, i_{Lin_{1,2}},$ and $i_{LR}$ defined as the voltage and current of those components respectively, are the state-space variables of the converter. System operation is described in 6 stages. To address the switches, $SW_1$ and $SW_2$ are referred as the leading and the lagging switches respectively. As shown in Figure 4-19, the leading switch operation is described in stages 1-3 and operation of the lagging one is demonstrated in stages 4-6. It is assumed that at least one switch is on at any instant. To study the transient behavior of the converter, the following assumptions are made: (1) all components are Ideal; (2) inductors’ initial currents are zero; (3) input and output voltages are constant. Figure 4-20 shows the equivalent circuit in each stage.

Stage 1 ($t_0 - t_1$): Operation of the converter starts by turning $SW_1$ ON. During this stage, all diodes and $SW_2$ are OFF. Figure 4-20(a) shows the converter equivalent circuit in this interval. As
the voltage across $L_{in1}$ is constant, this inductor is charged linearly while other state-space variables remain zero in this period. The voltage and current waveforms of the converter in the following stages are dependent on $i_{Lin1}$ at $t_1$, and hence, the controller keeps $SW_1$ on until $L_{in1}$ gains enough current to guarantee the proper operation of the system. Equations (4.21)-(4.26) describe states-space variables in this stage.

$$v_{SW1} = 0$$  \hspace{1cm} (4.21)  
$$v_{SW2} = V_{in}$$  \hspace{1cm} (4.22)  
$$i_{Lin1} = \frac{V_i}{L_{in1}}(t - t_0)$$  \hspace{1cm} (4.23)  
$$i_{Lin2} = 0$$  \hspace{1cm} (4.24)  
$$i_{Lr} = 0$$  \hspace{1cm} (4.25)  
$$I_{0,1} = I_{Lin1}(t_1) = \frac{V_i}{L_{in}}(t_1 - t_0)$$  \hspace{1cm} (4.26)  

**Stage 2** ($t_1$-$t_2$): At $t_1$, since the input current $I_{Lin1}$ reaches $I_{0,1}$, controller turns $SW_1$ off. At this point, $SW_2$ and rectifier diodes are still off, and no current flows through the resonant inductor $L_r$, and $L_{in1}$ carries $I_{0,1}$ entirely. During this stage, $L_{in1}$ and the parallel capacitor $C_1$ form a resonance circuit until the capacitor voltage reaches the equivalent output voltage in the primary side. As the ratio of the transformer is 1:1, the equivalent output voltage is $V_O$. Figure 4-20(b) shows the equivalent circuit diagram of the converter during stage 2. The converter equations in this stage are given as follows:

$$v_{sw1}(t) = V_i\left(1 - \cos(\omega_1(t - t_1))\right) + I_{0,1}Z_1\sin(\omega_1(t - t_1))$$  \hspace{1cm} (4.27)  
$$v_{sw2} = V_{in}$$  \hspace{1cm} (4.28)  
$$i_{Lin1}(t) = \frac{V_i}{Z_1}\sin(\omega_1(t - t_1)) + I_{0,1}\cos(\omega_1(t - t_1))$$  \hspace{1cm} (4.29)  

95
\[ i_{\text{Lin}2} = 0 \]  
\[ i_{Lr} = 0 \]  
\[ (t_2 - t_1) = \frac{1}{\omega_1} (\sin^{-1}(\frac{N_1}{M_1}) + \varphi_1) \]  
\[ I_{1,1} = i_{\text{Lin}1}(t_2) \]  

where:

\[ Z_1 = \sqrt{\frac{L_{\text{in}1}}{C_1}}, \quad \omega_1 = \frac{1}{\sqrt{L_{\text{in}1} C_1}} \]
\[ N_1 = V_0 - V_i, \quad M_1 = \sqrt{V_i^2 + (l_{0,1} Z_1)^2} \]
\[ \varphi_1 = \tan^{-1}\left(\frac{V_i}{l_{0,1} Z_1}\right) \]

**Stage 3 (t_2 - t_3):** Stage 3 starts when the voltage across SW_1 reaches the converter output voltage, \( V_O \). In a proper switching scheme, at \( t_2 \), SW_2 is on. When \( v_{SW_1} \) reaches the output voltage, \( D_2 \) and \( D_4 \) turn on. Therefore, as shown in Figure 4-20(c), the resonant inductor \( L_r \) and output voltage source (\( V_O \)) are involved in the resonant circuit. During this interval, inductors \( L_{\text{in}1}, L_r \) and the parallel capacitor \( C_1 \) resonate until the capacitor voltage reaches its peak and then falls to zero at \( t_3 \). Consequently, SW_1 turns on under zero voltage condition. The peak voltage across the switch and the required time to turn the switch on with ZVS are given by (4.34) - (4.38).

\[ v_{sw_1}(t) = V_0 + \frac{(V_i-V_o) L_r}{L_r + L_{\text{in}}} (1 - \cos(\omega_2 (t - t_2))) + I_{1,1} Z_2 \sin(\omega_2 (t - t_2)) \]  
\[ i_{\text{Lin}1}(t) = I_{1,1} + \frac{(V_i-V_o)}{(L_r + L_{\text{in}})} (t - t_2) + \frac{I_{1,1} Z_2}{L_{\text{in}1} \omega_2} (1 - \cos(\omega_2 (t - t_2))) \]  
\[ + \frac{(V_i-V_o) L_r}{(L_r + L_{\text{in}}) L_{\text{in}1} \omega_2} \sin(\omega (t - t_2)) \]
\[ i_{lr}(t) = \frac{(V_i-V_o)}{(L_r+L_{in})} (t - t_2) + \frac{l_1 Z_2}{L_r \omega_2} (1 - \cos(\omega_2 (t - t_2))) - \frac{(V_i-V_o)L_r}{(L_r+L_{in})L_r \omega_2} \sin(\omega (t - t_2)) \quad (4.36) \]

\[ V_{peak} = \frac{V_o L_{in} + L_r V_i}{L_r + L_{in}} + \sqrt{L_1 Z_2^2 + \left(\frac{(V_i-V_o)L_r}{L_r + L_{in1}}\right)^2} \quad (4.37) \]

\[ t_3 = t_2 + \frac{1}{\omega_1} \left(\sin^{-1}\left(\frac{N_1}{M_1}\right) + \varphi_1\right) \quad (4.38) \]

\[ Z_2 = \sqrt{\frac{L_{eq}}{C}}, \omega_2 = \frac{1}{\sqrt{L_{eq} C}}, L_{eq} = \frac{L_r L_{in}}{(L_r + L_{in})} \]

The first switching cycle of the leading switch ends at \( t_3 \). Following stages describe the first switching cycle of the lagging switch, \( SW_2 \). As shown in Figure 4-19, leading and lagging stages are simultaneous.

**Stage 4** \((t_4 - t_5)\): At \( t_4 \), \( SW_2 \) turns ON. During this stage, the voltage across \( SW_2 \) is equal to zero and the input inductor \( L_{in2} \) is being charged. Because voltage and current waveforms of the next stage are dependent on initial input current, the controller keeps \( SW_2 \) on until \( L_{in2} \) gains enough current to guarantee proper operation of the system. Figure 4-20(d) demonstrates the equivalent circuit of the converter in this stage. The converter equations in this stage are given as follows:

\[ v_{SW2} = 0 \quad (4.39) \]

\[ i_{Lin2} = \frac{V_i}{L_{in2}} (t - t_4) \quad (4.40) \]

\[ I_{0,2} = I_{Lin2}(t_5) + I_{lr}(t_5) = \frac{V_i}{L_{in}} (t_5 - t_4) \quad (4.41) \]

**Stage 5** \((t_5 - t_6)\): At \( t_5 \), \( I_{Lin2} \) reaches \( I_{0,2} \) and the controller turns \( SW_2 \) off. \( C_2 \) limits \( dv/dt \) of the switch and minimizes the switching loss. As shown in Figure 4-20(e), \( L_r \) and the output voltage
source are a part of the equivalent circuit. $L_{in2}$, $L_r$ and $C_2$ resonate until the resonant inductor current ($I_{Lr}$) reaches zero at $t_6$. At this point, $D_2/D_4$ pair turns off and $D_1/D_3$ pair turns on. Because $L_r$ is in series with the rectifier circuit, di/dt of these diodes are limited and the diodes turn-off losses are minimized. Equation (4. 42)-(4. 46) describe the involved state space variables in this stage.

$$v_{sw}(t) = \frac{V_i L_r - V_o L_{lin2}}{L_r + L_{in2}} \left( 1 - \cos(\omega (t - t_5)) \right) + i_{0,2} Z_2 \sin(\omega (t - t_5))$$  \hspace{1cm} (4. 42)

$$i_{Lin}(t) = I_{Lin2}(t_5) + \frac{(V_i + V_o)}{(L_r + L_{in})} t - \frac{i_{Lin2}(t_5) Z_2}{L_{in} \omega_2} \left( 1 - \cos(\omega (t - t_5)) \right) + \frac{V_i L_r - V_o L_{Lin2}}{(L_r + L_{in}) L_r \omega_2} \sin(\omega (t - t_5))$$  \hspace{1cm} (4. 43)

$$i_{Lr}(t) = I_{Lr}(t_5) - \frac{(V_i + V_o)}{(L_r + L_{in})} t - \frac{i_{Lr}(t_5) Z_2}{L_r \omega_2} \left( 1 - \cos(\omega (t - t_5)) \right) + \frac{V_i L_r - V_o L_{Lin2}}{(L_r + L_{in}) L_r \omega_2} \sin(\omega (t - t_5))$$  \hspace{1cm} (4. 44)

$$I_{1,2} = i_{Lin}(t_6)$$  \hspace{1cm} (4. 45)

$$V_{c0} = v_{sw}(t_6)$$  \hspace{1cm} (4. 46)

**Stage 6** ($t_6$-$t_7$): this period starts after the $i_{Lr}$ reaches zero at $t_6$. At this moment, if the voltage across $C_2$ is higher than the equivalent output voltage, $D_1$ and $D_3$ turns on. As shown in Figure 4-20(f), the operation of the converter in this interval is similar to stage 5, but the polarity of the output voltage is reversed. During this stage, $L_{in2}$, $L_r$ and $C_2$ resonate until capacitor voltage reaches zero or controller turns $SW_2$ on at $t_7$. The equations of the converter in this stage are given by (4. 47)-(4. 50). This stage is the last stage of the first cycle.
\[ v_{sw2}(t) = \frac{-V_c0(L_{in2} + L_r) + V_Lr + V_o L_{Lin}^2}{L_r + L_{in2}} \times (1 - \cos(\omega_2(t - t_5))) + V_c0 + I_{12}Z_2 \sin(\omega_2(t - t_5)) \] (4.47)

\[ i_{Lin2}(t) = I_{Lin2}(t_6) + \frac{(V + V_o)}{(L_r + L_{in})} t - \frac{I_{12}Z_2}{L_{in}\omega_2} (1 - \cos(\omega_2(t - t_5))) + \] \(\frac{-V_c0(L_{in2} + L_r) + V_Lr + V_o L_{Lin}^2}{(L_r + L_{in})L_r\omega_2} \sin(\omega(t - t_6))\) (4.48)

\[ i_{Lr}(t) = I_{Lr}(t_6) - \frac{(V + V_o)}{(L_r + L_{in})} t - \frac{I_{12}Z_2}{L_r\omega_2} (1 - \cos(\omega_2(t - t_5))) + \] \(\frac{-V_c0(L_{in2} + L_r) + V_Lr + V_o L_{Lin}^2}{(L_r + L_{in})L_r\omega_2} \sin(\omega(t - t_6))\) (4.49)

\[ V_{peak} = \frac{V_o L_{in} + L_r V_i}{L_r + L_{in}} + \sqrt{I_{12}Z_2^2 + \left(\frac{V_Lr + V_o L_{Lin}}{L_r + L_{in}} - V_c0\right)^2} \] (4.50)

By selecting a proper timing strategy, the transient peak voltage is limited to steady-state values and zero voltage switching in the second cycle can be achieved. Arbitrary and asymmetrical timing strategy requires a fast and complicated control circuit which is in contrast to the simplicity of on-off control strategy. The same strategy is used to calculate the first ON-time for \(SW_1\). Because the modes of operation for the first switch, \(SW_1\) is similar to the single-ended converter. For the second switch, modes of operation are similar to the steady state operation with different initial values.

Proper timing for this switch is calculated and stored for any input voltage. The calculated \(T_{on1}\) and \(T_{on2}\) in order to restrict the switches’ peak voltage and, to achieve soft turn-on in the next cycle are applied to the converter at the beginning of each power pulse. Then overvoltage and hard switching losses are then minimized.
Figure 4-19: Double-ended converter startup key waveforms.
Figure 4-20: Double ended converter equivalent circuits in startup transient.
4.4.2 Simulation

This section presents PSIM simulation results of the 1kW isolated converter in Chapter 3 as shown in Figure 4-21. The converter was simulated for 1kW peak output power, nominal input and output voltages of 300/400 V.

Figure 4-21: The simulated converter schematic

Figure 4-22 illustrates the behavior of the converter when the conventional on-off method is used. In the first few cycles, switches peak voltage are about 20% higher than steady-state peak voltage. As this voltage stress occurs in every power pulse, a switch with a higher breakdown voltage is required. To improve the converter performance, the first cycle timing of the switch is calculated based on the analysis in section 4.4.1. As shown in Figure 4-23, voltage stress is bounded to steady state voltage and the hard switching losses of the converter are limited to the first cycle.
Figure 4-22: Simulation results for 3MHz on-off conventional.
Figure 4-23: Simulation results for 3MHz double-ended converter using first cycle control.
4.4.3 Experimental results

This section evaluates the performance of the converter described in the previous sections. Figure 4-24 shows a picture of the 1000W converter operating at 3MHz. TMS320F28335 Experimenter Kit is utilized for generating gate signals. As mentioned before, one benefit of the converter is the ground referenced switches. Hence no isolation is required between the controller board and the converter. However, an isolation board is used to protect the TMS320F28335 board during tests.

![Diagram of converter components](image)

**Figure 4-24: Double-ended 3MHz prototype.**

Figure 4-25 shows the converter key waveforms in conventional on-off control method. As predicted in the simulations, the peak voltage is higher in the first cycles of a power pulse. To control the voltage overshoot, the predefined timing of the first cycle is stored in the DSP and applied at the beginning of each power pulse. From the second cycle and after, steady state gate command is sent to the converter until the output voltage reaches the higher threshold voltage. Shown in Figure 4-26, the method is been effective to control the peak voltage of both switches in the beginning of each power pulse.
4.5 Conclusion

In this chapter, first cycle control was proposed to improve the performance of on-off control methods. Theoretically, on-off control methods offer simplicity and stability of the control structure.
while maintains the nominal efficiency at any load. However, startup and shutdown behavior of the converter affects the overall performance of the controller. Therefore, first cycle control was proposed to enhance the performance of the converter. This method improves the transient behavior of the converter and reduces the voltage stress and power loss during each power pulse. To validate the analysis and simulations, this technique was applied to the isolated and non-isolated quasi-resonant converters. The number of hard switching cycles was reduced by 60% in the non-isolated converter and voltage stress was reduced by 20% in the isolated converter. According to the simple controller and switching structure, this method can be implemented by simple digital circuits.
Chapter 5

A New ZVT Auxiliary Cell for a High-Frequency Quasi-Resonant Converter in on-off Control Modes

5.1 Introduction

In Chapter 4, a first cycle control technique was proposed to improve the start-up transient of quasi-resonant converters. This method effectively eliminates most transient power losses and reduces the switch’s voltage stress. However, this technique cannot eliminate the switching loss in the first cycle of each power pulse. The stored energy in the resonant capacitor is dissipated in the switch at the beginning of each power pulse, which degrades the efficiency at high modulation frequencies. In this chapter, a fully zero voltage transient (ZVT) auxiliary cell is proposed to minimize the startup and shutdown losses in the on-off control method. This cell guarantees zero voltage switching for all active components without imposing significant conduction losses. The modulation frequency, therefore, can be increased with no negative impact on the overall efficiency and the performance of the circuit. A fully ZVS operation, simple structure, the privation of inductive components, and low voltage and current stresses are the main advantages of this circuit. To verify the mathematical analysis, simulations and experimental results are provided.

5.2 Why ZVT Cell

In bang-bang control mode, the circuit turns on and off at a rate much lower than the main switching frequency. The power flow and the output voltage are regulated by changing the ratio of on-time to off-time. Optimum operation during on-time and minimum losses during off-time lead to a higher efficiency at light-load conditions. In this method, the switching frequency determines the size of resonant components while the modulation frequency decides input/output filter size and
converter response time. So, to reduce input and output filter sizes, a higher modulation frequency is required.

Despite the ideal operation in active and idle modes, on-off and off-on transients are troublesome. More frequently turning the converter on and off, more startup and shutdown transients and thus more power dissipation occur in the system. To improve the transient behavior of the converter, the first cycle timing control was proposed in Chapter 4. This technique is able to reduce the components stress and power losses at the beginning of each pulse. However, the first switching cycle of each power pulse is not lossless. One solution to achieve zero voltage switching in the first cycle is using Zero Voltage Transient (ZVT) circuits. Many ZVT auxiliary circuits have been proposed to achieve zero voltage switching in conventional hard switching converters such as buck and boost [94] and [95]. The turn-off power loss of the main switch is minimized by a parallel snubber capacitor. And then, this capacitor is discharged by the auxiliary cell just before the main switch is turned on to minimize turn-on losses. Therefore, the zero voltage switching operation is provided for the main circuit. The auxiliary cell only operates in a short period of time. Then the current rating of the auxiliary switch is lower and its size is smaller compared to the main circuit.

Figure 5-1 (a) shows a boost converter with an auxiliary circuit [93]. The main switch (S_{main}) turns on and off under ZVS condition while the auxiliary switch (S_{aux}) turns on under Zero Current Switching (ZCS) condition and turns off under ZVS condition. Figure 5-1(b) shows key waveforms of this circuit. Using ZVT circuits has some drawbacks as well. First, additional components make the system more complex. Second, additional conduction loss is the price of achieving ZVS in the circuit. In [96] and [97], the auxiliary switch turns off under hard switching condition. In [98], stored energy in the auxiliary circuit is not retrieved. Both of the main and the auxiliary switches turn on and off without switching loss in [99] - [109], but for example in [99] an extra switch in the power path causes additional conduction loss. In [100] - [102], the main switch tolerates significant current peak (up to 2 times the nominal current). The current stress on the auxiliary switch is a
noticeable problem in [103] that results in conduction loss in the converter. In [104], although the current stress is acceptable, using 3rd switch makes the structure complicated and difficult to implement. The operation of the circuit proposed in [105] is limited in DCM mode. Floating switch in the auxiliary circuit complicates the gate drive circuit in [106]. Proposed topology in [107] transfers the auxiliary circuit energy to the input, so efficiency decreases slightly. Although voltage and current stresses are acceptable in [108], the series diode with the auxiliary MOSFET as well as the Zener diode in parallel with coupled inductor increases the total loss and complexity of the system. The drawbacks of already proposed auxiliary cells, show up the need for a proper ZVT circuit that achieves ZVS without imposing extra voltage and current stress or power loss to the system. In the next section, a fully ZVS auxiliary cell is proposed to minimize the converter on-off transients and switching power losses.

![ZVT Boost converter schematic](image)

(a) Schematic  (b) Key waveforms

**Figure 5-1: An example of a ZVT Boost converter in [93]**

### 5.3 ZVT Cell for a Quasi-Resonant Circuit

The proposed ZVT cell operates at the beginning and the end of each power pulse to obtain zero voltage switching operation. This circuit, as shown in Figure 5-2, is a bidirectional switch which can be implemented by a MOSFET in series with a diode or two series MOSFETs in opposite directions. This cell is placed in parallel with the input inductor ($L_{in}$).
During a power pulse, the main circuit operates at the switching frequency while the auxiliary cell is off. To regulate the output voltage, the controller turns the main circuit off and turns the auxiliary cell on under ZVS condition. This cell arranges a short circuit path for the input inductor current $i_{Lin}$ and clamps the main switch voltage to $V_i$. Hence, $i_{Lin}$ remains constant when the converter is idle. The preserved current in $L_{in}$ is used to achieve lossless turn-on in the next power pulse. In a proper design, both auxiliary and main switches are turned “on” and “off” under zero voltage switching. By removing the first cycle switching losses, higher modulation frequencies and thus smaller filter sizes are feasible in the design.

The operation of the ZVT cell is explained in 7 different intervals. The first and the second intervals represent the steady-state operation of the converter which was extensively explained in Chapter 3. The analysis starts with the last switching cycle of a power pulse and ends by the first cycle of the next power pulse. Figure 5-3 shows the proposed circuit and the key waveforms in each individual interval. To simplify the operation of the converter, rectifier intrinsic capacitor, diodes forward voltages and parasitic resistive components are neglected.

**Figure 5-2: The proposed auxiliary ZVT cell configurations**
Interval 1 \((t_0 - t_1)\): This period is a part of the steady-state operation of the converter in which the auxiliary cell is off. The detailed operation of the converter in this period was explained in Chapter 3. The equivalent circuit of the converter in this mode is shown in Figure 5-4 (a). At the beginning of this interval, \(C_1\) and \(C_2\) are discharged and \(C_3\) is standing \(V_i\). At \(t_0\), \(Q_{main}\) is turned off under ZVS because the snubber capacitor \(C_1\) limits \(dv/dt\) of the \(v_{C1}\). The series-parallel combination of \(C_1\), \(C_2\) and \(C_3\) plays the role of resonant capacitor \(C_{eq1}\) (resonance capacitor \(C\) in Chapter 3). The resonance nature of the circuit creates a half-sine waveform across \(C_{eq1}\). During
this interval, the resonance capacitor is charged to its peak voltage and then discharged to zero. Consequently, the main switch can be turned on under ZVS at the end of this interval.

The proper operation of the circuit requires $D_{aux}$ remains off between $t_0$ and $t_1$. If $D_{aux}$ is turned on between $t_0$ and $t_1$, $i_{c3}$ average becomes positive (instead of zero). So, $C_3$ will not be fully charged to $V_i$ ($v_{c3}$ initial value at $t_0$) and $C_2$ will not be fully discharged to zero ($v_{c2}$ initial value at $t_0$) at $t_1$. This residual voltage in $C_2$ causes switching losses when $Q_{aux}$ is turned on at $t_2$. If $D_{aux}$ turns on, so this diode must stay off in steady-state operation. Critical condition to keep $D_{aux}$ off is given in (5-5).

$$C_{eq1} = C_1 + \frac{C_2 C_3}{C_2 + C_3}$$  \hspace{1cm} (5-1)

$$v_{c1} + v_{c2} + v_{c3} = V_{in},$$  \hspace{1cm} (5-2)

$$v_{c1}(t_0) = v_{c2}(t_0) = 0, \hspace{0.5cm} v_{c3}(t_0) = V_{in},$$  \hspace{1cm} (5-3)

$$i_{c2} = i_{c3} \rightarrow \Delta v_{c2} = \Delta v_{c3} \times \frac{C_3}{C_2} \rightarrow v_{c3}(min) = V_{in} - v_{c1}(peak) \times \frac{C_2}{C_2 + C_3}$$  \hspace{1cm} (5-4)

$$v_{c3}(min) > 0 \rightarrow \frac{V_{in}}{v_{c1}(peak)} = \frac{C_2}{C_2 + C_3} \frac{v_{c3}(peak) = 3.56 + V_{in}}{V_{in}} \rightarrow C_2 \approx 2.5 C_3$$  \hspace{1cm} (5-5)

**Interval 2 ($t_1 - t_2$):** This interval is also a part of the steady-state operation of the converter which was explained in Chapter 3. At $t_1$, $C_1$ and $C_2$ are discharged to zero. Hence, $Q_{main}$ is turned on under ZVS condition. During the second interval, the voltages across $Q_{main}$ and $Q_{aux}$ are zero while $D_{aux}$ is standing the input voltage. In addition, input voltage source is charging the input inductor via $Q_{main}$. Figure 5-4(b) shows the equivalent circuit of the converter in this mode. During a power pulse, the first interval starts after this interval. But, at the end of a power pulse, this interval follows by interval three.
**Interval 3** \((t_2 - t_3)\): after a number of switching cycles, nominal power is delivered to the output and the output voltage is increased to the upper threshold. Therefore, the controller commands to turn the converter off. For a proper operation, this command must wait until the switching cycle is completed at \(t_2\). Then, the controller turns the main switch off and the auxiliary switch on. \(C_1\) limits \(dv/dt\) of \(Q_{\text{main}}\), and hence, turn-off loss of this switch is minimized. As mentioned in interval 2, \(v_{C2}\) is zero between \(t_1\) and \(t_2\). So, \(Q_{\text{aux}}\) is turned on under ZVS condition. In this interval, \(C_2\) is bypassed by \(Q_{\text{aux}}\). Hence, \(C_1\), \(C_3\), and \(L_{\text{in}}\) are involved in the resonant network. Initial state-space values at \(t_2\) are as follows. \(C_1\) and \(C_2\) are fully discharged. Input inductor carries \(I_3\), and resonant inductor carries zero current. Finally, \(C_3\) holds the input voltage. This interval begins by charging \(C_1\) and discharging \(C_3\). This period continues until \(v_{C3}\) reaches zero and \(D_{\text{aux}}\) turns on. Figure 5-4(c) presents the equivalent circuit in this interval. Equations (5-6)-(5-18) explain the state space parameters between \(t_2\) and \(t_3\)

\[
v_{C1}(t) = V_i(1 - \cos(\omega_3(t - t_2))) + I_3 Z_3 \sin(\omega_3(t - t_2)) \quad (5-6)
\]

\[
v_{C2}(t) = 0 \quad (5-7)
\]

\[
v_{C3}(t) = V_i - v_{C1}(t) \quad (5-8)
\]

\[
i_{L_{\text{in}}}(t) = \frac{V_i}{Z_1} \sin(\omega_3(t - t_2)) + I_3 (1 - \cos(\omega_3(t - t_2))) \quad (5-9)
\]

\[
i_{L_{r}}(t) = 0 \quad (5-10)
\]

\[
(t_3 - t_2) = \frac{1}{\omega_3} \left( \sin^{-1} \left( \frac{N_3}{M_3} \right) + \varphi_3 \right) \quad (5-11)
\]

\[
N_3 = V_i, \quad M_3 = \sqrt{\frac{V_i^2 + (I_0 Z_3)^2}{C_{eq3}}}, \quad \varphi_3 = \tan^{-1} \left( \frac{V_i}{I_0 Z_3} \right) \quad (5-12)
\]

\[
C_{eq3} = C_1 + C_3, \quad Z_3 = \sqrt{\frac{L_{\text{in}}}{C_{eq3}}}, \quad \omega_3 = 1/\sqrt{L_{\text{in}} C_{eq3}} \quad (5-13)
\]

\[
v_{C1}(t_3) = V_i \quad (5-14)
\]
\begin{align*}
v_{C2}(t_3) &= 0 \quad (5-15) \\
v_{C3}(t_3) &= 0 \quad (5-16) \\
i_{Lin}(t_3) &= I_4 = \frac{V_i}{Z_3} \sin(\omega_3(t_3 - t_2)) + I_3(1 - \cos(\omega_3(t_3 - t_2))) \quad (5-17) \\
i_{Lr}(t_3) &= 0 \quad (5-18)
\end{align*}

**Interval 4** ($t_3 - t_4$): when $D_{aux}$ turns on at $t_3$, $v_{C1}$ is clamped to $V_i$ and the ZVT cell provides a circulating short circuit path for $i_{Lin}$. This interval is a kind of hibernate mode for the converter. Because state-space parameters are almost constant and the delivered power to the output is zero. Meanwhile, the output capacitor is slowly discharged in the load. This interval ends when the controller turns $Q_{aux}$ off to start the converter operation and deliver power to the output. Figure 5-4(d) shows the equivalent circuit of the converter in the 4th interval.

**Interval 5** ($t_4 - t_5$): power delivery to the load is zero in interval 4. So, the output capacitor is slowly discharged in the load. Then, to regulate the voltage, the controller turns $Q_{aux}$ off at $t_4$ to start a new power pulse. $Q_{aux}$ is turned off under zero voltage switching condition because of the parallel snubber capacitor $C_3$. At the beginning of this period, both switches and rectifier diodes are off. During this interval, the input current is divided between $C_1$ and $C_2$. Therefore, $i_{Daux}$ is positive and this diode remains on. $C_1$, $C_3$, and $L_{in}$ are the resonance components between $t_4$ and $t_5$. This interval ends when $v_{C1}$ reaches the output voltage and rectifier diode $D_1$ turns on at $t_5$. Initial state-space values at $t_4$ are as follows. $C_2$ and $C_3$ are fully discharged. Input inductor carries $I_3$ which is named $I_5$ in this interval. The resonant inductor, $L_r$ carries zero current and $C_1$ holds the input voltage. State-space parameters in this interval are described in (5-19)-(5-31). Figure 5-4(e) shows the equivalent circuit in this mode.
\begin{align*}
v_{C1}(t) &= V_i + l_5 Z_5 \sin(\omega_5(t - t_4)) \tag{5-19} \\
v_{C2}(t) &= -l_5 Z_5 \sin(\omega_5(t - t_4)) \tag{5-20} \\
v_{C3}(t) &= 0 \tag{5-21} \\
i_{L_{\text{lin}}}(t) &= l_5 (1 - \cos(\omega_5(t - t_4))) \tag{5-22} \\
i_{L_r}(t) &= 0 \tag{5-23} \\
(t_5 - t_4) &= \frac{1}{\omega_5} \left( \sin^{-1} \left( \frac{N_5}{M_5} \right) \right) \tag{5-24} \\
N_5 &= V_O - V_i, \quad M_5 = l_5 Z_5, \tag{5-25} \\
C_{\text{eq5}} &= C_1 + C_2, \quad Z_5 = \sqrt{\frac{L_{\text{lin}}}{C_{\text{eq5}}}}, \quad \omega_5 = \frac{1}{\sqrt{L_{\text{lin}} C_{\text{eq5}}}} \tag{5-26} \\
v_{C1}(t_5) &= V_O \tag{5-27} \\
v_{C2}(t_5) &= V_i - V_O \tag{5-28} \\
v_{C3}(t_5) &= 0 \tag{5-29} \\
i_{L_{\text{lin}}}(t_5) &= I_6 = l_5 (1 - \cos(\omega_5(t_5 - t_4))) \tag{5-30} \\
i_{L_r}(t_5) &= 0 \tag{5-31} \\
\end{align*}

**Interval 6 (t_5 - t_6):** when the switch voltage \(v_{C1}\) reaches \(V_O\), \(D_1\) turns on, and connects the resonant inductor to the output capacitor. By adding \(L_r\) to the resonant circuit, state space equations are changed to (5-32)-(5-44). Figure 5-4(f) shows the converter equivalent circuit in this period. The resonance continues until \(v_{C1}\) and \(v_{C3}\) reach their corresponding peaks at \(t_6\). Because capacitor current is the derivative of the capacitor voltage, the capacitor current becomes zero when the capacitor voltage reaches its peak. Therefore, \(i_{C_1}, i_{C_3}\) and \(i_{\text{aux}}\) become zero and \(D_{\text{aux}}\) turns off at \(t_6\).

\begin{align*}
v_{C1}(t) &= V_o + \frac{(V_i - V_O) L_R}{L_R + L_{\text{lin}}} \left( 1 - \cos(\omega_6(t - t_5)) \right) + l_6 Z_6 \sin(\omega_6(t - t_5)) \tag{5-32}
\end{align*}

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\[ v_{C2}(t) = 0 \]  
\[ v_{C3}(t) = V_i - v_{C1}(t) \]  
\[ i_{Lin}(t) = I_6 + \frac{(V_i-V_o)}{(L_R + L_{in})} (t - t_5) + \frac{I_6Z_6}{L_{in}\omega_6} (1 - \cos(\omega_6(t - t_5))) \]  
\[ + \frac{(V_i-V_o)L_R}{(L_R + L_{in})L_{in}\omega_6} \sin(\omega_6(t - t_5)) \]  
\[ i_{LR}(t) = \frac{(V_i-V_o)}{(L_R + L_{in})} (t - t_2) + \frac{I_6Z_6}{L_R\omega_6} (1 - \cos(\omega_6(t - t_5))) \]  
\[ - \frac{(V_i-V_o)L_R}{(L_R + L_{in})L_R\omega_6} \sin(\omega_6(t - t_5)) \]  
\[ t_6 = t_5 + \frac{1}{\omega_6} \sin^{-1}\left( \frac{N_6}{M_6} \right) + \varphi_6 \]  
\[ N_6 = V_\nu, \quad M_6 = \sqrt{\frac{(V_i-V_o)L_R}{L_R + L_{in}}}^2 + \frac{I_6Z_6}{L_{in}\omega_6}^2, \]  
\[ \varphi_6 = \tan^{-1}\left( \frac{(V_i-V_o)L_R}{(L_R + L_{in})I_6Z_6} \right) \]  
\[ C_{eq6} = C_1 + C_2, \quad Z_6 = \sqrt{\frac{L_{in}}{C_{eq6}}}, \quad \omega_6 = 1/\sqrt{L_{in}C_{eq6}} \]  
\[ v_{C1}(t_6) = V_{peak} = V_0L_{in} + L_R\nu_i + \sqrt{\frac{I_6Z_6^2}{L_R + L_{in}}}^2 + \frac{(V_i-V_o)L_R}{(L_R + L_{in})L_R\omega_6}^2 \]  
\[ v_{C2}(t_6) = 0 \]  
\[ v_{C3}(t_6) = 0 \]  
\[ i_{Lin}(t_6) = I_7 = I_6 + \frac{(V_i-V_o)}{(L_R + L_{in})} (t_6 - t_5) + \frac{I_6Z_6}{L_{in}\omega_6} (1 - \cos(\omega_6(t_6 - t_5))) \]  
\[ + \frac{(V_i-V_o)L_R}{(L_R + L_{in})L_{in}\omega_6} \sin(\omega_6(t_6 - t_5)) \]  
\[ i_{LR}(t_6) = \frac{(V_i-V_o)}{(L_R + L_{in})} (t_6 - t_2) + \frac{I_6Z_6}{L_R\omega_6} (1 - \cos(\omega_6(t_6 - t_5))) \]  
\[ - \frac{(V_i-V_o)L_R}{(L_R + L_{in})L_R\omega_6} \sin(\omega_6(t_6 - t_5)) \]
**Interval 7** ($t_6 - t_7$): by turning $D_{aux}$ off, the operation of this interval becomes similar to the first stage with slightly different initial values. The main switch voltage starts falling at $t_6$. This falling continues during this mode until $v_{c1}$ reaches zero at $t_7$. Then, $q_{main}$ can be turned on under zero voltage switching condition. Figure 5-4(g) shows the equivalent circuit in this mode and (5-45)-(5-54) describe the operation of the converter in this interval.

\[
v_{c1}(t) = V_o + \frac{(V_i - V_o)L_R}{L_R + L_{in}} (1 - \cos(\omega_7(t - t_6))) + \left(V_{peak} - V_o\right) \cos(\omega_7(t - t_6))
\]  
\[v_{c2}(t) = (V_i - V_{peak}) - \frac{C_3}{C_3 + C_2} v_{c1}(t)\]  
\[v_{c3}(t) = V_{Peak} - \frac{C_2}{C_3 + C_2} v_{c1}(t)\]

\[
i_{Lin}(t) = I_6 + \frac{(V_i - V_o)}{(L_R + L_{in})} (t - t_6) + \frac{l_6 Z_7}{L_{in} \omega_7} (1 - \cos(\omega_7(t - t_6)))
\]  
\[+ \left(V_{peak} - V_o\right) \frac{(V_i - V_o) L_R}{(L_R + L_{in})} \times \frac{1}{L_{in} \omega_6} \sin(\omega_7(t - t_6))\]

\[
i_{L_R}(t) = \frac{(V_i - V_o)}{(L_R + L_{in})} (t - t_{62}) + \frac{l_6 Z_7}{L_R \omega_7} (1 - \cos(\omega_7(t - t_6)))
\]  
\[+ \left(V_{peak} - V_o\right) \frac{(V_i - V_o) L_R}{(L_R + L_{in})} \frac{1}{L_R \omega_7} \sin(\omega_7(t - t_6))\]

\[t_6 = t_5 + 1/\omega_6 (\sin^{-1}\left(N_6/M_{66}\right) + \phi_6)\]

\[N_6 = V_o + \frac{(V_i - V_o)L_R}{L_R + L_{in}}, \quad M_{66} = \sqrt{\left(V_{peak} - V_o\right) + \left(V_i - V_o\right) L_R \left(L_R + L_{in}\right) + (l_6 Z_6)^2},\]

\[\phi_6 = \tan^{-1}\left(\frac{V_i}{l_5 Z_6}\right)\]

\[C_{eq7} = C_1 + \frac{C_2 C_3}{C_2 + C_3}, \quad Z_7 = \frac{L_{in}}{C_{eq7} \omega_7}, \quad \omega_7 = 1/\sqrt{L_{in} C_{eq7}}\]

\[v_{c2}(t_7) = 0\]  
\[v_{c3}(t_7) = V_i\]  

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After the 7th stage, converter enters the steady-state operation (intervals one and two) and power delivery continues until the output voltage reaches the upper threshold. Then, the controller starts interval three to stop power delivery. The converter passes a full cycle of active and idle operations without any switching losses and the output voltage is regulated by controlling the ratio of active to idle periods. The ZVS operation of the system allows the designer to increase the modulation frequency without significant extra power losses.

Figure 5-4: Converter equivalent circuits in the individual intervals
5.4 ZVT Cell Design

5.4.1 Voltage and Current Ratings

Components ratings, power losses, and timing sensitivity of the circuit should be assessed for evaluating the benefits of the auxiliary cell. The peak voltage stress of $D_{aux}$ is equal to the maximum input voltage which is about 30% of the main switch voltage stress. As the voltage stress of the auxiliary cell is equal to the main switch stress minus input voltage, the auxiliary switch must stand 70% of the main switch stress. Average and RMS currents of the cell are functions of the load. When the converter is working under nominal output power, the auxiliary cell is fully off. By decreasing the load, the ZVT cell active duty cycle and its current losses are increased. Equations (5-55)-(5-56) give the average and RMS current of the cell.

\[ I_{AVG} = I_{input} \left(1 - \frac{P_{load}}{P_{Nominal}}\right) \]  \hspace{1cm} (5-55)

\[ I_{RMS} = I_{input} \sqrt{1 - \frac{P_{load}}{P_{Nominal}}} \]  \hspace{1cm} (5-56)

5.4.2 ZVT Cell Power Loss

Although the proposed circuit reduces the switching losses, this circuit introduces extra conduction loss. Because the auxiliary circuit/switch is carrying a constant current, the additional conduction loss is almost independent of the modulation frequency, but a function of on-off duty cycle. So, at very low modulation frequencies where the number of hard switching cycles is negligible, this conduction loss is higher than the promising saved switching losses. By increasing the modulation frequency, hard switching loss is increased and the ZVT cell becomes useful. Equation (5-57)-(5-60) give conduction and switching power losses as functions of operating condition and modulation frequency.
\[ P_{\text{aux}} = I_{\text{input}} \left( 1 - \frac{P_{\text{load}}}{P_{\text{Nominal}}} \right) V_{\text{forward}} \]  
(5-57)

\[ P_{\text{Qaux}} = I_{\text{input}}^2 \left( 1 - \frac{P_{\text{load}}}{P_{\text{Nominal}}} \right) R_{\text{Qaux}} \]  
(5-58)

\[ P_{\text{Lin}} = I_{\text{input}}^2 \left( 1 - \frac{P_{\text{load}}}{P_{\text{Nominal}}} \right) R_{\text{DC}} \]  
(5-59)

\[ P_{\text{Switching}} = \frac{C_{\text{eq}} V_i^2}{2} F_{\text{Modulation}} \]  
(5-60)

When the ZVT cell is on, the input inductor and the ZVT cell carry a constant DC current. So, proximity effect, skin effect, and magnetizing losses are zero and the inductor loss is limited to its DC resistance conduction loss. The auxiliary switch conduction loss is a function of its on-resistance which can be reduced by using a proper MOSFET. Finally, \( D_{\text{aux}} \) forward voltage drop is a significant cause of power loss in the circuit. Total conduction loss of the cell is decreased by replacing this diode with a synchronous rectifier MOSFET.

### 5.4.3 Effect of Auxiliary Cell Parasitic Capacitors

It should be noted \( C_2 \) and \( C_3 \) are not required for a proper operation. In fact, the operation of the cell is simpler without these capacitors. However, intrinsic capacitance of auxiliary diode and switches affect the converter operation and should be considered in the design. As mentioned in interval one, a proper ratio of the \( C_3 \) and \( C_2 \) is required to achieve ZVS for the auxiliary switch. When \( C_3/C_2 \) is less than 2.5, a or maybe residual charge is trapped in \( C_2 \) and \( C_3 \). So, \( C_3 \) is not fully discharged at \( t_2 \) and ZVS operation cannot be achieved for \( Q_{\text{aux}} \). To calculate the effect of these capacitors values on the trapped charge, we assume that the switch voltage \( (v_{C_1}) \) is a half-sine waveform and its peak value is 3.56 times the input voltage (as shown in Figure 5-5). This is divided on \( C_3 \) and \( C_2 \). According to the direction of \( D_{\text{aux}} \) and \( Q_{\text{aux}} \), \( v_{C_3} \) is always higher or equal to zero and
$v_{C2}$ is always lower or equal to zero. At $t_0$, $v_{C3}$ is equal to $V_i$, $v_{C1}$ and $v_{C2}$ are equal to zero. By rising $v_{C1}$ from zero to its peak, $v_{C3}$ is decreasing correspondingly. If $v_{C3}$ reaches zero before $t_1$, $D_{aux}$ turns on and bypasses $C_3$. Then, $C_2$ will be charged to the difference between the peak voltage and $V_i$. In the falling part of the waveform, the auxiliary cell current is negative, $D_{aux}$ is off, and $C_3$ is in series with $C_2$. Then at $t_2$, $C_2$ will not be fully discharged and $C_3$ will be charged with a voltage higher than the input voltage. This charge trapping continues until $v_{C3}$ is negative enough to keep $D_{aux}$ off during steady-state operation. Equation (5-63) shows the required $v_{C2}(t_0)$ to keep the diode off during steady-state operation. The minimum $C_3/C_2$ is given in (5-64).

![Circuit model](image1)

![Waveforms](image2)

Figure 5-5: Auxiliary residual charge model

\[ t_0: \quad v_{C1} = 0, \quad v_{C2} = v_{C2}(t_0), \quad v_{C3} = v_{C3}(t_0) \]  

(5-57)

\[ t_1: \quad v_{C1} = V_{peak}, \quad v_{C2} = v_{C2}(t_1), \quad v_{C3} = 0 \]  

(5-58)

\[ t_1: \quad v_{C1} = V_{peak}, \quad \Delta v_{C2} = \Delta v_{C3} \times \frac{C_3}{C_2}, \quad v_{C2}(t_1) = V_i - V_{peak} \]  

(5-59)
\[ \Delta v_{c3} = v_{c2}(t_0) - V_i \rightarrow \Delta v_{c2}(t_0) = (v_{c2}(t_0) - V_i) \times \frac{C_3}{C_2} \]  

(5-60)

\[ \Delta v_{c2}(t_0) = v_{c2}(t_1) - v_{c2}(t_0) = V_i - V_{peak} - v_{c2}(t_0) \]  

(5-61)

\[ V_i \left( 1 + \frac{C_3}{C_2} \right) - V_{peak} = v_{c2}(t_0) \left( 1 + \frac{C_3}{C_2} \right) \]  

(5-62)

\[ v_{c2}(t_0) = \frac{V_i \left( 1 + \frac{C_3}{C_2} \right) - V_{peak}}{\left( 1 + \frac{C_3}{C_2} \right)} \]  

(5-63)

\[ v_{c2}(t_0) = 0 : V_i \left( 1 + \frac{C_3}{C_2} \right) = V_{peak} \text{ or } \frac{C_3}{C_2} = 2.56 \]  

(5-64)

### 5.4.4 Timing Accuracy and Propagation Delay

In all zero voltage switching circuits, a proper ZVS operation depends on the accurate switching timing. In practical circuits, timing accuracy of the system is limited by the gate drive circuit, controller, and signal generator circuits. Signal propagation delay is one of the important obstacles in precise switching timing which is a function of temperature and operating conditions. A significant variation in the propagation delay leads to the system malfunctioning. Therefore, handling more than one switch in MHz switching converters is difficult or even impossible unless the timing is not very sensitive. To evaluate the feasibility of the proposed ZVT cell, the timing requirements of the circuit should be reviewed.

One advantage of the proposed ZVT cell is its simple timing. Among the 7 intervals, 6 of them are either autonomous or only the state of one switch is changed. Only in the 3rd interval, both main and auxiliary MOSFETs were switched simultaneously (turning the main switch off and auxiliary switch on). However, in this interval, voltage and current of the auxiliary switch are zero between \( t_1 \) and \( t_2 \). This switch can then be turned off anytime between \( t_1 \) and \( t_2 \) without interfering with the operation of the circuit. In fact, the system is able to tolerate a delay of up to a half switching cycle.
between turning the auxiliary switch on and the main switch off. Figure 5-6 shows the acceptable interval to turn $Q_{aux}$ on without any impact on the system operation.

5.5 Simulation Results

To verify the operation of the proposed ZVT cell, simulation results are provided in this section. LTPICE simulated prototype is shown in Figure 5-7. Table 5-1 gives the components details. 300V input, 400V output, 300kHz modulation frequency and 30% duty cycle are the operating condition in this simulation.
Table 5-1: Component’s values in the ZVT circuit

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{in}$</td>
<td>27µH</td>
</tr>
<tr>
<td>$L_R$</td>
<td>6.5µH</td>
</tr>
<tr>
<td>$C_1$</td>
<td>160 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>50 pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>Switch intrinsic capacitance</td>
</tr>
<tr>
<td>$Q_{main}$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$Q_{aux}$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$D_{aux}$</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>$D_1$</td>
<td>UPSC600</td>
</tr>
<tr>
<td>$D_2$</td>
<td>UPSC600</td>
</tr>
</tbody>
</table>

Figure 5-8 illustrates the behavior of the converter without the proposed ZVT cell. Figure 5-8 (a) shows a pulse power train. As we can see in Figure 5-8(b), the main switch turns on under non-ZVS condition in the first three cycles. Hence more energy is dissipated in each power pulse.
addition, the converter does not have enough time to settle. As shown in Figure 5-8(c), input inductor current falls to zero before reaching the steady-state value.

Figure 5-8: The behavior of the converter when the conventional on-off control method is used
Figure 5-9(a) shows a power pulse train for the converter using the ZVT cell. As shown in Figure 5-9(b), when the converter is turned off, $v_{c1}$ is clamped to the input voltage. At the beginning of the next pulse, $v_{c1}$ rises to its peak and then falls to zero just before the switch is turned on. Therefore, the main switch is turned on and off under ZVS condition at the beginning, during and the end of each power pulse. Figure 5-9(c) shows the auxiliary switch operation. Drain-source voltage rises slowly after the switch is turned off which minimizes the turn-off loss and drain-source voltage is zero before the switch is turned on. The zero voltage switching condition in every cycle is provided for this switch. As we can see, the auxiliary switch peak voltage is about 70% of the main switch voltage. Figure 5-9(d) shows the auxiliary diode voltage. Maximum voltage stress on this switch is equal to the input voltage. Finally, as shown in Figure 5-9(e), the input inductor current is clamped to the steady-state peak value when the converter is turned off. Therefore, the converter enters the steady-state operation just after the auxiliary switch is turned off.
Figure 5-9: The behavior of the converter when ZVT cell is used
5.6 Experimental Results

To evaluate the performance of the ZVT circuit, this cell is implemented on the none-isolated quasi-resonant converter designed in chapter 3. The basic characteristics and component values are similar to the simulated converter in the previous section. The prototype and controller circuits are shown in Figure 5-10. The ZVT cell is located under the input inductor. TMS320F28335 Experimenter Kit is utilized for generating gate signals. Although one benefit of the converter is the ground reference switch, the ground reference of the auxiliary circuit is different from the main circuit. Therefore, an isolated gate drive is required to turn $Q_{aux}$ on and off. The source terminal of this switch is connected to the input voltage terminal which is a constant voltage node. Therefore, high-frequency switching difficulties are minimized. Moreover, $Q_{aux}$ is turned on and off at a modulation frequency which is lower than the main switching frequency.

![Converter, DSP, Isolation](image)

Figure 5-10: The 3MHz prototype converter

Figure 5-11 shows the converter key waveforms in conventional on-off control method. Hard switching operation in the first two cycles of each power pulse is observed. Therefore, the stored energy in the parallel capacitor is dissipated in the main switch. This hard-switching operation not only increases the power losses but also boosts EMI in the circuit.
ZVT cell is able to solve the converter hard switching operation and power losses problem. As we can see in Figure 5-12 (a), both switches turn on and off under ZVS condition and the converter enters the steady-state operation in the first cycle of each power pulse. In fact, the short circuit path provided by the ZVT cell preserves the input inductor current at the end of each power pulse and utilizes this current to achieve ZVS in the next power pulse.

During each power pulse, the steady-state gate signal is applied to the main switch while the auxiliary switch is kept off. The converter operation continues until the output voltage reaches the higher threshold point and the controller turns the converter off to regulate the output. Figure 5-12 (b) shows a full on-off operation cycle.

Figure 5-11: Experimental results for 3MHz non-isolated converter using conventional on-off
Figure 5-13 shows the converter waveforms at the end of each power pulse. In contrast to the conventional on-off method, no oscillation appears on the switches voltage. As mentioned before, ZVT cell freezes state-space variable when the converter is turned off. By minimizing the on-off switching loss of the system, modulation frequency can be increased significantly. Figure 5-14 shows the effect of $C_3/C_2$ ratio on the auxiliary MOSFET zero voltage switching operation when $C_2$ and $C_3$ are equal. In this situation, the auxiliary switch turns off under hard switching condition.
The converter overall efficiency is plotted in Figure 5-15 as a function of output power. Chroma 6630 power analyzer was used to measure input and output power to calculate the efficiency of the system. For more accurate results, gate power loss is added to the input power. Converter overall efficacy drops about 2% for a load variation of 385W to 85Watt at a modulation frequency of up to 600kHz. The satisfactory efficiency of the converter at a modulation frequency close to the switching frequency verifies the proper performance of the converter.
5.7 Conclusion

In this chapter, a novel ZVT cell was introduced to improve the performance of a non-isolated quasi-resonant converter using on-off control method. This cell provides zero voltage switching condition for both main and auxiliary switches. Simple structure, low number of components, and avoidance of inductive components in the cell are advantages of the circuit. Higher modulation frequency, lower input and output filter size, and faster dynamic response are the benefits of this method. Simulation results were presented to verify analytic results and the experimental prototype was built and tested to validate the design. The zero voltage switching operation of all semiconductor components allows the designer to increase the modulation frequency without any significant drop in the overall efficiency. A maximum efficiency of 95.8% at 385W output and 93.4% at 85W load were observed at up to 600kHz on-off frequency.
Chapter 6

Conclusion and Future Work

6.1 Summary

This thesis has presented topologies and control solutions to decrease switching losses and component voltage stress of MHz resonant converters across a wide load range. The motivation of this research has been driven by the growing demands for lighter, smaller, and more efficient converters with premium performance over a wide load and voltage range. Based on the review of the present DC-DC topologies and available control strategies in Chapter 2, single-ended MHz resonant converters such as Class E and quasi-resonant converters are popular candidates to respond to this demand. Although these circuits are designed to operate at high switching frequencies, issues such as parasitic components, converter dynamics, and control shortcomings limit their performance to a narrow load variation range. To resolve these issues, this thesis proposed new quasi-resonant boost converter, a novel first cycle control scheme, and a new auxiliary ZVT cell.

6.1.1 New Quasi-Resonant Boost Converters with reduced voltage stress and losses

A new quasi-resonant converter topology and a novel approach to analyze and design these types of converters are proposed in Chapter 3. These solutions improve the compatibility of quasi-resonant converters for MHz DC-DC applications. These improvements are as follows: (i) Up to 50% reduction in the rectifier diode voltage stress compared to the conventional quasi-resonant boost converters. This reduction is achieved without sacrificing the traditional benefits of this converter. An additional low current rating diode in the rectifier circuit reduces the unwanted oscillation and voltage stress in the non-isolated converter. This topology improvement allows the use of lower voltage diodes in quasi-resonant converters for a certain output voltage level when
compared to the existing converter topologies. (ii) More flexibility in the converter design. A new approach in synthesizing the converter’s equations provides a better insight into the operation of the circuit and the converter’s design. The analysis and design based on the resonant input inductor add more flexibility to the component selection. In addition, utilizing a finite input inductance enhances the dynamic response of the system, which makes the converter compatible with the on-off control. Measured results of a 300V/400V 1kW converter at 3MHz confirms a peak powertrain efficiency close to 96% for the non-isolated converter, and close to 93% for the isolated one.

6.1.2 Novel First Cycle Control Method for Isolated and Non-Isolated Quasi-Resonant Converters

Chapter 4 introduces a novel first cycle control method that enhances the performance of the so-called on-off control, which is a popular control method for the high-frequency converters. Theoretically, on-off control methods offer simplicity and stability of the control structure and maintain the efficiency of the system at almost its maximum level independent of the load variations. However, this method loses its credibility for higher on-off rates. The proposed first cycle control method drives a predetermined gate signal at the beginning of each power pulse that substantially alleviates the voltage stress and switching losses, and thus improves the transient behavior of the converter. This achievement enhances the switches’ utilization factor and paves the way for further increases in the on-off rate. To validate the performance of the proposed method, it has been applied to an isolated and a non-isolated quasi-resonant converter. The implementation of this method resulted in a 60% reduction in the number of hard switching cycles in the non-isolated converter and a 20% voltage stress reduction in the

6.1.3 A New ZVT Auxiliary Cell for a High-Frequency Quasi-Resonant Converter in on-off Control Modes
The proposed first cycle control method, presented in Chapter 4, would still suffer from the switching loss in the first switching cycle of each power pulse despite all its benefits discussed previously. Therefore, Chapter 5 proposes a novel ZVT auxiliary cell to ensure ZVS operation in every switching cycle. A simple structure, low number of components, and exclusion of inductive components in the cell are advantages of the circuit. Higher modulation frequency, lower input and output filter sizes, and faster dynamic response are the benefits of this method. The zero voltage switching operation of all semiconductor components allows the designer to increase the modulation frequency without any significant drop in the overall efficiency. The simple and robust timing sequence makes this structure suitable for very high-frequency operation. A maximum efficiency of 95.8% at 385W output and 93.4% at 85W load were observed while the maximum modulation frequency was 600kHz.

6.2 Contributions

The thesis contributions are summarized as follows:

(a) An improved non-isolated quasi-resonant converter with reduced rectifier voltage stress

(b) A new first cycle control method to reduce voltage stress and switching losses in on-off control method

(c) A new ZVT auxiliary cell to achieve fully ZVS operation in on-off control method

(d) A new analysis and design procedure of isolated and non-isolated quasi-resonant boost converters based using resonant input inductor

(e) Performance evolution of the proposed topologies and control method by simulation and experimental results
6.3 Conclusion

In conclusion, the main advantages of the proposed circuits and the control method are:

(i) Potentially higher efficiency due to lower voltage stress and power losses;
(ii) Higher on-off rate and smaller input/output filters due to the improved startup and shut down transient;
(iii) Lower EMI due to the fully ZVS operation by using a ZVT auxiliary cell

A detailed set of conclusions are listed as follows:

(1) Proposed quasi-resonant topology:
   i. Quasi-resonant circuits are tailored for MHz DC-DC converters since they utilize parasitic components in the resonant circuit
   ii. An additional low current rating diode reduces the rectifier voltage stress by 50%
   iii. Converter analysis based on resonant input inductor adds more flexibility to the component selection and enhances the dynamic response of the system

(2) Proposed first cycle control:
   i. The first cycle control method enhances the on-off control strategy performance by introducing a significant reduction in the converter voltage stress and in the number of hard switching cycles in each power pulse
   ii. The first cycle control method can be implemented effectively on isolated and non-isolated quasi-resonant converters
   iii. Light-load efficiency improves 2% by using the first cycle control method compared to the conventional on-off control method
   iv. The first cycle control limits the switching losses to the first switching cycle in each power pulse as and restricts the maximum switch voltage stress to the steady state peak voltage

(3) Proposed ZVT auxiliary cell
   i. The proposed cell is effective in removing all switching losses for the on-off control method
ii. Simple structure and absence of inductive components in the circuit make this cell suitable for compact power converters.

iii. Very high on-off rate is feasible without a significant drop in the efficiency due to the full ZVS operation and the significantly reduced start-up and shutdown transient times.

iv. Less than 3% efficiency drop at 600kHz on-off rate confirms the superior performance of the cell.

6.4 Future work

The proposed topologies and control method improved the operation of quasi-resonant converters across a wide operation range. However, more research and study are suggested on the following issues:

i. The first cycle control method could be implemented on other high-frequency topologies at even higher frequencies than those implemented in this work.

ii. A simple and practical combination the first cycle on-off control method and conventional control methods such as frequency control could lead to a better performance and smaller filter sizes compared to the proposed solution here.

iii. The cost of ZVT circuit could be reduced by introducing a new structure based on a ground reference switch. A potential solution could be the implementation of the circuit by coupled inductors.
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**Publications related to this thesis:**


