Very High Efficiency Bridgeless Boost Totem-Pole PFC using Gallium Nitride HEMTs

by

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Abstract

Data centers have become the backbone of the global economy. The electricity demand for data centers grew tremendously over the last ten years. U.S. data centers consumed 91 billion kilowatt-hours of electricity in 2013 and are on track to consume 140 billion kilowatt-hours of electricity annually by 2020. AC – DC Rectifiers are the equipment to power the data centers. They convert the AC power from electric utilities into DC power with two power stages. The first stage is the PFC stage that converts the input 220V AC voltage into a 400V DC voltage. The second stage is the DC – DC stage that converts the 400V into 12V which is fed into the motherboard of the data center. Because of the huge electricity bill for the operating of data centers, very high efficiency AC – DC rectifiers are needed. Existing PFC AC – DC converters use MOSFETs as switching devices. Innovations in MOSFET switches over the last three decades have enabled a steady improvement in power supply design. However, the performance of the MOSFET has reached its theoretical limits. GaN switching technology offers significantly better performance than that of MOSFETs. It grants the opportunity to improve the power density and efficiency of power supplies.

A Bridgeless Boost Totem-Pole PFC topology is selected and designed for maximum efficiency by utilizing GaN switches. Merits include: a custom wound inductor to aid in increasing overall efficiency, a detailed PCB layout for the GaN switches and their respective gate drivers, a high and low-side gate resistance analysis for the GaN switches to reduce the rise and fall time of the gate signals while mitigating the Miller Effect, current control of the synchronous MOSFETs to achieve ideal diode emulation, a soft-start function during the zero-crossings of the line voltage to reduce AC current spikes, a fast voltage control loop for better dynamic performance, and two heatsink designs to reduce GaN switch temperatures during high load operation.
Mathematical analysis, simulation and hardware testing were done to verify the performance of the design. The performance tests consisted of start-up performance, dynamic step-load changes and steady-state performance via PF and THD measurements as well as efficiency recordings over a range of loading conditions.
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Chapter 1 - Introduction and Purpose of Research

1.1 Introduction

Power Electronics deals with the control and conversion of electrical power. Voltage can be stepped up or down and can be converted from AC to DC or DC to AC.

There are four classifications for power conversion systems based on their input and output:

- AC-DC Rectifier; which converts an AC voltage to a DC voltage.
- DC-AC Inverter; which converts a DC voltage to an AC voltage
- DC-DC Converter; which alters a DC voltage by stepping it up or down
- AC-AC Converter; which alters an AC voltage by stepping it up or down

Power Electronic systems can be found in almost all electrical devices. Applications are wide ranging and include computers and mobile devices among many others. When designing power electronics systems, the most important considerations include efficiency, size, reliability, and cost. Of course, the specifics of these requirements vary by application, and part of the challenge of design is balancing trade-offs.

In recent years, data centers have become the backbone of the global economy. The electricity demand for data centers grew tremendously over the last ten years. U.S. data centers consumed about 91 billion kilowatt-hours of electricity in 2013 and are on track to consume roughly 140 billion kilowatt-hours of electricity annually by 2020 [1].

AC – DC Rectifiers (also known as AC – DC power supplies) are the equipment to power the data centers. They convert the AC power from electric utilities into DC power with two power stages. The first stage is the PFC (Power Factor Correction) stage that converts the input AC voltage (120V or 220V) into a 400V DC voltage. The second stage is the DC – DC stage that converts the 400V into 12V which is fed into the motherboard of the data center. Because of the huge electricity bill for the operating of data centers, very high efficiency, such as 99%, AC – DC rectifiers are needed [2] [3].
The existing PFC AC – DC converters use MOSFET (Metal–Oxide–Semiconductor Field-Effect Transistor) as switching devices. The innovations made in the MOSFET in the last three decades have enabled a steady improvement in power supply design. However, the performance of the MOSFET has already reached its theoretical limits [4]. Gallium Nitride (GaN) switches offers significantly better performance than that of MOSFETs (3,000 times better in theory). It offers the opportunity to significantly reduce the physical size and improve the power density and efficiency of power supplies [5] [6].

In order to increase power density, it is necessary to operate converters at higher switching frequencies. Operation at higher switching frequencies decreases the necessary size of magnetics, meaning the converter size is also minimized and power density of the converter is maximized. Maximizing power density is very desirable, especially in mobile and computing applications. For these applications, board space taken up by a converter is space that could have been utilized for other functionalities or could have led to a reduction in size of the device. High frequency operation also leads to better transient performance.

However, there are costs that comes with high switching frequencies [7]. These include:

- Increased switching loss, since the switches are turned on and off more frequently in a given time period.
- Increased impact of dead time leading to increased diode conduction loss.
- Increased gate drive loss.

These losses have typically limited realistically achievable switching frequency, however, with the implementation of GaN switches, the losses from increased switching frequency can be reduced. This is due to several factors [6]:

- Low gate capacitance and charge ($C_{G}$, $Q_{G}$) for faster turn-on and turn-off, higher switching speed and reduced gate drive losses.
- Low output capacitance and charge ($C_{oss}$, $Q_{oss}$) for faster switching, higher switching frequencies and reduced switching losses.
- Low $R_{DSS}$ ($<5\text{mohm/cm}^2$ vs SI $>10\text{mohm/cm}^2$) yielding lower conduction loss.
- No ‘body diode’ ($Q_{RR}=$ zero) yielding no reverse recovery losses and reduced ringing on switch node and EMI.

1.2 Thesis Objectives

The main objective of this thesis is to develop a very high efficiency design for the first stage of the data centre power supply: the PFC stage (AC – DC converter). The design should lead to improvements in efficiency, with a target of 99% efficiency, while maintaining high PFC through a full range of loading conditions, low THD, and a low component count.

As seen from the literature review presented in the next chapter, a variety of boost PFC topologies have been explored for this application. However, these topologies are theoretically not able to achieve the requirements outlined above. This is in part due to high component count and high losses in the components. In this thesis a Bridgeless Boost Totem Pole PFC is selected and used to achieve the maximum efficiency by utilizing GaN transistors.

1.3 Thesis Outline

The contents of this thesis are organized into 6 Chapters.

Chapter 1 introduces Power Electronics and the motivation behind this research. It discusses high power density as well as high frequency operation, including their merits and challenges, with a focus on the limitations of Silicon MOSFETs. GaN technology is brought forth as a potential solution for these challenges. The objectives of this thesis are established.

Chapter 2 is a literature review. The concepts of power factor and total harmonic distortion are explored, including the introduction of passive and active PFC structures and modes of operation. This review goes into more depth about the losses experienced by PFC converters. Different active PFC
topologies are discussed in detail, including the Conventional PFC circuit and different improved PFC circuits. Finally, the selected topology is discussed briefly, along with the challenges of designing with Gallium Nitride technology.

Chapter 3 introduces the Bridgeless Boost Totem Pole PFC converter and explains its operation. The PFC control method is discussed before laying out the design requirements and component calculations to meet these requirements. The supporting circuits to the topology’s main power circuit are discussed and more component selection is done. A power loss analysis is performed to verify the feasibility of a target 99% efficiency. The entire design including a fully digital control scheme was simulated in PSIM.

Chapter 4 goes over the hardware design by starting with the specifics of the first PCB layout. Steps to get the converter operational are outlined and a first efficiency test is done. Details to increase efficiency via component tuning and control changes are discussed. A second PCB layout is performed with a thermal analysis that follows.

Chapter 5 provides the final results of the converter design. Power factor, total harmonic distortion, and efficiency are compared at various loading condition, along with waveforms of steady-state and start-up operation.

Chapter 6 is the conclusion and summarizes the thesis and the contributions made. The chapter ends with the possible scope for future work.
Chapter 2 - Background and Literature Review

2.1 Power Factor and Power Factor Correction

Power Factor is simply defined as the ratio of real power to apparent power, or:

\[
PF = \frac{\text{Real Power (Watts)}}{\text{Apparent Power (VA)}}
\]  

(2.1)

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of voltage. If both the current and voltage are sinusoidal and in phase, the power factor is 1. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. However, this is only a special case when the load is solely comprised of resistive, capacitive, and inductive elements that are all linear (invariant of current and voltage) [8] [9].

Switched-mode power supplies present a non-linear impedance to the mains due to the input circuitry which usually consists of a half-wave or full-wave rectifier followed by a storage capacitor capable of maintaining the voltage at approximately the peak voltage of the input sine wave until the next peak comes along to recharge the capacitor. In this case current is drawn from the input only at the peaks of the input waveform, and this current pulse must contain enough energy to sustain the load until the next peak. It does this by dumping a lot of charge into the capacitor in a short period, after which the capacitor slowly discharges the energy into the load until the cycle repeats. Because of this, the current pulse is usually 10-20% of the input width resulting in a current pulse that is 5 to 10 times larger than the average current [9]. See Figure 1.
Figure 1: Input characteristics of a typical switched-mode power supply without PFC [9].

Figure 2 shows the harmonic content of the current waveform. The fundamental frequency (60Hz) is shown with an amplitude of 100%, and the higher harmonic frequencies are given with their amplitudes shown as percentages of the fundamental amplitude. The even harmonics are barely seen as a result of the symmetry of the waveform. Since only the fundamental component produces real power, while the other harmonics contribute to the apparent power, the actual power factor is well below 1. This deviation is represented by a term called the distortion factor and mainly responsible for the non-unity power factor of switched-mode power supplies (SMPS) [8].

\[
\text{Distortion Factor} = \frac{1}{\sqrt{1 + \text{THD}^2}} = \frac{I_{1,\text{rms}}}{I_{\text{rms}}} \quad (2.2)
\]

Where, \textit{Total Harmonic Distortion (THD)} = \sqrt{\frac{\sum_{n=2}^{\infty} I_n^2}{I_1^2}} and \(I_n\) refers to the nth harmonic of the current waveform. \(I_{1,\text{rms}}\) and \(I_{\text{rms}}\) are the magnitudes of the fundamental component rms current and the total combined rms current respectively.

The displacement factor is the cosine of the angle between the fundamental components of the voltage and current waveforms.

\[
\text{Displacement Factor} = \cos(\phi - \theta_1) \quad (2.3)
\]

The overall power factor is the product of the distortion and displacement factors.
The power factor of the power supply with the waveform in Figure 1 is approximately 0.6.

\[ PF = \frac{I_{1,rms}}{I_{rms}} \cos(\phi_1 - \theta_1) \]  

The freedom from harmonics also minimizes the interference with other devices being powered from the same source.

Another reason to employ PFC in many of today’s power supplies is to comply with regulatory requirements. In Europe and Japan, electrical equipment must comply with the IEC61000-3-2 standard which affects most electrical appliances with input power of 75W (Class D) or greater, and it specifies
the maximum amplitude of line-frequency harmonics up to and including the 39th harmonic.

Additionally, many energy efficiency requirements also carry a PFC requirement such as the 80 Plus certification intended to promote efficient energy use in computer power supply units (PSUs) [10].

![Harmonic Number](image)

*Figure 3: Input characteristics of a power supply with near-perfect PFC [9].*

### 2.2 Passive PFC Circuit

The earliest topology applied in AC-DC power conversion is Passive Power Factor Correction (PPFC) technique. This is the simplest way to control the harmonic current and uses a filter that passes current only at line frequency (50 or 60 Hz). The filter consists of capacitors or inductors, and makes a non-linear device look more like a linear load. The scheme places a filter inductor between the rectifier and bus capacitor as in Figure 4 [11].

![PPFC Circuit](image)

*Figure 4: A typical PPFC circuit [11].*
In practical application, inductor is put between AC source and rectifier bridge. As shown in Figure 5, the improved PPFC topology will not have DC component in the inductor, which can prevent the inductor from saturation. The advantages of PPFC are that it is simple, reliable, without need of real-time control and low cost. In addition, this topology will limit the current total harmonic distortion under 30% by suppressing odd harmonics. In this application, the inductor, L, is the “core” of the design. When inductance is larger, the Total Harmonic Distortion (THD) is smaller and the current waveform is more sinusoidal. However, the phase difference will become bigger [9] [12].

The main disadvantage of the topology is that the passive components are often heavy with low power factor. This makes the power loss severe and produces a lot of heat. The noise of power frequency vibration is also a problem. The application is adopted under 300W, especially applied in occasions that have no constraints or limits for space and weight but is cost sensitive [12].

2.3 Active PFC and Conventional Topology

The most common topology for AC-DC application is Active Power Factor Correction (APFC). Active PFC is the use of power electronics to change the waveform of current drawn by a load to improve the power factor. Some types of the active PFC are buck, boost, buck-boost and synchronous condenser. Active power factor correction can be single-stage or multi-stage [9].
In the case of a switched-mode power supply, and in the case of this thesis, a boost converter is inserted between the bridge rectifier and the main input capacitors. The boost converter attempts to maintain a constant DC bus voltage on its output while drawing a current that is always in phase with and at the same frequency as the line voltage. Figure 6 shows the topology of a conventional APFC circuit that makes use of a full-controlled semiconductor device. This topology consists of a full bridge rectifier and a boost pre-regulator. The boost stage can operate in CCM, or DCM/critical conduction mode (CrCM) with zero/valley voltage switching for improved efficiency.

![Figure 6: A conventional boost APFC circuit](image)

Figure 7 shows the principle block diagram of APFC. The basic method involves rectifying the alternating voltage to direct voltage, and then conduct DC-DC transformation on the rectified voltage. There are two control loops; one for voltage and one for current. The outer voltage loop ensures that the bus voltage keeps up with the set value. The inner current loop ensures that the current waveform can track the input voltage waveform in real-time [12].
The control scheme will help reduce the THD of the current below 5% and make the PF value over 0.99 high [11]. APFC techniques can effectively reduce harmonic content and improve power factor to satisfy current standards. The disadvantages of the topology is the high cost and complexity of the controlling circuits. Besides, with higher switching frequency, the switched loss becomes significant. Thus, it is applied in low power (<1kW) applications.

Passive PFC can achieve power factor of about 0.7–0.75, SMPSs with active PFC, up to 0.99 power factor, while a SMPS without any power factor correction have a power factor of only about 0.55–0.65 [9].

2.3.1 Review of Losses in an APFC Circuit

With the conventional APFC circuit, a large portion of system loss are in the diode bridge and cannot be avoided even with zero voltage switching on the Boost stage. This fact inherently limits the peak
efficiency of the conventional PFC stage. The primary component losses of a conventional APFC circuit are broken down as follows:

**Bridge Diode Losses**

As mentioned, the diode bridge is used to rectify the input voltage to an only DC component. Diodes have two modes of operation; forward biased (the anode terminal voltage is positive with respective to the cathode terminal) which allows the current to flow through it, and reverse biased (the cathode terminal voltage is positive with respective to anode terminal), which will block the flow of current. When the current flows through the diode some part of the current will be wasted as heat energy [15]. This is known as conduction loss and is calculated as:

\[
P_{con} = V_f I_d
\]  
(2.5)

Where \( V_f \) is the forward voltage drop across the diode and \( I_d \) is the forward current flow through the diode.

A rectifier diode found in the bridge, has a typical 1V forward voltage drop and there are 2 diodes in the current path, which could account for around 1-2% of total efficiency loss. A well-designed PFC stage can probably achieve efficiency around 97 to even 98%, but efficiency higher than 98% (very high efficiency) becomes very challenging for standard PFC due to the fixed diode bridge loss [3].

**MOSFET and Boost Diode Loss**

The MOSFET is found in the boost stage of the conventional APFC. The MOSFET acts as a switch to stop or allow current flow from it’s drain to source.
MOSFET loss is heavily dependent on switching frequency. Though desirable to increase switching frequency for higher power density and smaller and cheaper magnetics, it also results in higher losses for MOSFETs due to an increased number of MOSFET switching in a given time period. Switching loss occurs when a MOSFET is turned on or off and is the result of a simultaneous positive switch current and drain-to-source voltage across the MOSFET. When MOSFETs are switched with non-zero values of current and drain-to-source voltage they are considered to be hard-switched. MOSFETs are considered to be soft-switching when they turn on or off with either zero voltage or zero current. Switching loss can be reduced by minimizing the time it takes to turn the MOSFET on and off [7][15].

MOSFETs also have a conduction loss which is independent of switching frequency. It is the result of the drain-to-source resistance of the MOSFETs. It can be calculated as:

\[ P_{con, m} = I_{ds}^2 R_{ds,on} \]  

(2.6)

Where \( R_{ds,on} \) is the resistance form the drain to source of the MOSFET and \( I_{ds} \) is the forward current flow through the MOSFET.

The boost diode is also found in the boost stage and needs to be a fast recovering diode in order to operate the circuit at a high switching frequency. This results in a diode with a higher \( V_f \) and therefore higher conduction loss [8].

There is one additional loss associated with the boost diode. This loss is called reverse recovery loss, and is an unwanted side-effect resulting from the stored charges in a conducting diode. If we apply a reverse voltage across the diode, current through the diode comes to zero value, and the diode continues to
conduct in the opposite direction because of the presence of stored charges in the depletion layer and the p or n layer. The reverse diode current flows for a period called reverse recovery time, $T_{rr}$. This is the time between when the instant forward diode current becomes zero and the instant reverse recovery current decays to 25% of its reverse maximum value [15].

![Diagram showing turn-off characteristics of a power diode.](image)

Figure 10: Turn-off characteristics of a power diode. A) Variation of the current $i_f$ B) Variation of the voltage drop $v_f$ C) Variation of the power loss [16].

Time $t_a$: Charges stored in the depletion layer removed.

Time $t_b$: Charges from the semiconductor layer is removed.

Total recovery time is $T_{RR} = t_a + t_b = \frac{2Q_{RRC}}{\sqrt{dI/dt}}$ (2.7)

Peak reverse current is $I_{RM} = t_a \cdot \frac{di}{dt} = \sqrt{2Q_{RRC} \cdot \frac{di}{dt}}$ (2.8)

Where reverse-recovery charge, $Q_{RRC}$, is the amount of charge that flow through the diode when diode changes its state from forward conduction mode to reverse blocking mode.
From a practical point of view, one is more concerned about the $T_{RR}$ and $I_{RM}$ which are clearly dependent on the stored charge $Q_{RRC}$ and the reverse applied $di/dt$.

While reverse recovery loss is not an issue with the MOSFET in the conventional PFC configuration (due to the fact that the body diode does not conduct), in a half-bridge orientation, the body diode will conduct and is susceptible to reverse recovery loss. This will be explored later on.

**Inductor Loss**

Inductor loss can be broken down into two types of losses; copper loss, and core loss. Copper loss is simply due to the electrical resistance of the copper windings (known as DCR) and is calculated in much the same way as the MOSFET conduction loss. Core loss is generated by the changing magnetic flux field within a material, since no magnetic materials exhibit perfectly efficient magnetic response [17]. Core loss density ($PL$) is a function of the peak AC flux swing ($B_{pk}=\frac{1}{2}B$) and frequency ($f$). It can be approximated from core loss charts or the curve fit loss equation:

$$PL = aB_{pk}^b f^c$$  \hspace{1cm} (2.9)

Where $a$, $b$, $c$ are constants determined from curve fitting, and $B_{pk}$ is defined as half of the AC flux swing:

$$B_{pk} = \frac{\Delta B}{2} = \frac{B_{ACmax}-B_{ACmin}}{2}$$  \hspace{1cm} (2.10)

Units typically used are (mW/cm$^3$) for $PL$, Tesla (T) for $B_{pk}$, and (kHz) for $f$. The task of core loss calculation is to determine $B_{pk}$ from known design parameters.

Once known, the core loss density is multiplied by the path length and the core cross-sectional area to get the core loss [18].
Inductor losses can be reduced by reducing the resistance of the copper windings, or by limiting core loss through faster changing flux magnetic cores or reducing switching frequency (which is undesirable for power density) [17].

**Output Capacitor Loss**

The loss associated with the output capacitor falls under a similar category as the loss in an inductor caused by the DCR. In a capacitor, this electrical impedance is known as Equivalent Series Resistance or ESR. Capacitor loss is calculated in the same manner as the copper loss for an inductor, i.e., multiplying the squared RMS current by the ESR. There is not too much to be done to limit the output capacitor loss apart from choosing a capacitive component with a low ESR value [15] [19].

2.3.2 PFC Modes of Operation

The boost stage of the PFC circuit can operate in three modes: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Critical Conduction Mode (CrCM). Figure 11 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for the same voltage and current conditions. By comparing DCM among the others, DCM operation seems simpler than CrCM, since it may operate in constant frequency operation, however DCM has the disadvantage that it has the highest peak current compared to CrCM and also to CCM, without any performance advantage compared to CrCM. For that reason, CrCM is a more common practice design than DCM. CrCM may be considered a special case of CCM, where the operation is controlled to stay at the boundary between CCM and DCM. CrCM usually uses constant on-time control; the line voltage is changing across the 60 Hz line cycle, the reset time for the boost inductor is varying, and the operating frequency will change as well in order to maintain the boundary mode operation. CrCM dictates the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle. The inductor current ripple (or the peak current) in CrCM is twice of the average value, which
greatly increases the MOSFET RMS currents and turn-off current. But since every switching cycle starts at zero current, and usually with ZVS operation, turn-on loss of MOSFET is usually eliminated. Also, since the boost rectifier diode turns off at zero current as well, reverse recovery losses and noise in the boost diode are eliminated too, another major advantage of CrCM mode. The high input ripple current and its impact on the input EMI filter tends to eliminate CrCM mode for high power designs unless interleaved stages are used to reduce the input HF current ripple [9] [12] [19]. A high efficiency design can be realized that way, but at substantially higher cost. The power stage equations and transfer functions for CrCM are the same as CCM. The main differences relate to the current ripple profile and switching frequency, which affects RMS current and switching power losses and filter design. CCM operation requires a larger filter inductor compared to CrCM. While the main design concerns for a CrCM inductor are low HF core loss, low HF winding loss, and the stable value over the operating range (the inductor is essentially part of the timing circuit), the CCM mode inductor takes a different approach. For the CCM PFC, the full load inductor current ripple is typically designed to be 20-40% of the average input current [9] [12]. This has several advantages:

- Peak current is lower, and the RMS current factor with a trapezoidal waveform is reduced compared to a triangular waveform, reducing device conduction losses.
- Turn-off losses are lower due to switch off at much lower maximum current.
- The HF ripple current to be smoothed by the EMI filter is much lower in amplitude.

On the other side, CCM encounters the turn-on losses in the MOSFET, which can be exacerbated by the boost rectifier reverse recovery loss due to reverse recovery charge, Qrr. For this reason, ultra-fast recovery diodes or silicon carbide Schottky Diodes with extreme low Qrr are needed for CCM mode [19].
2.4 Improved APFC Topology

In a bridgeless PFC, the bridge diode losses can be eliminated so efficiencies of 99% or higher are made possible to meet highest efficiency standards. Various bridgeless PFC topologies have been proposed to overcome the high diode bridge losses. One of the most popular is the 2-Phase Bridgeless PFC. This topology, shown in Figure 12, is essentially two boost legs with each one taking control during each half of the AC cycle. S1/S2 are typically superjunction MOSFETs and D1/D2 can be diodes, or for higher efficiency, SiC diodes. It has, in the past years, been the popular bridgeless PFC topology on the market because it is easy to implement using conventional Si MOSFETs with control similar to a standard PFC circuit, and efficiency is improved as it eliminates one diode from the current path [14] [20] [21] [22]. However, it comes with following drawbacks:
• Low power density and component utilization: it doubles the part counts and each one of the boost stages only works during one half cycle, which reduces the power density and adds to the bill of materials cost.

• Additional return diodes: for EMI purpose, diodes D3/D4 are needed to provide a return current path and reference DC link ground to N to reduce the common mode noise [7].

• D1/D2 needs to be fast SiC diodes: higher VF (conduction loss) and relatively higher cost than AC rectifier diodes.

• Complicated current sensing circuit: S1/S2 body diodes and D3/D4 share the return current.

• No bidirectional capability: This PFC topology cannot be utilized in applications that require bidirectional power flow between AC and DC ends. Due to the aforementioned high reverse recovery loss D1/D2, cannot be replaced by MOSFETs.

Because of these issues, outlined above, particularly the complex sensing circuits, and the high component count, the 2-Phase Bridgeless PFC is not a suitable design for the first stage of the data centre power supply, and the requirements of this thesis.
2.5 Bridgeless Boost Totem-Pole PFC Topology

Another bridgeless PFC structure is the Bridgeless Boost Totem-Pole PFC (BTPPFC), Figure 13(a). This topology can be considered as a conventional boost PFC in which one half of the diode bridge is replaced by active switches S1 and S2 in a half bridge configuration, hence the name “totem-pole”. The diode D1/D2 forms the slow 50/60Hz line frequency leg which can either be slow AC rectifier diodes or can be replaced by low-RDS(on) synchronous (SR) MOSFETs for improved efficiency, as shown in Figure 13(b).

The BTPPFC overcomes many issues which existed in the 2-phase bridgeless PFC and has the following advantages:

- Improved efficiency: main current only flows through two switches at a time. S1/S2 are driven synchronously with complimentary PWM signals and the S3/S4 on the slow line frequency legs can be low RDS(on) Si MOSFETs to further reduce the conduction loss.
• Lower part counts, higher power density and lower bill of materials cost. It uses fewer parts and has a simpler circuit: It needs only one inductor and neither SiC diodes nor AC return diodes are required.

• Bidirectional power flow. BTPPFC is inherently capable of bidirectional operation, which is ideal applications which may require power flow in both directions, such as Energy Storage Systems (ESS) and On-board Bidirectional Battery Chargers (OBBC).

BTPPFC is not a new topology and has been proposed before, however, its application has been very limited until recently. The major challenge is the poor reverse recovery performance of conventional silicon MOSFETs in the half bridge configuration, which makes CCM operation impractical due to the excess Qrr loss at turn-on. To avoid body diode conduction, BTPPFC with silicon MOSFETs must work in CrCM/DCM modes, which only fits for lower power and has more complicated control. Usually, multi-phase interleaved configurations are used to get higher power levels and improved current ripple, which again adds extra cost and complexity [14].

The absence of a body diode (zero Qrr) and the fast switching nature of GaN make a GaN HEMTs a good fit for CCM hard switching half bridge power stage. As can be seen in Figure 14(a), Qrr measured using standard test methods include both Qrr of the high side body diode and Qoss of the MOSFET, though Qrr usually dominates for Si MOSFETs. By contrast, GaN exhibits significantly lower hard turn-on loss as there is only Qoss loss – the loss induced at hard switching device during turn-on due to the output capacitance charging current of free-wheeling switch [13].
Table 1 compares the switch-on loss caused by $Q_{rr}$ (or $Q_{oss}$ for GaN) between a silicon MOSFET and a GaN E-HEMT device from GaN Systems. GaN has zero $Q_{rr}$ and its output capacitance charge can be more than an order of magnitude smaller than 650 V silicon MOSFETs. Even compared to CoolMOS CFD with an ultra-fast body diode, GaN shows much superior reverse recovery performance. Assuming a CCM BTPPFC operating at 50 kHz, GaN dissipates 0.75 W switching loss due to the $Q_{oss}$ loss at turn-on, while a similar CoolMOS CFD2 has about 20 W at switch-on because of the $Q_{rr}$ alone [14]. This excellent hard switching performance makes GaN HEMT the perfect candidate for CCM BTPPFC design.

<table>
<thead>
<tr>
<th></th>
<th>Si CoolMOS CFD2 with Fast Body Diode IPW65R080CFD</th>
<th>GaN HEMT GS66508B</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(ON)}$</td>
<td>80</td>
<td>50</td>
<td>mΩ</td>
</tr>
<tr>
<td>$Q_{BR}$</td>
<td>1000</td>
<td>0</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{OSS}$ @ $V_{DS} = 400V$</td>
<td>318</td>
<td>57</td>
<td>nC</td>
</tr>
<tr>
<td>Turn-on loss due to $Q_{rr}/Q_{OSS}$ @ $f_{sw} = 50kHz$</td>
<td>20</td>
<td>0.75</td>
<td>W</td>
</tr>
</tbody>
</table>

Table 1: $Q_{rr}/Q_{oss}$ loss comparison of 650V GaN HEMT vs. Si CoolMOS [14].

The zero $Q_{rr}$ of GaN makes the totem-pole bridgeless PFC practical. It meets the demand for increasing power density of switched-mode power supplies by adopting high switching frequency while not increasing the switching losses associated with pulse width modulated (PWM) converters. The BTPPFC
topology with GaN HEMTs and SR MOSFETs meets all of the outlined criteria for a high efficiency, high power density, and low component count design for the PFC stage of the data centre power supply. It is for this reason that the selected design will utilize the BTPPFC topology with CCM operating conditions.

2.5.1 GaN HEMT Technology

It has been stated that the theoretical performance of GaN switching technology is 3000 times better than that of traditional Si switching technology. This is primarily due to the combination of several factors: better performance at high voltages, faster switching characteristics, higher power density, and cheaper fabrication when scaled up [5]. The GaN switches offers the opportunity to significantly improve the efficiency and power density of a PFC Boost converter. However, direct replacement of conventional MOSFET with GaN switches cannot unleash the full potential of a GaN switch. GaN switches have unique characteristics that need to be treated differently. This is in part due to the structure of the technology. HEMTs operate on the same principle as a MOSFET, with an electric field applied on the gate terminal of the device which is used to vary the current flow through the drain and source terminals. The difference with the technologies is that HEMTs make use of a heterojunction as the channel between drain and source instead of a doped semiconductor region. The benefit of this is that electrons can move quickly through the heterojunction without colliding with any impurities that are used to dope a semiconductor. This results in a channel with high electron mobility and low resistivity [47].

There are multiple challenges associated with GaN switching technology and the BTPPFC topology which need to be overcome in order to achieve the objectives of this thesis. The following summarizes the problems and the proposed methods to solve these problems.
2.5.2 Challenges of Designing with GaN

**Accurate Gate Driver Supply Voltage**

One major concern of using a GaN switch is stringent gate voltage versus the conventional Silicon MOSFET [5]. A conventional Silicon MOSFET has a maximum gate to source voltage of +20V. However, the maximum gate to source voltage with a GaN switches is about 7V [13]. On the other hand, gate voltage should be higher than 5V to fully turn-on a GaN switch. This is a very narrow voltage band, comparatively, and so the gate voltage should be precisely controlled. A voltage regulator is needed to convert the unregulated supply voltage to a tightly regulated voltage.

<table>
<thead>
<tr>
<th>Gate Bias Level</th>
<th>GaN Systems</th>
<th>Si MOSFET</th>
<th>IGBT</th>
<th>SiC MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Rating</td>
<td>-10/+7V</td>
<td>+/-20V</td>
<td>+/-20V</td>
<td>-8/+20V</td>
</tr>
<tr>
<td>Typical Gate Bias Values</td>
<td>0 or -3/+5-6V</td>
<td>0/+10-12V</td>
<td>0 or -9/+15V</td>
<td>-4/+15-20V</td>
</tr>
</tbody>
</table>

*Table 2: Gate bias voltage comparison for the different semi-conductor switching technologies [13].*

**High Side Driver Constraints**

When driving GaN FETs, the dead-time generally hurts the overall efficiency of the converter. The reason is that the GaN devices have no standard anti-parallel diode (only majority carriers are involved in GaN device conduction) so there is zero recovery time and a reverse forward drop higher than the one in reverse diode for the Silicon MOSFET.

The dead time should be as short as possible to minimize the extra loss and it should also be long enough to avoid shoot-through. In order to provide such an accurate dead time, the propagation delay matching between high-side and low-side is a parameter of concern. Generally keeping it in a range of 2 ns or less is enough to prevent the shoot-through in the circuit. The optimum dead time changes with
input and output conditions and components tolerance. In the conventional design, the dead time is usually designed to meet the worst-case condition, which sacrifices the efficiency [13].

Spurious Turn-On Due to High DV/DT

The presence of really fast dV/dt (that can reach peaks of 30 kV/μs) together with the unfavourable ratio between gate drain capacitance and gate source capacitance (low Ciss and Vg(th)) increase the risk of Miller turn-on and direct conduction of the half bridge leg to dangerous levels.

The high dv/dt voltage change on the switching node induces a large charging current between the drain and the gate terminals of a GaN switch [5] [13]. This charging current can lift the gate voltage when it is supposed to be pulled down by a gate driver. As a result, both high and low side GaN switches will turn on which causes a surge current to shoot through from high to low side GaN switches and damage them.

Parasitic Inductance Between Driver and Gate/Source of GaN

Parasitic inductances between the leads of the driver to the gate and source of GaN switches can lead to ringing in the gate drive signal, reliability issues, and switching losses. This is primarily due to the Miller Effect current at turn-off and turn-on, Figure 15(a/b) respectively. Gate drive impedance (Rg and Lg) is critical for turn-off, but less so at turn-on [6] [5] [13].
During turn-off: Lg must be kept as low as possible to avoid ringing, while Rg must also be kept low to provide a strong pull-down voltage on the gate to prevent false turn-on.

During turn-on: maintain a low Lg but a reasonably high Rg to limit gate oscillations while ensuring that Vgs-pk does not exceed the absolute minimum gate voltage (-10V) or else the device may be damaged.

There must be a balance for the Rg value, such that it is low enough to provide a strong pull-low during turn-off, but high enough to limit oscillations, while not being too high as increased Rg yields increased switching losses.

2.5.3 Challenges with the Selected Topology

**Ideal Diode Emulation**

In the totem-pole bridgeless PFC, synchronize rectifier MOSFETs are used. One common issue with SR operation is reverse current conduction under light load conditions [23]. As the high side duty cycle, D_H and low side duty cycle, D_L are arranged in a complementary manner, the inductor current will increase toward negative after it reaches zero, as shown in Figure 16(b). Light load ideal diode emulation aims to turn-off the conducting MOSFET when the inductor current approaches zero. It should also be noted that negative inductor current under light load unnecessarily increases the conduction loss.
AC Input Current Spike During Vac Zero-Crossing

With the totem-pole bridgeless PFCs shown in Figure 13(b), a high current spike might be induced during input AC voltage zero-crossing. For example, when Vac is at positive half line cycle right before the zero-crossing, the switch Q4 is always on, and the duty cycle of Q1 is almost 0%. Immediately after Vac goes to negative half line cycle, the switch Q4 is turned off, and the duty cycle of Q1 abruptly increases to almost 100%. Therefore, the DC bus voltage is applied to Q4 (Vac is almost zero) suddenly and reversely biases its body diode with a high current spike [23] [24]. Similarly, the DC bus voltage reversely biases the body diode of Q3 with a high current spike when Vac changes from negative half line cycle to positive half line cycle.
Better Dynamic Response

To reduce total harmonic distortion (THD), the feedback loop of a PFC is forced to be designed with very narrow bandwidth, such as 5 – 10Hz. Thus, an existing PFC responded very slowly to a transient condition, particularly to the AC input voltage disturbance. The output voltage will deviate from the desired range, which adds extra difficulty to design the second stage DC – DC converter in a server power supply [9] [11]. A digital control algorithm can be developed to improve the transient response of the PFC while at the same time maintaining a low THD.

Thermal Analysis and Management

In order to achieve higher power density, the PFC will be designed with smaller size. One of the key design considerations is to avoid hotspots, which can deteriorate the reliability of the PFC. The likely component candidates that will be a focus for hotspots under operation are the high frequency GaN switches and the inductor. Different thermal strategies for GaN device package and PCB layout will be proposed and evaluated using an experimental prototype.
Chapter 3 - Design of Bridgeless Boost Totem-Pole PFC

3.1 Basic Operating Principle

The selected PFC circuit is shown in Figure 18. Switches S1 and S2 are GaN HEMT devices that are arranged in a half-bridge totem-pole structure. Being in this structure means that the PWM signal to the two devices are complimentary, with only one device turned-on at a time. When one device is operating at duty cycle with on-time, $D$, in a switching cycle, the other device will have duty cycle with on-time, $1-D$, turned on after duration $D$.

![Figure 18: The selected PFC circuit.](image)

Switches S3 and S4 are n-channel MOSFETs that act as voltage rectifiers for the AC sinusoid input voltage. This being the case, only one switch is on at a time, depending on the input half-cycle. Vac is the input sinusoid voltage source with L representing the line voltage and N representing the neutral voltage. The + and – symbols represent the terminal polarity of the AC source and help to indicate the flow of current in the circuit (from + to -). Finally, Vout is the 400V output voltage bus with respect to ground.
The BTPPFC operates in two modes depending on the polarity of the AC input voltage and is comprised of four intervals of operation. The intervals of operation are labelled on Figure 20 and described after it.

**Figure 19:** Complimentary duty cycle operation for high and low side GaN switches [25].

**Interval 1 - Positive line cycle inductor charging mode**

Referring to Figure 20(a): During the positive half line cycle (line > neutral), S2 is the main switch and S1 is driven with a complementary PWM signal. S1/S2 and L1 form the boost DC/DC stage. During this positive half cycle, half bridge leg S4 is turned on and S3 is always inactive. During the time when the main switch S2 is turned on, current flows from L1->S2->S4 and back to N. In this interval, the inductor,
L1, is charging current while the output capacitor, \( C_L \), discharges to maintain a regulated voltage at the output.

**Interval 2 - Positive line cycle inductor discharging mode**

Referring to Figure 20(b): Still in the positive half line cycle, during the period of \((1-D)\) when \( S_2 \) is turned off, \( S_1 \) is turned on and current flows through \( S_1 \) and back to \( N \) via \( S_4 \). In this interval, the inductor, \( L_1 \), is discharging current to the output while the output capacitor, \( C_L \), charges voltage.

In positive half line cycle operation (intervals 1 and 2) the DC bus ground \( V_{DC-} \) is tied to \( N \) potential as \( S_4 \) is conducting all the time. Intervals 1 and 2 repeatedly loop for the duration of the positive half cycle.

**Interval 3 - Negative line cycle inductor charging mode**

Referring to Figure 20(c): During negative half line cycle (neutral > line), the operation in the negative half cycle is similar except the role of top and bottom switches are swapped. Now \( S_1 \) becomes the main switch and \( S_2 \) is free-wheeling, and \( S_3 \) is turned-on leaving \( S_4 \) inactive. During the time when the main switch \( S_1 \) is turned on, current flows from \( L_1 \rightarrow S_3 \rightarrow S_1 \) and back to \( L \). In this interval, the inductor, \( L_1 \), is charging current while the output capacitor, \( C_L \), discharges to maintain a regulated voltage at the output.

**Interval 4 - Negative line cycle inductor discharging mode**

Referring to Figure 20(d): Still in the negative half line cycle, during the period of \((1-D)\) when \( S_1 \) is turned off, \( S_2 \) is turned on and current flows through \( S_3 \) and back to \( L \) via \( S_2 \). In this interval, the inductor, \( L_1 \), is discharging current to the output while the output capacitor, \( C_L \), charges voltage.

In negative half line cycle operation (intervals 3 and 4) the DC bus \( V_{DC+} \) is tied to \( N \) potential as \( S_3 \) is conducting all the time. Intervals 3 and 4 repeatedly loop for the duration of the negative half cycle.
3.2 Control Method

Since CCM operation was chosen for this design, average current mode control will be used as it is the most convenient method for achieving a CCM operation PFC [9] [11] [14] [26]. As mentioned in the literature review, power factor is defined as the ratio between AC input’s real power and apparent power. Assuming that the input voltage is a perfect sine wave, PF can be defined as the product of current distortion and phase shift. Therefore, the PFC control loops’ tasks are:

- **Control the Inductor Current**, which makes the current sinusoidal and maintains the same phase as the input voltage.
- **Control the Output Voltage**, which makes the output voltage equaled to target value.

![Figure 21: Control scheme for the BTPPFC.](image)

PFC arithmetic can be divided into three parts:

- **Voltage outer loop**, which insures the output voltage follows the reference-constant voltage output.
- **Reference arithmetic**, which insures that the current reference follows the sine reference.
- **Current inner loop**, which insures the input current follows the given current reference.

In analog arithmetic, the input voltage sample is introduced as the input current’s reference, so the ripple voltage is introduced to current control at the same time.

\[ i_{ref} = \frac{V_{ac}V_c}{V_{rms}^2} \]  \hspace{1cm} (3.1)

Where:

\( V_{ac} \) is the input voltage involved to ensure the current wave follows the input voltage wave.
$V_c$ is the output of voltage regulator

$V_{\text{rms}}$ is the RMS value of input voltage

The measured signals are DC output voltage $V_{dc}$, inductor current $i_L$, and input voltage $V_{acL}$ and $V_{acN}$, as seen in Figure 22. From above, the input current reference can be obtained by multiplying the output of the voltage regulator with the rectified value of the AC input voltage and divided by the square of input AC RMS voltage. The output from the current loop drives the PWM modulator to generate the gate signals. Therefore, the line current can be tracked to the input voltage waveform as shown in Figure 23.

Figure 22: Overall control block diagram [14].
3.3 Component Selection for the Power Circuit

In order to determine the main power component values, and eventually selection, for the PFC circuit, the design specifications first have to be determined. Table 3 provides all of the specifications for the power stage of the BTPPFC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (RMS)</td>
<td>180-220V</td>
</tr>
<tr>
<td>Input Current (RMS)</td>
<td>2.7A (max)</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>400V</td>
</tr>
<tr>
<td>Output Power Steady State</td>
<td>600W (max)</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>100kHz</td>
</tr>
<tr>
<td>Inductor Current Ripple</td>
<td>25% at full load</td>
</tr>
<tr>
<td>Output Voltage 120Hz Ripple</td>
<td>10Vpk-pk</td>
</tr>
<tr>
<td>Power Factor</td>
<td>&gt; 0.95</td>
</tr>
<tr>
<td>Current THD</td>
<td>10% (max)</td>
</tr>
<tr>
<td>Efficiency</td>
<td>Target 99%</td>
</tr>
</tbody>
</table>

Table 3: Specifications for the power stage of the BTPPFC design.

Figure 24 shows the schematic of the power circuit which houses all of the main power related components of the selected design. The addition of several components not seen in Figure 19 should be noted. These components include input filter capacitors and a common-mode choke, a bridge rectifier, a flux gate, and a relay with a parallel connected power resistor.
Figure 24: Altium schematic for the entire power stage of the BTPPFC design.

The input filter components are to eliminate any high frequency harmonics coming from the mains and prevent them from entering the PFC circuit. The values of the input filter capacitors were selected from a similar PFC design, and the choke selection as well [11]. The flux gate is a magnetic field sensor which makes use of the Hall-effect to sense the magnitude of the current through the inductor. Further discussion and selection of this device will be outlined in a later section of this thesis. The bridge rectifier (Bridge1), power resistor (R1) and relay (K1) are used during start-up of the PFC with the rectifier and resistor being shorted out by the relay once steady-state has been achieved. Their selection is outlined below along with the selection for the inductor, output capacitor, SR MOSFETs, and GaN switches.

3.3.1 Inductor Selection

The PFC filter inductor value and its maximum current are determined based on the specified maximum inductor ripple as shown:

\[
L = \frac{1}{%\text{ripple}} \frac{V_{ac, min}^2}{P_0} \left(1 - \frac{\sqrt{2}V_{ac, min}}{V_o}\right) T = \frac{1}{0.25 \times 600W} \left(1 - \frac{\sqrt{2} \times 180V}{400V}\right) \frac{1}{100 \times 10^3 Hz} = 785 \mu H
\]

(3.2)

\[
I_{L,max} = \frac{\sqrt{2} P_0}{V_{ac, min}} \left(1 + \frac{%\text{ripple}}{2}\right) = \frac{\sqrt{2} \times 600W}{180V} \left(1 + \frac{0.25}{2}\right) = 5.3 A
\]

(3.3)

With this, the inductor saturation current must be rated for greater than 5.3A and have a minimum of 785\(\mu H\). This value is atypical for common inductor manufacturers, so a more standard value for
inductance of 820μH was chosen. The Bourns 1140-821K-RC inductor with a ferrite core and 7.2A saturation current was selected [27].

3.3.2 Output Capacitor Selection

The output capacitor was sized to meet both of the hold-up time or the AC line voltage period of 16.6ms, and the low frequency voltage ripple requirements. The capacitor value is selected to have the larger value among the two equations in below:

\[ C_o \geq \frac{2P_{hold}}{V_o^2 - V_{o,min}^2} = \frac{2 \times 600W \times 16.6ms}{400V^2 - 340V^2} = 448\mu F \]  \hspace{1cm} (3.4)

\[ C_o \geq \frac{P_o}{2\pi f_{line} \Delta V_o V_o} = \frac{600W}{2\pi \times 60Hz \times 10V \times 400V} = 398\mu F \]  \hspace{1cm} (3.5)

\( C_o \) must be greater than 448μF, so a common capacitance value of 470 μF was selected. The Nichicon LGX2H471MEC58 electrolytic capacitor, rated for 500V was selected [28].

3.3.3 SR MOSFET Selection

The requirements for the SR MOSFETs are solely related to the maximum switching voltage in the design (400V) as well as the maximum conducting current, which was calculated above to be 5.3A. However, in order to maximize the efficiency of the PFC design, a power transistor with a low drain source resistance was selected. For this application, the Infineon 600V CoolMOS IPB60R099C6 transistors were selected due to their high continuous drain current of 37.9A and low \( R_{ds,on} \) of 90mOhm at room temperature [29].

3.3.4 GaN Switch Selection

It was already known going into this design process that the GaN switching devices would be products from GaN Systems. GaN Systems offers a variety of enhancement-mode high electron mobility transistors (HEMT) at the 650V level. The GS66504B 650V devices were originally chosen for the design.
as they offer a high enough drain-source current rating (15A) and low $R_{\text{ds(on)}}$ (100mOhm) with a bottom cooling package design that would eliminate the need for a heatsink [30].

Later on, in the design process it was discovered that the bottom cooling was insufficient for this application so a top cooled package in the 650V product range was chosen. The GS66506T devices were selected and offered a higher drain-source current rating (22.5A) and a lower $R_{\text{ds(on)}}$ (67mOhm) for even higher efficiency performance [31]. The details of this component selection and design change will be expanded upon later on in this thesis.

3.3.5 Relay, Power Resistor, and Diode Bridge Selection

The diode bridge rectifier (Bridge1) needed to have a high enough peak reverse voltage to ensure it doesn’t break down and reverse current flow during start-up while also being robust enough to potentially handle the full load current during a full-load start-up condition. Additionally, the diodes must have a lower voltage drop across them than the body diode drop from the GaNs (less than 1.67V) to ensure that the high start-up current does not pass through the GaN switches. For easy soldering, a through hole package was chosen. The component is the KBP06G from Diodes Incorporated. It has a 600V peak reverse voltage, 1.1V forward voltage drop, and 1.5A average rectified current which satisfies the full-load condition [32].

The power resistor ($R_{\text{20}}$) in the neutral terminal path ensures that the current spikes through the SR MOSFETs are limited so as to not damage them. A small resistance value with a high enough power rating is suitable. For this application, a resistance of 10Ohm with a rating of 50W was selected. The component is the NHS2B-10RJ1 from Riedon.

For the relay, the maximum current rating and the contact resistance determined this components selection. Since the relay shorts the power resistor and bridge during steady-state operation, the relay latch is constantly conducting the input line current. Therefore, it must be rated to at least the
maximum current of 5.3A. To reduce the conduction losses associated with this component, a relay with as low a latch resistance as possible was selected. The proposed relay (K1) is the G6C-2114P-US-P6CDC5 from Omron. It is rated for 10A continuous current and has a very low latch resistance of 30mOhm [33].

3.4 Preliminary Loss Analysis

To see if it is actually possible to achieve the targeted 99% efficiency with the selected design, a preliminary loss analysis of the main circuit components was performed using the datasheet specified electrical characteristics of the selected components.

It should be noted that a loss analysis was not performed for the input filter capacitors because the losses are small enough to be considered negligible, or for the choke because it was not necessary for the hardware tests performed on this design.

Loss analysis for switching devices is very complex for a PFC circuit in CCM operation due to the AC nature of the current through the switches. Under DCM or CrCM, due to the fact that the current tends to be zero at the turn-on of the Boost switch, as well as the turn-off of the Boost diode, the calculations are simpler. However, in CCM, this is not the case. In order to simplify the preliminary loss analysis, it was assumed that the circuit is operating in a purely boost converter (DC-DC) manner with CCM operation in steady-state, and under the worst case, highest loss, conditions. These conditions yield the largest input current, meaning the lowest acceptable input voltage, which gives Vin = 180V, Vout = 400V, and Pin = 600W.

These losses are calculated as follows:

3.4.1 Inductor Loss

**Inductor Copper Loss**

The inductor RMS current and the corresponding copper loss are:
\[ I_{L_{rms}} = \frac{P_o}{V_{AC_{min}}} = \frac{600W}{180V} = 3.33A \]  
(3.6)

\[ P_{L_{cond}} = I_{L_{rms}}^2 \cdot DCR = 3.33^2 \cdot 154\Omega = 1.707W \]  
(3.7)

**Inductor Core Loss**

In order to calculate the core loss, first, calculations for the minimum and maximum inductor current and the associated minimum and maximum magnetic force (H) have to be performed, then the fitted equation of that magnetic material is used to calculate the minimum and maximum magnetic flux (B). Finally, the AC flux swing can be used to calculate the core loss by using another fitted equation [18].

For the selected inductor:

Path length \( l_e = 5.3cm \) 
Cross Section area \( A_e = 0.654cm^2 \) 
Volume \( V_e = 3.466cm^3 \)

\( N = 40 \text{ turns} \)

The magnetic force at the peak of the line cycle can be found as:

\[ H_{\text{max}} = \frac{0.4\pi N I_{L_{max}}}{l_e} = \frac{0.4\pi 40(5.3A)}{5.3cm} = 50.27 \text{ oersteds} = \frac{4.01kA}{m} = -H_{\text{min}} \]  
(3.8)

The relative permeability of the ferrite core of the inductor is approximately 900 [34], so the specific permeability can be found using the relationship between relative permeability and the permeability of free-space:

\[ \mu = \mu_r \mu_0 = 900 \cdot 4\pi \cdot \frac{10^{-7}H}{m} = 1.134 \cdot \frac{10^{-7}H}{m} \]  
(3.9)

The flux density for the inductor material is:

\[ B_{\text{max}} = \mu H_{\text{max}} = 4.536\text{Tesla} = 45.36kGauss = -B_{\text{min}} \]  
(3.10)

\[ B_{\text{min}} = -4.536\text{Tesla} = -45.36kGauss \]  
(3.11)
The AC flux swing at the peak of the line cycle is:

\[
\Delta B = \frac{B_{\text{max}} - B_{\text{min}}}{2} = 4.536\text{ tesla} = 45.36 \text{ Gauss}
\]  

**Method 1:**

Peak core loss at the peak of the line cycle is [17] [18]:

\[
P_{\text{core, pk}} = \Delta B^2 \left(\frac{f}{10^3}\right)^{1.46} \cdot V_e \cdot 10^{-3} = 45.36^2 \left(\frac{60}{10^3}\right)^{1.46} \cdot 3.466 \cdot 10^{-3} = 0.117 \text{ W}
\]  

Average core loss across the line cycle is:

\[
P_{\text{core, ave}} = \frac{2P_{\text{core, pk}}}{\pi} = 75 \text{ mW}
\]  

**Method 2:**

The core loss density given by the curve fit equation is [17] [18]:

\[
PL = aB^b f^c = 62.65 \cdot 4.536^{1.781} \cdot 0.06 \text{ kHz}^{1.36} = \frac{20.17 \text{ mW}}{\text{ cm}^3}
\]  

The core loss then is:

\[
P_{\text{core}} = PL \cdot V_e = \frac{20.17 \text{ mW}}{\text{ cm}^3} \cdot 3.466 \text{ cm}^3 = 70 \text{ mW}
\]

Since the two methods are in close agreement to one another, the larger of the two will considered as the approximate core loss moving forward.

3.4.2 Output Capacitor Loss

With a dissipation factor of 0.15, the capacitor ESR loss is obtained as below:

\[
ESR = \frac{DF}{2\pi f C_o} = \frac{0.15}{2\pi \cdot 120 \text{ Hz} \cdot 470 \mu F} = 0.423 \Omega
\]
The capacitor RMS current across the 60Hz line cycle and the capacitor ESR loss can be calculated by the following equations:

\[
I_{\text{Corms}} = \sqrt{\frac{8\sqrt{2}P_o^2}{3\pi V_{\text{ACmin}}v_o^2}} = \sqrt{\frac{8\sqrt{2}\cdot 600W^2}{3\pi \cdot 180V \cdot 400V^2}} = 1.937A
\]

\[
P_{\text{Co}} = I_{\text{Corms}}^2 \cdot \text{ESR} = 1.937A^2 \cdot 0.423\Omega = 1.587W
\]

3.4.3 SR MOSFET Loss

Under the above conditions, only one SR MOSFET is active at a time and is undergoing only conduction loss with no switching losses. This should also be the case under normal PFC operation [45].

\[
P_{\text{SRcond}} = I_{\text{Lrms}}^2 \cdot R_{\text{DSon}} = 3.33A^2 \cdot 90m\Omega = 0.99W
\]

3.4.4 GaN Losses

**High Side Body Loss**

While operating in a purely boost manner, before the high side GaN turns on, the device is conducting similarly to a forward biased body diode. This loss is calculated as:

\[
P_{\text{Hbody}} = v_r I_{\text{Lrms}} f_{\text{con}} = 2.5V \cdot 3.33A \cdot 100kHz \cdot 200ns = 0.165W
\]

Where \(v_r\) is the reverse biased voltage drop that was found from Figure 25 below.
High & Low Side Capacitor Loss

During turn-on, the energy stored in the GaN switch’s output capacitance ($C_{oss}$) is dissipated. The amount of energy at this point is determined by the voltage across the device seen at turn-on. Figure 26 below shows this voltage, energy relationship. The voltage across the high-side GaN switch is equal to $V_{in}$ or 180V. This loss is:

$$P_{H_{loss}} = 1.33 \cdot 10^{-6} J \cdot 10^5 Hz = 0.133 W$$ (3.22)

The voltage across the low-side GaN switch is equal to $V_{in}$ or 400V. This loss is:

$$P_{L_{loss}} = 3.50 \cdot 10^{-6} J \cdot 10^5 Hz = 0.35 W$$ (3.23)
High & Low Side Switching Losses

The switching losses for the turn-on and turn-off of the GaN switches comes from the overlap of the voltage and current waveforms across and through the devices respectively. This overlap is due to the time duration it takes for the switch to turn-on, \( t_r \), and the time duration it takes for the switch to turn-off, \( t_f \) [15] [45].

For the high-side, this loss is calculated as:

\[
P_{Hton} = 0W
\]  

(3.24)

This is due to the fact that the high-side GaN switch is already conducting in the antiparallel “body diode” direction at turn-on

\[
P_{Htoff} = \frac{1}{2} V_{in} I_{rms} t_f = \frac{1}{2} \cdot 180V \cdot 3.33A \cdot 5 \cdot 10^{-9} s \cdot 100 kHz = 0.149W
\]  

(3.25)

For the low-side, this loss is calculated as:

\[
P_{Lton} = \frac{1}{2} V_{out} I_{rms} t_r = \frac{1}{2} \cdot 400V \cdot 3.33A \cdot 1.55 \cdot 10^{-8} s \cdot 100 kHz = 1.032W
\]  

(3.26)

\[
P_{Ltoff} = \frac{1}{2} V_{out} I_{rms} t_f = \frac{1}{2} \cdot 400V \cdot 3.33A \cdot 5 \cdot 10^{-9} s \cdot 100 kHz = 0.333W
\]  

(3.27)
Conduction Loss

Just like the conduction losses for the SR MOSFETs, the conduction loss for the GaN switches is can be found by the equation:

\[ P_{\text{Gcond}} = I_{\text{rms}}^2 \cdot R_{\text{DSon}} = 3.33A^2 \cdot 100m\Omega = 1.109W \]  

(3.28)

3.4.5 Relay Loss

The conduction loss for the relay is calculated as:

\[ P_{\text{Relaycond}} = I_{\text{rms}}^2 \cdot R_{\text{latc}} = 3.33A^2 \cdot 25m\Omega = 0.277W \]  

(3.29)

3.4.6 Total Power Loss

Summing the losses from the above components gives a reasonable estimate for the maximum theoretical efficiency of the design at full load, while operating at a worst case, minimum input voltage condition.

Total Loss = 7.95W

Efficiency (in %) = \( \frac{P_{\text{Out}}}{P_{\text{In}}} \times 100 = \frac{600 - 7.95}{600} \times 100 = 98.68\% = \sim 99\% \)  

(3.30)

It can be seen that the target efficiency of 99% is achievable with the selected components. Figure 27 below shows the percentage breakdown of the total losses for each type of loss associated with the main circuit components. Two of the largest losses come from the input inductor and output capacitor with approximately 20% of the total loss each. The next largest loss is the turn-on switching loss of the low GaN switch which equates to approximately 17% of the total loss. The low Gan turn-on switching loss is comprised of the low GaN turn-on overlap loss and the low Gan capacitor loss. Following this is the GaN conduction loss at around 14% of the total loss. The remaining smaller losses such as the SR
MOSFET conduction loss, turn-off switching losses for the high and low GaNs, turn-on switching loss for the high GaN and relay conduction loss make up the remaining 25% of the total losses. This analysis has been replicated for the entire range of acceptable input voltage conditions and can be found in a graphical form in Appendix A.

![Pie chart showing the percentage breakdown of the losses in the power stage.](image)

**Figure 27: Percentage breakdown of the losses in the power stage.**

3.5 Controller Selection and Circuit

Based on the control method mentioned above, a controller for this design must have the features outlined in the table below.
<table>
<thead>
<tr>
<th>Feature</th>
<th>Explanation with respect to the Control Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog-to-Digital Converter(ADC)</td>
<td>Line terminal input voltage sensing</td>
</tr>
<tr>
<td>ADC</td>
<td>Neutral terminal input voltage sensing</td>
</tr>
<tr>
<td>ADC</td>
<td>Inductor current sensing</td>
</tr>
<tr>
<td>ADC</td>
<td>Output voltage sensing</td>
</tr>
<tr>
<td>Digital Input</td>
<td>Input voltage polarity sensing</td>
</tr>
<tr>
<td>Digital Output</td>
<td>Relay control for steady state operation</td>
</tr>
<tr>
<td>Digital Output</td>
<td>Enable control for the GaN drivers</td>
</tr>
<tr>
<td>Digital Output</td>
<td>High side SR MOSFET control</td>
</tr>
<tr>
<td>Digital Output</td>
<td>Low side SR MOSFET control</td>
</tr>
<tr>
<td>Complimentary P WM Pair</td>
<td>High and low side PWM output for control of the GaN switches</td>
</tr>
</tbody>
</table>

*Table 4: Peripheral requirements of the digital controller for the BTPFPC design.*

Due to the familiarity and user friendliness of their products, a Microchip product was selected as the controller for this design. This component is the 16-bit microcontroller unit (MCU) dsPIC33FJ06GS101A [25]. It was selected for the following reasons:

- The device operates at 3.0V to 3.6V DC for low power consumption.
- It has a 16-Bit core with two 40-Bit Wide Accumulators, 32-Bit Multiply Support with up to 40 MIPS which is useful for higher precision, high speed calculations, and more accurate control.
- Features a low tolerance and accurate internal oscillator for clock reference as well as Programmable PLLs for clock customizability.
- Up to Three high-speed PWM Pairs with Independent Timing, specific Dead Time for Rising and Falling Edges and 1.04 ns of PWM Resolution for Dead Time, Duty Cycle, Programmable Fault Inputs, and Flexible Trigger Configurations for ADC Conversions. This small resolution is specifically important for this application as deadtime must be finely tuned to avoid shoot-through but also to limit losses and maximize the PFC efficiency.
• Up to 8 ADC input channels grouped into four conversion pairs with 10-bit resolution, Flexible and independent ADC trigger sources, and a Dedicated Result register for each. These ADC channel pairings allow for measurements to be taken almost simultaneously with each result saved to a specific register that can then be saved and altered later on in the control code. The customizable trigger sources are beneficial for synchronizing the voltage and current control loops to the PWM control.

• The Peripheral Pin Select (PPS) allows for function remap to suit the specific pin layout for the PCB design.

• Up to 13 analog or digital input/output (I/O) pins with external interrupts. The control for this design needs at least 5 I/O pins for various purposes and makes use of the external interrupt functionality for the input voltage polarity sensing as will be explained later on.

• In-circuit and in-application programming for quick code debugging and program upload to the device.

• Can be purchased in an easy to solder 18 pin SOIC package which has the exact number of pins for all of the inputs and outputs for the circuit control.

Figure 28 below shows the schematic and pin layout for the controller circuit. It is worth noting that all of the pins that have analog signal inputs have an external low pass RC filter network attached to them to filter out any high frequency noise that could yield unwanted measurements.
3.6 Detection/Sensing Circuits

The analog signal sensing circuits have to measure four quantities as mentioned above. These are the input AC voltage (between line and neutral), the inductor current, and the output DC voltage.

3.6.1 Input AC Voltage and Polarity

The input AC voltage ranges from 254-311V pk. In order to measure these voltages at the ADC of the controller, the voltage first has to be stepped down to a level suitable for the range of the ADC (0-3.3V). This is done by means of a voltage divider between 4Mohms and 27Kohms, with an additional parallel resistance to the 27Kohm for balancing the line and neutral voltages. With this voltage divider, the range is now:
\[ V_{\text{range}} = \frac{311 \times 27}{4027} = 2.085V \]  

(3.31)

Which is well within the limits of the ADC pin on the controller. Because the input voltage is alternating and tends to zero before crossing into it's negative half cycle, it is possible for the output of the voltage divider to see a slightly negative voltage. This can cause severe control errors and hurt the overall operation, so a small positive DC biasing voltage is connected to each of the output nodes of the voltage dividers. Refer to Figure 29(a). This is done by means of a stepped down 5V source via the following relationship:

\[ V_{\text{bias}} = \frac{5 \times 27}{1027} = 0.131V \]  

(3.32)

Yielding a new ADC voltage range of 0.131-2.216V to reflect the original 311V pk from the input.

Before the voltage signal from the output of the voltage divider reaches the ADC pin, each signal (line and neutral) goes through a voltage follower circuit which is comprised of a unity gain op-amp circuit. This voltage follower has very high input impedance that acts as a buffer to limit any current flow to the ADC pin of the controller which could potentially cause damage to the pin. This internal op-amp circuit can be seen in Figure 29(b).
To determine the polarity of the voltage at any given time, the line and neutral signals are additionally fed to the inputs of a comparator circuit which output either a logic high (around 3.3V) or a logic low (around 0V). When the line voltage is greater than the neutral voltage, the comparator outputs a logic high indicating the positive half cycle. When the neutral voltage is greater, the comparator outputs a logic low indicating the negative half cycle. From these logic highs or lows on a digital input pin of the MCU, it can always be known what half cycle the input voltage happens to be in. Figure 30 details the comparator circuit with the line and neutral signal inputs, and a square wave polarity output.
3.6.2 Inductor Current

Typical current sensing is done by means of a small resistor. By measuring the voltage drop across a known resistance, the current can be calculated. One major problem with this method is the conduction loss from the resistor. In order to achieve the targeted 99% efficiency, another sensing method without the inherent resistive loss needed to be used. The selected method for this design is to use a type of Hall-effect sensor known as a flux gate. Flux gates offer superior temperature characteristics (i.e., low drift), and accuracy when compared to other low loss current sensing methods like traditional Hall sensors.

The output of the flux gate is a voltage signal that is centred at 2.5V. This level corresponds to zero current through the flux gate. Depending on the direction of current flow, the voltage signal output changes linearly with respect to current. Refer to Figure 31 for the current to voltage relationship of the flux gate. In this specific application, the CASR6-NP was utilised with a two primary turn configuration to reduce the measurable current range and therefore increase the accuracy of the sensor. With this configuration the primary nominal rms current, $I_{PN}$, is 3A and has a maximum rms current, $I_{P(max)}$, of 10A [35].

![Figure 31: Current vs. voltage characteristics of the flux gate.](image-url)
Like the input voltage sensing, this output voltage range of 0.375-4.625V was too large for the ADC pin of the controller, so it had to be stepped down slightly by means of a voltage divider between 20Kohms and 39Kohms. This gives a new current range of:

$$V_{\text{cur, sense}} = \frac{V_{\text{old range}} \times 39}{20 + 39} = 0.248 \rightarrow 3.057V$$ \hspace{1cm} (3.33)

Which will reflect an inductor rms current reading from -10A to +10A with a zero-amp centre of 1.65V. Before the current sense voltage signal from the output of the voltage divider reaches the ADC pin, the signal goes through another two-stage voltage follower circuit that acts as a buffer to limit any current flow to the ADC pin of the controller, as well as reducing noise from the output of the flux gate sensor which could give erroneous current measurements. Figure 32 shows the inductor current sensing circuit. The ISNS tag connects directly to the output pin from the flux gate, refer to Figure 24 above.

![Inductor current sensing circuit.](image)

3.6.3 Output DC Voltage

The output voltage sensing circuit is much simpler when compared to the input voltage and inductor current sensing circuits. This circuit simply comprised of a voltage divider that feeds directly to the ADC pin of the controller. Because this voltage signal’s source shares the same system ground as the controller, a buffer circuit is not necessary. Figure 33 shows the output voltage sensing circuit.
Figure 33: Output voltage sensing circuit.

Under steady-state operation, the nominal output voltage is 400V which yields a voltage at the ADC pin of:

\[ V_{out, \text{sense}} = \frac{400 \times 10}{1510} = 2.650V \]  

This ratio of resistance in the voltage divider was specifically chosen as it leaves lots of room for output voltage overshoot (upwards of 500V) during start-up or step load conditions, that can still be registered by the ADC pin and hence provide reasonable data for the control algorithm to return the operation to steady-state.

3.7 Driver Selection and Circuits

Due to the many difficulties and constraints when working with GaN switches, as outlined above in the Section 2.5.1 literature review, special consideration had to be taken when selecting a driver for the GaN switches. The driver had to have dual outputs for the pull-high and pull-low signal that drive the GaN. This was necessary in order to tune the high and low gate resistances to eliminate any ringing or oscillations that might cause reliability issues or losses that are caused by the parasitic inductance between the driver and gate. Additionally, the driver had to have high isolation and common-mode transient immunity (CMTI) due to the fast switching and high dv/dt characteristics of GaN. It also had to
be compatible with the voltage driving requirements of GaN, i.e., a 6V pull-high and 0V pull-low reference. Finally, the selected driver had to have a low propagation delay, which is the time delay between the input PWM signal from the controller and the output gate drive signal to the switch [13]. The dual output SI8271GB-IS gate driver by Silicon Labs, with a very high CMTI of 400kV/us and a low propagation delay of 30ns, meets these requirements and was chosen as the gate driver for this design [36]. Figure 34 below shows the gate driver circuits for the high-side and low-side GaN switches.

Figure 34: Gate driver circuits for the high and low side GaN switches.

Unlike the gate drivers for the GaN switches, the gate drive requirements for the SR MOSFETs are much more lenient. The driver had to have a high input to output isolation as well as two independent isolated drivers (high and low) in a single package to reduce the number of components and the layout complexity. The dual driver package SI8230BB-D-IS-ND by Silicon Labs meets these requirements and was chosen as the gate driver for the SR MOSFETs [37]. Refer to Figure 35 for this gate driver circuit.

A higher gate voltage supply of 12V was selected as it yields a lower drain-source on-state resistance \( R_{ds(on)} \) for any given drain current [29]. This is important to minimize the conduction loss of the SR MOSFETs, therefore maximizing the overall PFC design efficiency. Additionally, for the high side gate voltage supply, the VDDA pin on the driver, the ground reference is directly connected to the neutral
terminal of the AC source which means that it is constantly changing or floating. In order to provide a positive 12V gate supply to this floating ground reference, a bootstrap circuit was used. The bootstrap capacitors (C66/67/68) are connected between the 12V the supply rail and the floating ground reference through a diode, to ensure proper current flow to charge the capacitors. Due to the charge storage characteristics of a capacitor, the bootstrap voltage will rise above the original 12V supply providing the needed gate drive voltage.

![Bootstrap Circuit Diagram](image)

*Figure 35: Gate driver circuit for the high and low side SR MOSFETs.*

3.8 Auxiliary Power Selection and Circuits

Based on the components selected for the PFC, the supplementary circuits to the power stage required multiple DC voltages to supply power for the various IC components in these circuits. These voltages are 12V, isolated 6V, 5V, and 3.3V. For simplicity, and to achieve the highest possible efficiency from the power stage of this PFC design, an external 12V power supply was planned to be connected directly to the PCB to provide this auxiliary power. From this input voltage, the other required voltages would be obtained from low power board mounted buck converters and LDOs.
To address the isolated 6V needed as a supply for the high and low side GaN drivers, two power supplies are needed. The chosen component for this application is the Recom R12P06S isolated DC/DC converter. It was selected due to its high isolation voltage and low isolation capacitance, as well as its high output voltage regulation accuracy and low output ripple which ensures an accurate turn-on voltage reference that will not cause damage to the GaN switches [38]. The low side reference has the 6V output grounded to the main power circuit ground, while the high side reference has the 6V output grounded to the floating voltage node after the inductor. It is this floating reference which necessitates the isolation between input and output of the supply. Figure 36 shows the 6V supply circuits for the GaN drivers.

![Figure 36: Isolated power supply circuits for the GaN gate drivers.](image)

To supply 5V needed for the various ICs including the flux gate, op amps, relay, drivers, and LDO, a non-isolated 12-5V DC/DC converter was selected. This component needed to have a small footprint but also deliver a reasonably large output current to satisfy the power draws from the more power intensive components like the relay. To meet these requirements, the chosen component is the VXO7805-500 from CUI as it can deliver up to 2.5W at the output or 500mA of current [39]. Figure 37 shows the 5V supply circuit which was suggested by the datasheet.
Finally, a 3.3V supply for the MCU and comparator was selected. Due to the very low power draw from these components, a low drop-out regulator (LDO) was chosen as it is simple and cost-effective for this application since it can regulate from the 5V supply. Figure 38 shows the 3.3V supply circuit with the AZ1084C-3.3 LDO component suggested by the datasheet [40].

3.9 Computer Simulations

Computer simulations were first performed with LTspice to verify the expected function of the more complex input voltage and polarity sensing circuits, as well as the inductor current sensing circuit. Next, the complete power stage of the PFC design, along with the sensing circuits and full closed loop control was simulated in Powersim to verify the proper function of the design and to refine the control algorithms and parameters.
3.9.1 Vac and Polarity Sensing Circuit Simulation

Figure 39: LTspice circuit simulation of the AC input voltage and polarity sensing.

Figure 39 above shows the LTspice circuit simulation for the input voltage and polarity sensing circuit. A 60Hz AC voltage source (V3) with a peak voltage of 311V pk connected to a diode bridge rectifier and load was used to ensure a proper current flow and approximate the loaded PFC circuit. The rest of the circuit, including the voltage divider resistance values, DC biasing, voltage followers, and comparator circuit are exactly the same as the originally designed sensing circuit.
Figure 40: Simulation results of the AC input voltage and polarity sensing.

From this simulation, it can be seen that the circuit will function as expected. The results yielded scaled input voltage waveforms well within the 0-3.3V range of the ADC input pin of the controller with a small positive biased voltage of around 130mV. The polarity waveform is a clean square wave also within 0-3.3V that is gives a logic high when the line terminal voltage is positive and a logic low when the neutral terminal voltage is positive. This verified the input voltage sensing and polarity circuit design.

3.9.2 Flux Gate Sensing Circuit Simulation

Figure 41: LTspice circuit simulation of the flux gate and input current sensing.
Figure 41 above shows the LTspice circuit simulation for the input voltage and polarity sensing. A 60Hz AC voltage source (V3) connected to a diode bridge rectifier and load was used to approximate the output voltage signal from the flux gate while undergoing a maximum AC rms inductor current through the component of 10A. Just like the previous simulation, the rest of the circuit is exactly the same as the originally designed inductor current sensing circuit.

From this simulation, it can be seen that the circuit will function as expected. The results yielded scaled flux gate output voltage waveforms well within the 0-3.3V range of the ADC input pin of the controller with a centred voltage, representing zero-amps, of 1.65V. This verified the flux gate current sensing circuit design.

3.9.3 Power Stage and Full Circuit Simulation
Figure 43 above displays the power stage circuit model used for the PSIM simulations. For simplicity, the input filter, and start-up components like the bridge rectifier, power resistor and relay have been ignored for the simulation as there is no worry about the physical limitations of the switches and other components in the simulation. The input voltage source has been set to 200Vrms, midway between the range of acceptable input voltage conditions, and a current source at the output acts as a variable load for the PFC circuit. Four MOSFETs are used to simulate the four switches in the BTPPFC topology. Switches 1 and 2 act as the high and low GaN switches, respectively, while switches 3 and 4 act as the SR MOSFET switches. The output capacitor and input inductor are set to the values of the design.

An equivalent version of the flux gate was implemented using a current sensor and voltage sensor with a reduced gain of 0.20433 to reflect the current/voltage relationship in the internals of the flux gate. This was then biased by a fixed voltage source to centre any signal at 2.5V, just like the reference voltage of the flux gate.

![PSIM circuit simulation of the voltage sensing circuits of the BTPPFC design.](image)

*Figure 44: PSIM circuit simulation of the voltage sensing circuits of the BTPPFC design.*
In keeping with the results from the LTspice models, the sensing circuits for the input voltage, output voltage, and polarity have been built according to the original circuit schematics.

Figure 45: PSIM circuit simulation of the digital c-block controller for the BTPPF simulation design.

The brains and control behind the simulation are done by a c-block controller, see Figure 45. The controller accepts various inputs and uses a program written in C language to provide the outputs that controls the power stage, just like the MCU will do in hardware. Apart from the known sensing signals, the c-block controller uses a square wave input to act as a system clock that can be used to set up the frequency of the current and voltage control loops. The outputs from the controller include two gate signals for switches 3 and 4, and three variables which are sent to the PWM generation circuit below in Figure 46.
These variables are PTPER, PDC1, and ENABLE. The variable names PTPER and PDC1 correspond to registers within the PWM module of the MCU that hold the integer values for the period and on-time of the duty cycle, respectively. Using the PWM circuitry, a constant integer on the PTPER output creates a PWM waveform with a period of 1ns multiplied by the PTPER value. In this manner a switching period representing 100KHz can be made. In a similar manner, the integer value on the PDC1 output creates an on-time with a duration of 1ns multiplied by the PDC1 value. The combination of these two values generate a variable duty-cycle PWM waveform to drive the high and low side GaN, switches 1 and 2. The ENABLE variable, depending on it’s value, can mask over the PWM waveform sent to the GaN switches. When ENABLE is set to “one”, the switches are driven by the desired PWM waveform generated by the control logic. When ENABLE is set to “zero”, both switches remain in a turned-off orientation. This action is used during the zero-crossings of the input voltage and current waveforms to ensure that the current does not oscillate in the positive and negative directions and is instead brought to zero like the input voltage waveform. This function reduces the current waveform noise around this region which can adversely affect PF and THD in the input current.
Description of C-Block Code

As mentioned above, the square wave clock input acts as a timer to determine when the control loop should sample the input pins for the voltage loop, reference arithmetic, and the current loop. The entire control structure runs off of an infinite “while” loop. The desired sampling and control loop frequency was to be half of the switching frequency, or 50KHz which is the same frequency as the clock input. When the clock input is high, the controller samples all of the inputs and stores them into variables, i.e., line and neutral AC input voltage, output voltage, AC input current, and the polarity. After this first sample, the output voltage is compared to the reference voltage then sent through a digital filter and PI feedback compensator to generate the voltage error, Vc. Next, the lesser of the line and neutral AC input voltages is subtracted from the greater, then multiplied with Vc, and their product is then divided by a constant Vrms^2 term to generate the current reference, Iref. Finally, the sampled input AC current is compared to the reference generated in the previous step and fed through another PI feedback compensator which outputs an integer that represents the on-time value of a PWM waveform. Before this value is sent to the PWM generation circuitry, the integer is clamped between 1% and 99% of the total period value (9579), or between 96 and 9483. This is to ensure that a valid duty cycle is sent to drive the GaN switches and does not cause an unwanted error. The last step is to utilise the polarity variable to determine the distribution of the duty cycle. When the input voltage is in the positive half cycle, with respect to the line terminal, the lower GaN switch acts as the Boost switch with the top as the Boost diode. When the input voltage is in the negative half cycle, the top GaN switch acts as the Boost switch with the lower as the Boost diode. Therefore, if the polarity variable is high, the PDC1 variable must be equal to the total period minus the integer representing the on-time from the current loop compensator. If the polarity variable is low, the PDC1 variable is exactly equal to the integer representing the on-time from the current loop compensator. The value stored in the PDC1 variable is then outputted to the PWM generation circuitry to drive the GaN switches.
This entire process is then repeated on the next logic high of the clock input, with the exception of the voltage loop which is only triggered every tenth sampling via a counter variable which keeps the voltage loop operating frequency at 5KHz. The output voltage loop is set at a high frequency to offer better performance under dynamic (step-load) conditions. This refers to a faster recovery of the system to steady-state operation after a sudden load change or perturbation. Traditionally, the bandwidth of the voltage loop is chosen to be 10Hz. This is selected to be well below the input frequency of 60Hz, so that the second harmonic ripple on the DC bus voltage is eliminated and the THD in the input current is reduced. To recreate this phenomenon, while operating at a higher frequency, a digital implementation of a dead-zone controller was used on the original output voltage error, before it is compensated by the PI controller. This dead-zone controller reduces the resolution of the sensed output voltage and places a higher weighting on the previous voltage error versus the current voltage error. By adding this filter, the error caused by the double line frequency ripple in the output voltage is virtually ignored, even while operating at this high loop frequency [41]. However, during a transient, the filter cannot ignore the error due to it’s larger magnitude and so the loop compensator can act as intended to quickly bring the system back to steady-state. Additionally, to aide in this quicker response, an algorithm was implemented within the PI controller structure to ignore the integral term and only act as a proportional controller during a transient occurrence. This algorithm relies on monitoring the magnitude of the voltage error. By operating with only proportional control, the system can respond faster to return to a more stable-state (smaller Verror) before reintroducing the integral term into the control structure [42] [43]. To reduce the AC current spike that can occur during the zero-crossing transitions, a soft-start function for the GaN switches was introduced similar to [24]. This function completely dictates the duty cycle for the GaN switches for a set period to slowly reach a maximum or minimum, depending on the switch and half line cycle, where the control loops take over again.
Also included in the c-block, is a function that slowly ramps up the output reference voltage to ensure a smooth start-up without causing instability. Additionally, there is control logic to provide an output signal to set the correct SR MOSFET high or low depending on the value of the polarity variable.

For a complete copy of the c-block code used in the simulation, refer to Appendix B.

**Selection of PI Parameters**

PI loop control is widely used and classical in industry control [11] [44]. In this application, the voltage and current loops adopt PI regulator arithmetic. Figure 47 represents the block diagram of the control structure in terms of its transfer functions.

![Block diagram of the control structure with regard to it's transfer functions.](image)

The gain constants $k_1, k_2, k_3,$ and $k_m$ are selected as:

\[
k_1 = \frac{1}{V_{DC}} = \frac{1}{400} = 0.0025
\]

\[
k_2 = \frac{1}{V_{ACmax}} = \frac{1}{\sqrt{2\times220}} = 0.00321
\]

\[
k_3 = \frac{1}{I_{ACmax}} = \frac{1}{5.33} = 0.187
\]

\[
k_m = \frac{V_{ACmax}}{V_{ACmin}} = \frac{311}{254.5} = 1.222
\]
The current compensator and resulting parameters are calculated and outlined below. The current loop bandwidth is chosen to be 10 kHz. This is selected such that the current accurately tracks the sinusoidal input voltage at 60 Hz. The current compensator ‘zero’ is placed by taking the digital delays into consideration. Therefore, for a phase crossover frequency of 10 kHz, the ‘zero’ placement is done well below this frequency. A frequency of 1000 Hz is chosen in this application for placing the current PI compensator ‘zero’.

The transfer function for the current error compensator is given by [44]:

\[
G_I(s) = k_{pi} + \frac{k_{li}}{s} = k_{pi} \left(\frac{1 + T_{co} \cdot s}{T_{co} \cdot s}\right)
\]

(3.39)

Where \(T_{co} = \frac{1}{2\pi f_z}\) and \(f_z\) is the location of the zero for the current PI controller

\[
G_I(s) = \frac{2\pi f_{BW}}{k_v V_{DC}} \cdot \frac{1 + T_{co} \cdot s}{T_{co} \cdot s} = \left(\frac{2\pi \cdot 820\mu H \cdot 10kHz}{0.187 \cdot 400}\right) \cdot \left(\frac{1 + 1.591E^{-4} \cdot s}{1.591E^{-4} \cdot s}\right)
\]

(3.40)

\[
G_I(s) = 0.689 \cdot \frac{1 + 1.591E^{-4} \cdot s}{1.591E^{-4} \cdot s}
\]

\[
G_I(s) = 0.689 + \frac{4329.34}{s} = k_{pi} + \frac{k_{li}}{s}
\]

\[
k_{pi} = 0.689, k_{li} = \frac{4329.34}{50kHz} = 0.0866
\]

The controller gain: \(k_{ci} = \frac{k_{li}}{k_{pi}} = 0.1257\)

(3.41)

To achieve an initial starting-point for the voltage error compensator parameters, it was designed to reflect the traditional approach with a very low frequency bandwidth of around 10Hz. This was done even though the actual voltage loop is operating at a much higher frequency of 5KHz because the dead-zone control filter before the voltage compensator allows this high frequency loop to mimic a much...
slower loop during steady-state operation. The voltage compensator ‘zero’ is the same as the voltage loop bandwidth, because at 10Hz, the digital delays are insignificant.

The transfer function for the voltage error compensator is given by [44]:

\[
G_V(s) = k_{pv} + \frac{k_{iv}}{s} = k_{pv} \left( \frac{1 + T_{co} s}{T_{co} s} \right)
\]  \hspace{1cm} (3.42)

Where \( T_{co} = \frac{1}{2\pi f_z} \) and \( f_z \) is the location of the zero for the voltage PI controller

\[
G_V(s) = \left( \frac{2k_2 k_3 k_m}{k_1} \right) \cdot \left( \frac{V_{DC}}{2 f_{cv}} \right) \cdot \left( \frac{1 + T_{co} s}{T_{co} s} \right)
\]  \hspace{1cm} (3.43)

\[
G_V(s) = \left( \frac{2 \cdot 0.00321 \cdot 0.187 \cdot 1.22}{0.0025} \right) \cdot \left( \frac{400}{1/2\pi \cdot 10 \cdot 470 \mu F} \right) \cdot \left( \frac{1 + 1.591E^{-2} \cdot s}{1.591E^{-2} \cdot s} \right)
\]

\[
G_V(s) = 6.927 + \frac{435.40}{s} = k_{pv} + \frac{k_{iv}}{s}
\]

\[
k_{pv} = 6.927, k_{iv} = \frac{435.40}{5kHz} = 0.0871
\]

The controller gain: \( k_{ci} = \frac{k_{ii}}{k_{pi}} = 0.01257 \)  \hspace{1cm} (3.44)

These initial values for the voltage and current loop kp and ki were implemented in the simulation and tuned, varying one term at a time, to yield the nicest shaped current waveform under various steady-state loads and also to yield a quicker response under step-load conditions.

**Closed Loop Simulation Results**

The final tuned values for the voltage and current loop kp and ki terms, taking their separate controller gains into consideration, are:
Voltage Error Compensation Parameters | Current Error Compensation Parameters
---|---
Proportional: $k_p = 0.09$ | Proportional: $k_p = 0.2$
Integral: $k_i = 0.001$ | Integral: $k_i = 0.015$

Table 5: Tuned compensation parameters that yielded the best simulation results.

With the tuned compensation parameter values, simulations were run to observe the start-up, steady-state, and dynamic performance of the PFC design.

**Start-up Performance**

*Figure 48: Start-up of the BTPPFC simulation model at 300W output load.*
Figure 49: Zoomed-in input current (top) and output voltage (bottom) waveforms of the start-up sequence above.

Steady-State Performance

Figure 50: Steady-state of the BTPPFC simulation model at 150W output load. Input current waveform on the top and input voltage and output voltage waveforms on the bottom.
Figure 51: Steady-state of the BTPPFC simulation model at 300W output load. Input current waveform on the top and input voltage and output voltage waveforms on the bottom.

Figure 52: Steady-state of the BTPPFC simulation model at 600W output load. Input current waveform on the top and input voltage and output voltage waveforms on the bottom.

For each loading condition in steady-state, the power factor and total harmonic distortion in the input current were analysed using the simulation tools in PSIM. Table 6 below summarizes these findings:

<table>
<thead>
<tr>
<th>Output Power (W)</th>
<th>Power Factor (PF)</th>
<th>Total Harmonic Distortion (THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>158</td>
<td>91.84%</td>
<td>31.12%</td>
</tr>
<tr>
<td>316</td>
<td>96.95%</td>
<td>15.52%</td>
</tr>
<tr>
<td>632</td>
<td>99.23%</td>
<td>6.47%</td>
</tr>
</tbody>
</table>

Table 6: Summary of the simulation PF and THD performance at various loading conditions during steady-state.
Dynamic Performance

It can be seen from the table and figures above that the control algorithm offers very good performance for start-up, steady-state, and dynamic conditions. During start-up, the output voltage quickly rises from the peak of the input line voltage in around 400ms and achieves nominal output after only 700ms after turn-on. Steady-state performance also offered good results, particularly between the half and full-load conditions. The output voltage waveforms are very stable, and the power factor is within the desired
range for the design. However, the input current waveform during light loading conditions did not achieve the targeted power factor. Additionally, the THD in the input current is far outside of the 10% requirements for the design with the exception of the full-load simulation. This large value of harmonics in the input current was likely caused by the discrete time nature of the calculations performed in the simulation as well as a lack of input filtering. The dynamic performance results meet and exceed the results from [11]. The simulated step change occurs for each test at 1s and lasts for only 1ms. During the 300-600W step change, the input current waveform stabilizes after approximately 125ms while the output voltage waveform stabilizes within 200ms of the step change. During the 600-300W step change, the input current waveform stabilizes after approximately 150ms while the output voltage waveform stabilizes within 200ms of the step change.
4.1 First Iteration PCB Design

For this Bridgeless Boost Totem-Pole PFC design, the AC input and DC output are both high voltage and high-power signals. Additionally, the control system is operating at high switching frequency of 100kHz with low magnitude feedback signals and very high dv/dt and di/dt switching that can cause noise. Because of these factors, the PCB layout needs to be well considered, especially for the following details:

- The input and output current loop routing.
- Distance considerations for the high voltage power loop.
- Heat dissipation for power components.
- The placement of noise absorption components.
- Distance considerations between the gate of the GaN switches and the GaN gate drivers.
- Power ground copper pouring and control system ground copper pouring to avoid influence by high frequency and high current signals.
- Routing method for the sensitive signals.
Figure 55: First iteration PCB layout as seen from the top side. Top layer is red, bottom is blue, all other coloured traces are internal.

Figure 56: First iteration PCB layout as seen from the bottom side.

In Figure 55,

Block 1 contains the signal sensing and control circuits;

Block 2 contains the input filter and EMC circuits;

Block 3 contains the power stage circuit for the design;
Block 4 contains the GaN switch gate driver circuits on the front and the SR MOSFET gate driver circuit on the back;

Block 5 contains the auxiliary power circuits.

The more sensitive circuits such as the detection and sensing circuits, as well as the control circuits, were kept isolated away from the high switching frequency and high-power traces of the power stage to reduce the impact of any EMI skewing the sensing and control signals. At the same time, the input AC voltage and current sensing were positioned between the input filter and EMC circuits and the digital controller.

The auxiliary power circuits, particularly the isolated 6V DC supplies were placed in close proximity to the GaN switch gate drivers that rely on their output. Being discrete supplies, there was no concern associated with EMI by placing them close to the power stage. The remaining supplies were placed next to the isolated supplies, but closer to the sensing and control circuits which make up the majority of the load for auxiliary power.

The input current traces for Line (cyan) and Neutral (magenta) in Figure 57, were done with wide copper pours to reduce resistance and thermal hotspots and arranged to bypass the sensing circuits when utilizing the top layer or run at least two layers below the top when necessary to run underneath the sensing circuits.
To reduce losses and noise from the high switching frequency, the high voltage switching loop of the power stage was oriented to limit the total distance travelled by the current through the four switches of the power stage. This loop starts from the DC output bus, through the GaN switches (Q4,5) to the power ground (cyan line), then back up through the SR MOSFET switches (Q1,2) to the DC output bus (magenta line). Refer to Figure 58 below.

High voltage ceramic capacitors, C31,32 and C30, C1071, are placed as close as possible to the high side GaN switch between it’s drain and the power stage ground, as seen in Figure 59. These ceramic
capacitors act to absorb the high frequency current spikes caused by the high $dv/dt$ switching characteristics of the GaN device and shunt these spikes to ground. The thermal pad of the GS66504B GaN device is shared with the source pad of the footprint. Because of this, large copper pours for the source pad were made to extend beyond the pad boundaries of the device footprint to provide more material for better thermal management.

*Figure 59: Absorbing capacitors, located immediately adjacent to the high side GaN switch.*

As mentioned above in Section 2.5.1, the GaN gate driver chip should be placed as close as possible to the GaN device, so that the loop for the drive signal to the gate pin, G, and the gate return path from the source pin, S, back to the driver should be as small as possible to limit unwanted inductance. This can be seen in Figure 60.
Figure 60: Gate signal traces between the isolated gate drivers and the GaN switches. High side on the left, low side on the right.

Being a high voltage power supply design, the grounding strategy is very important. An entire layer has been dedicated for the ground plane. Figure 61 shows the ground routing method. To limit circulating currents in the ground plane, the power ground, control ground and analog ground have all been separated into separate planes that are joined together with small traces. The power ground is divided between a large top layer plane and a midlayer plane that is connected to the dedicated ground plane with a large via in Figure 62.
The routing strategy for the sensitive signals from the MCU; PWM, ENABLE, etc., was to utilize a dedicated middle-layer to provide isolation and maintain the signal integrity even while running underneath the power stage components.
4.2 MCU Programming

As previously outlined, the control core of this design is the dsPIC33FJ06GS101A MCU. This low-cost controller has enough peripherals and features suitable for the implementation of a fully digitally controlled design of a Bridgeless Boost Totem-Pole PFC.

The programming for the controller is written in C language using the integrated development environment specifically designed by Microchip for its 8, 16, and 32-bit digital controllers, MPLAB IDE. The XC16 compiler tool, also designed by Microchip, was used to build and compile the control code for the controller. To upload the program to the controller, the ICD 3 hardware tool was utilized. This hardware tool connects to the DSC through a 6-pin jack on the PCB and to a
computer through a USB port and acts as an interface between the two in order to reprogram the controller or debug the current program on the controller.

This section describes the design of the software blocks, including software structure, configuration of the DSC peripherals, control timing, and implementation of the code. The majority of the programming, mainly the structure of the arithmetic for the PFC algorithm, was directly adopted from the c-block code written for the simulation. The specifics of the programming changes, which were done to ensure proper function with the DSC implementation, are outlined below in detail.

4.2.1 Parameter Normalization

In order to make full use of the DSC’s resources, all sensed physical quantities are normalized to a fixed-point decimal format, which is a Q15 format for this application.

The relationship between actual value of the physical quantity and its normalized value is shown as following:

\[
\text{Frac Value} = \frac{\text{Actual Value}}{\text{Quantization Range}}
\]  

(4.1)

Where,

- Frac value = the normalized value of the physical quantity
- Actual value = the actual value of the physical quantity expressed in units
- Quantization range = the maximum measurable value of this physical quantity

Once in this Q15 format, integer only arithmetic is performed according to the PFC control algorithm to determine the appropriate duty cycle based on the sensed conditions.
4.2.2 Program Control States

The control program operates in several states to control the system flow as in Figure 65. After a system reset, the DSC enters an infinite loop comprising of four control states. These are:

- **Initialization:** variable and peripheral initialization.
- **Wait:** the PWM output is disabled while the system is checking for the start conditions.
- **Run:** the PWM output is enabled and the control is working to achieve steady-state operation.
- **Fault:** the system faced a fault condition and the PWM output is disabled.

After the Initialization state, the application state machine continues into the wait state. The input voltage RMS is detected to see whether it satisfies the requirements. If this condition is met, along with the output voltage reaching a stable value, the output capacitor is charged enough to close the relay and continue into the Run state. In this state, the controller starts to take effect to achieve given output voltage and current according to load.

Under each state, if any fault is detected, the application state machine enters the Fault state. In this state, the software stays in a never-ending loop and the output of the converter is disabled. The system needs to power up again for a restart.
4.2.3 Clock and Peripheral Settings

Clock

The system clock signal for the MCU was set up using the internal oscillator and an internal PLL to operate the device at 80MHz which gives a processing speed of 40 million instructions per second (MIPS). Additionally, the auxiliary oscillator for the PWM and ADC peripherals was set up to its maximum of 120MHz as this maximum value is necessary to enable the PWM register to have a resolution of around 1ns. This high resolution in PWM signal is to lend a high degree of accuracy for the GaN drive signals to maximize efficiency and limit risk of shoot-through. The following block of c-code initializes the system clock and auxiliary PLL of the MCU to the parameters mentioned above:
void initClock(void)
{ /* Configure Oscillator to operate the device near 80Mhz
   Fosc= (N1*N2) / Fin*M, Fcy=Fosc/2
   Fosc= 7.37*(43)/(2*2) = ~80Mhz for Fosc, Fcy = ~40MIPS */

   /* Configure PLL prescaler, PLL postscaler, PLL divisor */
   PLLFBD = 41; // M = PLLFBD + 2
   CLKDIVbits.PLLPOST = 0; // N1 = 2
   CLKDIVbits.PLLPRE = 0; // N2 = 2

   //unlock sequence and clk set
   __builtin_write_OSCCONH(0x78);
   __builtin_write_OSCCONH(0x9A);
   __builtin_write_OSCCONH(0x01);
   //unlock sequence and initiate oscillator switch
   __builtin_write_OSCCONL(OSCCON | 0x0046);
   __builtin_write_OSCCONL(OSCCON | 0x0057);
   __builtin_write_OSCCONL(OSCCON | 0x0001);

   while(OSCCONbits.OSWEN == 1); // Wait for switch to be successful ie. FRC w/ PLL
   while(OSCCONbits.LOCK != 1); // Wait for PLL to Lock

   /* Now setup the ADC and PWM clock for 120MHz
   ((FRC * 16) / APSTSCLR ) = (7.37 * 16) / 1 = ~ 120MHz */

   ACLKCONbits.ASRCSEL = 0; // FRC Oscillator provides the clock for APLL
   ACLKCONbits.FRCSEL = 1; // FRC provides input for Auxiliary PLL (x16)
   ACLKCONbits.SELACLK = 1; // Auxiliary Oscillator provides clock source for PWM & ADC
   ACLKCONbits.APSTSCLR = 7; // Divide Auxiliary clock by 1
   ACLKCONbits.ENAPLL = 1; // Enable Auxiliary PLL

   while(ACLKCONbits.APLLCK != 1); // Wait for Auxiliary PLL to Lock

   return;
}

PWM

The dedicated high speed PWM1 module generates two complementary PWM signals with a constant frequency of 100kHz and variable duty cycle. The generated PWM signals are routed to the gate drivers for the generation of GaN drive signals. The TRIG1 register value and the TRGCON1bits.TRGDIV compare event is used to generate the 50kHz interrupt routine for the inner current loop. The following block of c-code initializes the PWM module of the MCU to the parameters mentioned above:
void initPWM(void){
    /*PWM setup for half-bridge*/

    PTPER = OPENLOOOPERIOD;

    IOCON1bits.PENH = 1; // PWM1H/L is controlled by I/O module
    IOCON1bits.PENL = 1;
    IOCON1bits.PMOD = 0; // Complimentary mode
    IOCON1bits.OVRDAT = 0;

    PWMCON1bits.DTC = 0; //was 2 // positive dead-time is enabled, using duty cycle - deadtime
    PWMCON1bits.IUE = 0; // disable immediate duty cycle updates
    PWMCON1bits.ITB = 1; //was 0 // select PTPER provides period value

    DTR1 = 100; //high side dead-time 100ns
    ALTDTR1 = 100; //low side dead-time 100ns

    FCLCON1bits.FLTMOD = 0; // Enable fault mode
    FCLCON1bits.FLTSRC = 0; // Fault Source FLT1-CURRENT
    FCLCON1bits.FLTPOL = 0; // Active High

    PHASE1 = OPENLOOOPERIOD;

    PDC1 = 4789; //8815; //1438; // Start with a duty cycle of 0.45

    TRIG1 = PTPER >> 2;
    STRIG1 = PTPER >> 4;
    TRGCON1bits.TRGSTRT = 1; // Trigger ADC after the first PWM
    TRGCON1bits.TRGDIV = 1; // Trigger generated every 2 cycles
    return;
}

Pins

All of the digital pins are set up in this function. This includes all of the digital outputs for the SR MOSFET gate control, the enable pin on the GaN drivers and the relay control. The digital input polarity pin is also set up and the priority of the interrupt is set to be higher than that of the ADC interrupt. This was done so the distribution of the duty cycle is always correct with respect to the input voltage polarity. The following block of c-code initializes the digital I/O pins of the MCU to the parameters mentioned above:

void initPins(void){
    //disable all serial communication-based peripherals
    SPI1STATbits.SPIEN = 0;
    I2C1CONbits.I2CEN = 0;
U1MODEbits.UARTEN = 0;

//Set up SR L/H Pins
ADPCFGbits.PCFG6 = 1; //pins are digital now
ADPCFGbits.PCFG7 = 1;
CNEN1bits.CN1IE = 0; //disable input change interrupt
CNEN1bits.CN4IE = 0;
CNEN1bits.CN2IE = 0;
TRISBbits.TRISB1 = 0; //pins are outputs
TRISBbits.TRISB4 = 0;
TRISBbits.TRISB2 = 0;

//Set up ENABLE Pin
CNEN1bits.CN5IE = 0; //disable input change interrupt
TRISBbits.TRISB5 = 0; //pins are outputs
RPOR1bits.RP3R = 0b000000;
PORTBbits.RB5 = 0; //set low initially
LATBbits.LATB5 = 0;

//Set up RelayCTL Pin
IEC0bits.INT0IE = 0; //disable ext interrupt pin INT0
CNEN1bits.CN3IE = 0; //disable input change interrupt
TRISBbits.TRISB3 = 0; //pins are outputs
RPOR2bits.RP5R = 0b000000;
PORTBbits.RB3 = 0; //set low initially
LATBbits.LATB3 = 0;

//Set up Polarity Pin
TRISBbits.TRISB4 = 1; //pin is input
CNEN1bits.CN4IE = 1; //enable pin as interrupt on change
IEC1bits.CNIE = 0; //do not enable CN interrupt yet
IFS1bits.CNIF = 0; //clear CN flag bit
IPC4bits.CNIP = 7; //set priority of interrupt, higher than adc
return;
}

ADC

The ADC converters, channels 0 and 1, are set to run simultaneously and are triggered by the
PWM1H trigger event. The ADC clock is set to 20MHz with a 10-bit integer format output when the
buffer is read. DSC pins AN0,1,2, and 3 are configured as analog inputs. The ADC channel 0 samples
the output DC voltage and input current. ADC channel 1 samples the line and neutral terminals of
the input AC voltage. The following block of c-code initializes the ADC module and ADC associated input
pins of the MCU to the parameters mentioned above:
void initADC(void){
    ADCONbits.FORM = 0;                                          // Integer data format
    ADCONbits.EIE = 0;                                           // Early Interrupt disable
    ADCONbits.ORDER = 1;                                         // converter odd channel first
    ADCONbits.SEQSAMP = 0;                                       // Select Simultaneous sampling
    ADCONbits.SLOWCLK = 1;                                       // APLL for the ADC
    ADCONbits.ASYNCSAMP = 0;                                     // Dedicated S&H starts sampling when trigger detected
    ADCONbits.ADCS = 5;                                          // ADC clock = FADC / 6 = ~120MHZ / 6 = 20MHZ
    ADCPC0bits.TRGSRC0 = 4;                                      // PWM1H triggers ADCP0 AN0/AN1
    ADCPC0bits.TRGSRC1 = 4; //16                                  // PWM1H triggers ADCP0 AN2/AN3
    ADPCFGbits.PCFG0 = 0;                                        // AN0,AN1,AN2,AN3 is configured as analog input
    ADPCFGbits.PCFG1 = 0;
    ADPCFGbits.PCFG2 = 0;
    ADPCFGbits.PCFG3 = 0;
    IFS6bits.ADCP0IF = 0;                                       //clear ADC interrupt flag
    IEC6bits.ADCP0IE = 0;                                       //disable ADC interrupt until after start-up
    IPC27bits.ADCP0IP = 6;                                       // set ADC interrupt priority as 6 level
    ADCONbits.ADON = 1;                                          // enable ADC now to allow time to stabilize
    return;
}

4.2.4 Control Timing

The PFC control code consists of two periodic interrupts. The first periodical interrupt,
ADCP0Interrupt(), is driven by the flag that represents when the ADC0 paired buffers are ready to
be read. This flag is triggered every other PWM cycle during the high side on-time. This routine is
configured for higher priority to execute the inner current loop calculation at 50kHz which is half of
the PWM switching frequency of 100kHz. Within this interrupt, all of the ADC buffers for input AC
voltage, input current, and output DC voltage are read and updated before the current loop related
calculations are run. Also, in this loop is a counter variable that will execute the voltage loop
calculations every tenth entry into the current loop which yields a voltage loop frequency of 5kHz.
The other periodic interrupt, CN4Interrupt(), is driven by the interrupt on change feature attached
to the RB4 pin. This pin holds the output of the comparator signal which determines the polarity of the input voltage. This interrupt on change is triggered with both a rising and falling edge seen at the RB4 pin. After it has been triggered, a digital read is performed on the pin to determine the input voltage polarity. This information is then used to determine the turn-on of the appropriate SR MOSFET and to determine the distribution of the calculated duty cycle. Just as it was done in the simulation. While in the Run state, these two interrupts are constantly looping through their actions indefinitely.

4.3 Testing Stages to Achieve Full Operation

Once the PCB had been populated, the discrete components were tested to verify a solid soldered connection on every pin. The detection circuits were individually verified using a small DC test voltage for the Line and Neutral input voltage sensing and for the output voltage sensing circuits. While testing the Line and Neutral input voltage, the output of the comparator was monitored to check proper operation of the Polarity sensing. The flux gate and current sensing circuit were tested with bi-directional DC currents that covered the entire nominal current range of the flux gate (-3A to +3A).

After this, all of the outputs from the MCU were tested by means of a short test-script that was written to continuously loop through the performance of all of the outputs. Initially, the PWM module was set to a 50% duty cycle with the enable output for the gate drivers set high, and the relay was turned-on. After a short delay, the high side SR MOSFET was turned-on. Another delay and the enable output was set low while the high side SR MOSFET was turned-off and the low side SR MOSFET was turned-on. Another delay, and the script looped to the beginning. This test-script was then repeated for various duty cycles between 2 and 98%, the lower and upper duty cycle bounds, respectively.
To conclude the systems check, a simulation tool within MPLAB IDE was used to compile the code and step through the voltage and current control loops with self-made detection values on the ADC buffers. The simulation was performed one line at a time, with the variable outputs monitored after each step. This was done to guarantee that no math or stack overflow errors would occur during the arithmetic calculations in the voltage and current control loops.

To get the physical hardware version of the converter working, the targeted end goal of closed loop operation was broken down into steps to slowly introduce aspects of the complete operation. The following sections expand on these individual steps.

4.3.1 Open Loop Control with a Rectified Input

The first of the steps utilized an open loop control scheme with a rectified AC input voltage. In this testing stage, the current control loop and duty cycle generation arithmetic could be tested without having to deal with the Polarity information for duty cycle distribution or the voltage loop interaction. To perform these tests, the power stage of the PFC design was altered to function in a purely DC manner as per the schematic in Figure 66. To provide all of the necessary information to the current control loop, a compensated error voltage, what would normally come as an output from the voltage control loop, was artificially replicated with an external DC power supply that was directly connected to the output voltage sensing ADC pin of the MCU in lieu of a connection to the DC output voltage bus. This external supply could then be varied to either increase or decrease the input current draw into the power circuit.
At the beginning of this test, only low input voltage and power were used to check for expected function. The input voltage and artificial error signal were slowly increased until the PFC converter was operating at the correct input voltage level and was achieving the approximate input to output voltage ratio, around 1:1.8, at half-load power conditions. Figure 67 below shows the rectified input voltage and input current waveforms at these conditions.
Figure 67: Input current waveform and rectified input voltage waveform under 300W output load condition.

4.3.2 Open Loop Control with an AC Input and Rectifying Diodes

The following step eliminated the input voltage bridge rectifier and reintroduced the rectifying diodes as per the schematic in Figure 68. With this step, only the Polarity information for the distribution of the duty cycle was introduced while still operating under an open loop, current control, scheme.

Figure 68: Circuit schematic for the BTPPFC operating with an AC input and synchronous rectifying diodes under open loop conditions. Note that there is no voltage sensing at the output.
Per the original control theory and methodology, the output of the comparator was to yield a clean square wave that alternated between a logic high and low at each half cycle of the input line voltage. In the physical hardware implementation, the comparator output was not a clean square wave but instead had multiple oscillations during each logic transition and caused issue within the interrupt on change and control logic of the MCU. As a solution, control logic was added within the MCU to compare the ADC buffer readings of the Line and Neutral input voltage during each current control loop and determine the Polarity in that manner.

Once the circuit was operational in this orientation and function, the input voltage and artificial error signal were slowly increased again until the PFC converter was operating at the correct input voltage level and was achieving the approximate input to output voltage ratio. The current error compensation parameters were then tuned from the values in the PSIM simulation to offer the highest PF and lowest THD in the input current under a full range of loading conditions. These new tuned values are shown below in Table 7 with the resulting input voltage and current waveforms in Figure 69.

<table>
<thead>
<tr>
<th></th>
<th>Voltage Error Compensation Parameters</th>
<th>Current Error Compensation Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional</td>
<td>NA</td>
<td>$k_p = 0.1$</td>
</tr>
<tr>
<td>Integral</td>
<td>NA</td>
<td>$k_i = 0.015$</td>
</tr>
</tbody>
</table>

*Table 7: Hardware tuned error compensation parameters for the current loop.*
4.3.3 Closed Loop Control with an AC Input and Rectifying Diodes

Following the completion and tuning of the open loop testing, the control loop had to be closed with the addition of the voltage control loop. With this step, the artificial error voltage signal was removed, and the output voltage sensing ADC pin of the MCU was reconnected to the output DC voltage bus as per the schematic in Figure 70.

![Image: Input voltage and current waveforms using the tuned error compensation parameters for the current loop. Gate signals for the SR MOSFETs are shown below the other waveforms.](image)
Figure 70: Circuit schematic for the BTPPFC operating with an AC input and synchronous rectifying diodes under closed loop conditions. Note that there is voltage sensing at the output.

By closing the system control loop with the addition of the voltage control loop, a start-up function was required to slowly raise the output voltage reference to the desired value. This start-up function was taken directly from the PSIM simulation and adapted to suit the hardware and the MCU. At the beginning of this test, only low input voltage and power were used with a fractional value for the output reference voltage to check for the expected function. An example of this low power start-up test at a fractional value for input and output voltage can be seen in Figure 71.
Figure 71: A low power start-up test at fractional input and output voltages. Output voltage is in green, input current in magenta.

The input voltage and output voltage reference value were slowly increased until the PFC converter was operating at the correct input voltage and output voltage level. The voltage error compensation parameters were then tuned from the values in the PSIM simulation to offer a stable output voltage and quick start-up while maintaining a high PF and low THD in the input current under a full range of loading conditions. These new tuned values are shown below in Table 8 with the resulting input voltage, input current, and output voltage waveforms in Figure 72.

<table>
<thead>
<tr>
<th></th>
<th>Voltage Error Compensation Parameters</th>
<th>Current Error Compensation Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional</td>
<td>( k_p = 0.15 )</td>
<td>( k_p = 0.1 )</td>
</tr>
<tr>
<td>Integral</td>
<td>( k_i = 0.005 )</td>
<td>( k_i = 0.015 )</td>
</tr>
</tbody>
</table>

Table 8: Hardware tuned error compensation parameters for the voltage and current loops.
4.3.4 Complete Operation

The final step to achieve the complete working operation of the BTPPFC converter was to eliminate the rectifying diodes and replace them with the SR MOSFETs as per the schematic in Figure 24, Section 3.3. The original plan was to utilize a short timer interrupt that waited around 500ms after a zero crossing to turn-on a FET. However, an issue arose due to the current ripple in the input inductor current that flows through the SR MOSFETs. If the FET is turned-on too early, the current can reverse direction and cause a very large negative current spike, upwards of 20A in magnitude, that can cause damage to the GaN switching devices or the SR MOSFETs. To avoid this phenomenon, logic that uses a voltage threshold with hysteresis was implemented to control the on-time for the SR FETs. For example, when the input voltage is above 50V the FET will turn-on, and when the input voltage falls below 35V the FET will turn-off. This hysteresis ensures that the FET will not alternate states multiple times, before staying in it’s

![Figure 72: Input voltage and current waveforms using the tuned error compensation parameters for the voltage and current loops. The regulated output voltage is shown in green.](image)
desired state, due to input voltage ripple or noise on the ADC pins. Again, low input voltage and power tests were conducted first to verify this new function. The start-up sequence for such a case can be seen in Figure 73.

![Figure 73: A low power start-up sequence to test the control method of the SR MOSFETs. Input current is in magenta, and SR gate signals are in green and cyan.](image)

Once verified, the BTPPFC converter was setup to nominal input and output voltage conditions. The steady-state waveforms for complete operation with closed loop control and SR MOSFETs are below in Figure 74. At this stage, the approximate on-time for the MOSFETs was around 5.7ms.
4.3.5 First Round Efficiency Test

With the converter running at a complete functional level, initial efficiency tests were performed to establish a benchmark and determine how much needed to be done to achieve the targeted 99% efficiency. The results of this first round of testing are detailed in the following Table.

<table>
<thead>
<tr>
<th>Vin (Vrms)</th>
<th>Pin (W)</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>Pout (W)</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>611</td>
<td>379.9</td>
<td>1.5602</td>
<td>592.7</td>
<td>97.0%</td>
</tr>
<tr>
<td>200</td>
<td>523</td>
<td>379.5</td>
<td>1.3392</td>
<td>508.2</td>
<td>97.2%</td>
</tr>
<tr>
<td>200</td>
<td>403</td>
<td>380.0</td>
<td>1.0313</td>
<td>391.9</td>
<td>97.2%</td>
</tr>
<tr>
<td>200</td>
<td>307</td>
<td>379.7</td>
<td>0.7835</td>
<td>297.5</td>
<td>96.9%</td>
</tr>
<tr>
<td>200</td>
<td>247</td>
<td>379.1</td>
<td>0.6321</td>
<td>239.6</td>
<td>97.0%</td>
</tr>
<tr>
<td>200</td>
<td>199</td>
<td>380.2</td>
<td>0.5068</td>
<td>192.7</td>
<td>96.8%</td>
</tr>
<tr>
<td>200</td>
<td>161</td>
<td>378.9</td>
<td>0.4091</td>
<td>155.0</td>
<td>96.3%</td>
</tr>
</tbody>
</table>

Table 9: Efficiency data from the first round of testing with the converter in full operation.
4.4 Efficiency Optimization

To reach the targeted 99% efficiency, the loss analysis performed earlier and outlined above in Section 3.4 was consulted to determine where improvements could come from. Referencing the loss analysis, the largest losses come from the conduction losses of the inductor, capacitor, MOSFETs and GaN switches.

Looking at the output capacitor, there is very little to be done to reduce the conduction loss developed from the ESR of the capacitor as the chosen component already has a lower than average dissipation factor, $DF$, which is directly related to ESR. There is also very little to be done to reduce the conduction loss of the GaN switches as the selected devices have a very low $R_{\text{ds(on)}}$ for their current rating and compared to other technologies on the market.

In an ideal situation, the SR MOSFETs are turned-on and conducting for the entirety of their respective half line cycles. However, in practice the MOSFETs can only be turned-on once the current flowing through them is at a high enough point from the zero-current level, as mentioned. Because of this, there

---

![Benchmark Efficiency vs. Load](image_url)

*Figure 75: Efficiency curve at various loading conditions for the first round of testing with the converter in full operation.*
is still room for improvement to increase the on-time of the MOSFETs as much as possible while still avoiding the negative current spike.

Unlike the capacitor, the DCR of input inductor can be reduced which should greatly improve the losses of the inductor associated with conduction. Additional losses which can be mitigated are found in the switching overlap loss of the GaN switching devices.

4.4.1 Inductor Optimization

To reduce the DCR of an inductor, the conducting wire that wraps around the magnetic core can be swapped for a lower resistive wire through a material change or an increase in wire gauge. DCR can also be reduced through fewer windings around the core while using the same material and gauge. However, by changing the number of turns, the inductance of the component is also changed [17].

For this application, it was decided to increase the apparent gauge of the wire by taking two lengths of the same gauge as the current inductor and twisting them together before winding it around the core. This additional amount of wire and material was unable to wrap the correct number of times around the core while staying inside the bounds of the drum core. To fix this issue, a larger drum core inductor with a similar ferrite core material was bought to better accommodate the extra material.

The selected inductor for this purpose was the 1539M32 from Hammond Manufacturing. Due to the change in material and physical characteristics of the core, such as cross-sectional area and path length, a new number of windings had to be calculated that would deliver the desired inductance of 820µH. This calculation is outlined below:

\[ L_{\text{new,ind}} = \frac{4\pi N^2 \mu A_e}{I_e} \cdot 10^{-9} = 10mH \]  

(4.2)

Where \( N = 240 \) turns and \( \frac{\mu A_e}{I_e} = 7.771 \) for the new inductor core.
Rearranging for $N$ gives:

$$N_{\text{required}} = \sqrt{\frac{L_{\text{desired}}}{4\pi \mu_0 \varepsilon_0 \cdot 10^{-9}}} = \sqrt{\frac{820 \cdot 10^{-6}}{4\pi \cdot 7.77 \cdot 10^{-9}}} = 69 \text{ turns}$$  \hspace{1cm} (4.3)

With the number of turns known, the new, larger inductor core was wound with the larger apparent gauged twisted wire. Figure 76 shows the finished inductor.

![Finished inductor](image)

*Figure 76: Finished new inductor to allow for lower copper loss.*

To verify that the DCR of the new inductor was lower than the previous inductor, an experiment was set up which involved running a large DC current through each inductor and measuring the voltage drop across it. These voltage and current measurements were then used to calculate each component’s DCR. Table 10 summarizes these findings.

<table>
<thead>
<tr>
<th>Inductor DCR Comparison</th>
<th>Old</th>
<th>New</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (A)</td>
<td>2.96</td>
<td>3.05</td>
</tr>
<tr>
<td>Voltage (V)</td>
<td>0.40</td>
<td>0.26</td>
</tr>
<tr>
<td>DCR (Ω)</td>
<td>0.135</td>
<td>0.084</td>
</tr>
</tbody>
</table>

*Table 10: DCR measurements of the old and new input inductor.*
4.4.2 MOSFET On-Time Optimization

Since the potential for a large negative current spike during turn-on of the SR MOSFETs is directly related to the magnitude of the current at turn-on, it was decided to change the control scheme for this feature to an input current control as opposed to relying on the input voltage waveform.

![Figure 77: Largest consistently achievable MOSFET on-time using voltage control at 300W output load.](image)

To test this new control method, it was first implemented in the PSIM simulation to verify it’s function. Once verified, the same control structure was replicated on the MCU for hardware testing. The specifics for this current control are similar to the voltage hysteresis method mentioned previously. Different current threshold values with a hysteresis margin between the turn-on and turn-off levels were tested. The outcome of this testing produced a set of current threshold values which maximized the MOSFET on-time for all loading conditions, while consistently ensuring that a MOSFET is always turned-on for every half cycle. An additional benefit to this change in control scheme, was a more accurate method to achieve IDE with the SR MOSFETs, particularly at lower loading conditions.
Figure 78 below shows the on-time result with this tuned threshold and new control method. It can be seen that at half-load conditions, 300W, the on-time is over 6.3ms. With the same threshold values, the on-time seen at full-load conditions, 600W, is approximately 7.0ms.

With a larger on-time observed with this adaptive current method, the anti-parallel body diodes of the MOSFETs are conducting for significantly shorter time period, as well as at a much lower current level. Therefore, the conducting losses associated with these synchronous switches are greatly reduced.

4.4.3 GaN Gate Resistance and Deadtime Optimization

To reduce the switching overlap loss of the GaN switches, the gate driving resistances of the switches needed to be reduced. As was explored, ringing and oscillations can occur at the gate of the GaN switch due to parasitic inductance between the gate driver and gate of the GaN as well as the high dv/dt and low gate to source capacitance of the GaN. Limiting the distance of this loop can only do so much to
prevent ringing so a large enough gate resistance is used to provide damping on this switching signal during the transitions from low to high and high to low. During the first round of testing to initially get the BTPPFC converter working, larger than recommended values for the high and low gate resistors were used to eliminate any potential switching failures caused by ringing or oscillations [13]. These values were $50\,\Omega$ and $2\,\Omega$ respectively. However, with these larger gate resistances, the transition times for the gates of the GaN switches to turn-on and turn-off have been increased which leads to greater overlap loss during switching.

In order to safely reduce these gate resistances, another board was partially populated to operate as a fixed duty cycle, synchronous DC/DC boost converter with the GaN switches. This test scenario allowed for the gate signals of the GaN switches to be monitored while starting at lower risk, lower input and output voltage conditions. The high and low gate resistances were varied one resistance at a time and monitored up until the test circuit was operating at $200\text{Vin}$ and $400\text{Vout}$, similar to the operating voltages of the BTPPFC converter.
Figure 79: Original GaN gate signals with 50/2 Ohm resistances. High side in cyan, low side in green.

Figure 80: Optimally tuned GaN gate signals with high side 10/2 Ohm resistance in the top two images and low side 20/1 Ohm resistance in the bottom two images.
For the high gate resistance, values of 50, 30, 20 and 10Ω were tested, and for the low gate resistance, values of 2, 1 and 0Ω were tested. All of these intermediary gate waveforms can be found in Appendix C.

By comparing the waveforms, the optimum resistance values for each gate driver were found. It was desirable to not only reduce the transition time, but to also limit the magnitude of any voltage spikes that occur during these transitions. Table 11 below summarizes the selected gate resistance values for both GaN switch gate drivers.

<table>
<thead>
<tr>
<th></th>
<th>Low Gate Resistance</th>
<th>High Gate Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-Side GaN</td>
<td>1Ω</td>
<td>20Ω</td>
</tr>
<tr>
<td>Switch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-Side GaN</td>
<td>2Ω</td>
<td>10Ω</td>
</tr>
<tr>
<td>Switch</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Table 11: Hardware tuned gate resistance values for the GaN switches.*

In addition to the gate resistances, the deadtime value between the high and low side complimentary PWM signals was reduced slightly from the 100ns used in the initial round of testing. By using the following equation, and referring to [13]:

\[
    t_{d_{\text{PWM}}} > t_{\text{delay,skew}} + (t_{d(\text{off})} - t_{d(\text{on})})
\]  \hspace{1cm} (4.4)

Where:

\( t_{\text{delay,skew}} \) is the propagation delay of the gate driver, for Si8271; 45ns typical and 75ns maximum [36],

\( t_{d(\text{off})} \) is the transition time for the voltage gate signals to turn-off,

\( t_{d(\text{on})} \) is the transition time for the voltage gate signals to turn-on.

\[
    t_{d_{\text{PWM}H}} > 75ns + (16ns - 30ns)
\]

\[
    t_{d_{\text{PWM}L}} > 61ns
\]

\[
    t_{d_{\text{PWM}L}} > 75ns + (16ns - 16ns)
\]
\[ t_{d,\text{pwmL}} > 71\text{ns} \]

Based on the above calculations, it was decided to use the larger of the values for the new deadtime parameter. To reduce the risk of accidental shoot-through, caused by the turn-on overlap of both switches, a safety margin of 15% was added to the larger of the deadtimes to give a value of 85ns.

This reduced deadtime leads to reduced body diode conduction time and therefore lower losses in the GaN switches.

4.4.4 Second Round Efficiency Test

After the component tweaks and optimizations outlined above, another round of efficiency testing was performed. The results of this second round of testing are detailed in the following Table.

<table>
<thead>
<tr>
<th>Vin (Vrms)</th>
<th>Pin (W)</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>Pout (W)</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>607</td>
<td>380.5</td>
<td>1.5592</td>
<td>593.3</td>
<td>97.7%</td>
</tr>
<tr>
<td>200</td>
<td>517.5</td>
<td>380.9</td>
<td>1.3289</td>
<td>506.2</td>
<td>97.8%</td>
</tr>
<tr>
<td>200</td>
<td>405</td>
<td>380.8</td>
<td>1.0434</td>
<td>397.3</td>
<td>98.1%</td>
</tr>
<tr>
<td>200</td>
<td>310</td>
<td>381.0</td>
<td>0.7991</td>
<td>304.5</td>
<td>98.2%</td>
</tr>
<tr>
<td>200</td>
<td>244</td>
<td>380.6</td>
<td>0.6299</td>
<td>239.7</td>
<td>98.3%</td>
</tr>
<tr>
<td>200</td>
<td>198</td>
<td>380.7</td>
<td>0.5118</td>
<td>194.8</td>
<td>98.4%</td>
</tr>
<tr>
<td>200</td>
<td>157</td>
<td>381.1</td>
<td>0.4022</td>
<td>153.3</td>
<td>97.6%</td>
</tr>
</tbody>
</table>

*Table 12: Efficiency data from the second round of testing with the converter in full operation.*
As can be seen, the improvements in efficiency are lower than expected, as the converter is still unable to reach the targeted efficiency of 99%. The most likely reason for this lack of efficiency improvement, particularly at the higher power end, is the excess temperature of the GaN switches which drastically increases the losses experienced by the switches during conduction [30]. Thermal imaging was taken and verified this hypothesis. As can be seen in Figure 82, the bright yellow and white region in the bottom left corner of the box represents the temperature of the two GaN switches. The temperature of these components while only operating at around 400W is already close to 100 degrees Celsius. For better thermal management of fast switching components, it is typical to add a heatsink to eliminate the waste heat from losses and cool these components. However, because the GaN switches are of a bottom cooled package design, adding an external heatsink on their top surface is an ineffective method to reduce the temperature of the switches. To progress the project and push to achieve the highest possible efficiency, it was decided to make another PCB design using a top cooled package design for the GaN switches with a designated layout for the addition of a heatsink. It should also be noted that the selected top cooled GaN switch component, GS66506T, is rated for a larger continuous drain-source
current than the bottom cooled GS66504B and has a lower Rdson, 67mΩ compared to 100mΩ, which will allow for fewer conduction losses and greater efficiency [30] [31].

![Thermal image](image)

*Figure 82: Thermal image of the first PCB design converter operating at 400W. The inductor is seen centred with the GaN switches to the left.*

4.5 Second Iteration PCB Design

A second iteration PCB design utilizing top cooled GaN switching devices was done. The bulk of the new PCB design remains unchanged apart from the power stage that has been altered for the footprint of the GS66506T GaN components and to provide better thermal management. Figure 83 below shows the redesigned PCB layout of the power stage.
Figure 83: Second iteration PCB layout of the power stage as seen from the top side. Top layer is red, bottom is blue, all other coloured traces are internal. GaN switches are outlined in black, gate drivers in white.

It can clearly be seen that the new design has many more copper planes on various layers to better reduce the internal resistance of the copper traces that make up the high-power circuit while also providing surfaces on the top layer that are not electrically connected to any other circuit nodes. These free-floating copper planes were added to act as a sort of heat sink when working with copper fins to provide component cooling directly to the GaN switches. This concept will be explored in further detail later on. For additional cooling, multiple vias were added in the copper layers that directly connect to the drain and source pads of the high and low GaN switches. These vias introduce greater surface area that provide good passive air cooling.

Other important concepts, such as close proximity of the gate drivers to the GaN switches as well as a tight current loop between the four switches and absorption capacitors next to the high side GaN, are maintained in this new PCB layout.
4.5.1 Gate Resistance Tuning

Due to the change in layout of the gate drive traces, as well as the component change for the GaN switches, the test outlined above to tune the high and low gate driver resistances was repeated on the new PCB layout. Table 13 below summarizes the selected gate resistance values for both GaN switch gate drivers.
### Table 13: Hardware tuned gate resistance values for the GaN switches for the second PCB layout.

<table>
<thead>
<tr>
<th></th>
<th>Low Gate Resistance</th>
<th>High Gate Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-Side GaN Switch</td>
<td>1Ω</td>
<td>10Ω</td>
</tr>
<tr>
<td>High-Side GaN Switch</td>
<td>1Ω</td>
<td>20Ω</td>
</tr>
</tbody>
</table>

4.5.2 Thermal Analysis

Once the new PCB layout was populated and tested, a thermal analysis was done on the BTPPFC converter running at full operation over the entire rated loading range. Multiple tests were conducted using various thermal management options that are outlined below. For the tests conducted with a fan, a standard 12V CPU fan was placed at a fixed distance (approximately 6 inches) from the test converter setup. Table 14 provides a summary of the thermal analysis with the various thermal management options tried and tested. It can be seen that the aluminum heat sink offered the best thermal performance by keeping the GaN switch temperatures the lowest of all the tests.

<table>
<thead>
<tr>
<th></th>
<th>Temperature 300W Test no Fan</th>
<th>Temperature 300W Test with Fan</th>
<th>Temperature 600W Test no Fan</th>
<th>Temperature 600W Test with Fan</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Heat Sink</td>
<td>94°C</td>
<td>83°C</td>
<td>100+°C</td>
<td>100+°C</td>
</tr>
<tr>
<td>Copper Fins using Thermal Paste</td>
<td>NA</td>
<td>70°C</td>
<td>NA</td>
<td>100+°C</td>
</tr>
<tr>
<td>Copper Heat Sink using Thermal Pad</td>
<td>70°C</td>
<td>54°C</td>
<td>88°C</td>
<td>65°C</td>
</tr>
<tr>
<td>Aluminum Heat Sink using Thermal Pad</td>
<td>68°C</td>
<td>46°C</td>
<td>81°C</td>
<td>55°C</td>
</tr>
</tbody>
</table>

Table 14: Summary of the thermal analysis performed on the second PCB layout.

**Case 1: No Heatsink**

For a base-line measurement, the converter was run over the full range of loading conditions with no additional heatsink. The tests were performed with and without a fan for additional component cooling. During the 300W test, this setup allowed the GaN switches to get to 94 degrees Celsius without a fan.
and 83 degrees Celsius with the fan. Figure 86 below shows the thermal image of the GaN switches during this test.

![Thermal Image of the No Heatsink Test at 300W](image)

*Figure 86: Thermal image of the no heatsink test at 300W.*

During the control test at 600W while using the fan, the GaN switches reached well above 100 degrees Celsius before a device failure occurred.

**Case 2: Copper Fins with Thermal Paste**

As mentioned above in the discussion of the second iteration PCB layout, the thermal management strategy with the copper fins was the primary focus for the power stage circuit redesign. Referring below to Figure 87, thin copper fins are soldered directly to the large copper planes on the top layer surrounding the power stage. Each fin is then shaped and folded over to rest on top of the thermal pad of each GaN switch with a layer of thermal paste between the two to provide electrical isolation and thermal conduction.
To limit risk to the GaN switches during the testing with the copper fins, only the testing with the fan was done to provide additional cooling. During the 300W test, the addition of the copper fins allowed the GaN switches to get to 70 degrees Celsius. Upon raising the load to get to 600W, the temperature of the GaN switches again reached well above 100 degree Celsius and a device failure occurred. Through the use of thermal imaging, it appeared that the thermal paste was not conducting the heat very well to the copper fins as the temperature was primarily localized to the area just above the switches. The most likely cause for this phenomenon was an issue with the contact between the thermal paste and the copper.

Case 3: Heatsink with Thermal Pad

The implementation of a heatsink that utilized a thermal pad and hardware to fasten it to the top surface of the GaN switches was proposed as a solution to this contact issue. A suitable area on the PCB was found as a location for a heatsink with through hole hardware.
Two heatsink of different design and material were built and tested to achieve the lowest operating temperature of the GaN switches during loading.

**Copper Heatsink**

A copper heatsink for a TO265 packaged MOSFET was altered by adding a thin copper sheet to the bottom and drilling a hole in the centre for hardware to fix it to the board, Figure 88. A small sheet of silicon elastomer thermal pad material, 5583S from 3M, was cut to the outline shape of the copper heatsink and self adhered to the GaN switches and surrounding area that the heatsink will cover. With
the copper heatsink attached to the board, thermal testing was done with and without a fan. During the 300W test, this setup allowed the GaN switches to get to 70 degrees Celsius without a fan and 54 degrees Celsius with the fan. During the 600W test, this setup allowed the GaN switches to get to 88 degrees Celsius without a fan and 65 degrees Celsius with the fan. Figures 89 below show the thermal image of the GaN switches and heatsink during this test with the fan.

![Thermal image of the copper heatsink test with a fan at 600W.](image)

**Figure 90: Thermal image of the copper heatsink test with a fan at 600W.**

**Aluminum Heatsink**

![Aluminum heatsink.](image)

**Figure 91: Aluminum heatsink.**

A basic stick-on adhere aluminum heatsink was altered by drilling a hole in the centre for hardware to fix it to the board, Figure 90. Another small sheet of silicon elastomer thermal pad material, 5583S from 3M, was cut to the outline shape of the aluminum heatsink and self adhered to the GaN switches and
surrounding area that the heatsink will cover. With the aluminum heatsink attached to the board, thermal testing was done with and without a fan. During the 300W test, this setup allowed the GaN switches to get to 68 degrees Celsius without a fan and 46 degrees Celsius with the fan. During the 600W test, this setup allowed the GaN switches to get to 81 degrees Celsius without a fan and 55 degrees Celsius with the fan. Figure 91 below shows the thermal image of the GaN switches and heatsink during this test with the fan.

![Thermal image of the aluminum heatsink test with a fan at 600W.](image)

Figure 92: Thermal image of the aluminum heatsink test with a fan at 600W.
Chapter 5 – Results

5.1 System Performance

Having found a solution to the thermal management issue of the GaN switches, final tests were performed to discover the system performance of the BTPPFC design. The following table and figures provide an overview of the total efficiency, PF, and input current THD performance over the entire loading range of the converter.

<table>
<thead>
<tr>
<th>Vin (Vrms)</th>
<th>Pin (W)</th>
<th>Vout (V)</th>
<th>Iout (A)</th>
<th>Pout (W)</th>
<th>Efficiency</th>
<th>Power Factor</th>
<th>THD in input Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>608.1</td>
<td>380.8</td>
<td>1.5708</td>
<td>598.2</td>
<td>98.4%</td>
<td>0.992</td>
<td>4.3%</td>
</tr>
<tr>
<td>200</td>
<td>514.4</td>
<td>381.0</td>
<td>1.3295</td>
<td>506.5</td>
<td>98.5%</td>
<td>0.990</td>
<td>5.2%</td>
</tr>
<tr>
<td>200</td>
<td>457.8</td>
<td>380.7</td>
<td>1.1857</td>
<td>451.4</td>
<td>98.6%</td>
<td>0.988</td>
<td>5.8%</td>
</tr>
<tr>
<td>200</td>
<td>403.6</td>
<td>381.1</td>
<td>1.0441</td>
<td>397.9</td>
<td>98.6%</td>
<td>0.986</td>
<td>6.1%</td>
</tr>
<tr>
<td>200</td>
<td>305.5</td>
<td>380.5</td>
<td>0.7922</td>
<td>301.4</td>
<td>98.7%</td>
<td>0.982</td>
<td>6.9%</td>
</tr>
<tr>
<td>200</td>
<td>250.4</td>
<td>380.9</td>
<td>0.6477</td>
<td>246.7</td>
<td>98.5%</td>
<td>0.975</td>
<td>8.7%</td>
</tr>
<tr>
<td>200</td>
<td>197.6</td>
<td>380.6</td>
<td>0.5107</td>
<td>194.4</td>
<td>98.4%</td>
<td>0.964</td>
<td>9.9%</td>
</tr>
<tr>
<td>200</td>
<td>155.8</td>
<td>381.1</td>
<td>0.3998</td>
<td>152.4</td>
<td>97.8%</td>
<td>0.960</td>
<td>14.6%</td>
</tr>
</tbody>
</table>

Table 15: Overall system performance at various loading conditions.

From Table 15, it can be seen that converter design did not meet the target efficiency of 99%, however it did come quite close by achieving over 98.5% efficiency from 250W to over 500W at the output.

Additionally, per the 80 Plus certification standards, the converter was able to achieve the Titanium level of efficiency, for a first stage power supply design. Based on the design specifications, the PF met the requirement of over 0.95 for the loading range while the THD in the input current only met the 10% maximum requirement from 200-600W at the output.
Figure 93: Power factor value curve at various loading conditions.

Figure 94: Input current total harmonic distortion curve at various loading conditions.
Figure 95: Efficiency curve at various loading conditions.

5.1.1 Start-up Performance

Figure 96: Start-up of BTPPF design at 300W output loading.
5.1.2 Steady-State Performance

Figure 97: Steady-state of BTPPFC at 150W output loading.
Figure 98: Steady-state of BTPPFC at 300W output loading.

Figure 99: Steady-state of BTPPFC at 450W output loading.
Figure 100: Steady-state of BTPPFC at 600W output loading.
5.2 Final Design Prototype

Figure 101: Final design prototype.
Chapter 6 - Conclusion and Future Work

6.1 Summary

A Bridgeless Boost Totem Pole PFC converter was developed for a first stage of the data centre power supply operating at a reasonably high switching frequency and utilizing Gallium Nitride switches and a low component count. The aim of developing the Bridgeless Boost Totem Pole PFC was very high efficiency, good PFC and THD performance, and a low component count. A variety of boost PFC topologies have been explored for this application, however, these topologies were not able to achieve the requirements outlined above. This was in part due to high component count and high losses in the components when operating at a higher switching frequency. As discussed in Chapter 2.3.1, switching related losses – switching loss, diode conduction loss, gate drive loss – all increase at higher switching frequencies. To mitigate these higher switching losses Gallium Nitride technology was proposed for the switches in this design.

The operation of the PFC converter was described in Chapter 3, followed by the control methodology to obtain a stable DC voltage output and PFC. With the design requirements and specifics outlined, component selection was performed for the power circuit. After this, a loss analysis was done on the power components to verify that the target efficiency was achievable. With the analysis done, the remainder of the circuits for control, gate driving, sensing, and auxiliary power were designed, and component selection performed.

The operation of the sensing circuits and complete design of the PFC converter were verified via simulation. This included the writing of a c code control algorithm that was later adapted to hardware. Two printed circuit boards were built with one utilizing a bottom cooled Gallium Nitride switch package, and the other utilizing a top cooled Gallium Nitride switch package. Both designs were optimized by
referencing the loss analysis previously performed, to achieve the highest possible efficiency without sacrificing high PFC and a low THD performance. Thermal analysis was done on each design, resulting in the top cooled GaN design that could handle the full-load at the lowest temperature with the implementation of an aluminum heatsink. With better thermal management, the maximum efficiency of the design was 98.7% at 300W and over 98.5% for the majority of the load range.

6.2 Contributions

The main contributions of this thesis are summarized below:

1. A Bridgeless Boost Totem Pole PFC converter was introduced in this thesis, designed for low component count and very high efficiency. Use of Gallium Nitride switches in the boost stage of the converter along with a custom wound inductor aided in increasing the overall efficiency. Loss analysis as well as hardware testing over a range of loading conditions was performed to verify this high efficiency operation.

2. Due to the use of GaN switches in the design, and the hard-switching application by operating the converter in CCM, the gate drive circuit has been optimized. This included selecting a proper gate driver and isolated power supply to provide a very precise gate reference, as well as the gate resistances, deadtime selection, and PCB layout. To optimize efficiency, further analysis on various gate resistances was performed to reduce the turn-on and turn-off time of the switches while reducing ringing and oscillations on the gate signal.

3. To limit negative currents during the boost stage switching which can cause large conduction losses, particularly at light-loads, current control was used for the gate signals of the synchronous MOSFETs to achieve close to ideal diode emulation.
4. For better THD performance, the input current waveform was analyzed to reduce the AC current spikes during the zero-crossing transition from one half-line cycle to the next. To reduce these current spikes, a soft-start function was developed to force the duty cycle to set values during these transition periods.

5. To allow for better dynamic performance, a fast voltage control loop along with a dead-zone controller and error filter were implemented in the digital control structure. The effectiveness of this strategy was verified with simulation only.

6. After component tuning and control optimization, a thermal analysis performed on the second PCB design offered a solution to the excessive heat issue of the GaN switches during full-load operation. Two heatsink designs with different materials were tested and verified their effectiveness by reducing GaN temperatures significantly.

6.3 Future Work

In this section future work on this topology with the goal of developing a more efficient, robust and higher performance design are outlined:

1. A thermal analysis was only performed on the GaN switches. However, it was noted that the SR MOSFETs get quite hot as well, approximately 80+ degrees Celsius at full load. A new layout could be done that allows the FETs to be placed vertically for better cooling. This new layout would also have a designated area for the heatsink that covers the GaN devices with other sizes and shapes that could be tested for better thermal management. Lower temperatures would allow for slight increases in efficiency as well. This layout would also be done with a primary aim of achieving high power density.
2. For better low power performance, specifically to achieve a lower THD in the input current, a burst-mode control algorithm could be implemented. This algorithm would variably enable and disable the GaN switching which would create a more sinusoidal current waveform. One potential trade-off with a burst-mode algorithm would be higher “body-diode” losses in the GaN switches.

3. The design could be changed to increase switching frequency. Higher switching frequency would allow for smaller and cheaper magnetic components and increased power density. Higher switching operation would also allow for better dynamic response, at the expense of higher switching losses.

4. The design should be tested to verify the dynamic response of the converter in hardware.
References


[35] LEM, "Insulated Highly Accurate Measurements from 1.5 to 50Arms," CAS / CASR / CKSR series Current Transducers datasheet.


[37] Silicon Labs, "0.5 and 4 Amp ISOdrivers (2.5 and 5 kVrms)," Si823x datasheet, May 2018.


Appendix A – Power Loss Calculations with Varying Input Voltage

<table>
<thead>
<tr>
<th>Input Voltage RMS (V)</th>
<th>180</th>
<th>190</th>
<th>200</th>
<th>210</th>
<th>220</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitor Loss (W)</td>
<td>1.580</td>
<td>1.454</td>
<td>1.333</td>
<td>1.224</td>
<td>1.126</td>
</tr>
<tr>
<td>MOSFET Loss (W)</td>
<td>0.990</td>
<td>0.898</td>
<td>0.810</td>
<td>0.735</td>
<td>0.669</td>
</tr>
<tr>
<td>Inductor Loss Total (W)</td>
<td>1.840</td>
<td>1.611</td>
<td>1.461</td>
<td>1.332</td>
<td>1.220</td>
</tr>
<tr>
<td>Low GaN Turn-on Overlap Loss (W)</td>
<td>1.032</td>
<td>0.979</td>
<td>0.930</td>
<td>0.886</td>
<td>0.845</td>
</tr>
<tr>
<td>Low GaN Turn-off Overlap Loss (W)</td>
<td>0.333</td>
<td>0.316</td>
<td>0.300</td>
<td>0.286</td>
<td>0.273</td>
</tr>
<tr>
<td>Low GaN Capacitor Loss (W)</td>
<td>0.350</td>
<td>0.350</td>
<td>0.350</td>
<td>0.350</td>
<td>0.350</td>
</tr>
<tr>
<td>High GaN Turn-off Overlap Loss (W)</td>
<td>0.149</td>
<td>0.149</td>
<td>0.149</td>
<td>0.149</td>
<td>0.149</td>
</tr>
<tr>
<td>High GaN Capacitor Loss (W)</td>
<td>0.133</td>
<td>0.133</td>
<td>0.133</td>
<td>0.133</td>
<td>0.133</td>
</tr>
<tr>
<td>High GaN Body Conduction Loss (W)</td>
<td>0.165</td>
<td>0.158</td>
<td>0.150</td>
<td>0.143</td>
<td>0.136</td>
</tr>
<tr>
<td>GaN Conduction Loss (W)</td>
<td>1.109</td>
<td>0.997</td>
<td>0.900</td>
<td>0.816</td>
<td>0.744</td>
</tr>
<tr>
<td>Relay Loss (W)</td>
<td>0.277</td>
<td>0.249</td>
<td>0.225</td>
<td>0.204</td>
<td>0.186</td>
</tr>
<tr>
<td><strong>Total (W)</strong></td>
<td><strong>7.958</strong></td>
<td><strong>7.293</strong></td>
<td><strong>6.741</strong></td>
<td><strong>6.258</strong></td>
<td><strong>5.832</strong></td>
</tr>
</tbody>
</table>

Calculated Power Loss and Efficiency for the Entire Range of Acceptable Input Voltages @ 600W Input Power
 Appendix B – C-block Control Code for PowerSIM Simulation

#include <Stdlib.h>
#include <String.h>

int g_nInputNodes=0;
int g_nOutputNodes=0;
int g_nStepCount=0;

double clock;

// Input Definitions
double VadcRef;
double VadcL;
double VadcN;
double Iadc;
double Iadc2;
double Iadc2temp;
double IQ215;
double Vacsen;
double VacLsen;
double VacNsen;
double Voutsen;
double Idcsen;
double VacLtemp;
double VacNtemp;

// PWM Parameters
double PWMPeriod;
long PWMDuty;
long Duty;
double MAXDuty;
double MINDuty;
long PWMTest;

// Voltage Loop Parameters
double VoutRefQ15;
double VoltageSaturationFlag;
double GA;
double GAi;
double k2Hz_Cnt;
double count;

// Current Loop Parameters
double CurrentSaturationFlag;
double IKp;
double IKi;
double k50Hz_Cnt;

// Filter Parameters;
double Alpha;
double Beta;

// Voltage Loop Parameters
double VoltageError;
double PreVoltageError;
double VoltageRefTemp;
double VdcQ15;
double Poutput;
double Ioutput;
double PIoutput;
double VoltageCounter;
long PoutputTemp_Long;
long IoutputTemp_Long;

// Current Loop Parameters
double CapCurrentStar;
double Iref;
double IQ15;
double PreIdcQ15;
double CurrentError;
double CurrentPoutput;
double CurrentIoutput;
double CurrentPIoutput;
double CurrentCounter;

long Iref_Long;
long CurrentError_Long;
long CurrentPoutputTemp_Long;
long CurrentIoutputTemp_Long;

// Final Output Parameters
double FinalOutput;
long FinalOutput_Long;

// Other Parameters
double FirstPass;
double SoftStart;
double VacQ15;
double VacLQ15;
double VacNQ15;
double Qlevels;
double POLARITY;
double POLARITY2;
double ENABLE;
double FETHigh;
double FETlow;
double mosenable;

/////////////////////////////////////////////////////////////////////
// FUNCTION: SimulationStep
// This function runs at every time step.
//double t: (read only) time
//double delt: (read only) time step as in Simulation control
//double *in: (read only) zero based array of input values. in[0] is the first node, in[1] second input...
//double *out: (write only) zero based array of output values. out[0] is the first node, out[1] second output...
//int *pnError: (write only) assign *pnError = 1; if there is an error and set the error message in szErrorMsg
//    strcpy(szErrorMsg, "Error message here...");
// DO NOT CHANGE THE NAME OR PARAMETERS OF THIS FUNCTION
void SimulationStep(
    double t, double delt, double *in, double *out,
    int *pnError, char * szErrorMsg,
    void ** reserved_UserData, int reserved_ThreadIndex, void * reserved_AppPtr)
{
    g_nStepCount++;

    // In case of error, uncomment next two lines. Set *pnError to 1 and copy Error message to szErrorMsg
    //*pnError=1;
    //strcpy(szErrorMsg, "Place Error description here.");

    VadcL=in[0];
    VadcN=in[1];
    VadcRef=in[2];
    clock=in[3];
    POLARITY2=in[4]+1;
    Iadc2=in[5];
    Voutsen=in[6];

    if(clock==1)
    {
        ladc2 = Iadc2-512;
        if(ladc2<0){
            ladc2= -ladc2;
        }
        Iadc2temp = ladc2*2.5;
        IQ215 = Iadc2temp*32;
        VdcQ15 = Voutsen*32;
        //VoutRefQ15 = VadcRef*42;
        IQ15 = Iadc * 32;
VacLtemp = VacLtemp + VadcL;
VacNtemp = VacNtemp + VadcN;

if(count > 9){ //was 4 9
    VacLQ15 = VacLtemp/5*32;
    VacNQ15 = VacNtemp/5*32;
    VacLtemp = 0;
    VacNtemp = 0;
    if (VacLQ15 >= VacNQ15){
        VacQ15 = VacLQ15 - VacNQ15;
    }
    else {
        VacQ15 = VacNQ15 - VacLQ15;
    }
    VoutRefQ15++;
    if(VoutRefQ15 > 26040){
        VoutRefQ15 = 26040;
        if((IQ215 > 3500) && (mosenable == 1)){ //for low power < 250W
            was 5000 otherwise ((VacQ15 > 7000) && (mosenable == 1)){
                mosenable = 0;
                if(POLARITY2 > 1){ //positive half cycle
                    FEThigh = 0;
                    FETlow = 1;
                }
                else{ //negative half cycle
                    FETlow = 0;
                    FEThigh = 1;
                }
            }
        }
    }
}

VoltageRefTemp = VoutRefQ15;
VoltageError = VoltageRefTemp - VdcQ15;
VoltageError = VoltageError * Alpha + PreVoltageError * Beta;
PreVoltageError = VoltageError;

Poutput = VoltageError * GA;
if (VoltageSaturationFlag == 0){
    IoutputTemp_Long = IoutputTemp_Long + VoltageError * GAi;
}
if (IoutputTemp_Long > 32767){
    IoutputTemp_Long = 32767;
}
else if (IoutputTemp_Long < -32767){
    IoutputTemp_Long = -32767;
}
Ioutput = (double) IoutputTemp_Long;
PloutputTemp_Long = (long) Poutput + (long) Ioutput;
if (PloutputTemp_Long > 32767){
    PloutputTemp_Long = 32767;
    VoltageSaturationFlag = 1;
}
else if (PloutputTemp_Long < -32767){
    PloutputTemp_Long = -32767;
    VoltageSaturationFlag = 1;
} else{
    VoltageSaturationFlag = 0;
}
Ploutput = (double) PloutputTemp_Long;
CapCurrentStar = PIoutput;

//---------------NEW---------------------
Iref = CapCurrentStar* VacQ15/4096;//32767;

Iref_Long = (long) Iref;
if (Iref_Long > 32767){
    Iref_Long = 32767;
}
else if (Iref_Long < -32767){
    Iref_Long = -32767;
}
//Iref = (double) Iref_Long;
count = 0;
}
count++;
//-------------------------------------------------------------------------------------
if(IQ215 < 1650){  //was 2080 1600 1800
    FETlow = 0;
    FEThigh = 0;
    if(IQ215 < 500){
        mosenable = 1;
    }
}
if(VacQ15 < 640){  //approx. 10V
    ENABLE = 0;
}
if(VacQ15 > 1300){  //approx 20V
    ENABLE = 1;
}

//-------------------------------------------------------------------------------------
CurrentError_Long = Iref_Long - (long) IQ215;
if (CurrentError_Long > 32767)
{
    CurrentError_Long = 32767;
}

else if (CurrentError_Long < -32767)
{
    CurrentError_Long = -32767;
}

CurrentError = (double) CurrentError_Long;

CurrentPoutput = CurrentError * IKp;
if (CurrentSaturationFlag == 0)
{
    CurrentIoutputTemp_Long = CurrentIoutputTemp_Long + CurrentError * IKi;
}

if (CurrentIoutputTemp_Long > 32767)
{
    CurrentIoutputTemp_Long = 32767;
}
else if (CurrentIoutputTemp_Long < -32767)
{
    CurrentIoutputTemp_Long = -32767;
}

CurrentIoutput = (double) CurrentIoutputTemp_Long;

CurrentPLoutputTemp_Long = (long) CurrentPoutput + (long) CurrentIoutput;

CurrentPLoutput = (double) CurrentPLoutputTemp_Long;

FinalOutput_Long = (long) CurrentPLoutput;
if (FinalOutput_Long > 32767)
{
    FinalOutput_Long = 32767;
}
else if (FinalOutput_Long < 0)
{
    FinalOutput_Long = 0;
}

FinalOutput = (double) FinalOutput_Long;

Duty = FinalOutput * PWMPeiod/8192;//16384;//8192;//32767;
if (Duty >= MAXDuty)
{
    CurrentSaturationFlag = 1;
    Duty = MAXDuty;
}
else if(Duty < MINDuty)
{
    Duty = MINDuty;
    CurrentSaturationFlag = 1;
}
else
{
    CurrentSaturationFlag = 0;
}

PWMTes = Duty;
if(POLARITY2 > 1)
{
    PWMTes = PWMPeiod-PWMTes;
if(POLARITY == 0){
    Duty = PWMPeriod-Duty;
}

if(VacQ15 < 3300) {  // approx. 35V was 2300 1440
    if(POLARITY2 > 1) {
        PWMDuty = 2873; // MINDuty;
    } else {
        PWMDuty = 6706; // MAXDuty;
    }
} else {
    PWMDuty = PWMTst; // Duty;
}

out[0] = PWMPeriod;
out[1] = PWMDuty;
out[2] = VacQ15;
out[4] = FETlow;
out[5] = FETHigh;
out[6] = ENABLE;

/////////////////////////////////////////////////////////////////////
// FUNCTION: SimulationBegin
// Initialization function. This function runs once at the beginning of simulation
// For parameter sweep or AC sweep simulation, this function runs at the beginning of each simulation cycle.
// Use this function to initialize static or global variables.
// const char *szId: (read only) Name of the C-block
// int nInputCount: (read only) Number of input nodes
// int nOutputCount: (read only) Number of output nodes
// int nParameterCount: (read only) Number of parameters is always zero for C-Blocks. Ignore nParameterCount and pszParameters
// int *pnError: (write only) assign *pnError = 1; if there is an error and set the error message in szErrorMsg
// strcpy(szErrorMsg, "Error message here... ");
// DO NOT CHANGE THE NAME OR PARAMETERS OF THIS FUNCTION
void SimulationBegin(
    const char *szId, int nInputCount, int nOutputCount,
    int nParameterCount, const char ** pszParameters,
    ...
int *pnError, char * szErrorMsg,
void ** reserved_UserData, int reserved_ThreadIndex, void * reserved_AppPtr)
{
    g_nInputNodes = nInputCount;
    g_nOutputNodes = nOutputCount;

    // In case of error, uncomment next two lines. Set *pnError to 1 and copy Error message to szErrorMsg
    //*pnError=1;
    //strcpy(szErrorMsg, "Place Error description here.");

    Qlevels=1024;

    // PWM Parameters
    PWMPeriod = 9579;
    Duty = 0;
    MAXDuty = 0.99 * PWMPeriod;
    MINDuty = 0.01*PWMPeriod;
    PWMDuty = 4789;
    PWMTest = 4789;

    // Voltage Loop Variable
    VoltageRefTemp = 0;
    VdcQ15 = 0;
    VoltageError = 0;
    PreVoltageError = 0;
    Poutput = 0;
    Ioutput = 0;
    VoltageCounter = 0;
    PIoutputTemp_Long = 0;
    IoutputTemp_Long = 0;
    VoltageSaturationFlag = 0;
    k2Hz_Cnt = 50;
    VoutRefQ15 = 19400; // was 24970;
    count = 6;

    // Current Loop Variables
    CapCurrentStar = 0;
    Iref = 0;
    IQ15 = 0;
    IQ215 = 0;
    CurrentError = 0;
    CurrentPoutput = 0;
    CurrentIoutput = 0;
    CurrentPIoutput = 0;
    CurrentCounter = 1;
Iref_Long = 0;
CurrentError_Long = 0;
CurrentPloutputTemp_Long = 0;
CurrentIoutputTemp_Long = 0;
CurrentSaturationFlag = 0;
k50Hz_Cnt = 2;

// Final PI Output
FinalOutput = 0;
FinalOutput_Long = 0;

// Filter Parameters
Alpha = 0.4; //0.09
Beta = 0.6; //0.91

// Other Parameters
FirstPass = 1;
SoftStart = 1;
POLARITY = 0;
ENABLE = 1;
VacLtemp = 0;
VacNtemp = 0;
FEThigh = 0;
FETlow = 0;
mosenable = 0;

// Controller Parameters
GA = 0.15; //was 0.005 0.01 0.02 0.05 0.07 0.09
GAI = 0.001; //was 0.001
IKp = 0.2; //was 0.2
IKi = 0.015; //was 0.01

}

/////////////////////////////////////////////////////////////////////
// FUNCTION: SimulationEnd
// Termination function. This function runs once at the end of simulation
// For parameter sweep or AC sweep simulation, this function runs at the end of each simulation cycle.
// Use this function to de-allocate any allocated memory or to save the result of simulation in an alternate file.
// Ignore all parameters for C-block
// DO NOT CHANGE THE NAME OR PARAMETERS OF THIS FUNCTION
void SimulationEnd(const char *szId, void **reserved_USERData, int reserved_ThreadIndex, void *reserved_AppPtr)
{
}

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Appendix C – Screenshots from GaN Gate Resistance Tuning

GaN gate signals with 50/2 Ohm resistances. High side in cyan, low side in green.
GaN gate signals with 30/2 Ohm resistances. High side in cyan, low side in green.
GaN gate signals with high side 20/2 Ohm resistance in the top two images and low side 20/2 Ohm resistance in the bottom two images.
GaN gate signals with high side 10/2 Ohm resistance in the top two images and low side 10/2 Ohm resistance in the bottom two images.