LOW-NOISE MIXING CIRCUITS
IN CMOS MICROWAVE INTEGRATED CIRCUITS

by

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Abstract

In this thesis, three low-noise active mixing circuits are presented in CMOS technology. Mixers can be found at the front-end of almost every communication systems. However, despite many advantages the active mixers have, one drawback is their poor noise performance. One mixer that has been widely used in integrated circuit is the Gilbert cell. This thesis demonstrated that by merging the low-noise amplifier (LNA) with the Gilbert cell, a low-noise active mixer can be realized. This kind of mixer relaxes the front-end design, allows higher circuit integration, and reduces power consumption.

The first circuit is a narrowband low-noise mixer that operates at 5.4 GHz in 0.18 \( \mu \text{m} \) CMOS. An inductive degenerated LNA is used as the transconductor. Together with a current bleeding circuit, a gain of 13.1 dB and a low 7.8 dB single-sideband noise figure are achieved. The circuit was fabricated and measured. Simulation and measurement results are compared and discussed.

The second circuit is a broadband low-noise mixer that operates between 1 and 5.5 GHz in 0.13 \( \mu \text{m} \) CMOS. The noise-cancelling technique is used to design the transconductors. This technique does not require the use of inductors while able to achieve a sub 3 dB noise figure and input matching over a large bandwidth. To further extend the mixer bandwidth, the series inductive peaking was used. Measured and
simulated results showed great agreement. It has a high gain of 17.5 dB, a bandwidth of 4.5 GHz, and a low average double-sideband noise figure of 3.9 dB. This mixer has the best broadband noise performance ever reported in CMOS.

Finally, a double-balanced low-noise self-oscillating mixer (SOM) in 0.13 µm CMOS is presented. This is a current-reuse, highly integrated circuit that combines an LNA, mixer, and oscillator seamlessly into a single component. The oscillator generates the required LO while serving as the mixer load simultaneously. Measured and simulated results showed excellent agreement. A low double-sideband noise figure of 4.4 dB and a gain of 11.6 dB were measured. This type of SOM and loading structure are the first ever reported.
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Nomenclature

Latin Symbols

\( A_v \)  
Voltage Gain \([\text{V/V}]\)

\( C_{cb} \)  
Channel to Bulk Capacitance \([\text{F}]\)

\( C_{gd} \)  
Gate to Drain Capacitance \([\text{F}]\)

\( C_{gs} \)  
Gate to Source Capacitance \([\text{F}]\)

\( C_{ox} \)  
Gate Oxide Capacitance per Unit Area \([\text{F/mm}^2]\)

\( F \)  
Noise Factor

\( f \)  
Frequency \([\text{Hz}]\)

\( f_c \)  
Flicker Noise Corner Frequency \([\text{Hz}]\)

\( f_{1F} \)  
Frequency of the IF signal \([\text{Hz}]\)

\( f_{LO} \)  
Frequency of the LO signal \([\text{Hz}]\)

\( F_{min} \)  
Minimum Noise Factor

\( f_{RF} \)  
Frequency of the RF signal \([\text{Hz}]\)

\( f_T \)  
Unity current gain frequency \([\text{Hz}]\)

\( \Delta f \)  
System Bandwidth \([\text{Hz}]\)

\( G \)  
Gain

\( g_{d0} \)  
Drain-Source Conductance at \( V_{DS} = 0 \text{ V} \) \([\text{A/V}]\)

\( g_m \)  
Transconductance \([\text{I/V}]\)

\( g_{mb} \)  
Back Gate Transconductance \([\text{I/V}]\)

\( |i_{nd}|^2 \)  
Drain Current Noise Spectral Density \([\text{A}^2/\text{Hz}]\)

\( |i_{nd,\text{sub}}|^2 \)  
\( |i_{nd}|^2 \) from the Substrate\([\text{A}^2/\text{Hz}]\)

\( |i_{ng}|^2 \)  
Gate Current Noise Spectral Density \([\text{A}^2/\text{Hz}]\)

\( k \)  
Boltzmann’s constant \([\text{J/K}]\)

\( L \)  
Transistor Gate Length \([\mu\text{m}]\)

\( Q \)  
Quality Factor

\( q \)  
Electron Charge \([\text{C}]\)

\( R_{\text{load}} \)  
Load Resistance \([\Omega]\)

\( R_n \)  
Noise Resistance \([\Omega]\)

\( r_o \)  
Transistor Drain-Source Resistance at Saturation \([\Omega]\)

\( R_{\text{sub}} \)  
Substrate Resistance \([\Omega]\)

\( T \)  
Absolute Temperature \([\text{K}]\)
$V_{bd}$  Bleeding Circuit Bias Voltage [V]
$V_{DD}$  DC Supply Voltage [V]
$V_D$  DC Drain-Source Voltage [V]
$V_{DS_{\text{sat}}}$  DC Drain-Source Voltage at Saturation [V]
$V_{GS}$  DC Gate-Source Voltage [V]
$V_{IF}, v_{IF}$  Signal Voltage at IF [V]
$v_{in}$  Differential Input Voltage [V]
$V_{LO}, v_{LO}$  Signal Voltage at LO [V]
$|v_{ng}|^2$  Gate Voltage Noise Spectral Density $[V^2/\text{Hz}]$
$V_{RF}, v_{RF}$  Signal Voltage at RF [V]
$V_T$  Transistor Threshold Voltage [V]
$W$  Transistor Width [$\mu$m]
$Y_{\text{opt}}$  Optimum Source admittance [S]
$Z_0$  Characteristic Impedance [$\Omega$]
$Z_{\text{opt}}$  Optimum Source Impedance [$\Omega$]

Greek Symbols

$\gamma$  Transistor Noise Coefficient
$\gamma_{\text{eff}}$  Effective Transistor Noise Coefficient
$\delta$  Gate Noise Coefficient
$\omega$  Angular Frequency [rad/s]
$\omega_{IF}$  Angular frequency of the IF signal [rad/s]
$\omega_{LO}$  Angular frequency of the LO signal [rad/s]
$\omega_{RF}$  Angular frequency of the RF signal [rad/s]
$\omega_T$  Unity Current Gain Angular Frequency [rad/s]
$\mu_n$  electron mobility $[\text{cm}^2/\text{V} \cdot \text{s}]$

Acronyms

A/D  Analog-to-Digital Converter
ADS  Advanced Design System (from Agilent)
AM  Amplitude Modulation
AMOS  Accumulation-mode Metal Oxide Semiconductor
CG  Voltage Conversion Gain [V/V]
CMOS  Complimentary Metal Oxide Semiconductor
CMRR  Common-Mode Rejection Ratio
CPW  Coplanar waveguide
DC  Direct Current
DSB  Double-Sideband
FET  Field Effect Transistor
GaAs  Gallium arsenide
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>GSG</td>
<td>Ground-Signal-Ground</td>
</tr>
<tr>
<td>GSGSG</td>
<td>Ground-Signal-Ground-Signal-Ground</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>IBM</td>
<td>International Business Machines Corporation</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input-referred Third-Order Intercept Point</td>
</tr>
<tr>
<td>IM3</td>
<td>Third-order Intermodulation Products</td>
</tr>
<tr>
<td>LNA</td>
<td>Low noise amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>MMIC</td>
<td>Microwave Monolithic Integrated Circuit</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>n-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>NF&lt;sub&gt;DSB&lt;/sub&gt;</td>
<td>Double-Sideband Noise Figure</td>
</tr>
<tr>
<td>NF&lt;sub&gt;SSB&lt;/sub&gt;</td>
<td>Single-Sideband Noise Figure</td>
</tr>
<tr>
<td>P&lt;sub&gt;1dB&lt;/sub&gt;</td>
<td>1 dB Compression Point</td>
</tr>
<tr>
<td>PCSNIM</td>
<td>Power Constrained SNIM</td>
</tr>
<tr>
<td>PMOS</td>
<td>p-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SNIM</td>
<td>Simultaneous Noise and Input Match</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-a-Chip</td>
</tr>
<tr>
<td>SOM</td>
<td>Self-Oscillating Mixer</td>
</tr>
<tr>
<td>SSB</td>
<td>Single-Sideband</td>
</tr>
<tr>
<td>TSMC</td>
<td>Taiwan Semiconductor Manufacturing Company</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 General Introduction

As technology advances, the demand for compact, multi-functional, low-power wireless electronics is growing. During the past decade, the size of the electronic systems has changed from bulky units such as the first generation analog cell phones to wireless devices of very small size. Not only do these compact devices attract consumers, but also reduce manufacturing costs. This trend will continue in the foreseeable future as System-on-a-Chip (SoC) continues to increase in complexity.

CMOS has been the dominant technology in digital applications due to its low-cost and high yield. It has also attracted microwave monolithic integrated circuit (MMIC) engineers to this technology as an alternative to other, more expensive and lower yield technologies, such as GaAs. Therefore CMOS has been in constant development and imported into the RF/microwave analog realm. Many passive components such as inductors and capacitors have been given much attention to make them possible in CMOS. Furthermore, with the constant scaling of the transistor gate lengths, the
frequency limit of the technology has been increasing and it is becoming the MMIC technology of choice in the microwave range for small-signal applications [1–3].

In a typical receiver architecture, a receiver is composed of building blocks such as low-noise-amplifiers (LNA), mixers, oscillators, and demodulators that are application specific. The characteristics of these building blocks are different in order to meet different standards such as GSM and WCDMA. Due to the advancement of digital hardware, receivers are becoming simpler as digital signal processing is replacing many analog building blocks such as modulators and demodulators. Figure 1.1 shows a block diagram of a typical heterodyne receiver.

LNA’s and mixers are important components at the receiver front-end. Proper designs are paramount in order to meet the strict requirements of a particular standard. These components are normally designed separately and compromises in terms of performance of the individual block usually need to be made during system integration. The filters shown in Figure 1.1 are normally off-chip passive filters since it is very difficult to realize high Q narrow-band filters on chip. Passive or active mixers can be used depending on the receiver requirement. However, active mixers are usually preferred as they can provide gain to compensate the loss from the filters.

![Figure 1.1: Block diagram of a typical receiver.](image-url)
A well-known active mixer is the Gilbert cell mixer [4]. It has been widely used in IC design due to its gain, high port-to-port isolation, and compact size. However, the noise figure (NF) of a typical Gilbert cell mixer can be quite high, around 15 dB single-sideband in most cases [5].

One of the key parameters of a receiver is its signal-to-noise ratio (SNR). It can also be characterized by its noise figure. Noise is particularly important in receivers. The dynamic range, bit-error-rate are all related to system noise and how well the receiving system interprets the input signal. The overall NF of a receiving system depends on the noise and gain of each individual stage and their relationship can be described by the Friis equation [6],

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_n - 1}{G_1 \cdots G_{n-1}}$$  \hspace{1cm} (1.1)

where $F_n$ is the noise factor of the $n^{th}$ and $G_n$ is the gain of the $n^{th}$ stage. It can be seen that the noise and gain of the first few stages have a large impact on the overall system noise. This is so because as the input signal gets amplified, the noise of subsequent stages become less important. Thus the overall NF is dominated by the first few stages. In order to achieve a good NF, the first few stages, namely the LNA and mixer, must be carefully designed [5].

In contrast to single-diode or single transistor mixers, the Gilbert cell mixer exhibits high noise due to its use of at least six transistors. The filters at the front-end also have an impact on the system noise figure. They impose a strict requirement for the noise figure of the LNA preceding the mixer to achieve a particular signal to noise ratio. This usually requires either one very low noise LNA or two LNA’s in cascade that have enough total gain and low noise figure to suppress the noise from the mixer.
Designing a very low noise LNA with high gain and high input 1 dB compression point (the power level at which the gain is compressed by 1 dB) is difficult to achieve in the microwave range and above. Power consumption is also a problem as the LNA noise figure decreases when larger transistors are used. Having two LNA’s increases power consumption and chip space, which translates to costs. Furthermore, the high gain from the LNA’s might drive the mixer into saturation when a high power interferer is presented at the input [7]. Not only does this compromise the system performance, but also complicates the design process. However, these design requirements can be much relaxed if the mixer block exhibits a low noise figure and a good amount of gain [8]. With a low-noise mixer, the noise or gain requirements of the first LNA stage can be relaxed and still meet or exceed the performance goals of the receiver. In some cases, it is possible to simply eliminate the preceding LNA in the system [5, 9].

In this thesis, the noise performance of the Gilbert cell mixer is improved by developing new circuit topologies. The classic Gilbert cell is selected in this thesis as the starting point because it is one of the most widely used mixers in communication applications. By reconfiguring the Gilbert cell, all of its aforementioned attributes in terms of gain and port-to-port isolation can be retained in addition to low noise figure.

As a starting point, the noise figure of the Gilbert cell mixer can be drastically reduced by combining the LNA and the mixer into a single component. This type of current-reuse structure is favourable in low-cost and low-power applications. It can be easily achieved by replacing the transconductor by an LNA. The first low-noise mixer demonstrated is a fully-integrated Gilbert cell at 5.4 GHz. The low-noise transconductors, designed with inductive degeneration, together with the current bleeding
technique significantly lower the noise figure while maintaining a reasonable gain and IIP3 at the same time. The second design is a novel broadband low-noise Gilbert cell mixer that employs an active noise-cancelling technique. Noise cancellation has been known in LNA design and the technique is utilized in the transconductor for broadband input matching and noise reduction. This broadband and low-noise characteristic is well suited for multi-band, multi-standard receivers. The third design is a new low-noise self-oscillating mixer (SOM). Three different components, namely an oscillator, a mixer, and a LNA, are merged seamlessly to form a super-current-reuse structure. A negative gm oscillator is reconfigured to sit above a low-noise Gilbert cell core while serving as a fully balanced load and providing an LO signal to the mixer at the same time. This SOM is a fully balanced, differential structure that uses no resistive loads at which precious voltage headroom may be lost. By incorporating this SOM into a receiver such as the one shown in Figure 1.1, the receiver structure is simplified; it has less components; and power consumption is significantly reduced.

The following is a brief summary of the contributions of this thesis:

- The low-noise mixer with inductive degeneration is a fully integrated CMOS low-noise mixing circuit designed at 5.4 GHz in 0.18 μm CMOS. It has a great single-sideband noise figure of 7.8 dB and a power conversion gain of 13.1 dB. The input $P_{1dB}$ and IIP3 are $-17.8$ dBm and $-6.2$ dBm respectively. All of the inductors are on-chip and the size of the mixer core is only 380 μm x 350 μm (0.133 mm²).

- The broadband low-noise mixer with noise cancellation was designed in standard CMOS 0.13 μm technology that operates between 1 to 5.5 GHz. Measured results show excellent noise and gain performance across the frequency span,
with an average double-sideband noise figure of 3.9 dB and a conversion gain of 17.5 dB. It has an input $P_{1dB}$ of $-10.5$ dBm and an IIP3 of $+0.84$ dBm at 5 GHz. $S_{11}$ is less than $-8.8$ dB across the entire band and the mixer is also very compact with the size of the mixer core only being 0.315 mm$^2$.

- The double-balanced low-noise self-oscillating mixer was also designed in standard CMOS 0.13 μm technology that downconverts a 8 GHz signal to 300 MHz. Measured results showed great noise and gain performance. The measured $N_{F_{DSB}}$ was 4.4 dB with a power conversion gain of 11.6 dB. It has an input $P_{1dB}$ of $-13.6$ dBm and an IIP3 of $-8.3$ dBm. A good input match at the RF input was obtained, with an $S_{11}$ of $-12$ dB. The design was very compact, with the core occupying an area of 0.47 mm$^2$.

1.2 Thesis Organization

The thesis is organized as follows:

Chapter 2 begins with an overview of different types of mixers as well as an analysis of the Gilbert cell mixer. A brief review on transistor noise is provided next, and it is followed by an in-depth noise analysis of the Gilbert cell. Finally, different types of noise reduction techniques that have been previously proposed by other researchers are discussed.

Chapter 3 introduces the low-noise mixer with inductive degeneration. The designs of the individual parts within the mixer are given in detail with a strong emphasis on the transconductor design. The circuit performance is then confirmed by both simulation and measurement results.
CHAPTER 1. INTRODUCTION

The novel broadband low-noise mixer is described in Chapter 4. A quick review of the active noise-cancelling theory is provided followed by a theoretical design analysis on the low-noise transconductor and an explanation of the inductive peaking technique. Finally, simulation and measurement results are presented and discussed.

Chapter 5 presents the new low-noise self-oscillating mixer. The operation of the self-oscillating mixer is studied in detail. The designs of a negative gm oscillator as well as each of the mixer’s individual part follow, concluding the chapter with simulation and measurement results.

Chapter 6 concludes the thesis with a summary of the performances of and the benefits from the mixers. Performance enhancement and modification recommendations for future work are also included.
Chapter 2

Literature Review

2.1 Introduction

Since mixers are inherently non-linear systems, it is especially important to understand their operation to gain any design insight. This chapter provides background information on basic mixing circuits with a strong emphasis on the Gilbert cell mixer. Before proceeding to an in-depth analysis on mixer noise, there will be a brief review of transistor noise where both thermal and flicker noise are discussed. Finally, a literature review on mixer noise reduction techniques and their benefits and disadvantages are given at the end. Because this thesis focuses on down-converting mixers, the mixers discussed herein refer to down-converting mixers unless otherwise stated.

2.2 Mixer Overview

In contrast to linear systems where one wants to suppress harmonics and nonlinear terms, mixers require non-linearities in the circuit to function. This section gives an
overview on the subject and some of the basic mixing circuits being used today.

In essence, a mixer multiplies two signals based on the following equation,

\[ Y_1 = A_1 \cos(\omega_1 t) \quad \text{and} \quad Y_2 = A_2 \cos(\omega_2 t) \]
\[ Y_1 Y_2 = \frac{A_1 A_2}{2} \left\{ \cos[(\omega_1 + \omega_2) t] + \cos[(\omega_1 - \omega_2) t] \right\} \] \hspace{1cm} (2.1)

Thus, depending on \( \omega_1 \) and \( \omega_2 \) and the side band that is chosen, the signal is either up-converted \((\omega_1 + \omega_2)\), down-converted \((\omega_1 - \omega_2)\), or directly converted \((\omega_1 + \omega_2 = 2\omega_2 \text{ or } \omega_1 - \omega_2 = 0)\). Besides the signal frequency of interest, there exists an image frequency \( (f_{image}) \) on the other side of the LO with respect to the RF signal that will fall into the same IF after down conversion. Typically, the image signal is prevented from being down converted into the band of interest.

The problem of spurious response is a serious one. Spurious response arises when unwanted signals at different frequencies are up or down converted into the band of interest. Due to non-linearities in the active devices, the harmonics of the spurious signal and LO mix as well. It is sometimes possible for the mixing products of the harmonics to land at the same frequency of interest as the signal. Those harmonics can be calculated using the equations shown in Table 2.1, where \( f_{RF} \) is the signal frequency, \( f_S \) is the spurious frequency, \( f_{IF} \) is the frequency of interest, \( n \) is the \( n^{th} \) harmonics of the LO, and \( m \) is the \( m^{th} \) harmonics of the spurious signal. If the above

<table>
<thead>
<tr>
<th></th>
<th>[ n(1 - f_{RF}/f_{IF}) + m f_S/f_{IF} = 1 ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sum Mixer</td>
<td></td>
</tr>
<tr>
<td>Difference Mixer (High Side LO)</td>
<td>[ n(f_{RF}/f_{IF} + 1) - m f_S/f_{IF} = \pm 1 ]</td>
</tr>
<tr>
<td>Difference Mixer (Low Side LO)</td>
<td>[ n(f_{RF}/f_{IF} - 1) - m f_S/f_{IF} = \pm 1 ]</td>
</tr>
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</table>

Table 2.1: Mixer spurious response [7].
equation with respect to the specific mixer is satisfied, then the mixing products due to the harmonics will appear in the IF band [7]. Generally for down converters, the lower the IF, the less spurious responses there are. However, if the IF is too low, it can be difficult to filter out the image frequency, as both the image and signal frequencies move closer to the LO.

Mixer noise analysis is not as straight forward as linear time invariant noise analysis where there is no frequency translation. The main difference is the ever-present image frequency. As discussed above, signals from both the RF and the image frequency are down-converted into the same IF band and they cannot be distinguished after down-conversion. The noise at the image frequency, therefore, gets down-converted and added to the down-converted RF noise. This process is known as “noise folding” and is shown in Figure 2.1 [10]. Assuming a flat white noise spectrum at the input of a noiseless mixer with 0 dB gain across the entire spectrum, the noise folding action reduces the SNR at the IF output by half, which translates to a 3 dB noise figure. The noise figure defined in this case is called single-sideband noise figure (NF_{SSB}) as the signal only appears in one of the sidebands. However, if the signal appears at both of the sidebands, then the ideal noise figure is 0 dB. Figure 2.2 shows the two cases where the signal appears at both sidebands. Figure 2.2 (a) shows a downconversion to IF. With a 0 dB gain mixer, the noise and signals at both bands get folded together, thus the SNR stays the same and the NF is 0 dB. Figure 2.2 (b) shows a

![Figure 2.1: Noise folding around IF for a single-sideband signal after [10].](image-url)
CHAPTER 2. LITERATURE REVIEW

Figure 2.2: Double-sideband noise folding: (a) at IF and (b) direct conversion.

direct downconversion. Again, the NF is 0 dB because the signal appears at both sidebands. The noise figure defined in these cases is called the double-sideband noise figure (\(\text{NF}_{\text{DSB}}\)).

Ideally, the LO should be pure sinusoidal. However, LO harmonics are always present due to oscillator non-idealities. The effect of the LO harmonics can be seen in Figure 2.3. The noise components near the LO harmonics are mixed and translated to the IF, which further increases the noise figure. However, this effect is not very significant because of the limited RF input bandwidth and gain roll-off at high frequencies [10].

Figure 2.3: Noise at different frequencies get downconverted to IF by LO and its harmonics from [8] with permission ©1999 IEEE.
2.2.1 Passive Mixers

Passive mixers do not require any DC power to operate. Most types of diode and superconductor mixers fall into the passive mixer category. They have been widely used in microwave applications due to their simplicity, low noise figure, and their ability to operate at frequencies that are not accessible to transistor-based mixers. However, due to their passive nature, there is conversion loss instead of gain.

The simplest diode mixer is the single diode circuit shown in Figure 2.4. It has the lowest conversion loss relative to other diode topologies [11]. The mixing occurs as a result of the non-linear I-V curve of the diode. The diode current is related to the voltage across its terminals by

$$i(t) = I_S(e^{\frac{q}{kT}v(t)} - 1)$$  \hspace{1cm} (2.2)

where $I_S$ is the saturation current, $q$ is the electron charge, $k$ is Boltzmann’s constant, $T$ is the absolute temperature in Kelvin, and $n$ is the diode ideality factor. The voltages at the RF and LO ports are added in the frequency domain. The following relationship is obtained after expanding Equation (2.2) and retaining the first three
terms \[12\],
\[
i(t) = I_0 + G_d[v_{RF}(t) + v_{LO}(t)] + \frac{G'_d}{2}[v_{RF}(t) + v_{LO}(t)]^2 + \cdots \tag{2.3}
\]
where \(G_d\) and \(G'_d\) are the diode dynamic conductances and \(I_0\) is the DC current. It can be easily seen that the third term of the equation leads to frequency mixing.

It can also been seen that a series of mixing products, besides the mixing product of interest, are also generated across the frequency spectrum. LO-to-IF and RF-to-IF feedthrough is inevitable in this design. These characteristics are undesirable because a large LO power, or the power of the mixing products may drive the next stage, usually an IF amplifier, into saturation. Thus, a low-pass or a bandpass filter tuned to the IF is placed after the diode to remove the harmonics and feedthrough signals. It is also important to short the input at the IF to minimize its effect on the input of the device. Usually, an RF choke placed in shunt with the input will suffice. Not only does it act as a filter for the IF, but it also provides a DC path for the rectified LO current to flow in. Otherwise, a negative DC voltage would develop and affect the mixing behaviour \[7\].

The RF and LO port isolation is usually very poor in this design since the ports are directly connected. RF and LO filters can be placed at the input of each port to filter the unwanted signal and provide input matching at the same time. However, the RF and LO frequency are usually very close. This can require a very high Q bandpass filter, which is difficult to achieve at high frequencies.

A single-balanced diode mixer is able to obtain good port-to-port isolation from LO-IF and RF-LO. The circuit of a typical single-balanced diode mixer is shown in Figure 2.5. Essentially, the diodes, driven by the large LO signal, act as switches.
Figure 2.5: Single-balanced diode mixer.

The on-off action of the switches can be idealized by a square-wave. The IF output is therefore the product of the RF signal multiplied by a square-wave, hence the mixing action.

To simplify the single-balanced mixer analysis and understand why it is a balanced mixer, an assumption that the diodes are perfect switches should be made. The balun first transforms the single-ended LO into a differential signal. Since the diodes are connected in reverse, their conductances are in-phase, meaning they both turn on and off together. When the LO turns positive, both diodes are on and the RF is directly connected to the IF. Shown in Figure 2.6, the RF signal is a common-mode signal and adds constructively at the IF port. When the LO is negative, the RF port is disconnected from the IF port.

It is evident that there is high isolation between LO and IF. The balanced LO

Figure 2.6: Phase relationships between RF, LO, and IF describing the mixing action after [11].
signal appears across two identical diodes with the IF connected at the middle. That mid-point is in fact a virtual ground for the LO. Very high LO-to-IF isolation can thus be achieved, and hence the name “balanced” mixer. It also has the ability to reject AM noise from the LO due to the same mechanism. The LO noise that appear at the inputs of the diodes are correlated and $180^\circ$ out of phase, which behaves exactly like the LO. The IF port becomes a virtual ground for the noise signal so no LO noise appears at the IF. Besides LO noise rejection, spurious responses from even order mixing products are also rejected. The dynamic range increases as well because the RF signal is divided between two diodes. However, a larger LO drive compared to single-ended designs is required and there is no isolation between the RF and IF port.

In contrast to single-ended diode design, the performance of the single-balanced mixer depends heavily on the performance of the balun. The transformer shown in Figure 2.5 only applies to low frequencies. At high frequencies, microwave couplers are needed. A wide range of $90^\circ$ and $180^\circ$ couplers can be used to achieve the same performance as the transformer [13]. They can also be used in MMIC at very high frequencies. An MMIC version of a microwave coupler single-balanced mixer was demonstrated in [14] where the operating frequency is at 94 GHz.

Double-balanced mixer is introduced to provide high isolations between all ports, LO noise cancellation, broad-bandwidth, higher dynamic range, and even-mode harmonics from both RF and LO rejection [15]. It consists of two baluns and four diodes connected in ring, star or bridge configuration. Shown in Figure 2.7 is a double-balanced mixer in a ring configuration. Its operation is very similar to the single-balanced mixer. The large LO power switches the diodes to achieve mixing. During the positive LO cycle, the left two diodes are on. Assuming RF is positive,
the IF current will be flowing into the transformer. During the negative LO cycle, the right two diodes are on and the IF current will be flowing out of the transformer.

Unlike the single-balanced mixer, the IF port is connected to the virtual ground of the RF transformer. This provides high RF-to-IF isolation. It is also intuitive that there are high LO-to-RF and LO-to-IF isolations since the outputs of the RF transformer are connected to the virtual LO grounds and the outputs of the LO are connected to the virtual IF grounds. Furthermore, the even-order harmonics generated by the diodes are rejected because they are common-mode signals. The dynamic range is high as the RF power is distributed across the four diodes that leads to an increase in IIP3 and P_{1dB}. However, it requires more LO power to drive four diodes.

As in the case with single-ended diode design, the performance greatly depends on the balun structures. Typical conversion loss is around 6 dB, isolation of 30 dB, and P_{1dB} of 1 dBm [5]. Higher linearity can be achieved at the expense of LO power. The performance also greatly depends on the diodes. A fully-integrated double-balanced diode mixer is demonstrated in [16] where wide bandgap diodes and large LO power
were used to improve linearity significantly. Other double-balanced configurations such as the star double-balanced mixer are also widely used at millimeter-wave frequencies and in MMIC form [17].

The above mentioned diode mixers can be reconfigured for FETs. The transistors can be connected in a double-balanced manner similar to Figure 2.7 as in Figure 2.8. The FET passive mixers retain the diode mixers properties in terms of high linearity and low noise. The advantage of FET’s is they require less LO power than diodes to operate. The FET configuration is very favourable in CMOS because of the excellent switches offered by the technology. However, there are limitations of passive FET mixers, one of which is the relatively lower frequency response than that of diode mixers.

Figure 2.8: Passive double-balanced FET mixer.

2.2.2 Active Mixers

Although passive mixers are able to operate in the 100 GHz and Terahertz range, one drawback is the associated conversion loss. On the other hand, active mixers
are able to provide gain at the cost of a higher noise figure and lower bandwidth. Conversion gain is important in receiver design because it reduces the number of amplifiers needed in the system. Without conversion gain, the noise performance of a receiver can be compromised and the design of the IF stage becomes critical [15]. Thus, much of the design requirement for the IF stage can be lifted with the help of active mixers. Furthermore, the growth of CMOS for microwave applications favours transistor-based mixer designs.

The simplest active mixer is a single-ended mixer. Similar to its single diode counterpart, poor port-to-port isolation requires filters at each port to filter out unwanted mixing products and feedthroughs. Two typical single FET configurations are shown in Figure 2.9. Essentially, the large LO changes the transistor’s bias point and in turn changes its transconductance ($g_m$). For the gate-pumped mixer in Figure 2.9 (a), the transistor is biased at pinch-off where it experiences the largest non-linearity while still in saturation. Thus a small change in $V_{GS}$ leads to a large change in $g_m$. The LO continuously pumps the $g_m$ from a low state to a high state and vice versa to achieve the desired mixing behaviour. The transconductance can be quantified by

![Figure 2.9: Single FET mixers: (a) gate-pumped and (b) drain-pumped.](image-url)
the following equation [12].

\[ g(t) = g_0 + 2 \sum_{n=1}^{\infty} g_n \cos(n \omega_{LO} t) \] (2.4)

and the power conversion gain assuming all ports are matched is

\[ G = \frac{g_1^2 R_d}{4 \omega_{RF}^2 C_{gs}^2 R_i} \] (2.5)

where \( R_d \) is the output resistance and \( R_i \) is the input resistance of the transistor. The RF-to-LO isolation is very poor. High Q filters or microwave couplers are required to separate the two ports. A low-pass filter at the output is also required to filter out the RF and LO feedthroughs.

The drain-pumped configuration in Figure 2.9 (b) has several advantages over the gate-pumped mixer. Since the RF and LO, which are usually very close, are feeding into different ports, there is higher isolation between the RF and LO as the transistor is a voltage-controlled-current-source. However, the isolation is limited by \( C_{gd} \). The transistor in this configuration is biased just at saturation, with \( V_{DS} = V_{DS_{sat}} \) and \( V_{GS} > V_T \). The non-linearity achieved in this case is more pronounced [18]. Recent designs using both configuration can be seen in [19] for the gate-pumped mixer and [20] where a sub-harmonic mixer is designed based on the drain-pumped mixer.

A dual-gate FET can be used to improve the LO-RF isolation. Two transistors are connected in cascode as in Figure 2.10. Better isolation is expected because the LO and RF feed into different ports and it is limited by \( C_{gs} \) and \( C_{gd} \). The transistor at the bottom is biased at the edge between triode and saturation while the top transistor is biased in the saturation region. The bottom transistor is the primary mixer while
the top transistor is both a common-gate amplifier and a source-follower. To achieve mixing, the LO signal modulates the $V_{DS}$ of the bottom transistor. Therefore, the Dual-gate mixer is essentially a drain-pumped mixer. Due to its simplicity and low power consumption, it is still in use in receiver designs [21].

The mixing action for the aforementioned active mixers is caused by the changing of transconductance. Besides the desired mixing product, a wide range of undesired spectral components are also generated. In addition to poor port isolation, filters are placed with a heavy burden to prevent overloading the IF amplifier and the LO signal from re-radiating back out through the antenna. Furthermore, filters are generally off-chip because on-chip filters with high Q are hard to realize. This increases the manufacturing costs and assembly process. Single-balanced mixers are able to offer high LO-to-RF and RF-to-IF isolation as well as gain. In contrast to passive balanced mixers, no hybrids are required.

The mixer consists of three transistors and two load resistors as depicted in Figure 2.11 (a). The bottom transistor is the transconductor which converts the incoming RF voltage into a current. The top two transistors form a switching pair.
Figure 2.11: Single-balanced FET mixer: (a) circuit schematic and (b) mixer operation.

by a large LO signal, the current from the transconductor is steered into different branches. Figure 2.11 (b) shows an idealized version of the mixer. To understand the current steering action, one could view the switching pair as a differential amplifier. In a differential amplifier, full current steering happens if the applied differential voltage exceeds the maximum allowed voltage, which is given by the following [22],

\[ |v_{in}|_{\text{max}} = \sqrt{2}(V_{GS} - V_T) \]  

(2.6)

With a large LO, current can be steered or commutate from one side to the other at the LO frequency. The tail RF current is effectively multiplied by a square-wave. The mixing action is therefore in the current domain. This type of mixer is known as a current-commutating mixer.

To calculate the voltage conversion gain, the switching action is idealized by a square-wave, whose function can be approximated by

\[ f_{\text{square wave}}(t) = \frac{4}{\pi} \cos(\omega_{LO} t) - \frac{4}{3\pi} \cos(3\omega_{LO} t) + \frac{4}{5\pi} \cos(5\omega_{LO} t) + \cdots \]  

(2.7)
The differential switching pair cancels out the even-ordered harmonics as they are common-mode signals. The current through the IF loads is therefore equal to

\[ I_{IF} = [I_{DC} - g_m V_{RF} \cos(\omega_{RF}t)] f_{\text{square wave}}(t) \]

\[ = \frac{4}{\pi} I_{DC} \cos(\omega_{LO}t) - \frac{2}{\pi} g_m V_{RF} [\cos(\omega_{RF} - \omega_{LO}t) + \cos(\omega_{RF} + \omega_{LO}t)] + \cdots \]  \hspace{1cm} (2.8)

and the mixer transconductance is therefore

\[ G_c = \frac{2}{\pi} g_m \]  \hspace{1cm} (2.9)

Notice from Equation (2.8) there is no LO-to-IF isolation as the switching-pair modulates the DC current with the LO, and thus there is no LO noise rejection. Odd-order LO harmonics also appears at the output. However, high RF-to-IF isolation is expected if the output is taken differentially. Furthermore, there is high LO-to-RF isolation because in theory the source of the differential pair acts as a virtually ground to the LO signal. In reality, it is a rectifier that doubles the LO frequency. In addition, the common-source transconductor provides even more isolation. This mixer is compact and contains only one more transistor than the dual-gate mixer while having more isolation between more ports. It is one of the mixers that has been widely used in receiving systems such as in [23–25].

In contrast to single-balanced mixers which does not have LO-to-IF isolation nor LO noise rejection, double-balanced mixer is able to counter these problems while keeping all of the advantages of a single-balanced mixer. A famous double-balanced active mixer that has been used in almost all of the communication systems is the Gilbert cell mixer, and it deserves a section of its own due to its importance.
2.3 The Gilbert Cell Mixer

The Gilbert cell mixer [4] was originally conceived as a four-quadrant multiplier, but it has found significant use as a microwave mixer because of its compact size, high port-to-port isolation, high gain, and spurious response cancellation. The Gilbert cell is essentially two single-balanced mixers with cross-coupled drains as shown in Figure 2.12. The input ports are differentially fed in and the output IF is taken differentially as well.

Transistors $M_1$ and $M_2$ are the transconductors converting the differential RF voltage into RF current. Two cross-coupled switching pairs $M_3$-$M_4$ and $M_5$-$M_6$ commutate the current to achieve mixing. Similar to the single-balanced mixer, the RF current is basically multiplied by a square-wave. Qualitatively, the two single-balanced mixers are connected in an anti-parallel fashion in terms of the LO and parallel in terms of the IF. The LO signal is therefore cancelled while the IF appears differentially at the output. High LO-to-IF isolation can thus be achieved.

![Figure 2.12: Gilbert cell mixer.](image)
To quantify the above view, the output voltage must be calculated. It is clear that the two branches of the mixer are 180° out of phase. The superposition approach can be used in the analysis, namely separating the two branches and analyzing them individually and subtracting their responses at the end. The output voltages due to $V_{RF}^+$ and $V_{RF}^-$ at $V_{IF}^+$ and $V_{IF}^-$ respectively are

$$V_{IF}^+ = \left[ \frac{I_{DC}}{2} - g_m V_{RF}^+ \cos(\omega_{RF}) \right] f_{\text{square wave}}(t) R_{load}$$

$$= \frac{2}{\pi} I_{DC} R_{load} \cos(\omega_{LO} t) - \frac{2}{\pi} g_m R_{load} V_{RF}^+ \{ \cos [(\omega_{RF} - \omega_{LO}) t] + \cos [(\omega_{RF} + \omega_{LO}) t] \} + \cdots \quad (2.10)$$

$$V_{IF}^- = \left[ \frac{I_{DC}}{2} - g_m V_{RF}^- \cos(\omega_{RF}) \right] f_{\text{square wave}}(t) R_{load}$$

$$= \frac{2}{\pi} I_{DC} R_{load} \cos(\omega_{LO} t) - \frac{2}{\pi} g_m R_{load} V_{RF}^- \{ \cos [(\omega_{RF} - \omega_{LO}) t] + \cos [(\omega_{RF} + \omega_{LO}) t] \} + \cdots \quad (2.11)$$

respectively, where $f_{\text{square wave}}(t)$ is from Equation (2.7). After substituting $V_{RF}^+$ with $V_{RF}/2$ and $V_{RF}^-$ with $-V_{RF}/2$ and subtracting Equation (2.10) and Equation (2.11), the total output voltage at the IF is

$$V_{IF} = -\frac{2}{\pi} g_m R_{load} V_{RF} \{ \cos [(\omega_{RF} - \omega_{LO}) t] + \cos [(\omega_{RF} + \omega_{LO}) t] \} + \cdots . \quad (2.12)$$

The voltage conversion gain is therefore

$$CG = \frac{2}{\pi} g_m R_{load}. \quad (2.13)$$

Equation (2.13) is the maximum conversion gain that can be achieved when there is
perfect switching. In reality, the switching pairs are not perfect. There is a switching
time interval \( t_{\text{switch}} \), during which both switches are on and the switching pairs become
differential amplifiers. This happens when \(|V_{\text{LO}}|\) is less than \(|v_{\text{in}}|_{\text{max}}\) in Equation (2.6). The conversion gain that accounts for this non-ideality is [26]

\[
CG \approx \frac{2}{\pi} \frac{\sin(\pi f_{\text{LO}} t_{\text{switch}})}{\pi f_{\text{LO}} t_{\text{switch}}} g_m R_{\text{load}}.
\] (2.14)

\( t_{\text{switch}} \) can be lowered in two ways to maximize the conversion gain. One way is to
increase the LO voltage, which is less appealing as the high LO voltage might drive
the transconductor stage into triode, thereby reducing gain and linearity. The other
way is to reduce the switching voltage, \(|v_{\text{in}}|_{\text{max}}\), which is directly proportional to the
overdrive voltage \( V_{\text{GS}} - V_T \). Because less voltage is needed for switching, the switch
time is lowered and more ideal switching can be obtained while a lower power LO can
be used which is very favourable in low-power applications [27, 28].

The linearity of the mixer depends on the switches, the transconductors, and the
tail current source. In [29], it was shown that the imperfect switches have an effect
on the linearity of the mixer, which is roughly the sum of the intermodulation values
of the transconductors and the switches. To reduce non-linear behaviour, the switch-
on voltage should be made low and a large LO power should be used. However,
excessive LO drive could cause higher non-linearity because of the capacitive loading
at the switching pairs’ common-source nodes [29]. Thus, a moderate LO drive ensures
reliable switching.

If the switches are perfect, then the IIP3 of the mixer is determined by the
transconductors [5]. Classical linearity extension techniques employed in LNA designs
can be used here as well. One classic technique is source degeneration. In resistive
Figure 2.13: Gilbert cell with inductive degenerated transconductors.

degeneration, two resistors are connected to the sources of the transconductors in series. However, due to the limited voltage headroom and noise figure, inductive degeneration in Figure 2.13 is usually used instead. In [30], it was shown that inductive degeneration increases linearity by providing some sort of cancellation, which cannot be achieved by resistive and capacitive degeneration. One drawback is that inductors are large and take up costly chip space. Other transconductor linearization methods such as the multi-tanh principle [31], the modified class AB transconductor [32], and the crossed-coupled differential transconductor [33] can also be used to increase mixer linearity.

It has been shown that the mixer exhibits higher non-linearity with the use of a current source. With a current source, the transconductor becomes a differential amplifier whose output current is given by [23]

\[
I_{\text{drain1}} - I_{\text{drain2}} = \frac{\mu_n C_{ox}(W/L)}{2} V_{RF} \sqrt{\frac{2I_{DC}/[(1/2)\mu_n C_{ox}(W/L)]}{2}} - V_{RF}^2
\]  

(2.15)
assuming long-channel operation. However, if the sources of the transconductors are directly connected to ground, the output current from these square-law devices becomes

\[ I_{\text{drain}1} - I_{\text{drain}2} = \mu_n C_{\text{ox}} (W/L) V_{RF} (V_{GS} - V_T) \]  

(2.16)

where \( V_{GS} \) is the DC bias voltage. The grounded transconductor pair has no third-order intermodulation products. Of course in reality, short-channel effects influence the linearity of the transconductor pair. Nevertheless, the analysis suggests the mixer has better linearity without the current source.

As the scaling of CMOS continues, the operating frequency keeps increasing. A 60 GHz Gilbert cell mixer has been demonstrated in [34]. Although the general design theory is similar, the interconnects should be accurately modelled and shielded transmission lines are often used.

Next, the mixer noise will be discussed. The noise analysis is somewhat involved due to the non-linearities of a mixer. Before proceeding to the details, a brief review on transistor noise is first provided in the next section.

### 2.4 Transistor Noise

The major noise contribution in CMOS transistors are flicker noise and thermal noise. Since there are no pn junctions in a MOSFET, there is no shot noise and it will therefore not be discussed any further.

Figure 2.14 shows the noise spectrum typically seen in a transistor. At low frequencies, the noise is dominated by flicker noise whereas thermal noise dominates at high frequencies. Flicker noise is usually defined by the corner frequency, \( f_c \), at which
the noise spectral densities of flicker and thermal noise are equal.

Thermal noise arises from the random movements of thermally agitated charges that gives rise to random noise current and in turn noise voltage. It is called white noise because it has a predominantly flat frequency response for frequencies below the optical frequencies.

Since FET’s can be viewed as voltage controlled resistors and all resistors have thermal noise, FET’s have thermal noise [5]. The thermal noise generated by the channel is the drain current noise and it can be expressed as

\[ |i_{nd}|^2 = 4kT\gamma g_{d0}\Delta f \]  \hspace{1cm} (2.17)

where \( k \) is Boltzmann’s constant, \( T \) is temperature in Kelvin, \( \gamma \) is a bias dependent factor, \( g_{d0} \) is the drain-source conductance at zero \( V_{DS} \), and \( \Delta f \) is the system bandwidth. When \( V_{DS} \) varies between 0 and \( V_{DS_{sat}} \), the transistor is in triode mode and the conductance varies, so does the noise current it generates. \( \gamma \) is therefore here to adjust for the change in channel conductance where it changes from unity to a value.
of 2/3 in saturation for long-channel devices. However, for short-channel devices, $\gamma$ can be much greater than one. Since the channel thickness depends on the gate bias $V_{GS}$, $g_{d0}$ depends on the gate voltage also.

The substrate can introduce drain-current noise by modulating the channel [5]. The thermal noise generated by substrate resistance $R_{sub}$ modulates the voltage of the backplate like in Figure 2.15. At low frequencies such that the channel-bulk capacitance $C_{cb}$ can be ignored, the drain-noise current from the substrate resistance is

$$|i_{nd,sub}|^2 = 4kT R_{sub} g_{mb}^2 \Delta f.$$  \hfill (2.18)

The total drain-current noise due to thermal noise is

$$|i_{nd}|^2 = 4kT (\gamma g_{do} + R_{sub} g_{mb}^2) \Delta f = 4kT \gamma_{eff} g_{d0}.$$  \hfill (2.19)

where

$$\gamma_{eff} \approx \gamma + \frac{g_{mb}^2 R_{sub}}{g_{d0}}.$$  \hfill (2.20)

At frequencies where $C_{cb}$ cannot be ignored, the noise current expression becomes [5]

$$|i_{nd,sub}|^2 = \frac{4kT R_{sub} g_{mb}^2}{1 + (\omega R_{sub} C_{cb})^2} \Delta f.$$  \hfill (2.21)
It can be seen from the above expression and Figure 2.15 that $C_{cb}$ and $R_{sub}$ forms a low-pass filter, thus the noise contribution from the substrate decreases as frequency increases [35]. At frequencies far beyond the pole of the RC filter, the substrate thermal noise can be neglected. This is usually around 1 GHz for many IC processes [5]. This noise current can be reduced by minimizing the substrate resistance through the use of closely spaced contacts around the transistor. Proper layout becomes very important.

Besides drain-current noise, the noisy channel couples capacitively to the gate and gives rise to gate-current noise. The expression for this current is

\[
|i_{ng}|^2 = 4kT \delta_g \Delta f
\]  

(2.22)

where

\[
g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}.
\]

(2.23)

The value for $\delta$ in a long-channel device is around $4/3$. Just like $\gamma$, $\delta$ can be much larger in short-channel devices. Figure 2.16 (a) shows the noise circuit model of

![Gate noise circuit models: (a) current representation and (b) voltage representation.](image)

Figure 2.16: Gate noise circuit models: (a) current representation and (b) voltage representation.
the gate. It can be seen that this noise current has a frequency dependency unlike thermal noise as this noise is proportional to $\omega^2$. To remove the current dependency, the voltage representation of the model can be used as in Figure 2.16 (b). The noise voltage is given by

$$|v_{ng}|^2 = 4kT\delta r_g \Delta f$$

where

$$r_g = \frac{1}{g_g} \frac{1}{Q^2 + 1} \approx \frac{1}{5g_d}.$$  \hfill (2.25)

In this model, the noise source and the elements are all frequency independent. Since the gate noise and drain noise share the same noise source, i.e. the channel, it is not surprising that the two noise are correlated and their correlated coefficient is

$$c \equiv \frac{i_{ng} \cdot i_{nd}^*}{\sqrt{|i_{ng}|^2 \cdot |i_{nd}|^2}}.$$  \hfill (2.26)

Another noise source at the gate is thermal noise from the polysilicon resistance. Due to the distributive nature, this resistance can be modelled by a series of resistances, each with their own noise source. Assuming only one end of the gates is connected, the overall effective gate resistance is give by [36]

$$R_{gate} = \frac{R_{\Box} W}{3n^2L}$$

where $R_{\Box}$ is the polysilicon sheet resistance, $n$ is the number of fingers, and $W$ and $L$ are the total gate width and length respectively. The 1/3 term is due to the distributive nature of the gates and becomes 1/12 if both ends are connected [37].
From a noise standpoint, $R_{\text{gate}}$ should be made as small as possible. Thus multifingered transistors should be used and the gates should be connected at both ends.

Besides thermal, MOSFET’s also exhibit flicker noise or 1/f noise. It is known as 1/f noise because the noise power is inversely proportional to frequency. Flicker noise arises from the surface defects between the gate and the channel. Impurities and the rapid generation and recombination of charges give rise to a drain-current noise that can be expressed as [5]

$$
|\langle i_{nd} \rangle|^2 = \frac{K}{f} \frac{g_m^2}{W L C_{ox}} \Delta f \approx \frac{K}{f} \omega_T^2 A \Delta f
$$

(2.28)

where $C_{ox}$ is the gate oxide capacitance per unit area, $K$ is a device-specific constant, $A$ is the area of the gate, and $\omega_T$ is the unit current gain frequency. It can be seen that flicker noise can be reduced by increasing the gate area. The physical explanation is that the increased gate capacitance smooths out the channel fluctuation. Thus, a large device should be used if flicker noise is a concern. PMOS devices, however, exhibit a lower flicker noise than NMOS due to buried channel behaviour [38].

The noise model in Figure 2.17 summarizes all the main intrinsic noise contributions in a MOSFET. The extrinsic noise components such as the gate resistance noise can be added easily to the intrinsic model.

Figure 2.17: MOSFET noise model.
2.5 Noise in Gilbert Cell Mixers

The noise analysis is quite involved in the Gilbert cell because of its time-varying nature and cyclostationary noise sources. The authors in [39] provided an intuitive view on mixer noise where both flicker and thermal noise were discussed in detail and their analysis is summarized in this section.

2.5.1 Low Frequency Noise

Flicker noise has been observed in down-converters with resistive loads even though it was believed that flicker noise in the transconductors and the switching pairs would have been up-converted to the LO band. The noise comes from three sources, namely the transconductors, the switches, and the IF loads.

Flicker noise at the transconductors can be treated as a signal. The frequency mixing translates the flicker noise to $\omega_{LO}$ and its harmonics and the noise does not appear at the output. However, due to device mismatch of the switches, a small amount of flicker noise will appear without frequency translation. Therefore, the switches layout should be done carefully to reduce the amount of mismatch.

Since there is no frequency translation at the IF loads, the type of loads being used would contribute to mixer flicker noise. Due to limited voltage headroom, active loads are often used. The flicker noise from the PMOS or NMOS loads appears at the output with no frequency translation. Therefore, if flicker noise is a concern, a PMOS load can be used whose flicker noise is less than that of the NMOS load or the loads can be implemented with polysilicon resistors which have no flicker noise.

Flicker noise at the switches also appears at the IF output without frequency
The single-balanced mixer in Figure 2.18 is used to explain this phenomenon. The switch flicker noise is referred to the gate with the noise voltage $v_n$. Since the flicker noise corner is usually very far away from the $\omega_{LO}$, it is possible to say that the noise is a much more slowly varying signal than the LO. Assuming the switches are perfect and switching occurs at the zero-crossings, the noise voltage that is superimposed onto the LO signal affects the switching time by either advancing it or delaying it. The change in switching time $\Delta t$ in Figure 2.19 is equal to $v_n(t)/S$, where $S$ is the slope of the LO at the zero-crossing. If the current switching can be viewed as a perfect square-wave, then the effect of flicker noise is adding current impulses with an amplitude of $2I$ with widths of $\Delta t$ to the output current as shown.

Figure 2.18: Single-balanced mixer with switch noise referred to the gate.

Figure 2.19: Input switching voltage with noise from [39] with permission ©2000 IEEE.
Figure 2.20: Mixer output current with noise: (a) ideal output current and noise impulses and (b) impulse sampling train and flicker noise both from [39] with permission ©2000 IEEE.

in Figure 2.20 (a). The average noise current in one LO period is [39]

\[ i_{o,n} = \frac{2}{T} \times 2I \times \Delta t = \frac{2}{T} \times 2I \times \frac{v_n}{S} = 4I \frac{v_n}{S} \times \frac{1}{T} \]  \hspace{1cm} (2.29)

where \( T \) is the LO period. From the expression, it can be clearly seen that the switch flicker noise appears at the output without frequency translation.

From another point of view, flicker noise is actually being sampled by an impulse train at \( 2\omega_{LO} \) as in Figure 2.20 (b). From the sampling theorem, the flicker noise thus appears at DC and integer multiples of \( 2\omega_{LO} \). Equation (2.29) suggests that flicker noise decreases as the slope of the LO increases and the bias current \( I \) decreases. The slope can be increased simply by increasing the LO power, thus making the
swtiches more ideal. The gate area of the switches can also be increased to reduce $v_n$. However, flicker noise cannot be eliminated even with a infinite slope due to an indirect mechanism.

The indirect mechanism has something to do with the tail capacitance $C_{tail}$ in Figure 2.18. When one of the switches, $M_1$ for example, is on, it acts like a source-follower with a capacitive load. The noise voltage appears at the source during this period. When $M_2$ is on, the noise source is disconnected. $C_{tail}$ therefore gets charged up exponentially by the noise voltage during half of the cycle and discharges during the other half. This change in voltage develops a tail current that has the same frequency as the LO. However, due to current commutation, the output current is at $2 \omega_{LO}$ with a non-zero DC value, which indicates that flicker noise is present. The output noise current can be expressed as

$$i_{o,n} = \frac{2C_{tail}}{T} v_n \cdot \frac{(\omega_{LO}C_{tail})^2}{g_{ms}^2 + (\omega_{LO}C_{tail})^2}$$

(2.30)

where $g_{ms}$ is the transconductance of a switch. In summary, if the tail capacitance is dominated by the transconductor’s junction capacitance, flicker noise can be reduced by using larger switches with large LO. If the capacitance is dominated by the switches, increasing switch size will increase the amount of flicker noise.

### 2.5.2 High Frequency Noise

Similar to low frequency noise, high frequency noise comes from the same three sources: the transconductors, the switches, and the IF loads. The same analysis method for direct flicker noise can be used to analyze switch thermal noise. The thermal noise of the switches can be referred to the differential input. Here, the noise
appears at the output when both of the switches are on and acting like a differential amplifier. Since the switches are on twice in one LO cycle, the impulse train with \(2\omega_{LO}\) can be used again. When the switches are on, they have a transconductance of \(G_m(t)\) which is periodic at \(2\omega_{LO}\). The impulse train can then be expressed as

\[
p(\omega_{LO}t) = \sum_n G_m\left(t - \frac{nT}{2}\right)
\]

(2.31)

and the output current is

\[
i_{o,n} = p(\omega_{LO}t) \cdot v_n(t)
\]

(2.32)

which is white and cyclostationary. After some manipulation, the power spectral density of the noise current at the output due to one switch is

\[
|\overline{i_{o,n}}|^2 = 4kT\gamma \frac{I}{\pi A_{LO}}
\]

(2.33)

where \(A_{LO}\) is the LO amplitude. Therefore, the switch noise only depends on the bias current and the LO amplitude and does not depend on switch size if tail capacitance is neglected. However, \(C_{tail}\) does affect the switch noise at high frequency. Consider the case when only one switch is on. Since \(C_{tail}\) provides a finite impedance to ground, the drain noise current of the “on” switch will flow into \(C_{tail}\). The current-commutating switches then translates that noise to the IF output [10]. Furthermore, the large \(C_{tail}\) affects the gain of the mixer at high frequency which directly translates to an increase in noise figure.

For the transconductors, since the noise appears just like the RF signal, thermal noise with respect to each odd harmonics of the LO gets translated to IF as depicted in Figure 2.21. Due to the balanced structure, the noise around the even-order harmonics
are cancelled out. For the IF loads, their thermal noise appears directly at the output.

2.6 Gilbert Cell Noise Reduction Techniques

The Gilbert cell mixer has been widely used due to its gain and high port-to-port isolation. However, this mixer produces high levels of noise due to the number of active devices used. Thus, some noise reduction techniques for Gilbert cell mixers have been proposed and a brief review will be presented here.

2.6.1 Flicker Noise Reduction

As described in subsection 2.5.1, the switches are the main source of mixer flicker noise if resistive loads are used at the output. To reduce the low frequency noise, a large LO power and low overdrive voltage should be used.

To ensure high conversion gain while minimizing bias current in the switches, the transconductors and the switches must be decoupled in terms of the DC current flow. The charge-injection method, or commonly known as current bleeding, can be used [40–43]. Figure 2.22 shows a double-balanced mixer with bleeding. The high output impedance of the current source forces all RF current into the switching pairs. Although current bleeding can reduce flicker noise from the direct mechanism, the
current source increases the tail capacitance which enhances flicker noise from the indirect mechanism. If the source of flicker noise is due to the indirect mechanism, an inductor can be used to resonate out the tail capacitance to reduce flicker noise [44]. Current bleeding is therefore usually used in conjunction with an inductor that is placed in parallel with the tail capacitance at $f_{LO}$ [43, 45–47]. Not only does this resonate out the tail capacitance, but also increases conversion gain.

Another flicker noise reduction technique is dynamic current injection [48]. Essentially it is a current bleeding circuit but one that only injects currents when both the switches are on, which reduces the noise impulses in Figure 2.20 (a). The injection circuit is off so that a large DC current flows through the on-switch, thus lowering its input impedance and less RF current will go into the tail-capacitance. The authors in [49] modified the injection circuit to make it more efficient by placing a tail-inductor to resonate out $C_{tail}$ at $2f_{LO}$.
2.6.2 Thermal Noise Reduction

One major source of thermal noise is from the transconductors. Thus, by replacing the transconductors with LNA’s, the mixer noise figure can be reduced significantly as demonstrated in [25, 43, 44, 46, 47, 50–52].

Figure 2.23 (a) is a quadrature down-converting Gilbert cell with the transconductors designed with classic LNA design technique [44] to achieve a DSB noise figure of 3.2 dB. Figure 2.23 (b) shows another quadrature low-noise mixer with common-gate LNA’s [43].

Current bleeding is also used in [46, 47] as it can reduce the noise contribution of the switches through reducing the DC current as suggested in Equation (2.33). Furthermore, since the switches and the transconductor are weakly DC coupled, large transconductors can be used which can provide enough gain to suppress the noise from the switches. Shown in Figure 2.24 (a) and (b) are the bleeding mixers used in [46] and [51] respectively. The bleeding circuit also reduce flicker noise in [46].

Similar to flicker noise reduction, a parallel inductor can be placed to resonate out

![Figure 2.23: Low-noise transconductors](image-url)
the large tail-capacitance created by the current bleeding circuit and the switching pairs. High gain can thus be achieved at higher frequencies.

2.7 Conclusion

This chapter provided detailed overviews on different types of mixer topologies, their advantages, and drawbacks. In particular, the Gilbert cell mixer was explored in detail demonstrating its advantages over other mixer topologies in terms of gain, feedthrough, and filter-free design. A qualitative analysis on noise of the Gilbert cell was provided, showing the different mechanisms that lead to frequency translation of noise. Finally, different noise reduction techniques that have been proposed were shown and explained.
Chapter 3

Low-Noise Mixer with Inductive Degeneration

3.1 Introduction

As described in the previous chapter, the noise figure of a Gilbert cell can be significantly lowered if the transconductor is replaced by an LNA. Figure 3.1 shows a typical low-noise mixer. In [44], such circuit was successfully demonstrated in 0.35 \( \mu \text{m} \) CMOS at 2.1 GHz. However, the gate inductors are off-chip and a large 10 nH inductor was used to resonate out the tail capacitance. The authors in [46] simulated their low-noise mixer together with a current bleeding circuit and it required a 10 nH inductance at 1.32 GHz as well. At low frequencies, the inductor is still realizable. Due to the large area the inductor takes up, the Q diminishes very quickly as frequency increases. Thus at high frequencies, it is not practical and impossible to implement such large size inductors.

The low-noise transconductors shown in Figure 3.1 uses the Simultaneous Noise
and Input Match (SNIM) technique to achieve the lowest possible noise figure and input match at the same time [53]. The drawback of this technique is that the large $C_{gs}$ required in the transistor results in large current consumption. Since the required $C_{gs}$ at a particular frequency is roughly independent of technology, the drain current increases substantially when shorter gate-length transistors are used. Technology scaling causes the supply voltage to go down as well. The limited voltage headroom requires heavy current bleeding in the mixer to keep the gain up. This translates to large bleeding transistors and an increase in tail-capacitance. High-frequency performance suffers without resonating out $C_{tail}$. However, large inductances are not practical at high frequencies as explained before.

In this design, the goal is to improve the performance of the low-noise mixer in several ways. First, all of the components including inductors are to be realized on chip and no off-chip components are required. Second, the conversion gain of the mixer must be at a reasonable level such that there is no compromise in gain in using this mixer topology compared with other mixer topologies. Third, the noise figure
must be low enough to justify the purpose of low-noise mixers.

### 3.2 Low-Noise Mixer Concept

Figure 3.2 is the circuit of the proposed mixer. It is designed at 5.4 GHz with an IF of 300 MHz in CMOS 0.18 µm. The main design focus is on the low-noise transconductors because the mixer current consumption depends on the transconductor bias. The purpose is to reduce the transconductor current while maintaining its function as an LNA. The Power Constrained Simultaneous Noise and Input Match (PCSNIM) technique [53] is used for the low-noise transconductors. However, as will be explained in subsection 3.3.1, the PCSNIM technique reduces the size of the transistors but increases the sizes of the source and gate inductors. It is well-known that the inductor quality factor, $Q$, in CMOS is usually not very high, and therefore the gate and source inductance must be kept as small as possible so as to maximize their $Q$. Thus there is a point where further reduced in power consumption will increase the

![Figure 3.2: Proposed low-noise mixer.](image)
inductor sizes to a point where high Q inductors can no longer be realizable. This sets the lower bound of sizes of $M_1$ and $M_2$.

To maximize gain, the current bleeding circuit is then used to supply most of the DC current the low-noise transconductors need. Because PCSNIM reduces the power consumption, it also reduces the size of the bleeding transistors, $M_7$ and $M_8$, as heavy bleeding is no longer required. A parallel inductor is not needed as the effect of tail-capacitance is not significant at this frequency. This allows the mixer to work at higher frequencies and reduce chip space. Furthermore, PCSNIM alleviates the gate scaling problem as it decouples the transistor size requirement and the DC power consumption. This particular mixer design can therefore be scalable together with the technology.

### 3.3 Circuit Implementation

This section describes the design of the mixer in much greater details. Theoretical analysis is given and circuit simulation results are also provided to prove the design concept.

#### 3.3.1 Inductive Degenerated Low-Noise Transconductor

The performance of the transconductors is crucial because they generate most of the noise in a Gilbert cell. The noise contribution from the switches can be reduced simply by decreasing the DC current and increasing the LO amplitude. Other than this, there are few other options available. The transconductor needs to be low-noise and have a large $g_m$ to overcome the noise generated by the switches and the loads.
The general noise figure is defined as

\[
F \equiv \frac{\text{Total output noise power}}{\text{Output noise power from the source}}.
\]

A transistor can be modelled as a 2-port network as in Figure 3.3 (a), where \(i_s\) and \(Y_s\) are the source current and source admittance respectively. To calculate the noise figure of a transistor, the noise sources can be referred to the input by a noise voltage and a noise current source as shown in Figure 3.3 (b). After some mathematic manipulation as shown in [54], the noise figure of a transistor amplifier is

\[
F = F_{min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2
\]

where \(F_{min}\) is the minimum NF achievable, \(R_n\) is the noise resistance, \(G_s\) is the real part of the source admittance, and \(Y_{opt} = G_{opt} + jB_{opt}\) is the optimum source admittance to achieve \(F_{min}\). For a MOSFET, these parameters can be expressed as

\[
R_n = \frac{\gamma}{g_m^2}
\]

Figure 3.3: Different representations of a 2-port noisy network: (a) Y representation and (b) ABCD representation.
To achieve the lowest noise figure, the source admittance should be chosen to be equal to \( Y_{opt} \). However, the input admittance \( Y_{in} \) of a common-source amplifier is purely capacitive and can be expressed as \( j\omega C_{gs} \) assuming the extrinsic gate resistance is negligible. From Equation (3.4) and Equation (3.5), it can be seen that the complex conjugate of \( Y_{in} \) is very different from \( Y_{opt} \). Therefore, both noise and input matching cannot be accomplished at simultaneously.

The SNIM technique allows simultaneous noise and input match by transforming both \( Y_{in} \) and \( Y_{opt} \) into 20 mS or 50 Ω impedance. One configuration that has been widely used is inductive degeneration. Figure 3.4 shows the basic inductive degenerated circuit. The values of noise parameters, namely \( F_{min} \) and \( R_n \), of the inductive degenerated circuit are as same as those without degeneration. \( Y_{opt} \), however, is changed. If the optimum noise admittance is expressed as an impedance \( Z_{opt} \), then it

\[
B_{opt} = -j\omega C_{gs} \left( 1 + \frac{g_m}{g_{d0}} |c| \sqrt{\frac{\delta}{5\gamma}} \right) \quad (3.4)
\]

\[
G_{opt} = \omega C_{gs} \frac{g_m}{g_{d0}} \sqrt{\frac{\delta}{5\gamma}} (1 - |c|^2) \quad (3.5)
\]

\[
F_{min} \approx 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2).} \quad (3.6)
\]
can be shown that the $Z_{\text{opt}}$ with degeneration can be expressed as

$$Z_{\text{opt with } L_s} \approx \text{Re}(Z_{\text{opt}}) - j \left( \omega L_s - \frac{1}{\omega C_{gs}} \right)$$

(3.7)

The input impedance is

$$Z_{\text{in with } L_s} = \frac{L_s g_m}{C_{gs}} + j \left( \omega L_s - \frac{1}{\omega C_{gs}} \right).$$

(3.8)

Note that there is a real term whereas the input impedance with no degeneration is purely capacitive. This is a crucial point because for SNIM, $Z_{\text{opt}}$ must be equal to $Z_{\text{in}}^*$. The source impedance is usually 50 $\Omega$ and has no imaginary part but the imaginary terms in Equation (3.7) and Equation (3.8) are usually present. To resonate out those terms, a series inductor is placed at the gate as shown in Figure 3.5 and the new $Z_{\text{opt}}$ and $Z_{\text{in}}$ become

$$Z_{\text{opt SNIM}} = \text{Re}(Z_{\text{opt}}) - j \left( \omega (L_s + L_g) - \frac{1}{\omega C_{gs}} \right) = \text{Re}(Z_{\text{opt}})$$

(3.9)

$$Z_{\text{in SNIM}} = \frac{L_s g_m}{C_{gs}} + j \left( \omega (L_s + L_g) - \frac{1}{\omega C_{gs}} \right) = \frac{L_s g_m}{C_{gs}}.$$  

(3.10)

Figure 3.5: Simultaneous Noise and Input Match LNA.
To design the LNA, the transistor size is first chosen according to Equation (3.5) by making $G_{opt}$ equal to 20 mS. For most advanced CMOS processes, Equation (3.5) can be simplified into

$$G_{opt} \approx \frac{\omega C_{gs}}{2} = \frac{1}{Z_o} \quad (3.11)$$

and the required $C_{gs}$ is

$$C_{gs} \approx \frac{2G_{opt}}{\omega} \quad (3.12)$$

Once the transistor size is determined, a bias point is chosen to achieve the lowest $F_{min}$ possible. It is usually biased with a drain current density of 0.13 mA/µm gate width because that yields the lowest noise figure [55]. Next, $L_s$ is chosen using

$$L_s = \frac{Z_o C_{gs}}{g_m} \quad (3.13)$$

to make the real part of $Z_{in}$ equal to $Z_o$. Finally, $L_g$ can be chosen to resonate out the imaginary part of $Z_{in}$ if it is still present after degeneration.

The drawback of this design technique is apparent from Equation (3.12). The required $C_{gs}$ is roughly a constant for a particular frequency. As an example, for TSMC’s 0.18 µm CMOS process, an LNA at 10 GHz will require a 0.64 pF $C_{gs}$ which translates to a total gate width of 650 µm. That is 260 fingers for a 2.5 µm finger width. The power consumed is too significant. Furthermore, as the gate length scales down, the power consumption will keep on increasing. This technique is therefore not suitable for low-power applications and not “scaling friendly”.

The PCSNIM technique remedies the above problems. First, $C_{gs}$ must be reduced to reduce power consumption. Second, SNIM must be met. To simultaneously satisfy these conditions, a parallel capacitor $C_{ex}$ is placed between the gate and source of the
transistor as in Figure 3.6. Equations (3.12) and (3.13) are modified into

\[
C_T = C_{gs} + C_{ex} \approx \frac{2G_{opt}}{\omega} = \frac{2}{Z_0\omega} \tag{3.14}
\]

\[
L_s = \frac{Z_0(C_{gs} + C_{ex})}{g_m}. \tag{3.15}
\]

Now, the transistor size can be chosen to whatever value that satisfied the power constrained given for that design.

However, this design method is not perfect. The noise resistance in Equation (3.2) is a measure of the LNA’s sensitivity to the variance of the source admittance. The larger the \( R_n \), the more sensitive the noise figure is to process variation and the lower the LNA yield is. Equation (3.3) shows an inverse relationship between \( R_n \) and \( g_m \). The shrinking of the transistor also leads to a reduced in \( g_m \). Therefore, PCSNIM is more sensitive and has a smaller bandwidth then SNIM. Furthermore, \( \omega_T \) is approximately equal to \( g_m/C_{gs} \), or \( g_m/C_T \) in PCSNIM, so it goes down as well. According to Equation (3.6), \( F_{\text{min}} \) increases. Therefore designers should not blindly minimize the transistor size.

From equations (3.15) and (3.10), it seems that PCSNIM increases \( L_s \) but reduces \( L_g \). In reality, this is not true. One very important assumption that lead to simple
derivations of the above equations is the negligible impact of $C_{gd}$. The input Miller capacitance is expressed as

$$C_1 = C_{gd}(1 - K)$$

(3.16)

where $K$ is the voltage gain across $C_{gd}$. For a cascode amplifier whose transistors have the same size, $K$ is equal to $-1$. For an inductive degenerated cascode amplifier with no $L_g$, the voltage gain across the common-source amplifier while neglecting $C_{gd}$ is

$$A_v = \frac{-1}{1 - \omega^2 L_s C_T + j\omega L_s g_m}$$

(3.17)

To gain more insight from the above equation, it is further assumed that $\omega = \omega_0 = 1/\sqrt{L_s C_T}$ and $L_s$ is chosen according to Equation (3.15) and $C_T$ is constant. The voltage gain becomes

$$A_v = \frac{-1}{j\sqrt{Z_0 g_m}}.$$  

(3.18)

It can be seen from this first order approximation that by reducing $g_m$ through transistor size reduction, the voltage gain increases which leads to an increase in Miller capacitance. PCSNIM therefore increases the size of $L_g$ rather than decreasing.

Nevertheless, PCSNIM is used in this mixer design because of its scaling-friendly and low power consumption characteristics. A moderate size transistor is used such that high $Q$ $L_g$ is realizable. The finger width is set to 2.5 $\mu$m and the transistor is biased to have a drain-current density of 0.13 mA/$\mu$m. Table 3.1 shows the inductances used in the low-noise transconductor design.

<table>
<thead>
<tr>
<th>Freq (GHz)</th>
<th>$L_s$ (pH)</th>
<th>$L_g$ (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.4</td>
<td>330</td>
<td>4.2</td>
</tr>
</tbody>
</table>

Table 3.1: Low-noise transconductor inductor values.
The inductors were first designed using ASITIC. Agilent’s ADS Momentum was used next to do a full 2.5-D EM simulation. Finally, the S-parameter files from Momentum were used to extract the inductances and the associated parasitics. The circuit model of a spiral inductor is displayed in Figure 3.7 (a). Component extractions is difficult with this model and time consuming. Figure 3.7 (b) is a much simplified model and the components can be easily extracted from a S-parameter file. The simplified model is a Y-network. Thus the S-parameters need to be transformed in Y-parameters. After the Y-parameters was obtained, the following equations are used to extract the component values

\[
\frac{-1}{y_{21}} = R_s + j\omega L \tag{3.19}
\]

\[
y_{11} = \frac{1}{R_s + j\omega L} + \frac{1}{R_{sub} - \frac{j}{\omega C_{ox}/2}} \tag{3.20}
\]

The Q of the inductors can be calculated using

\[
Q = \frac{-\text{Im}(y_{11})}{\text{Re}(y_{11})} \tag{3.21}
\]
A Q of 9 was achieved for the 4.2 nH inductor and the Q of $L_s$ was 5.9. The extracted inductors are put back into the circuit and the simulated noise figure as well as the return-loss of the complete low-noise transconductor are shown in Figure 3.8. Using the spiral inductors, a 1.88 dB noise figure is achieved at 5.4 GHz with a $S_{11}$ of $-40.2$ dB and it draws 8.89 mA of current from a 1.8 V supply.

### 3.3.2 Switching Pairs and Current Bleeding Technique

As described in subsection 2.5.2, the noise from the switching pairs can be reduced by decreasing the DC current and increasing the LO power.

The amount of current the low-noise transconductors draws reduces the load size and a large over-drive voltage is required for the switches to handle this current, making the switches less ideal. The current bleeding circuit is used to alleviate these problems. Figure 3.9 is a typical bleeding circuit with two PMOS transistors providing DC current into the two transconductors. PMOS transistors are preferable because the common-source configuration provides a high output impedance at the drain.
of the transistors. This large output impedance is in parallel with the small input impedance of the switching pair at the source which is about $1/g_m^\text{switch}$. Therefore, the weak RF signal is forced to go into the switching pairs. The loading effect is, thus, much smaller compared to a NMOS bleeding circuit, where the output impedance at the source is $1/g_m^{\text{bld}}$, which is significantly lower than that of the PMOS. For a single-balanced mixer with bleeding, it can be shown that the output current is [45]

$$i_{LO} = \frac{R_{bld\; out}[g_{m\text{switch},1}(t) - g_{m\text{switch},2}(t)]}{1 + R_{bld\; out}[g_{m\text{switch},1}(t) + g_{m\text{switch},2}(t)]} \cdot i_{RF},$$

where $g_{m\text{switch},n}(t)$ is the $g_m$ of the $n^{th}$ switch and $R_{bld\; out}$ is the output impedance of the bleeding circuit. PMOS bleeding is therefore more suitable.

By supplying most of the current required, the turn-on voltage is reduced and a lower LO power can be used for switching. However, aggressive bleeding is to be avoided due to the ever-present parasitic tail capacitance. The $C_{gs}$ of the switches, the output Miller capacitance from the transconductor, and the output capacitance of the bleeding circuit can significantly reduce the gain if a large bleeding transistor is used for heavy bleeding purposes. This would require a parallel inductor to resonating out the tail capacitance.

The bleeding transistors are therefore kept as small as possible. By supplying only
half of the DC current, the transistors can be made small while staying in saturation at all times. The transistors in the switching pairs are usually sized to be as big as the transconductor, as is the case in this design. This decision is based on the switching-voltage. Figure 3.10 (a) is used to demonstrate how the size of the differential pair affects the switching-voltage. A constant DC tail current is applied and the input voltage is varied from $-V$ to $+V$, where $V$ is the differential voltage required to completely swing the current of a 5 finger differential pair from one branch to the other. The per-finger width was set to $2.5 \mu m$ and the number of fingers was swept ranging from 5 to 40 with a step of 5. Figure 3.10 (b) shows a normalized plot of the output current of one branch of a differential amplifier versus the differential input voltage for different number of fingers. It can be seen that although $|V|$ is required for full switching with a 5 finger differential pair, only 60% of that voltage is required with a 10 finger differential pair. The switching-voltage is inversely proportional to the transistor size for the same amount of DC current. However, there is no significant
Figure 3.11: Low-noise mixer with inductive degeneration and current bleeding.

decrease in the switching-voltage for finger numbers beyond 20. Finger number more
than 20 is therefore suitable. In this design, close-to-perfect switching is required for
maximum SNR. Thirty fingers was chosen because it is a good compromise between
switch capability and gain.

The LO power cannot be too high because it can drive the transconductors into
the triode region, thereby adversely affecting the gain, which in this case is very
important because a high transconductance is required to overcome the noise from
the switches and the loads. A moderate LO of 0 dBm is chosen as this is the point
at which there is maximum gain and lowest noise figure.

The low-noise mixer circuit was shown in Figure 3.2 and is shown here in Fig-
ure 3.11 again for convenience. The load resistors are set to 100 Ω. The physical
size of $L_g$ (4.2 nH) is 135 µm × 135 µm and $L_s$ (330 pF) is 60 µm × 60 µm. The
circuit was simulated with both Spectre RF and ADS to confirm the performance.
Since the output of the mixer will be connected to the Spectrum Analyzer during
measurements, an output buffer is thus necessary to eliminate the loading effect from the Spectrum Analyzer’s 50 Ω load. An ideal buffer is used with the output buffer load being 100 Ω to account for the differential load the mixer should be driving. Figure 3.12 shows the buffer circuit used.

Baluns are required to convert the single-ended RF and LO inputs into differential signals. Off-chip baluns are used, so ideal baluns were used in simulations. Figure 3.13 (a) shows the simulated 300 MHz IF output power versus the 5.4 GHz RF input power. The power conversion gain is 12.6 dB. To find the input 1 dB power compression point ($P_{1dB}$), the gain of the mixer is reduced by 1 dB and replotted as shown by the dotted line. The intersection point is the $P_{1dB}$ and it is $-9.64$ dBm.

Figure 3.13: Simulated output power and $S_{11}$ with an ideal buffer: (a) simulated output power vs input power and (b) mixer input reflection coefficient.
The input reflection coefficient of the mixer is simulated and Figure 3.13 (b) shows that it has a good match at 5.4 GHz with a $-26.4$ dB $S_{11}$. The simulated SSB noise figure of the mixer is 6.171 dB. This is significantly lower than that of a typical CMOS Gilbert cell which is about 15 dB.

Another important mixer parameter is the input referred third order intermodulation product (IIP3), which is a measure of mixer linearity. Two tones separated by 1 MHz were injected to obtain the IIP3 point. Figure 3.14 (a) shows the IF and the third intermodulated product (IM3) outputs as well as the extrapolated IIP3, which is $-0.9$ dBm.

Another important Gilbert cell attribute is port-to-port isolation. Figure 3.14 (b) shows the port-to-port isolation with respect to input power. It can be seen that more than 70 dB isolations can be achieved for all ports below the $P_{1dB}$ point. Finally, the mixer is drawing 17.8 mA of current from a 1.8 V supply. The mixer core design is complete and the ideal buffer should now be replaced by a real buffer.
3.3.3 Output Buffer

Buffers are essential during testing and measurement. Since the input impedance of most measuring equipment such as the Spectrum Analyzer is a constant 50 Ω resistance, it will significantly load the mixer output and reduce its gain. Buffers are thus required to provide a high impedance to the mixer output while also providing a 50 Ω resistance to the equipment input for matching purposes.

The buffer in this design also serves another purpose. The mixer output is differential but the equipment has a single-ended input. One approach is to have two single-ended buffers on-chip and use a off-chip balun to combine the outputs. Another approach is to place this burden to buffer design, which simplifies the measurement process. The latter approach was taken and a differential-to-single-ended buffer was designed and shown in Figure 3.15.

The buffer is essentially a differential amplifier with an active current mirror load. If resistive loads are used instead and the output taken single-endedly, the common-mode rejection property of a differential amplifier is significantly degraded. With a

![Figure 3.15: Differential to single-ended buffer.](image-url)
current mirror load however, the current of one branch is mirrored onto the other branch. The currents add together if they are differential and feed into the output load and subtract if they are common-mode. In this mixer design, the design goal is to obtain a low noise figure. The low-noise mixer has a differential output. Therefore, this active load differential buffer is used to combine the differential signal and reject the common-mode signal.

The buffer is put into the mixer and Figure 3.16 shows the complete circuit of the low-noise mixer. The buffer is DC coupled to the mixer because at the decoupling capacitor required at the desired IF is too large and hard to realize on chip. It is important to make sure that the buffer does not affect, either positively or adversely, the performance of the mixer since it is the true performance of the mixer that is of importance. The circuit should have the same performance regardless of the presence of the buffer. Thus, the buffer is designed to provide no gain but to only combine the differential signals into a single-ended signal that feeds into a 50 Ω system. Simply put, it is a high input impedance power combiner.
3.4 Simulation Results

The circuit was layout using Cadence Virtuoso. Figure 3.17 shows the layout of the chip including all of the pads. The area for the low-noise mixer core is about 380 µm x 350 µm (0.133 mm²) and the total chip size including pads is 700 µm x 670 µm (0.469 mm²). The layout and parasitic capacitors were extracted and a post-layout simulation was conducted in Cadence Spectre RF to verify its performance. To further confirm the layout performance, another post-layout simulation was run in ADS through the ADS Dynamic Link. Ideal baluns were used in the simulation to generate the required differential RF and LO signals.
Figure 3.18: Post-layout output power and input match simulation: (a) output power versus input power and (b) input reflection coefficient.

Figure 3.19: Post-layout IIP3 and isolation simulation: (a) IIP3 and (b) port-to-port isolation.

Figure 3.18 (a) shows the output power versus input power of the mixer. The power conversion gain is 12.85 dB and the $P_{1dB}$ is $-14.63$ dBm. The mixer has a good match near the design frequency and the $S_{11}$ shown in Figure 3.18 (b) at 5.4 GHz is -28.94 dB. The new SSB noise figure is 6.78 dB. Figure 3.19 (a) shows
the new IIP3 to be $-7.1$ dBm and the port-to-port isolation is beyond 40 dB for all ports as shown in Figure 3.19 (b). The gain is only affected by 0.25 dB and the noise figure by 0.609 dB, which is from the buffer. $P_{1dB}$ and IIP3 are also affected. This is so because in a system point of view, they are both limited by latter stages. Since the buffer is designed to have minimum noise and no gain but not high linearity, the $P_{1dB}$ and IIP3 degradation is expected.

To see if the common-mode rejection property is retained, the common-mode gain was simulated to be -48.48 dB. The common-mode rejection ratio (CMRR), defined by

\[ CMRR = \frac{A_{\text{differential}}}{A_{\text{common-mode}}} \]  

(3.23)

where $A_{\text{differential}}$ is the differential gain and $A_{\text{common-mode}}$ is the common-mode gain, provides a measure of how good the system rejects common-mode signal. The CMRR of the mixer is therefore equal to 60.97 dB. The buffer is therefore behaving as it is intended.

### 3.5 Measurement Results

The chip was fabricated with TSMC’s CMOS 0.18 $\mu$m process. Figure 3.20 shows a microphotograph of the complete chip. Since both RF and LO signals need to be fed differentially into the test chip, two off-chip baluns were used to convert the single-ended signal from the test equipment into full differential signals. All measurements were done on wafer with the use of two differential Ground-Signal-Ground-Signal-Ground Coplanar Waveguide (GSGSG CPW) probes and one single-ended Ground-Signal-Ground Coplanar Waveguide (GSG CPW) probe for the IF output. For the
RF, the signal generator was connected to a broadband 180° hybrid. For the LO, it was connected to a power splitter first and the outputs of the splitter are connected each to a phase shifter to generate the differential LO. The LO input power was set to a constant 0 dBm for all measurements. The chip was tuned by the biasing voltages to have the best possible noise figure and then they were kept constant throughout the measurement process. The RF power was swept and the IF output power of the mixer was measured by a Spectrum Analyzer. Figure 3.21 (a) shows the measured output power with respect to different input power levels. The measured conversion gain is 13.06 dB with an input referred $P_{1dB}$ of $-17.8$ dBm. Figure 3.21 (b) shows...
Figure 3.21: Measured output power and gain: (a) IF output power with versus input power and (b) power conversion gain versus input power.

Figure 3.22: Measured S_{11} and isolation: (a) input reflection coefficient and (b) LO-to-IF and RF-to-IF isolation.

the measured as well as the simulated conversion gain of the mixer, which are very close to each other. To measure the NF_{SSB}, an input filter is required to filter out the noise from the image sideband. Since no filters were available during that time, a DSB measurement was done instead. To find the NF_{SSB}, a −3 dB compensation
was added in the Loss Compensation Table of the Spectrum Analyzer to account for the extra 3 dB gain result from the DSB measurement as explained by the manual [56]. The measured NF_{SSB} was 7.8 dB with an uncertainty of 0.26 dB. To verify the accuracy of the measurement, the gain measured in noise figure mode was found to be 13.06 dB, which was the same as the one measured in spectrum mode. The −3 dB assumption is therefore valid.

Shown in Figure 3.22 (a) is the measured input reflection coefficient. Since only a 2-port network analyzer was available, a full 2-port measurement was conducted for the input differential ports in order to extract the differential $S_{11}$. Once the full 2-port data was recorded, Equation (3.24) was used to find the equivalent differential mode $S_{11}$ [57].

\[
S_{d,dd} = \frac{1}{2} (S_{11} - S_{21} - S_{12} + S_{22})
\]  

Due to unwanted coupling between the gate inductors, the frequency for best match drifted upwards. Nevertheless, at 5.4 GHz, the measured $S_{11}$ is −11.1 dB. Figure 3.22 (b) shows the measured RF-to-IF and LO-to-IF feedthrough as a function

![Graph showing measured output spectrum from 0 to 6 GHz with an input power of -25.5 dBm at 5.4 GHz and an LO power of 0 dBm at 5.1 GHz.](image)

Figure 3.23: Measured output spectrum from 0 to 6 GHz with an input power of -25.5 dBm at 5.4 GHz and an LO power of 0 dBm at 5.1 GHz.
Figure 3.24: Measured linearity response: (a) output spectrum of a 2 tone test with an input power of -30 dBm and (b) IF and third order intermodulation product outputs.

of RF input power and at a fixed LO power of 0 dBm. Good port-to-port isolation was achieved by making the layout as symmetric as possible. The RF feedthrough is $-28$ dB or less and the LO feedthrough is below $-33$ dB. The LO-to-RF feedthrough was also measured, and it is $-61.8$ dB. The measured spectrum with an input power of $-25.5$ dBm is shown in Figure 3.23 from 0 to 6 GHz. The suppressed LO-to-IF and RF-to-IF feedthroughs can be clearly seen in the plot.

To measure the IIP3, a two-tone test was conducted with the two tones separated by 1 MHz. Figure 3.24 (a) shows the output spectrum in a two-tone test with an input power level of $-30$ dBm. The input power levels were swept and the output powers of the IF and IM3 outputs were measured. Figure 3.24 (b) includes both the measured IF and IM3 output powers. From the plot, the extrapolated IIP3 is $-6.2$ dBm. Finally, the DC voltage $V_{DD}$ applied was 2 V. The complete mixer including the output buffer consumes 31 mA, while the mixer core only consumes 18 mA of current.
CHAPTER 3. LOW-NOISE MIXER WITH INDUCTIVE DEGENERATION

The noise figure is only around 1 dB higher than expected from simulations. There are several possible causes. First, the coupling between inductors $L_s$ and $L_g$ was not taken into account during simulation. This affects the effective value of $C_{ex}$ which in turn leads to the increase in noise figure. Second, parasitic resistances could not be extracted and were not included in the post-layout simulation. The effective $g_m$ of the mixer is lowered and biasing voltages were adjusted to obtain the same gain and lowest possible noise figure during measurement. The matching network is therefore not optimized, which explains why the dip of the measured $S_{11}$ was shifted. The measured $P_{1dB}$ drop can also be explained by the same reasons. Furthermore, the mixer is no longer noise and input matched, which may have lead to the increase in noise figure. Third, the buffer is DC coupled to the mixer. Adjusting the mixer biases affects the buffer performances. Nevertheless, the mixer has a superior noise and gain performance and a good match at the operating frequency.

Important parameters of this low-noise mixer are compared to other works as shown in Table 3.2. While a number of papers have appeared describing low-noise mixers with current bleeding and inductive degeneration, a lot of them report only simulation results such as [46] and [47], and are therefore not included in the table. The SSB NF of this work is 7.8 dB while the others only quote DSB noise. Since $NF_{SSB}$ is usually +3 dB higher than $NF_{DSB}$, then the $NF_{DSB}$ of this work is around 4.8 dB, which compares very favourably with the other designs.

<table>
<thead>
<tr>
<th>Reference</th>
<th>CMOS Technology</th>
<th>Input Frequency (GHz)</th>
<th>Conversion Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>IIP3 (dBm)</th>
<th>DC Power (mW)</th>
<th>Area (mm²)</th>
<th>All Inductors On-Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>[44]</td>
<td>0.35 µm</td>
<td>2.1</td>
<td>23 (Voltage)</td>
<td>3.2 (DSB)</td>
<td>−1.5</td>
<td>21.6</td>
<td>-</td>
<td>No</td>
</tr>
<tr>
<td>[58]</td>
<td>90 nm</td>
<td>0.1 – 3.85</td>
<td>12.1 (Power)</td>
<td>8.4 – 11.5 (SSB)</td>
<td>N/A</td>
<td>9.8</td>
<td>0.88</td>
<td>Yes</td>
</tr>
<tr>
<td>This Work</td>
<td>0.18 µm</td>
<td>5.4</td>
<td>13.1 (Power)</td>
<td>7.8 (SSB)</td>
<td>−6.2</td>
<td>36 (core)</td>
<td>0.133</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 3.2: Comparison of several low-noise mixers with this work.
3.6 Conclusion

In this chapter, a fully integrated on-chip low-noise mixer utilizing the PCSNIM and current bleeding techniques in 0.18 µm CMOS technology was presented. A thorough design analysis was given and a design guideline was provided. The noise reduction techniques reduce the circuit size and noise figure while maintaining a reasonable gain and linearity. The dependency for power consumption and noise and input match in SNIM is eliminated through the use of PCSNIM, which allows this mixer design to be scalable with technology. The mixer works at 5.4 GHz with a 300 MHz IF and has a power conversion gain of 13.1 dB, a low 7.8 dB SSB noise figure, and an IIP3 of $-6.2$ dBm. The mixer core itself only consumes 18 mA from a 2.0 V supply and the complete test circuit consumes 31 mA.
Chapter 4

Broadband Low-Noise Mixer

4.1 Introduction

In the previous chapter, the mixer was a narrowband mixer and it was designed only to operate at a narrow frequency band of interest. Currently, electronic devices are moving towards more functionalities in very compact sizes. This could mean the device is capable of communicating with devices in other networks having different frequency bands. In other words, it is a multiband, multi-standard device. If narrowband mixers are used, they need to be designed individually to accommodate each frequency band. The complete multiband multi-standard receiving system might have many branches, each for one frequency band. Not only does this architecture increase the overall system size which in turn increases the costs, but it also complicates the design process, especially the case with low-noise mixers, due to their narrowband nature and the number of inductors used. However, with a broadband low-noise mixer, the design of such system can be much simplified.

In this chapter, a new broadband low-noise mixer will be presented that directly
targets this issue. Due to the large bandwidth of the mixer, only a single mixer would be required in a multiband multi-standard receiver. The mixer is designed to operate between 1 GHz to 6 GHz with a constant IF of 250 MHz using IBM’s CMOS 0.13 µm technology.

4.2 Mixer Concept

The Gilbert cell core is again used in this design. To design a broadband low-noise mixer, the transconductors must be broadband in terms of noise figure and gain. The goal is to make the gain and noise figure response as flat as possible in terms of frequency. The broadband LO signal is assumed to be generated on chip and thus does not require a broadband matching network. It is also assumed that the mixer is preceded by either an external LNA or an external filter, both of which have an output impedance of 50 Ω. Thus, the mixer should also be broadband matched to 50 Ω. Another reason for broadband input matching is that the mixer is designed as a standalone component that can be sold as-is, assuming a VCO will also be integrated onto the same chip.

The design of the low-noise transconductor is similar to a broadband LNA design. A lot of broadband and ultra-wideband (UWB) LNA’s have been proposed [59–61]. In [59], an active feedback approach was used to achieve broadband matching and gain. Although it has a flat gain up to 6.5 GHz, both noise figure and input matching exhibit a sharp rise characteristic. The $S_{11}$ is below $-10$ dB for frequencies below 4.5 GHz and quickly rises to $-5$ dB at 7 GHz. The noise figure rises from about 3.3 dB at 1 GHz to about 6.3 dB at around 6.5 GHz. The high NF is due to the large difference between $\Gamma_s$ and $\Gamma_{opt}$, which is usually very far away from the 50 Ω input.
for CMOS. It is not possible for this configuration to have low noise and good input match at the same time [18]. The circuits for [60] and [61] are shown in Figure 4.1 (a) and Figure 4.1 (b) respectively. The filters enable broadband input matching. It is, however, not possible for broadband SNIM. Nevertheless, $\Gamma_s$ and $\Gamma_{opt}$ are very close in MOS devices [5]. Thus, good noise performance can still be obtained. The drawback of these LNA’s is that they require complicated filter networks to achieve broadband matching. The number of inductors is high and this directly translates into higher costs.

A feed-forward noise-cancelling LNA design technique was proposed in [62]. Here an active device is used for input impedance matching. A common gate amplifier, for example, can be used that is able to provide good input match for a very large bandwidth [63]. The input matching circuit, which has a very poor noise performance, is then followed by a noise-cancelling circuit to eliminate the large amount of noise generated from the input matching stage as shown by the block diagram in Figure 4.2.
This methodology has multiple advantages over other LNA designs. First, there is broadband input matching. Second, sub 3 dB noise figure is achievable at the lower end of the spectrum. Third, the circuit is very compact since no inductors are used. Fourth, a high wideband gain with a low NF is achievable. Due to these advantages, this technique is used to design the low-noise transconductors for the mixer in this chapter.

To extend the bandwidth of the mixer, the inductive peaking technique is used where inductors are placed between the transconductors and the mixer switching
pairs. The current bleeding technique is also used to decouple the DC current dependence between the switching pairs and the transconductors. Figure 4.3 shows a block diagram of the proposed broadband low-noise mixer. The LNA and mixer are therefore merged seamlessly into a single component. This current-reuse topology is very attractive because the mixer current is completely reused by the LNA.

4.3 Circuit Implementation

This section describes the design of noise-cancelling transconductors, switching pairs and bleeding circuit as well as the inductive peaking technique in greater detail. In depth theoretical noise analysis and optimization analysis are given for the transconductors. Simulation and measurement results are provided at the end of the chapter.

4.3.1 Low-Noise Transconductor with Noise Cancellation

Figure 4.4 shows the schematic of the noise-cancelling transconductor without biasing circuitry. The circuit was inspired by the LNA’s proposed in [64] and [65]. The

![Figure 4.4: Noise-cancelling transconductor schematic.](image)
common gate (CG) transistor at the first stage is the input matching network since the impedance looking into to source is about $1/g_m$. The input impedance of $M_3$, which has a common source (CS) configuration, is large due to its $C_{gs}$. Therefore, the input impedance of the circuit is dominated by $M_1$ at low frequencies. As noted before, the noise generated from the CG matching network is high. Thus, a noise-cancelling circuit is placed after the matching circuit to cancel the noise and provide a high gain. The noise-cancelling circuit is comprised of two amplifiers ($M_2$ and $M_3$) in CS configuration. To see how the noise-cancelling method works, it is necessary to go back to the transistor noise model in Figure 2.17 in section 2.4.

The drain induced gate noise voltage was expressed by Equation (2.24) and the total drain-current noise including flicker noise can be expressed as

$$|i_{nd}|^2 = 4kT\frac{\gamma}{\alpha}g_m\Delta f + \frac{K}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f.$$  

(4.1)

For the input matching network, the gate noise can be referred to the output and combined with the drain noise. To simplify the model and the subsequent NF derivation, gate resistance noise and substrate noise are not included. However, they can be included to reflect the true noise performance of the CG amplifier. The noise model for the CG amplifier stage is shown in Figure 4.5, where $|i_{n_{mn}}|^2$ is the total noise current flowing through the matching transistor, from drain to source. This is

---

Figure 4.5: CG noise model.
an important property that is used later to achieve noise cancellation.

Figure 4.6 shows the noise voltages $V_x$ and $V_y$ across $R_1$ and $R_S$ respectively at the front-end. Two nodes are defined here: node x and node y. The input matching circuit is a CG amplifier, so the signal voltage at node x and node y are in phase. However, since the noise current of the amplifier flows through the transistor, the noise voltage at node x and node y are $180^\circ$ out of phase. Thus, if a voltage adder is placed after the input matching stage, the signals at nodes x and y will be added while the noise voltages will be subtracted. The adder can also be tuned such that the noise voltages are completely cancelled. It should be noted that only the noise voltages caused by the transistor $M_1$ are cancelled. The noise coming from $R_1$ is not cancelled. It will be shown later how to minimize its noise contribution. Furthermore, the noise coming from the voltage adder is not cancelled. Thus, the adder must provide a high gain to reduce its noise contribution and the overall NF.

A simplified version of the LNA is shown in Figure 4.7. Here, the adder comprises two ideal voltage controlled current sources. This configuration provides a large gain...
and consists of only three transistors. The noise current from $M_1$ at the output is

\[ |i_{\text{in}}|^{2} = |g_{m3}V_{x} - g_{m2}V_{y}|^{2} = |i_{\text{in}}|^2 (g_{m3}R_{S} - g_{m2}R_{1})^2. \]  

(4.2)

To achieve perfect cancellation, $g_{m2} = (R_{S}/R_{1})g_{m3}$. Thus, the noise from the noisiest component of the entire LNA is eliminated. It should be noted that $M_1$’s flicker noise, substrate noise, and thermal noise from the gate can all be cancelled as they can be referred to the output of the transistor [63].

Figure 4.8 shows the adder circuit that is realized with two CS amplifiers. The
signals at nodes x and node y are added at node z. On the contrary, the out-of-phase noise voltages at nodes x and y are subtracted at node z. At low frequencies, the high input impedance of the CS amplifier prevents the $M_1$ noise current from feeding through into node z, as this will complicate the design. It can be seen that this configuration is suitable at the low end of the frequency spectrum. However, as technology advances, smaller device size will be available with a higher $f_T$ which can push this noise-cancelling methodology into higher frequencies.

For the adder, the input matching constraint has been removed. The sizes of transistors $M_2$ and $M_3$ can be chosen freely as long as the noise cancellation criteria holds. First, a large $g_m$ is desired since it is directly proportional to the mixer gain. So a large device size is preferable. In addition, a large $g_m$ reduces the NF of the LNA. Second, the device size cannot be too big as the large $C_{gs}$ of $M_3$ will affect the input match, rendering the input matching circuit useless. Furthermore, a large $C_{gd}$ will affect the noise-cancelling ability of the adder. Undesired Miller effect will also affect the input matching network.

In order to obtain a design guideline and quantify the above view, the noise figure of the transconductor is derived. Since it is a transconductor, noise currents were used instead of noise voltages in the derivation. The body effect is also considered for $M_1$ as the body effect affects the noise performance and input matching. The circuit in Figure 4.4 is used in the derivation. The body terminal is connected to ground. To simplify the analysis, bias resistors, $C_{gd}$, and $C_{gs}$ are not included. Furthermore, only the channel thermal noise of the transistors was considered as the point of this analysis is to provide a design guideline for this particular circuit. The input impedance of the transconductor is roughly equal to the input impedance of the CG amplifier. The
Figure 4.9: CG small signal model used to calculate total noise current flowing through the matching network.

input impedance and effective transconductance are given by

\[ Z_{in} \approx \frac{r_{o1} + R_1}{1 + (g_{m1} + g_{mb1})r_{o1}} \]  \hspace{1cm} (4.3)

\[ g_{m_{eff}} = g_{m3} + g_{m2} \left[ \frac{1 + (g_{m1} + g_{mb1})r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right] \]  \hspace{1cm} (4.4)

where \( g_{mb1} \) is due to the body effect from transistor \( M_1 \). To calculate the noise current \( |i_{n_{mn}}|^2 \), the small signal model in Figure 4.9 is used and can be expressed by

\[ i_{n_{mn}} = \frac{i_{nd}}{1 + \frac{R_1 + R_S}{r_{o1}} + (g_{m1} + g_{mb1})R_S} \].  \hspace{1cm} (4.5)

Thus, the noise voltage at node x is

\[ V_x = i_{n_{mn}} R_S. \]  \hspace{1cm} (4.6)

The noise voltage at node y will be the sum of the noise voltages due to \( i_{n_{mn}} \) and \( R_1 \) and is given by

\[ V_y = -i_{n_{mn}} R_1 + \sqrt{4kTR_1}. \]  \hspace{1cm} (4.7)
The noise currents from $M_2$ and $M_3$ and the total noise current out of the transconductor are

$$i_{n2} = -g_{m2}i_{mn}R_1 + g_{m2}\sqrt{4kT}R_1 + \sqrt{\frac{4kT\gamma g_{m2}}{\alpha}}$$

(4.8)

$$i_{n3} = g_{m3}i_{mn}R_S + \sqrt{\frac{4kT\gamma g_{m3}}{\alpha}}$$

(4.9)

$$i_{nt,added} = i_{n2} + i_{n3}$$

$$i_{n2} = g_{m2}\sqrt{4kTR_1} + \sqrt{\frac{4kT\gamma}{\alpha}}(\sqrt{g_{m2}} + \sqrt{g_{m3}}) + i_{mn}(g_{m3}R_S - g_{m2}R_1)$$

$$i_{n3} = g_{m3}\sqrt{4kTR_S} + \sqrt{\frac{4kT\gamma}{\alpha}}(g_{m2} + g_{m3}) + \sqrt{g_{m3}}(g_{m3}R_S - g_{m2}R_1)^2.$$  

(4.10)

The noise voltage at the input as well as the noise current at the output due to the noise at the input from $R_S$ are

$$v_{iniz} = \sqrt{4kTR_S} \frac{Z_{in}}{R_S + Z_{in}}$$

(4.11)

$$i_{nout,in} = v_{iniz}g_{m,eff}$$

$$\frac{\mid i_{nout,in} \mid^2}{\mid i_{nout,in} \mid^2} = \frac{4kT}{R_S}(Z_{in}||R_S)^2 \left\{ g_{m3} + g_{m2} \left[ \frac{1 + (g_{m1} + g_{mb1})r_{ol}}{1 + \frac{r_{ol}}{R_1}} \right] \right\}^2.$$  

(4.12)

The noise factor is defined as

$$F = \frac{SNR_{iniz}}{SNR_{out}} = \frac{Noise_{out}}{G \cdot Noise_{iniz}}$$

$$= 1 + \frac{Noise_{added}}{G \cdot Noise_{iniz}} = 1 + \frac{\mid i_{nt,added} \mid^2}{\mid i_{nout,in} \mid^2}.$$  

(4.13)

After substituting Equation (4.10) and (4.12) into the above equation, the noise factor
becomes

\[
F = 1 + \frac{g_{m2}^2 R_1 + \frac{\gamma}{\alpha} \left[ g_{m2} + g_{m3} + \frac{g_{m1}(g_{m3} R_S - g_{m2} R_1)^2}{\left(1 + \frac{R_1 + R_S}{r_{o1}} + (g_{m1} + g_{mb1}) R_S \right)^2} \right]}{1 + \frac{1}{R_S} (Z_{in} || R_S)^2 \left\{ g_{m3} + g_{m2} \left[ \frac{1 + (g_{m1} + g_{mb1}) r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right] \right\}}.
\]

The above noise factor equation can be simplified to show how the components affect the NF. First, assume that there is perfect noise cancellation, which means \( g_{m2} = (g_{m3} R_S) / R_1 \). Next, it is assumed there is a perfect input match such that \( Z_{in} \approx 1 / g_{m1} = R_S \). It is further assumed that there is no body effect on \( M_1 \). The simplified noise factor becomes

\[
F = 1 + \frac{\frac{g_{m3}^2 R_S}{R_1} + \frac{\gamma}{\alpha} g_{m3} \left( \frac{R_S}{R_1} + 1 \right)}{1 + \frac{R_S}{R_1} + \frac{\gamma}{\alpha} \left( \frac{R_S}{R_1} + 1 \right) \frac{1}{g_{m3} R_S}}.
\]

The above equation provides a design guideline for this circuit. Since \( R_S \) is fixed, only the values of \( R_1 \) and \( g_{m3} \) can be changed. \( R_1 \) should be made as big as possible to reduce its noise contribution. However, \( Z_{in} \approx \frac{r_{o1} + R_1}{1 + (g_{m1} + g_{mb1}) r_{o1}} \), which is proportional to \( R_1 \). If \( R_1 \) is too big, the transconductor will lose its broadband input matching ability. The body effect is desired for \( M_1 \) because a larger \( R_1 \) can be used while maintaining a good input match. The body effect also increases \( g_{m_{eff}} \) which reduces the overall noise. A large \( g_{m3} \), which is directly related to \( g_{m2} \), is preferred as it not only provides a high gain, but also reduces the noise coming from \( M_2 \) and \( M_3 \). Again, they can’t be too big as \( C_{gs} \) from \( M_3 \) could ruin the input matching circuit. It should
be noted that the above equation is only a first order approximation as it ignores some high frequency and noise parameters.

The layout for the transistors $M_2$ and $M_3$ is very important. Due to their large sizes, undesired noise coupling as well as gate resistance noise and substrate noise can be amplified significantly and drastically increase the noise figure. In section 2.4, it was explained that the thermal noise from the polysilicon gates can be reduced by using multiple fingers and dual connected gates. For a fixed total device width, more fingers translates to shorter per-finger width. By reducing individual finger width, the thermal resistance noise can be significantly reduced. However, there is an optimum point beyond which shrinking the per-finger width will increase the transistor noise. This is caused by the gate-bulk capacitance ($C_{gb}$). By having more fingers, the number of contact pads, whose size is large relative to the gate length, increases. If the gates are dual connected, the number of pads required is $2 \cdot N$, where $N$ is the number of fingers. This increases $C_{gb}$ and $F_{\text{min}}$. In [66], it was shown that for CMOS 0.13 $\mu$m technology, the optimum width for best noise performance is around 2 $\mu$m.

The finger width for the mixer proposed in this chapter is therefore 2 $\mu$m. All of the gates are dual connected and triple wells are used $M_2$ and $M_3$ to reduce substrate coupled noise. The body of $M_1$ is connected to ground to increase the body effect of the CG amplifier. In this CMOS technology, transistors $M_2$ and $M_3$ are biased with a 0.6 V gate voltage to achieve minimum NF for each transistor.

### 4.3.2 Switching Pairs and Current Bleeding

The sizing of the switching pairs and the bleeding circuit are essentially the same as described in subsection 3.3.2. To reduce the switching voltage to have more ideal
switching and lower power LO, the number of fingers should be more than 20. In this
design, 40 fingers are used for the switches. The bleeding circuit is used to reduce the
DC current through the switches to reduce their noise contribution and to increase
the gain since larger load resistors can be used.

As explained in the previous section, large $M_2$ and $M_3$ are desired in order to
reduce their own noise contribution in the overall circuit. The amount of current
draw subsequently increases. In this design, each transconductor draws 12.2 mA of
current. Heavy current bleeding is necessary to achieve a high, or even moderate,
gain. Therefore, the bleeding circuit is designed to supply 80% of the transconductor
current in order to keep the gain above 15 dB. Figure 4.10 shows the switching pairs
and bleeding circuit as well as the IF load resistors in this mixer.

The mixer bandwidth can be significantly affected by the large output capacitance
from $M_2$ and $M_3$ as well as from the bleeding circuit and the switching pairs. The
bandwidth extension technique described in the next section is applied to increase
the bandwidth to meet the design goal of 6 GHz.
4.3.3 Inductive Peaking

Inductive peaking has been widely used for bandwidth extension. There exists the series, shunt, and series and shunt peaking techniques. Series peaking is used in this design and the peaking inductors are placed between the switching pairs and the current bleeding circuit as shown in Figure 4.11. To understand the purpose of these inductors, a simplified circuit is shown in Figure 4.12 when only one of the switches is on. Preceding the mixer core is the transconductor, which can be approximated by a voltage-controlled-current-source; $C_{\text{out}}$ is the collective output capacitance from the transconductor and the bleeding circuit; $R_{\text{load}}$ is the mixer load resistor, assuming there is no loss through the switch and the tail capacitance of the off switch is negligible compared to the load resistor.

The basic theory of inductive peaking can be explained with Figure 4.12 and a step response. Imagine the circuit without the inductor, the rise time at the output is about $2.2RC$ if the rise time is defined to be the elapsed time between 10% and 90% of the final output voltage value. To decrease the charge time, i.e. increase the

Figure 4.11: Inductive peaking mixer core.
bandwidth, the inductor is used. At $t = 0$, there is a sudden step change in the current source. The high impedance of the inductor decouples the resistor from the capacitor, which means all the current goes into charging the capacitor. Therefore, the rise time decreases and hence the bandwidth enhancement [67]. This is also why the peaking inductors are placed in between the bleeding circuit and switching pairs but not in between the transconductors and the bleeding circuit to take full advantage of the peaking inductors.

The transfer function for the circuit in Figure 4.12 can be expressed as

$$\frac{v_o}{i_{out}} = \frac{-R_{load}}{1 - \omega^2 L_{peak} C_{out} + j\omega C_{out} R_{load}}. \quad (4.16)$$

After substituting $L = m R_{load}^2 C_{out}$, where $m$ is a constant, and $s = j\omega$ into the above, the transfer function becomes

$$\frac{v_o}{i_{out}} = \frac{-1}{m R_{load} C_{out}^2} \cdot \frac{1}{s^2 + \frac{s}{m R_{load} C_{out}} + \frac{1}{m R_{load}^2 C_{out}^2}}. \quad (4.17)$$

The poles of this transfer function are

$$s_{1,2} = -\frac{1}{2m R_{load} C_{out}} \pm \sqrt{\frac{1}{4m^2 R_{load}^2 C_{out}^2} - \frac{1}{m R_{load}^2 C_{out}^2}}. \quad (4.18)$$
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Figure 4.13: Poles \( s_1 \) and \( s_2 \) in the complex plane moving with respect to \( m \).

With no inductor (\( m = 0 \)), the poles are at \(-1/R_{\text{load}}C_{\text{out}}\) and \(-\infty\). As the inductance increases, the poles start to move along the real axis towards \(-2/R_{\text{load}}C_{\text{out}}\) and meet at that point when \( m = 0.25 \). Beyond \( m = 0.25 \), the poles split into complex conjugates and travel along the circle with a radius of \( 1/R_{\text{load}}C_{\text{out}} \) and a center at \(-1/R_{\text{load}}C_{\text{out}}\).

Figure 4.13 depicts how the poles move in terms of the inductance or \( m \). Therefore, it can be clearly seen that the inductor plays an important role in expanding the bandwidth by introducing a new pole and subsequently affecting the existing pole in the transfer function.

4.4 Simulation Results

Figure 4.14 is the complete circuit of the noise-cancelling mixer. Inductors \( L_1 \) and \( L_2 \) are used in front of the transconductors to extend the input-matching range to 6 GHz. Shunt-and-series inductive peaking could have been used in the transconductors to further extend the bandwidth beyond 6 GHz. However, the large number of inductors used increases the chip size. Furthermore, the number of inductors would
be comparable to the UWB LNA’s mentioned at the beginning of the chapter, making this noise-cancelling approach less attractive.

No on-chip differential-to-single-ended buffer is used in this design. The buffer used in chapter 3 significantly degrades the performance of the mixer in terms of linearity and it required a large power consumption. Therefore, in this design, an off-chip differential-to-single-ended output buffer with a high input impedance and unity voltage-gain will be used in the measurement. The buffer is MAX4444 from Maxim Integrated Products, Inc. and it has a differential input resistance of 82 kΩ,
an output impedance of 0.7 Ω, and a voltage gain of 2 V/V. A 50 Ω SMA resistor is placed at the output of the buffer to provide output matching and change the overall buffer voltage gain to 1 V/V. Since no models are available for the buffer, Figure 4.15 was used to model the buffer in simulation.

Figure 4.16 shows the layout of the circuit using IBM CMOS 0.13 μm technology. The chip size is 1 mm by 1 mm (1 mm²) including pads. The size of the mixer itself is only about 500 μm by 630 μm (0.315 mm²). The layout was completed in Cadence and extracted by ASSURA using the RC option, which extracts both parasitic capacitance
and resistance. Post-layout simulation was run using ADS through the Cadence-ADS Dynamic Link. The mixer is designed to have an LO power of 0 dBm. For all simulation and measurement results, the IF is always kept at a constant 250 MHz, while the RF and LO frequencies are being changed together with the LO being 250 MHz lower than the RF. Ideal 180° hybrids were used in the simulation to generate the differential RF and LO.

Figure 4.17 (a) shows the simulated conversion gain of the mixer versus the RF frequency. The upper 3 dB cut-off frequency is at 6.1 GHz. The gain is reasonably flat with a gradual roll-off. The peaking inductors play an important role in achieving this bandwidth. Also included in this plot is the simulated result without the peaking inductors. The importance of the peaking inductors can be clearly seen in this plot, where there is a much sharper gain roll-off compared to the simulated result with peaking. Simulation shows that without the peaking inductors, the upper 3 dB frequency drops to 3.8 GHz and a downward-sloped gain across the entire bandwidth.
The peaking inductors have a value of 1.02 nH. Together with the two inductors at the input whose inductances are 467 pH, the bandwidth has been extended by 2.3 GHz. The gain at 1 GHz is 20.45 dB and at 6 GHz is 17.49 dB with an average value of 18.97 dB.

Figure 4.17 (b) shows the simulated double-sideband noise figure of the mixer. \( NF_{DSB} \) is simulated instead of \( NF_{SSB} \) is due to the difficulty encountered during the measurement of the previous mixer in chapter 3. Since no broadband tunable filters were available to filter the noise power of the image sideband, it is much easier to simply measure the \( NF_{DSB} \) and compare it the simulation results. It is also much accurate since no assumptions about the gain flatness or noise flatness need to be made in a DSB measurement.

From the plot, it can be seen that below 3 GHz, the noise is relatively flat with an average value of 3.35 dB. This is the region where significant noise cancellation is happening. Beyond 3 GHz, parasitics in the upper and lower paths of the transconductor affects its cancellation ability. This is due to \( C_{gs} \) and \( C_{gd} \) as well as any other parasitics that were not taken into account. The effect of these parasitics affects the

![Figure 4.18: Simulated differential input reflection coefficient.](image-url)
relationship between $g_{m2}$ and $g_{m3}$ such that noise cancellation is happening very well around the low end of the spectrum and not so well at the higher end. As the frequency is increased, there is more mismatches between the two paths which lead to the indefinite increase in noise figure. Nevertheless, the mixer shows excellent noise performance where the noise figure has an average value of 3.75 dB across the entire frequency band.

Figure 4.18 shows the simulated input reflection coefficient. Because of the CG matching network and the inductors at the input, the mixer is able to have a flat $S_{11}$ across the entire band. The $S_{11}$ is below $-10$ dB up to 6 GHz as shown in the plot.

The simulated input referred $P_{1dB}$ of the mixer is shown in Figure 4.19 (a). The $P_{1dB}$ is very consistent across the whole frequency band, hovering between $-17.9$ dBm and $-15.2$ dBm with an average value of $-16.3$ dBm.

To simulate the IIP3 of the mixer, a two-tone simulation was conducted across the whole bandwidth. Two signals separated by 1 MHz were injected into the mixer.
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Their power levels were swept and the IIP3 extrapolated. The results are plotted in Figure 4.19 (b). The IIP3 is, similar to $P_{1dB}$, very consistent from 1 to about 5 GHz, between $-8.6$ and $-7$ dBm. However, unlike $P_{1dB}$, the IIP3 increases sharply beyond 5 GHz. The sudden increase in IIP3 is due to the distortion cancellation property that the noise-cancelling transconductor also has. The noise cancellation mechanism can also be used as distortion cancellation [63]. The theory behind its operation is very much the same. However, the component values and $g_m$’s for perfect noise cancellation are different than perfect distortion cancellation. In the case of this mixer, noise cancellation is occurring at the low end of the spectrum while distortion cancellation is happening at the high end.

The LO-to-RF feedthrough is plotted in Figure 4.20. A large isolation is observed. It is at least more than 83 dB over the whole band and below 90 dB for frequencies below 2.7 GHz. The LO feedthrough increases as frequency increases. This is expected as parasitic capacitances and any unwanted electromagnetic coupling have a more dominant effect at higher frequencies.

The complete mixer draws a total current of 23.73 mA from a 1.5 V supply.
4.5 Measurement Results

Figure 4.21 is the microphotograph of the fabricated chip. The chip was fabricated with IBM’s CMOS 0.13 μm technology. It has 8 metal levels, namely 3 thin, 2 thick, and 3 RF metal layers. The inductors are all fabricated at the top most metal layer. In this CMOS process, the substrate that is directly underneath the inductors can be made highly-resistive. The Q of the inductors are therefore better when compared to the 0.18 μm technology used for the chip in the previous chapter of this thesis.

All three ports of the mixer are fully differential. GSGSG coplanar waveguide probes with a pitch of 100 μm were used for the RF and LO ports. Since fully differential signals are required for the RF and the LO, external 180° hybrids were used.

Figure 4.21: Microphotograph of the noise-cancelling mixer.
to convert the single-ended signals from the signal generators into fully differential signals. For the IF port, a GSGSG probe with a pitch of 150 µm was used. The external buffer is used to combine the differential IF signal into a single-ended output. A PCB was fabricated for the buffer and the buffer chip was soldered onto the PCB. The board is then connected directly to the probe to reduce the transmission line effect and provide a proper large impedance load to the mixer output. Figure 4.22 shows the measurement setup where the thick lines represent coaxial cables. The biasing voltages were first tuned so that the mixer could have the best possible broadband noise performance. Those voltages were then fixed and untouched and all of the subsequence measurements were conducted with the same biasing voltages across the whole frequency span.

The conversion gain of the mixer is measured across the input frequency ranging from 1–6 GHz. The input RF power was kept at -40 dBm and the input frequency was swept with a step size of 100 MHz. This step size was chosen so that the measured plot would have high frequency resolution since this is one of the most important measurement in a broadband circuit. Figure 4.23 (a) shows the measured results, which also contains the simulated results for easy comparison. The measured gain varies from 17.5 dB at 1 GHz to 13.6 dB at 6 GHz. The measured upper 3 dB frequency cut-off point is at 5.5 GHz, which means the fabricated mixer operates between 1 and 5.5 GHz, which has a 3 dB bandwidth of 4.5 GHz. The bandwidth
Figure 4.23: Measured conversion gain and NF\textsubscript{DSB} versus input frequency: (a) gain and (b) DSB noise figure.

decreases from the designed 5 GHz to 4.5 GHz. There is a roughly 3 dB difference in gain between simulation and measurement across the whole frequency span. The discrepancy is caused by the off-chip buffer that has some loading effect on the mixer output. Since no models were available for the buffer, it was not possible to include the effect of the buffer in the simulation. Nevertheless, it can be seen that both the simulated and measured gain responses share a similar shape even at very low frequencies, which means the discrepancy was not caused by parasitics that were not properly modelled within the chip itself.

Figure 4.23 (b) shows the measured double-sideband noise figure. Again, a frequency step size of 100 MHz was used in order to increase the resolution. The mixer has a low and relatively flat noise figure across a large 4.5 GHz bandwidth. The measured NF\textsubscript{DSB} is below 3.5 dB and 4 dB for frequencies below 2.2 GHz and 4 GHz respectively. The absolute NF\textsubscript{DSB} minimum was 2.4 dB at 1.2 GHz and the maximum was 5.1 dB at 5.5 GHz, with an average of 3.9 dB across the whole frequency
Figure 4.24: Measured IIP3 and \( P_{1\text{dB}} \) from 1 to 6 GHz: (a) IIP3 measurement at 5 GHz and (b) input referred \( P_{1\text{dB}} \) and IIP3 across the whole span.

Figure 4.25: Measured \( S_{11} \) and LO-to-RF isolation vs frequency: (a) input reflection coefficient and (b) LO-to-RF port-to-port isolation.

range. The average uncertainty was ±0.3 dB. There is a strong agreement between the measured and the simulated results. The slope of the measured NF is higher than that of the simulated NF. Due to the noise cancellation nature of the mixer, undesired parasitics affect the noise cancellation ability of the mixer. Therefore, it is more pronounced at high frequencies, hence the increase in slope.
The $P_{1\text{dB}}$ and IIP3 of the mixers were measured. To measure $P_{1\text{dB}}$, a single tone was injected and the output power measured versus different input power levels. At 5 GHz, the input referred $P_{1\text{dB}}$ was $-10.5$ dBm. To measure the IIP3, a two-tone signal separated by 1 MHz was used. Shown in Figure 4.24 (a) is the measured IF and IM3 output powers with the input RF frequency at 5 GHz and the extrapolated IIP3 was $+0.84$ dBm.

It would be of interest to also see the frequency responses of $P_{1\text{dB}}$ and IIP3. Figure 4.24 (b) shows the measured and simulated frequency responses. Both measured $P_{1\text{dB}}$ and IIP3 were higher than simulation because of the lost in gain mentioned previously. The measured $P_{1\text{dB}}$ has an average value of $-12.3$ dBm. The IIP3 is high, from $-5.64$ dBm at 1 GHz to $-1.48$ dBm at 6 GHz. It can be seen that the shape of the measured IIP3 from 1 to 6 GHz closely resembles the shape of the simulated IIP3 from 3 to 8 GHz. The biasing voltages adjusted at the beginning of measurement for best noise performance affected the linearity and distortion cancellation of the mixer and caused the frequency shift.

Figure 4.25 (a) shows the input reflection coefficient measured by a Vector Network Analyzer. There is a good input match across the entire frequency range and good agreement between simulation and measurement was observed. At 1 GHz, the measured $S_{11}$ was $-8.8$ dB and fell below $-10$ dB after 2.1 GHz.

The LO-to-RF port-to-port isolation was measured. Since the LO is 250 MHz lower than the RF, the isolation was measured from 750 MHz to 5.75 GHz. Figure 4.25 (b) shows the measured and simulated LO-to-RF isolation, where it shows there are more than 55 dB isolation across the entire frequency range, and more than 60 dB isolation at most frequencies.
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</table>

Table 4.1: Comparison of broadband down-converters with this work.

The complete mixer draws a total current of 23 mA from a 1.5 V supply. Table 4.1 shows a comparison between this work and recently published broadband down-converters in CMOS. The mixer outperforms others in terms of noise figure and linearity while still having a comparable gain. Their circuit structures are also different. Only this work and [68] have a current reuse structure whereas [69] is a LNA+Mixer+TIA in cascade and [58] is a folded mixer with a folded low-noise transconductor.

4.6 Conclusion

A new broadband low-noise mixer has been designed with the noise-cancelling technique in CMOS 0.13 µm technology. The noise-cancelling technique allows simultaneous broadband input matching and noise cancellation. Together with the current bleeding technique, a high conversion gain was also achieved. Experimental results show great noise and gain performance. The mixer operates from 1 to 5.5 GHz with an average DSB noise figure of 3.9 dB and a conversion gain of 17.5 dB. Broadband
input matching was achieved with an average $S_{11}$ of $-11.9$ dB. Due to the noise-cancelling transconductors, the mixer is able to have good performance in terms of linearity, with an IIP3 of $+0.84$ dBm at 5 GHz, despite its high gain. The mixer is also very compact, with the mixer core size being only $0.315$ mm$^2$. 
Chapter 5

Low-Noise Self-Oscillating Mixer

5.1 Introduction

Narrowband and broadband low-noise mixers introduced in the previous chapters demonstrated the feasibility of combining the LNA and a mixer to achieve low-power and highly integrated IC’s. In chapter 3, the narrowband low-noise mixer achieves those goals by relaxing the gain and noise requirement of the first stage LNA. In chapter 4, the broadband low-noise mixer achieves those goals by merging a broadband LNA with a mixer so that only one mixer is required in a multi-band, multi-standard system. Furthermore, the DC biasing current is reused in both cases. In this chapter, a new low-noise mixer is proposed where the VCO is integrated into the mixer. It is a current-reuse structure in which the VCO, mixer, and LNA form a single component where the VCO current is completely reused by the mixer and the LNA.

Low power and highly integrated IC’s have been the trend in IC design, especially in mobile communication where there is a limitation in battery life. To save power, combining the oscillator and mixer has been proposed. These oscillator-mixers are
known as self-oscillating-mixers (SOM). Examples can be found in [70, 71]. However, their noise figure is relatively high. To further save power, a single-balanced SOM with an integrated LNA was proposed in [72, 73]. Nevertheless, the single-balanced approach misses a lot of the advantages that the double-balanced approach has. Therefore, in this chapter, a new fully-integrated double-balanced low-noise self-oscillating-mixer is demonstrated to work with an RF of 8 GHz and an IF of 300 MHz.

5.2 SOM Concept

The main idea is to incorporate the LNA into the SOM. A lot of SOM circuits have been proposed over the years. Shown in Figure 5.1 is a simple SOM with the Gilbert cell configuration that was demonstrated in [70]. The SOM is a ring oscillator with four mixer blocks, one of which is shown in Figure 5.1 (a), that are put in cascade as

Figure 5.1: Quadrature self-oscillating ring mixer from [70] with permission ©1999 IEEE: (a) schematic of a single block and (b) overall system diagram.
Figure 5.2: Low-power oscillator mixer from [71] with permission ©2006 IEEE: (a) schematic and (b) block diagram.

shown in Figure 5.1 (b) to generate oscillation. It works at 1.2 GHz with a conversion gain of $-1$ dB and uses a 3.3 V supply. Unfortunately, this topology requires a high supply voltage due to the number of NMOS transistors and resistors stacked upon the Gilbert cell. Furthermore, four mixer blocks were used which increases power consumption.

Another approach that makes use of a LC oscillator was proposed in [71] to reduce the voltage headroom and improve the oscillator phase noise. The design, shown in Figure 5.2, stacks a Gilbert cell mixer on top of an LC oscillator. The oscillator hard switches the switching pairs as shown in Figure 5.2 (b) to achieve mixing. It would be difficult to convert this mixer into a low-noise mixer because the transconductors in this case are not time-invariant. Furthermore, each switching pair would require three to four inductors to turn it into a low-noise switching pair. The number of inductors all together would be around seven to nine.
A single-balanced SOM was proposed in [72]. The circuit, shown in Figure 5.3, is essentially a single-balanced active mixer with a low-noise transconductor and an LC oscillator stacked at the top. However, the single-balanced structure lacks a lot of advantages the double-balanced mixer has. $C_{diff}$ was used to close the oscillator loop at the oscillating frequency. In addition, a transimpedance amplifier (TIA) as opposed to a resistor is used as the IF load in order to achieve its 36 dB conversion gain and a 4.8 dB noise figure with an RF of 1.57 GHz.

The block diagram of the low-noise SOM that is proposed in this thesis is shown in Figure 5.4. In this design, a low-noise Gilbert cell mixer similar to the one in chapter 3 is used as the mixer core. A negative gm oscillator is stacked onto the mixer similar to Figure 5.3. However, the major difference is that the oscillator will be configured to be used as the differential loads. A lot of voltage headroom is saved, enabling the mixer to work at very low voltages. The mixer does not need to be used together with other circuits such as a TIA, thus making this low-noise SOM a complete standalone component, with all of the advantages of a double-balanced mixer. The current used
CHAPTER 5.  LOW-NOISE SELF-OSCILLATING MIXER

Figure 5.4: Proposed low-noise SOM block diagram.

by the oscillator is reused by the mixer core, which is further reused by the low-noise transconductors, making this SOM a super current-reuse structure. This circuit is designed using IBM’s CMOS 0.13 \( \mu \)m process with a voltage supply of 1.5 V at an RF of 8 GHz.

5.3 Circuit Implementation

This section provides a detailed description and design analysis of the major blocks in the proposed low-noise SOM. The LC oscillator will be discussed since it is an integral part in this mixer design. The current bleeding, switching pair, and low-noise transconductor blocks are described briefly in the first section since a detailed design analysis has been provided in chapter 3. It is followed by the SOM operation with a heavy emphasis on the oscillator load analysis and the conversion gain of the mixer is derived. Finally, the buffer circuit is briefly described.
5.3.1 Negative gm Oscillator

The LC oscillator used in this design is a cross-coupled negative gm oscillator as shown in Figure 5.5. Two identical transistors are cross-coupled to provide the negative resistance for the LC tank. $C_{\text{var}}$ are variable capacitors so that the oscillating frequency can be adjusted through the bias voltage $V_{\text{tune}}$. A bias transistor is placed at the bottom to control the tail current and output voltage swing.

To analyze this classic oscillator, the cross-coupled pairs and the LC tank are separated as shown in Figure 5.6. The input impedance of the cross-coupled pair can be calculated very easily and is found to be

$$Z_{in} = \frac{-1}{g_m - j\omega C_{gs}} = \frac{-1}{g_m \left(1 - j\frac{\omega}{\omega_T}\right)}$$  \hspace{1cm} (5.1)

which can be simplified to $Z_{in} = -1/g_m$ when the VCO is operating at a frequency much less than $\omega_T$, the frequency at which the current gain drops to unity. The

Figure 5.5: Negative gm oscillator.
Figure 5.6: The oscillator transistor pair and LC tank: (a) cross-coupled pair and (b) LC resonating tank.

The oscillating frequency is determined by the tank capacitance and the \( C_{gd} \)'s of the cross-coupled pair and can be expressed as

\[
\omega_o = \frac{1}{\sqrt{L_{tank} (C_p + C_{var} + 2C_{gd})}}. \tag{5.2}
\]

Due to the finite Q of the inductors and capacitors, the LC tank is actually a parallel RLC circuit. It is important to find the equivalent parallel circuit. The Q’s of the capacitors and variable capacitors are usually much higher than that of the inductor, therefore the Q of the inductor is the limiting factor in the tank. The non-ideal inductor can be modelled by a resistor in series with an ideal inductor and can be calculated as

\[
R_s = \frac{\omega L}{Q}. \tag{5.3}
\]

The series RL circuit needs to be converted into parallel RL circuit. It can be shown that near the resonant frequency of the tank, the parallel resistance and inductance
can be expressed as

\[ R_p = R_s(Q^2 + 1) = \frac{\omega L}{Q} (Q^2 + 1) \]  \hspace{1cm} (5.4)

\[ L_p = L_s \left( \frac{Q^2 + 1}{Q^2} \right) \]  \hspace{1cm} (5.5)

where \( Q \) is the unloaded inductor \( Q \) near the resonant frequency of the tank. For large \( Q \), \( L_p \) is approximately equal to \( L_s \). To start oscillation, the negative conductance provided by the cross-coupled pair needs to be larger than \( 1/R_p \). Using Equation (5.1), the \( g_m \) required can be calculated by

\[ \left| \frac{1}{R_m} \right| > \frac{1}{R_p} \]  \hspace{1cm} (5.6)

\[ g_m > \frac{Q}{\omega L(Q^2 + 1)} \]  \hspace{1cm} (5.7)

To ensure oscillation, \( g_m \) is usually made at least twice the value it should be to account for any parasitic resistances in the tank and the cross-coupled pair.

The oscillation action can be thought of as the transistors of the cross-coupled pair being turned on and off periodically. The output voltage swing is therefore dependent on and proportional to the tail current and the resonator \( Q \)

\[ V_{\text{tank}} \propto i_{\text{tail}} \cdot R_p \propto i_{\text{tail}} \cdot \frac{Q^2 + 1}{Q} \]  \hspace{1cm} (5.8)

To increase the RF power output, it is sensible to increase either the tail current or the inductor \( Q \). However, increasing the tail current increases power consumption. Therefore, there has been constant research on improving inductor \( Q \)'s. High \( Q \) inductor also means that the required \( g_m \) to start oscillation can be reduced.
This is true in the current-limiting region of the oscillator. However, there is a point where a further increase in current does not lead to an increase in RF output power. This is the voltage-limiting region where the output swing is limited by the DC voltage supply.

One of the design challenges in oscillator design is phase noise. Phase noise arises from thermal noise and flicker noise of the cross-coupled pair, tail transistor, and the LC tank. The injected noise affects the amplitude and phase of the oscillator. Figure 5.7 shows the spectrum of an ideal and a real oscillator. An ideal oscillator only oscillates at the designed frequency and its frequency spectrum is just an impulse at $\omega_o$, whereas the real oscillator has a spread-out spectrum due to the bandpass nature of the LC tank. In the time-domain, phase noise produces jitter and amplitude variation.

The effect of phase noise in a downconverting system can be explained by Figure 5.8. After downconversion, the desired signal and interferer overlap each other.
The finite power of the interferer appears as noise power that corrupts the desired signal. That is why reducing oscillator phase noise is one of the important design goals in oscillator design in order to meet a specific standard.

Phase noise is usually plotted in log scale and is shown in Figure 5.9 (a). An equation that characterizes phase noise was proposed by Leeson where a LTI model was used

\[
L(\Delta \omega) = 10\log \left[ \frac{2FkT}{P_{\text{sig}}} \left\{ 1 + \left( \frac{\omega_o}{2Q\Delta \omega} \right)^2 \right\} \left( 1 + \frac{\Delta \omega_1/f^3}{|\Delta \omega|} \right) \right] \quad (5.9)
\]

where \(P_{\text{sig}}\) is the output power, \(F\) is the noise figure, \(\Delta \omega_1/(f^3)\), and \(\Delta \omega\) is the frequency offset from the center frequency since phase noise is normally reported at a given offset. The \(-30\) dB/decade slope is due to flicker-noise; the \(-20\) dB/decade slope is from the circuit thermal noise; and the noise-floor is due to buffers and other parasitics resistances. It can been seen that phase noise can be reduced by increasing the output power and inductor Q.

![Figure 5.9: Phase noise spectrum](image_url)

(a) Phase noise plotted in log scale and (b) circuit noise to phase noise conversion from [74] with permission ©2000 IEEE.
The drawback of this equation is that it lacks the ability to quantitatively predict phase noise. An LTV model was proposed by Hajimiri and Lee [74] to model phase noise and it was found that oscillator phase noise is sensitive to the time the active element returns the energy to the LC tank. It was also found that noise at the fundamental frequency and the harmonics as well as flicker noise gets converted into phase noise as shown Figure 5.9 (b) [74]. This suggests that by putting a tail-capacitor at the sources of the cross-coupled pair can reduce phase noise by eliminating the high frequency noise from the bottom bias transistor. Furthermore, phase noise can be reduced through sizing of the transistors to reduce their flicker-noise [75].

The sizing and overdrive voltage of the cross-coupled pair are very important in terms of phase noise. In [76], it was found that the phase noise of a negative gm oscillator can be improved by setting the width of the cross-coupled pair to their minimum and bias the transistors with high overdrive voltage while maintaining a $g_m$ that is large enough for oscillation. In other words, increase their $f_T$ and therefore, linearity.

The varactors used in the LC tank also contribute to phase noise through AM-PM conversion. The capacitance of a varactor can be written as

$$C = C_0 + V_{tune}k_v.$$  \hspace{1cm} (5.10)

where $C_0$ is the zero bias capacitance and $k_v$ is the varactor sensitivity. This equation explicitly shows the AM-PM conversion. The amplitude noise in $V_{tune}$ affects the varactor capacitance which in turn the oscillation frequency and increases phase noise. If the LC tank has a large tuning range, $k_v$ will be large as well which results in a large phase noise. Therefore, there is a trade-off between phase noise and tuning
CHAPTER 5. LOW-NOISE SELF-OSCILLATING MIXER

range [77].

In this low-noise SOM, the negative gm oscillator was designed following the above guidelines to minimize phase noise. The fundamental oscillating frequency is at 8.3 GHz. Since the oscillator sits on top of the mixer, the total current through the oscillator must equal to the current through the mixer core. The mixer core plays the role of the tail transistor and so any noise from the mixer is turned into phase noise. The oscillator works at the current limiting region because of the low LO power required for the mixer core. The mixer core is optimized with a specific LO power. As explained in this section, if $P_{\text{sig}}$ is fixed then a high Q inductor should be used because of phase noise. The bias current therefore needs to be small in order to achieve the required power.

In this design, a 1.5 V power supply is used. With a limited headroom, the oscillator is allocated with 0.5 V and the mixer with 1 V to ensure its operation without sacrificing $P_{1\text{dB}}$ and gain. The cross-coupled pair is sized to use the allocated voltage space. This means minimum transistor width is used while still having the required current through each of the transistors. The reason for this sizing is to maximize $f_T$ which keeps the phase noise as low as possible. Using Spectre, the simulated $g_m$ is 12.2 mS.

The LC tank is made up of a symmetrical spiral inductor, two capacitors, and two varactors. Besides varactors, capacitors are also used for two reasons. One is that varactors have lower Q’s than capacitors, which can significantly affect the phase noise. Two is because of Equation (5.10), which states that large phase noise can arise from a large tuning range. The fixed capacitors reduce the size of the varactors together with the tuning range. The reason that two series-connected capacitor and
varactor pairs are used instead one parallel-connected capacitor and varactor is to make the LC tank as symmetric as possible.

The varactors used in this design are accumulation-mode MOS (AMOS) varactors. The cross-section of an AMOS varactor is shown in Figure 5.10, where a NMOS transistor is placed inside an n-well. This type of varactor is used because it has a better Q than the normal inversion-mode MOS varactor that sits in a p-substrate. The drain and source of the transistor are connected together. By varying the gate-source/drain voltage, the capacitance of the device is varied, hence the name variable capacitors or varactors.

The varactors are connected as shown in Figure 5.11 (a) where one terminal is connected to $V_{DD}$ and the other to $V_{tune}$. There are two ways to tune the capacitance: gate-biased or diffusion-biased. It was shown in [78] that the diffusion-biased varactors

![Figure 5.10: Accumulation-Mode MOS Varactors.](image)

Figure 5.10: Accumulation-Mode MOS Varactors.
have higher Q than biasing through the gates. The physical connection of a diffusion-biased varactor is shown in Figure 5.11 (b). In this design, the diffusion-biased varactor is used.

Figure 5.12 is the symmetrical spiral inductor for the LC tank. The inductors provided by this technology are octagonal spiral inductors. The octagonal spiral has a higher Q than a square spiral because the magnetic field is more confined and the overall wire length and area of the spiral are reduced which leads to a reduction in parasitic resistance and capacitance. The inductor uses the top two metal layers connected in parallel to achieve a higher Q at the cost of lowering the self-resonant frequency. A metal 1 slotted ground plane is also used to increase the Q.

The components in the LC tank are tuned to achieve the required output power. The inductor is 110 µm by 110 µm with a line width of 8.5 µm to achieve a 458 pH inductance whose self-resonant frequency is 9.65 GHz. The simulated Q is 21.

5.3.2 Low-Noise Mixer Core

The low-noise mixer structure in chapter 3 is used in the SOM design since it marries perfectly with the type of mixer that is required in Figure 5.4. The circuit is modified to suit the requirements of the SOM and the new circuit schematic is shown in Figure 5.13.
Figure 5.13: Low-noise mixer core for the SOM.

The transconductors are designed with the SNIM technique. Because of the relatively high RF frequency, which is 8 GHz in this case, the $C_{gs}$ required is less than that in chapter 3. A small transistor with a total device width of 60 $\mu$m would suffice. If a finger width of 2 $\mu$m is used, then the number of fingers required is only 30. The gate bias voltage for minimum noise figure is 0.6 V in this technology regardless of device size. The current through each transconductor transistor is only 3.84 mA. Thus, the PCSNIM technique is not needed to reduce the current and the design of the low-noise transconductors is much simplified. Furthermore, a smaller $L_g$ can be used because of the SNIM technique.

The inductances needed for $L_g$ and $L_s$ are 3.89 nH and 343 pH respectively. $L_s$ is a 120 $\mu$m by 120 $\mu$m regular octagonal spiral with a line width of 6 $\mu$m as shown in Figure 5.14 (a). For $L_g$, a large inductor is required. However, due to the number of inductors in this design and a chip space constrain of 1 mm by 1 mm, another approach was taken to realize this inductance. Instead of a regular spiral, two spiral
inductors are connected in series as shown in Figure 5.14 (b). The magnetic field is enhanced to realize a much higher inductance value with less space. The specified inductance was achieved with a 170 $\mu$m by 170 $\mu$m series spiral that had a line width of 7.5 $\mu$m. A slotted metal 1 ground plane is placed beneath each of the inductors to increase their inductances and Q’s. Using Equation (3.21), the simulated Q’s for $L_g$ and $L_s$ at 8 GHz are 17 and 18 respectively.

For the switching pairs, their finger number is kept at 40 similar to the previous designs. The bleeding-circuit, however, plays a more important role this time. The first goal is to provide the necessary current to the transconductors. The switching pairs can therefore be biased with a low overdrive voltage, which reduces the LO power needed for switching and makes the switching more ideal.

The second goal is to reduce the current through the oscillator. Since an LC oscillator is going to be placed on top of the mixer, the DC current through the oscillator is completely reused by the mixer. As a result, the current through the switching pairs determines the LO voltage swing of the oscillator. Without the bleeding circuit, all of the current required by the transconductors will flow through the oscillator, causing a very large LO. This would drive the entire mixer into saturation. The bleeding-circuit is therefore required to ensure the SOM operation.
The third goal is to reduce mixer flicker noise. Although the flicker noise of the mixer is of little concern when the IF is at 300 MHz, this is not the case with this particular SOM. As mentioned before, the oscillator circuit converts flicker and thermal noise into phase noise. Since the oscillator sits on top of the mixer so the mixer essentially plays the role of the tail transistor for the oscillator, flicker noise and thermal noise from the mixer get translated into phase noise. Basically the larger the flicker noise, the worse the phase noise would become. As explained in subsection 2.5.1, the flicker noise of the switching pairs directly appears at the output without frequency translation. To reduce the effect of the direct mechanism, the biasing current through the switching pairs should be reduced. The bleeding-circuit is needed to reduce as much of the DC current through the switching pairs as possible since they are the major contributor to flicker noise in the entire mixer core circuit.

The bleeding-circuit is designed to supply around three quarters of the DC current needed by the low-noise transconductors. The noise currents from the bleeding transistors are totally uncorrelated. Each noise current feeds into different switching pairs. Because of this uncorrelation, their noise contribution appears directly at the output, unlike common-mode noise. To minimize their noise contribution, the PMOS pair is also biased at a source-gate voltage of 0.6 V. Thus, larger area devices are needed in order to supply most of the DC current. By reducing the current in the switching pairs, the flicker-noise of the mixer core due to the direct mechanism is reduced.

However, the tail-capacitance from the transconductors, bleeding-circuit, and switching pairs becomes the source of mixer flicker-noise through the indirect mechanism. A parallel inductor, $L_{shunt}$, is placed to reduce as much of that capacitance
as possible and force the RF current to go into the switching pairs. The inductors in Figure 5.14 are inherently asymmetric. Symmetry is very important in the Gilbert cell. In order to achieve the best circuit symmetry possible, two series-connected inductors should be used, but at the cost of space. Instead, a symmetrical spiral inductor can be used in this case. The shunt inductor used in this design is shown in Figure 5.15. Due to the crisscrossing structure, the parasitics are more evenly distributed than the regular spirals, where it can be clearly seen that one side has more parasitic capacitance to the substrate than the other. The symmetric spiral used was 120 by 120 µm with a line width of 5 µm that had an inductance of 1.4 nH. Due to space constraints, four turns were used. Therefore, a high-resistivity substrate is used instead of a metal 1 ground plane so not to reduce the self-resonance frequency.

The mixer core was fine-tuned to work with a 0.45 mA of current through each switching transistors.

5.3.3 Differentially-Loaded SOM Core

The oscillator configuration in Figure 5.5 is not suitable to connect to the mixer core. Since it is on top of the mixer, the only way to connect them is through the source terminal of the cross-coupled pair, which is a single-ended connection. However, the cross-coupled pair can be reconfigured. A single transistor can be realized by
Figure 5.16: New cross-coupled configuration to act as mixer load.

connecting two transistors in parallel. The same cross-couple pair can thus be realized by four transistors as shown on the left of Figure 5.16, where the transistor size is half of the original. This configuration is also as same as connecting two cross-couple pairs in parallel. The source node of the two cross-couple pairs can be separated as shown on the right of Figure 5.16 because there is no current flowing between the sources. This new configuration is able to connect to the mixer core and act as a balanced load. The DC current through each branch is half of the original value and the size of the transistors is also half of that of the original. The effective $g_m$, DC current, and device size of the oscillator are therefore unchanged.

The mixer and the VCO are put together and the SOM core is shown in Figure 5.17. The output voltage of the LC tank is fed to the switching pair through two on-chip capacitors in series that act as DC block. Three different blocks with very much different functions share the same DC current. The DC current of the VCO is reused by the switching pairs, and then by the transconductors.

The $C_{gs}$ of the switching pairs directly load the LC tank. The oscillating frequency can thus be expressed as

$$\omega_o = \frac{1}{\sqrt{L_{\text{tank}}(C_p + C_{\text{var}} + 4C_{gd_{\text{osc}}} + C_{gs_m} + C_{gd_m})}} \quad (5.11)$$
where $C_{gd_{osc}}$ is the gate-drain capacitance from a cross-couple transistor and $C_{gs_m}$ and $C_{gd_m}$ are the gate-source and gate-drain capacitance of the switching transistor respectively. The output of the SOM is taken differentially at the drains of the switching pair like a normal Gilbert cell.

The cross-coupled pair acts as the differential load for the mixer. Figure 5.18 shows the operation of the SOM when $V_{LO}^+$ is high. The components and nets that are coloured in grey means that part of the circuit has been turned off. The dotted lines show the RF current flows. When the SOM is in full operation, meaning the oscillation has been stabilized, a sinusoidal voltage wave is generated across the LC tank. During the time when Node Plus is positive and Node Minus is negative,
transistors $M_3$, $M_6$, $M_{10}$, and $M_{12}$ are turned on while $M_4$, $M_5$, $M_9$, and $M_{11}$ are off. The RF current from $M_1$ goes through $M_3$ and $M_{10}$ towards Node Minus. On the other hand, the RF current from $M_2$ goes through $M_6$ and $M_{12}$ away from Node Minus. Node Minus acts as a differential ground for the downconverted RF current. Furthermore, at low IF, the symmetrical inductor is a short to $V_{DD}$. Thus, the mixer loads are the cross-coupled transistors.

From Figure 5.18, it becomes clear that flicker noise and noise at the fundamental and harmonics from the downconverted signal are all translated into phase-noise. This SOM, however, has a low-noise mixer, which reduces some of the phase-noise due to the commutated current. Furthermore, care was taken to reduce the mixer
flicker-noise, which also leads to a reduction in phase-noise at low frequency offset.

To find the conversion gain of the mixer, the time-varying load impedance must first be quantified. Figure 5.19 shows the circuit that was used to derive the input impedance of the cross-coupled pair where $\Delta V$ is the voltage difference between the drains to which the LC tank is supposed to connect. Shown in Figure 5.20 (a) is the input impedance of the cross-coupled pair with respect to the LC tank voltage swing. When $\Delta V$ is 0, both transistors are on and the input impedance can be expressed by $1/2g_{mdc}$, where $g_{mdc}$ is the DC transconductance of the cross-coupled pair.

Figure 5.20: Input impedance of the cross-coupled pair: (a) versus LO voltage swing and (b) versus time.
transistor. When $\Delta V$ increases, one transistor starts to shut off while the other’s $g_m$ is increasing. However, the first transistor turns off at a much faster rate, resulting in a rapid increase in impedance. The $g_m$ of the other transistor increases at a much slower rate, resulting in a slow decrease in impedance. The combined result is that the input impedance of the cross-coupled pair increases. The loading effect of the off-transistor quickly diminishes and the input impedance of the cross-coupled pair becomes approximately equal to the input impedance of the on-transistor. It increases to its maximum when $\Delta V$ reaches $\Delta V_1$. The on-transistor is still in saturation in this region and $R_{\text{max}}$ is approximately equal to $1/g_{\text{on}}$, the input impedance of the on-transistor. Beyond this point, the on-transistor goes into the triode region and its input impedance rapidly drops to its on-resistance, $R_{\text{on}}$. The optimum LO swing for maximum load is therefore at $\Delta V_1$. Unlike traditional mixer where a large LO swing is desired, a large LO would adversely affect the conversion gain of this SOM.

Figure 5.20 (b) shows the trapezoidal approximation of the time domain plot of the load impedance with the LO working at the optimum point. The load oscillates at twice the LO frequency with a constant DC value. To simplify the analysis, it is assumed that $C_{gs}$ and $C_{gd}$ have negligible effect and the input impedance is equal to input resistance. The time-varying load resistance can be expressed by a Fourier series. By approximating the plot as a trapezoid, the load can be expressed as

$$R_{\text{load}} = R_{\text{max}} - \frac{2\tau_r}{T_{\text{LO}}} \left( R_{\text{max}} - \frac{1}{2g_{\text{mdc}}} \right) - \frac{4\tau_A}{T_{\text{LO}}} \frac{\sin(\omega_{\text{LO}}\tau) \sin(\omega_{\text{LO}}\tau_r)}{\omega_{\text{LO}}\tau_r} \cos(2\omega_{\text{LO}}t) + \cdots$$ (5.12)

where $T_{\text{LO}}$ is the LO period, $\tau_r$ is the rise time from the minimum to the maximum,
\[ \tau = T_{LO}/2 - \tau_r, \text{ and } A = R_{\text{max}} - 1/2g_{m\text{dc}}. \] The effective transconductance of the inductive degenerated transconductor at \( \omega_{RF} \) is

\[ g_{m\text{eff}} = \frac{1}{L_s\omega_{RF}}. \] (5.13)

Based on Equation (2.14), the conversion gain of the SOM becomes

\[ CG \approx \frac{2}{\pi} \frac{\sin(\pi f_{LO} t_{\text{switch}})}{\pi f_{LO} t_{\text{switch}}} \frac{1}{L_s\omega_{RF}} R_{\text{load}} \] (5.14)

where \( t_{\text{switch}} \) is the time when the switches are all on and it is here to account for the effect of imperfect switching. To maximize gain, \( R_{\text{load}} \) should be maximized. Since it is related to \( g_{m\text{dc}} \), the lower the transconductance, the larger the gain. This is another reason why a low VCO bias current is desired and another important role play by the bleeding-circuit. The validity of Equation (5.12) and (5.14) is confirmed in the simulation section.

### 5.3.4 Output Buffer

Output buffers are required so that the SOM is not significantly loaded by the measurement equipment. The buffer used in this design is a common-source amplifier shown in Figure 5.21. A 4.8 pF capacitor is used as DC block so that the bias point

![Common-source output buffer](image)
of the buffer is not coupled to the drains of the switching pairs. The buffer is biased with 0.6 V gate voltage for best noise performance. The size of the transistor and the load resistor are designed so that the buffer provides a 1 V/V voltage gain and does not significantly affect the $P_{1dB}$ and IIP3 of the SOM core. The final resistor value used is 80 Ω, and it is also used for output matching.

5.4 Simulation Results

The complete schematic of the fully integrated differential low-noise self-oscillating mixer is shown in Figure 5.22. The circuit is optimized for gain, return-loss, and noise figure. It was found that the optimum LO power was -1.1 dBm.

![Complete differential low-noise self-oscillating mixer schematic.](image-url)
The complete chip layout is shown in Figure 5.23. The chip size is 1 mm by 1 mm (1 mm$^2$) including all of the pads, while the core of the circuit including the buffer is only 640 $\mu$m by 730 $\mu$m (0.47 mm$^2$). The gate voltage biases for the switching transistors, buffer, $V_{tune}$ were applied through on-chip 10 k$\Omega$ resistors which act as DC feeds. External bias-T’s are used to bias the low-noise transconductors.

The layout was completed using Cadence Virtuoso. It was then extracted with ASSURA RCX. Both parasitic resistances and capacitances are extracted. Through ADS Dynamic Link, the extracted layout is simulated using standard ADS simulators. Ideal baluns were used in the simulator to generate the differential RF signal and combined the differential IF output into a single-ended signal. Ideal bias-T’s were
used to bias the transconductors.

The simulated $S_{11}$ of the SOM is shown in Figure 5.24 (a). The RF port is very well matched at the desired RF of 8 GHz. To show that there is SNIM, $\Gamma_{opt}$ for optimum noise and $S_{11}$ are plotted in Figure 5.24 (b) with frequency sweeping from 7 GHz to 9 GHz. The frequency at which $S_{11}$ and $\Gamma_{opt}$ intersect is 8 GHz, at which point there is SNIM. For the output IF port, the simulated $S_{22}$ at 300 MHz is $-16$ dB. The input and the output are both matched.

The VCO differential output power is plotted in Figure 5.25 (a) where the power of the fundamental as well as the harmonics are shown. $V_{tune}$ was set to 1.25 V so that the free running oscillation frequency is at 8.3 GHz. The fundamental LO power is $-1.1$ dBm. It can be seen that the harmonic powers are well suppressed, with a difference of 74.3 dB between the fundamental and $2^{nd}$ harmonic and 49.6 dB between the fundamental and the $3^{rd}$. The phase-noise is plotted in Figure 5.25 (b). At a 1 MHz offset, the phase-noise is $-103$ dBC/Hz, which is comparable to $-104$ dBC/Hz from [71] and $-107$ dBC/Hz from [72]. This relatively high phase-noise is because of the
tuning range this SOM has. Figure 5.26 (a) shows the tuning range of the VCO and Figure 5.25 (b) shows the phase-noise at a 1 MHz offset during this tuning range. $V_{\text{tune}}$ is varied from 0.5 V to 2 V, which is the suggested AMOS varactor operating point before there is any breakdown. The LO has a tuning range of 1.4 GHz, which is about

Figure 5.25: Simulated VCO output power and phase-noise at $V_{\text{tune}}=1.25$ V: (a) VCO power in dBm and (b) phase-noise.

Figure 5.26: Simulated frequency tuning range and its associate phase-noise: (a) frequency tuning range and (b) phase-noise at a 1 MHz offset.
Figure 5.27: Simulated $R_{\text{load}}$ and output power: (a) $R_{\text{load}}$ versus time and (b) output power versus input power.

Figure 5.28: Simulated CMRR and isolation: (a) CMRR versus input power and (b) simulated port-to-port isolation with different input power.

16.8%, from 8.1 to 9.5 GHz. Figure 5.26 (b) shows that the phase-noise is proportional to the slope of Figure 5.26 (a), which has been explained in subsection 5.3.1.

The validity of Equation (5.12) and (5.14) is confirmed here. Figure 5.27 (a) shows the simulated $R_{\text{load}}$. Equation (5.12) was used first to find the load value. $R_{\text{max}}$ is
found to be equal to 110 Ω and $1/2g_{mdc}$ is equal to 75.7 Ω. $T_{LO}$ is 120 ps and $\tau_r$ is approximately equal to 15.8 ps. From (5.12), the DC value for $R_{load}$ is 101 Ω. Using Equation (5.14) with $L_s$ equal to 0.343 nH and assuming $t_{switch}$ is insignificantly small, the theoretical voltage conversion gain is then equal to 11.43 dB. The voltage conversion gain was simulated and is equal to 11.6 dB, which is very close to the theoretical gain and therefore validates the equations.

The IF output power for the complete mixer was simulated with the input power level ranging from $-40$ to $-10$ dBm. Plotted in Figure 5.27 (b), the power conversion gain is found to be 12.06 dB. The input referred $P_{1dB}$ is $-16.47$ dBm. The simulated DSB noise figure is 4.06 dB. The common-mode rejection ratio is plotted in Figure 5.28 (a) to demonstrate that the oscillator load is truly balanced. A CMRR of 48.5 dB is obtained, which confirms the balanced nature of the load and the SOM’s ability to reject common-mode noise.

Figure 5.28 (b) shows the port-to-port isolation. High port-to-port isolations are obtained, especially for LO-to-RF isolation where there is more than 73.4 dB isolation.

The complete circuit consumes 17.4 mA of current from a 1.5 V supply. The low-noise SOM core without the buffer consumes only 7.43 mA of current and the output buffers consume a total of 9.97 mA of current.

### 5.5 Measurement Results

Figure 5.29 shows the microphotograph of the SOM chip. The chip was fabricated with IBM’s CMOS 0.13 μm technology. The RF and IF ports are fully differential. Two GSGSG CPW RF probes that have a pitch of 100 μm were used. To generate the differential RF signal from a single-ended signal generator, an external 180° hybrid
was used. Another external $180^\circ$ hybrid was used at the IF port to convert the differential output into a single-ended signal, which was then fed into the spectrum analyzer. Figure 5.30 shows the measurement setup. The chip was tuned for best noise performance by adjusting the bias voltages. The varactor control voltage was also adjusted so that the circuit is oscillating at the desired frequency of 8.3 GHz. They were kept constant throughout the entire measurement.

Due to the large VCO tuning range, the low Q of the LC tank, and power supply
noise, the LO was drifting around 8.3 GHz. To solve this problem, the LO could be stabilized through injection locking [79, 80]. A sinusoidal injection signal at 8.3 GHz could be combined with the RF signal through a combiner and applied to the RF input port. The internal LO would mix with the injected signal and translate it to 16.6 GHz that feeds into the sources of the LC oscillator. The strong second harmonic
of the LO at the sources of the cross-coupled pairs would lock with the 16.6 GHz signal and thereby stabilizing the fundamental. The oscillator can therefore be thought of as a injection-locked frequency divider [81], with the mixer core acting as the tail transistor. However, the large injected signal would affect the linearity of the SOM by forcing it to go into early saturation. Since the LO was stable enough, no injection lock was used in the entire measurement in order to measure the true performance of the SOM.

The input power was swept and the output power at the downconverted frequency of 300 MHz was measured by a spectrum analyzer. Figure 5.31 (a) shows the measured spectrum of the downconverted signal. The spectrum has the shape similar to a free-running oscillator in CMOS. Figure 5.31 (b) shows the measured output power with different input power levels. The input $P_{1dB}$ was $-13.57$ dBm and $OP_{1dB}$ was $-2.97$ dBm. Figure 5.32 (a) shows the measured power conversion gain versus input power and it was 11.6 dB, which agrees well with simulation and theoretical calculation. The $NF_{DSB}$ was measured and it was 4.39 dB with an uncertainty of $\pm 0.26$ dB. This low noise figure is only 0.3 dB higher than simulation.

The differential input reflection coefficient was measured using a vector network analyzer from 7 to 9 GHz. Using Equation (3.24), the differential $S_{11}$ was found. Figure 5.32 (b) shows the measured differential $S_{11}$. At the designed RF input frequency of 8 GHz, the measured $S_{11}$ was $-12.1$ dB.

The tuning range of the oscillator was recorded. The varactor drain/source bias was varied from 0.5 to 2 V and the LO frequency was measured. Since there is no pads for the LO output, one way to measure the LO frequency is from the LO-to-IF feedthrough. The measured frequency range is shown in Figure 5.33 (a). The LO
Due to the limited chip space, no pads were allocated to the oscillator’s LO output, and therefore the LO output power and phase noise, therefore, could not be measured. Nevertheless, judging from the SOM’s performances, the LO power and phase noise frequency varied from 8.083 GHz to 9.7 GHz. Again, there is excellent agreement between the measured and simulated results.
should be quite close to simulation.

Figure 5.33 (b) shows the measured RF-to-IF isolation with respect to the input power and it was found to be 20.8 dB, with little dependence on the input power level. The reason that the feedthrough is higher than simulation can be attributed to a number of factors. A key factor is that a perfect $0^\circ$ and $180^\circ$ signal was injected into the SOM during simulations, whereas this is usually not the case during measurement. Another factor is that parasitics and EM coupling of the interconnects also affects port-to-port isolation.

Since the LO power was not precisely known, the LO leakage power at the IF port was measured instead of LO-to-IF isolation. Figure 5.34 (a) shows the measured output power at the LO frequency at the IF port with respect to input RF power. For small input RF power, the LO power at the IF port is around -44 dBm and it is close to simulation results. This feedthrough is not as significant as the RF-to-IF feedthrough because the LO is internal with a symmetric layout that is not affected by external baluns like the RF port. The LO-to-RF power feedthrough was measured to be $-59.1$ dBm.

To measure the CMRR, the input $180^\circ$ hybrid was replaced by a 3-dB power splitter. The common-mode signal was injected into the RF port and its output IF power was measured. The common-mode gain was calculated and from there, the CMRR was obtained using Equation (3.23). Figure 5.34 (b) shows the measured CMRR with respect to various input power levels. The measured CMRR was 33.6 dB regardless of input power levels, which is expected.

The IIP3 measurement requires some explanation. Although the LO was stable enough to conduct single-tone measurements, it was difficult to measure the IIP3 using
Figure 5.35: Measured linearity response: (a) output spectrum of a 2 tone test with an input power of -25.5 dBm and (b) IF and IM3 outputs.

A closely spaced two-tone input. A two-tone signal with a spacing of 40 MHz was used instead to determine the IIP3. The input RF power was swept and the output IF and

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<td>0.6 µm</td>
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<td>-1 (?)</td>
<td>10.9 (V/V)</td>
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Table 5.1: Comparison of other CMOS SOM with this work.
IM3 powers were measured. Figure 5.35 (a) shows the output spectrum with an input power of $-25.5$ dBm. Figure 5.35 (b) shows the measured IF and IM3 power with respect to input power and the associated IIP3. The extrapolated IIP3 is $-8.3$ dBm and the OIP3 is 3.3 dBm. In order to measure the IIP3 using a two-tone signal with very small spacing, a phase-locked loop (PLL) should be incorporated into the design.

The entire circuit consumes a total current of 21 mA from a 1.5 V supply. The core SOM excluding the buffers consumes only 8 mA from the supply and the core power consumption is 12mW. Table 5.1 compares several other CMOS SOM with this work, which compares favourably in almost all of the parameter metrics and it has exceptional noise performance.

5.6 Conclusion

This chapter introduces a double-balanced low-noise self-oscillating mixer that uses the oscillator as the load. To the author’s knowledge, it is the first of its kind. The mixer core is a merged LNA mixer with the load resistors replaced by an LC oscillator. The current of the oscillator is completely reused by the mixer and the LNA. This SOM is suitable for low power, low cost, and highly integrated circuit applications. A detailed analysis was provided on the oscillator load and the SOM operation. The SOM was designed to work with a 8 GHz input with its internal oscillator running at 8.3 GHz. Experimental results showed the SOM had a great noise performance, with a measured $\text{NF}_{\text{DSB}}$ of 4.4 dB. It had a gain of 11.6 dB and an input $P_{1\text{dB}}$ of $-13.6$ dBm. It had a good input match at the designed frequency and a low LO leakage at the RF port. The measured IIP3 and OIP3 were $-8.3$ dBm and 3.3 dBm respectively. There was excellent agreement between measured and simulated results. The SOM
was compact, only occupying an area of 0.47 mm$^2$. The core power consumption was 12mW. In order to measured the IP3 using a closely spaced two-tone input, a PLL should be used.
Chapter 6

Conclusions

6.1 Summary

Different types of low-noise mixing circuits have been proposed in this thesis. Since mixers can usually be found in the first few blocks of a receiver front-end, they would have a significant impact on the system noise figure if they are not carefully designed. Active mixers exhibit a lot of noise. This imposes strict design requirements on the LNA. By reducing the noise of the active mixer through combining an LNA and mixer into a single-component, highly integrated circuits can be achieved and power consumption can be reduced. Front-end system design is also simplified which leads to easier system integration.

The Gilbert cell mixer has been popular and widely used in IC design but has a high noise figure. Therefore, this thesis targeted at the noise issue of this particular mixer. The dominant source of noise comes from the transconductor. If it is replaced by an LNA, effectively merging the LNA and mixer, then the noise figure of the mixer can be significantly reduced. Three kinds of low-noise mixers had been demonstrated
based on the Gilbert cell structure: narrowband, broadband, and self-oscillating. These circuits demonstrated that low noise figure can be achieved for active mixers that have different purposes.

The narrowband low-noise mixer had an inductively degenerated LNA as its transconductor designed in 0.18 $\mu$m CMOS. Since the mixer had a current reuse structure, a large current would reduce the load resistance and conversion gain. General LNA design technique such as SNIM requires a large current. PCSNIM was thus used in this design. Comparing to the SNIM technique, PCSNIM reduces the power consumption while achieving SNIM at the same time. Together with the current bleeding circuit, the DC current required by the transconductors became independent of the switching pairs and the load resistors. This allowed the mixer to have a high gain even with a low voltage headroom, enabling this mixer topology scalable with technology. The mixer was designed with an RF of 5.4 GHz and an LO of 5.1 GHz. Measurement results showed it had a single-sideband noise figure of 7.8 dB and a conversion gain of 13.1 dB. The measured $S_{11}$ drifted upward in frequency. This shift was caused by the coupling between the inductors, which was not modelled in the simulation. This also caused the noise figure to be higher than simulation.

The broadband mixer had a similar structure, except with a broadband LNA as its transconductor. The broadband LNA was designed with the noise-cancelling technique because it does not require the use of inductors, unlike other broadbanding technique. Expensive chip real-estate can therefore be saved for other uses. This technique requires a large DC current. The current bleeding circuit was used again. The mixer was designed to have a 3 dB bandwidth of 5 GHz, from 1 to 6 GHz. In order to achieve this bandwidth, series inductive peaking was used. The mixer
was designed in 0.13 \( \mu \)m CMOS. It has an constant IF of 250 MHz. Experimental results showed that it had a gain of 17.5 dB with a bandwidth for 4.5 GHz, from 1 to 5.5 GHz. The measured average double-sideband noise figure across the whole band was 3.9 dB.

Finally, the low-noise self-oscillating mixer combined three components into one: LNA, mixer, and oscillator. It was based on the narrowband low-noise mixer structure, but had the load resistor replaced by an LC oscillator. The oscillator generates the required LO while also acting as an IF load. This structure is the first of its kind. The current of the VCO is reused by the mixer and then further reused by the transconductors. The SOM was again designed in 0.13 \( \mu \)m CMOS with an RF of 8 GHz and the oscillator running at 8.3 GHz. Measured results showed that it had a conversion gain of 11.6 dB and a double-sideband noise figure of 4.4 dB. There was a good input match with a \(-12\) dB \( S_{11} \) and a low LO-to-RF power leakage.

### 6.2 Future Work

Several improvements can be applied to each circuit to improve its performance. For the mixer in chapter 3, the inductors can be modelled more accurately by including the coupling effect. The layout can then be optimized. Due to unforeseen circumstances, this step could not be carried out before design submission.

For the broadband mixer, the bandwidth is mainly limited by the transconductor. The shunt peaking can be used in the matching circuit. The adder circuit can be modified. Inductive degeneration can be used to lower the noise contribution of the adder transistors so that their size can be reduced. The amount of current they draw will also be reduced, leading to a reduction in the bleeding circuit, and hence an
increase in bandwidth.

A phase-locked loop should be incorporated into the SOM design to lock the oscillator at precisely 8.3 GHz. The tuning range should be reduced to a few hundred megahertz to improve the free-running phase noise. A capacitor should also be placed at the sources of the cross-coupled pairs to close the loop at the oscillating frequency. This should provide higher stability and reduce the phase noise from the high frequency noise coming from the mixer.

Next, the mixers can all be modified into direct-conversion mixers, where double-sideband noise figure is used to characterize the noise performance. The mixers in this thesis were all for heterodyne receivers. Currently direct-conversion systems are being heavily researched upon because of the ease of system integration. The mixers presented have good input matching and great DSB noise figures, comparable to that of an LNA. The major concern for direct-conversion mixer is flicker noise since flicker noise appears at the output without frequency translation. The low-noise mixers proposed can be adjusted and modified to lower the flicker noise corner. Since the thermal noise has already been suppressed, the modified low-noise mixer with a low flicker noise corner will be very suitable for direct-conversion systems. With its low noise figure comparable to an LNA and good input match, it can replace the front-end LNA and much simplify the system front-end.
References


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REFERENCES


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