A CMOS QPSK Demodulator Frontend for GPON

by

Fei Chen

A thesis submitted to the
Department of Electrical and Computer Engineering
in conformity with the requirements for
the degree of Master of Applied Science

Queen’s University
Kingston, Ontario, Canada
June 2010

Copyright © Fei Chen, 2010
Abstract

This thesis examines the design of a QPSK demodulator frontend for GPON transceiver at end user’s side. Since lowering the cost of the terminal transceivers in an access network like GPON is a key requirement, CMOS technology is used and several area-saving design techniques are applied. The designed frontend circuit saved more than 80% area of the key components including the mixers and the QVCO than some published designs which can also fit the application. A measurement in frequency domain and a simulation in time domain verified that this frontend is able to demodulate a QPSK signal with a data rate as high as 5 Gbit/s.

Two structures of quadrature oscillators are firstly presented and compared. One is an LC QVCO centered at 5 GHz, which contains two spiral inductors and two varactors as resonance tanks. It has a tuning range of 3 GHz, a phase noise of -100.8 dBc/Hz at 1 MHz offset, and an area of 0.15 mm$^2$ excluding pads. On the other hand, the ring QVCO using two active delay stages only takes an area of 0.019 mm$^2$, which is only 13% of that taken by its LC counterpart. But it has a higher phase noise of -81 dBc/Hz at 1 MHz offset.

Then two broadband mixers are described separately. The first one provides a high conversion gain, but its input linearity is insufficient to meet the input power requirement under GPON standard and a system configuration with a 45 dBΩ TIA in front. The second mixer obtains required input linearity but with a trade-off of conversion gain. Both mixers have a broadband input impedance match from 2 GHz
to 8 GHz, and use Gilbert cell to isolate the LO to RF feedthrough to avoid self-
mixing. Current bleeding mechanism is also adopted for both mixers to minimize the
flicker noise as well as boosting the conversion gain. The first mixer has a conversion
gain of 8.5 dB and an input 1 dB compression point at -17 dBm. The second mixer,
which applies resistive source degeneration, has a conversion gain of -7 dB with an
on-chip buffer or -2.1 dB without buffer, but an input 1 dB compression point at -5
dBm. The conversion gain flatness of the second design is also improved by capacitive
peaking.

A frontend circuit is lastly presented. It integrates the compact ring QVCO,
two broadband mixers with high input linearity, and two second-order LC ladder
low pass filters. Frequency domain measurement shows the expected spectrum down
conversion of a 2.5 Gsym/s QPSK signal centered at 5 GHz. The whole frontend
circuit including pads takes 1 mm² area, and consumed 157 mW power. The results
of the time-domain simulation of the frontend are put into Appendix.
Acknowledgments

There are many people I would like to thank for their help and support during the course of my master research. The first person I would like to thank is my supervisor, Dr. Brian Frank for his guidance and encouragement over the past three years. He is always there to provide me with opportunities and trust to improve my research skills and problem-solving ability.

Second, I would like to thank Dr. Al Freundorfer and Dr. Carlos Saavedra for their generous sharing of knowledge and experience. I liked their lectures and enjoyed conversations with them.

I would also like to thank several graduate students in Microelectronics, Electromagnetics and Photonics research group. First, and foremost I would like to thank Ryan Bespalko for his lasting willingness and patience to share his ideas, knowledge and engineering skills. Many enlightening discussions and assistance on circuit design and measurement were also provided by John Carr, Michael O’Farrell, Stanley Ho, Ahmed El-Gabaly, Jiangtao Xu, Shan He, Ying Jiang, and Min Wang.

The integrated circuit fabrication was provided by CMC Microsystems. I would specially like to thank Patricia Greig of the Advanced Photonics Systems Lab. She was always friendly and supportive on any test equipment requests.

Without question, the person who gave me the most crucial support to the completion of my degree was my girlfriend, Yueting. Her understanding and encouragement from the other side of the ocean has been a constant energy source for me to move ahead.
# Table of Contents

Abstract i

Acknowledgments iii

Table of Contents iv

List of Tables vi

List of Figures vii

Nomenclature xi

Chapter 1: Introduction 1
  1.1 Access networks and GPON ................................. 1
  1.2 OSBM modulation scheme ................................ 3
  1.3 An integrated-circuit transceiver proposal .............. 5
  1.4 The work in my research ................................. 6

Chapter 2: Literature Review 9
  2.1 Oscillator Circuits Review .............................. 9
     2.1.1 LC Oscillators .................................... 11
     2.1.2 Ring Oscillators .................................. 17
  2.2 Mixer Circuits Review ................................. 24
     2.2.1 Gilbert-cell based Mixers .......................... 25
     2.2.2 Broadband Mixers ................................. 28
     2.2.3 High-linearity Mixers ............................. 33

Chapter 3: Quadrature LC Oscillator 37
  3.1 Introduction ........................................... 37
  3.2 Circuit Design ......................................... 37
  3.3 Experimental Results .................................. 43
  3.4 Summary .............................................. 48
## List of Tables

3.1 Comparison of symmetric spiral inductors of different geometries . . . 39

4.1 Performance comparison of quadrature VCOs . . . . . . . . . . . . . . 61

6.1 Input Voltage Range to Mixers . . . . . . . . . . . . . . . . . . . . . . 74

6.2 Gain of each stage of the broadband mixer with high input linearity . 81

6.3 Performance comparison of broadband mixers . . . . . . . . . . . . . 91

6.4 Noise calculation of two types of TIA, mixer combination . . . . . . 94
List of Figures

1.1 Passive optical network architecture ........................................... 2
1.2 The spectrum of the OSBM optical signal ..................................... 4
1.3 The spectrum of the electrical signal from the photodiode at the receiver 4
1.4 An integrated solution of OSBM transceiver ................................. 5
1.5 A CMOS OSBM receiver block diagram ....................................... 6
1.6 The block diagram of a QPSK demodulator frontend ...................... 7

2.1 Block diagram of a feedback oscillator circuit ............................... 9
2.2 Cross-coupled LC oscillator ..................................................... 11
2.3 Model of CMOS spiral inductors ............................................... 12
2.4 Feedback analysis of LC Oscillator .......................................... 13
2.5 AMOS varactors ...................................................................... 15
2.6 Complementary cross-coupled LC oscillator ............................... 15
2.7 Block diagram of two coupled oscillators .................................. 16
2.8 Three-stage ring oscillator ....................................................... 18
2.9 Static CMOS inverter .................................................................. 20
2.10 Sources of load capacitance of inverter gate ................................. 21
2.11 Stage propagation delay tuned by weighted sum of fast and slow path 22
2.12 Block diagram of four-stage quadrature output ring oscillator with sub-feedback loops ...................................................... 23
2.13 Block diagram of two-stage quadrature output ring oscillator ....... 23
2.14 Schematics of one delay stage of a two-stage ring oscillator .......... 24
2.15 Another delay stage of a two-stage ring oscillator ....................... 25
2.16 Gilbert-cell mixer ..................................................................... 26
2.17 Current injection into Gilbert-cell mixer ..................................... 27
2.18 CMOS wide-band mixer with LC-ladder impedance matching .... 29
2.19 Common-gate, common-source balun circuit ............................... 29
2.20 Three ways of inductive peaking .............................................. 30
2.21 Source degeneration of a common-source transconductor ........... 32
2.22 Passive mixer of one FET ......................................................... 35
2.23 Double-balanced passive mixer ........................................ 36
2.24 Single-balanced passive mixer ........................................ 36

3.1 Quadrature LC oscillator core circuit ............................... 38
3.2 Photograph of the fabricated CMOS Quadrature LC VCO chip ... 43
3.3 Test setup for LC VCO spectrum, tuning range and phase noise ... 44
3.4 Measured spectrum for 5 GHz quadrature LC VCO ............... 45
3.5 Measured oscillation frequency as a function of tuning voltage ... 46
3.6 Measured phase noise of quadrature LC VCO under injection lock ... 46
3.7 Time-domain measurement setup for the quadrature VCO .......... 47
3.8 Measured output waveforms of Q+ and I− channels of 5 GHz quadrature LC VCO .................................................. 48

4.1 Quadrature ring oscillator with differential outputs, consisting of two delay stages ......................................................... 50
4.2 A delay stage consisting of two amplifiers and two cross-coupled inverters 51
4.3 Circuit schematic of one delay stage for quadrature ring oscillator .... 51
4.4 Whole circuit of ring oscillator with buffers ............................ 53
4.5 Photograph of the fabricated Ring QVCO in a QPSK demodulation frontend .............................................................. 54
4.6 Test setup for Ring VCO’s spectrum, tuning range and phase noise . 55
4.7 Measured spectrum for 5 GHz quadrature Ring VCO ............... 56
4.8 Measured spectrum up to third-order harmonics of Ring VCO .... 56
4.9 Measured oscillation frequency as a function of control voltage for the ring oscillator ......................................................... 57
4.10 Measured phase noise of 5 GHz quadrature Ring VCO ............ 58
4.11 Time-domain measurement setup for the quadrature ring VCO .... 59
4.12 Measured output waveforms of I+ and Q+ channels of 5 GHz quadrature Ring VCO ......................................................... 60

5.1 Common-gate, common-source balun circuit ...................... 63
5.2 Small signal model of Common-Gate Circuit ....................... 64
5.3 Gilbert-cell based mixing stage .......................................... 65
5.4 Schematic of the combiner stage ....................................... 67
5.5 Broadband mixer circuit with three stages ......................... 68
5.6 Photograph of the fabricated CMOS chip of broadband mixer .... 68
5.7 Test setup for mixer’s conversion gain and P1dB .................... 69
5.8 Measured conversion gain as a function of RF signal frequency ... 70
7.1 The block diagram of a QPSK demodulator frontend ............... 96
7.2 A second order LC ladder low-pass filter .......................... 97
7.3 The layout of a QPSK demodulator frontend ....................... 98
7.4 Photograph of the fabricated CMOS QPSK demodulation front end 98
7.5 Demodulation setup to receive QPSK signal ......................... 99
7.6 The spectrum of a 2.5 Gb/s PRBS baseband signal .................. 100
7.7 Spectrum of a generated QPSK signal ............................. 101
7.8 The spectrum of the signal out of in-phase positive (I+) LO port 101
7.9 The spectrum of the demodulated signal in Q channel ............. 102
7.10 The spectrum of the demodulated signal without injection lock . 102

A.1 A block diagram of a four-phase Costas Loop ..................... 116
A.2 Picture of a limiting amplifier PCB ............................... 118
A.3 Picture of a multiplier PCB .................................. 119
A.4 The schematic of a subtractor and a loop filter on a PCB ....... 120
A.5 The PCB assembly of a subtractor and loop filter ................. 120
A.6 A proposal of measurement setup for Costas loop ............... 122
A.7 The generation of a QPSK signal ............................... 123
A.8 The phase error in the Costas loop after a 100 MHz frequency step 124
A.9 The VCO frequency recovery in the Costas loop after a 100 MHz frequency step .................................................. 124
A.10 The eye diagram of I and Q channels of the Costas loop ....... 125
Nomenclature

Latin Symbols

A         Gain of an amplifier [V/V]
B         Noise Bandwidth [Hz]
C         Capacitance [F]
C_{ds}    Drain to Source Capacitance [F]
C_{g}     Gate Capacitance [F]
C_{gd}    Gate to Drain Capacitance [F]
C_{gs}    Gate to Source Capacitance [F]
C_{L}     Load Capacitance [F]
C_{ox}    Unit Capacitance of Oxide [F/m^2]
C_{s}     Capacitance between windings of spiral inductor [F]
C_{w}     Capacitance of wire [F]
d(t)      Baseband data
E(t)      Electrical Field [V/m]
F         Noise Factor
f_{0\rightarrow1}  Frequency of 0 to 1 transitions [Hz]
f_{1\rightarrow0}  Frequency of 1 to 0 transitions [Hz]
f_{3dB}    3dB Bandwidth [Hz]
g_{m}      Transconductance [V/V]
g_{mb}     Back Gate Transconductance [V/V]
H  Transfer Function [V/V]
k  Boltzmann Constant [J/K]
L  Inductance [H]
\( \mathcal{L} \)  Phase noise [dBc/Hz]
m  Coupling Coefficient
NF  Noise Figure [dB]
Q  Quality Factor
q  Charge of an Electron [C]
R  Responsivity [A/W]
R_b  Bit Rate [bps]
R_s  Series Resistance of a Spiral Inductor [Ω]
\( r_{ds} \)  Drain to Source Resistance [Ω]
\( R_s \)  Series Resistance of a Spiral Inductor [Ω]
T  Temperature [K]
T  Symbol Period [s]
\( t_p \)  Propagation Delay [s]
\( V_{DST} \)  Drain-to-Source Saturation Voltage [V]
\( V_d \)  Drain Voltage [V]
\( V_g \)  Gate Voltage [V]
\( V_{g} \)  Gate Voltage [V]
\( V_{p-p} \)  Peak-to-Peak Voltage [V]

**Greek Symbols**

\( \Gamma \)  RMS Value of Impulse Sensitivity Function
\( \phi \)  phase [rad]
\( \tau \)  Time constant [s]
\( \omega \)  Angular Frequency [rad/s]
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>AMOS</td>
<td>Accumulative Mode MOSFET</td>
</tr>
<tr>
<td>AOWG</td>
<td>Arbitrary Optical Waveform Generator</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase-Shift Keying</td>
</tr>
<tr>
<td>CATV</td>
<td>Cable Television</td>
</tr>
<tr>
<td>CDR</td>
<td>Clock and Data Recovery</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DRO</td>
<td>Dielectric Resonator Oscillator</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital Subscriber Line</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>EM</td>
<td>Electro-Magnetic</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>FTTH/P</td>
<td>Fiber To The Home / Premise</td>
</tr>
<tr>
<td>GaAs</td>
<td>Galium Arsenide</td>
</tr>
<tr>
<td>Gbps</td>
<td>Giga bits per second</td>
</tr>
<tr>
<td>GPON</td>
<td>Gigabit-capable Passive Optical Network</td>
</tr>
<tr>
<td>HDTV</td>
<td>High Definition Television</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
</tbody>
</table>
IMOS  Inversion Mode MOSFET
InP  Indium Phosphide
IIP3  Input Third-order Intercept Point
IP3  Third-Order Intercept Point
ISI  Inter Symbol Interference
LA  Limiting Amplifier
LD  Laser Driver
LO  Local Oscillator
LPF  Low Pass Filter
Mbps  Mega bits per second
MIC  Microelectronic Integrated Circuit
MIM-Cap  Metal-Insulator-Metal Capacitor
NMOS  n-type Metal Oxide Semiconductor
NRZ  Non Return to Zero
OLT  Optical Line Termination
ONU  Optical Network Unit
OOK  On-Off Keying
OP-AMP  Operational Amplifier
OSBM  Offset Sideband Modulation
P1dB  1dB Compression Point
PCB  Printed Circuit Board
PIC  Photonic Integrated Circuit
PLL  Phase-Locked Loop
PMOS  p-type Metal Oxide Semiconductor
PON  Passive Optical Network
PPG  Pulse Pattern Generator
PRBS  Pseudorandom Binary Sequence
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase-Shift Keying</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>TIA</td>
<td>Transimpedance Amplifier</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra Wideband</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

The communication of multimedia information, such as high-definition TV (HDTV) or on-line gaming require access networks supporting high-speed (> 100 Mb/s), symmetric, and guaranteed bandwidths [1]. An access network is the part of a communications network which connects subscribers (end users) to their immediate service provider (central office). This chapter will provide a brief review of access network technologies for users at home or in premises.

1.1 Access networks and GPON

Digital Subscriber Line (DSL) was developed early in 1988 to transmit digital data over the telephone twisted-pair copper lines. The bit-rate-times-distance product of that medium is only 10 Mb/s · km [1]. In addition, the upstream data throughput is much lower than the downstream. For example, in standard Asymmetric Digital Subscriber Line (ADSL) [2], the band from 26.000 kHz to 137.825 kHz is used for upstream communication, while 138 kHz to 1104 kHz is used for downstream communication.

Cable Internet was developed in 1990 to provide data transmission over the coaxial copper cable of the cable television (CATV) network. Compared to twisted pairs, the
coaxial cable is a very good broadband medium. It has a bit-rate-times-distance product of 2,000 Mb/s · km. But the upstream data throughput is much lower than the downstream too.

Due to the bandwidth limit and the required electrical-powered equipment between central office and end users in DSL and Cable Internet, research and development on access network using optical fiber like fiber to the home/premises (FTTH/P) started in 1990s. Single-mode optical fiber as a transmission medium provides a bandwidth several order of magnitude higher, i.e. $10^6$ Mb/s · km for a single-wavelength channel. One promising implementation of FTTH/P is called passive optical network (PON). It requires no electrical power supply between central office and end users. A PON consists of an optical line terminal (OLT) at the service provider’s central office and a number of optical network units (ONUs) at the end users’ homes or premises. A typical PON architecture is indicated in Figure 1.1.

![Passive optical network architecture](image)

Figure 1.1: Passive optical network architecture


Unlike the backbone fiber systems, where cost is shared by thousands or millions of users using the same core network, in PON access network, however, end users will
directly bear the cost of PON equipment located in their homes or premises. So the designer of PON transceiver has to be very cost-conscious.

An integrated circuit (IC) GPON transceiver has a potential to provide compact, reliable, and cost-effective solution. But its major challenge is reducing the crosstalk between the transmitted and received signals. A laser driver at transmitter uses a large upstream baseband current to directly modulate a laser; while a photodiode at the receiver produces a slight downstream baseband current. The big upstream current from the laser driver can couple into the small downstream current from the photodiode, leaving an interfered baseband signal for further detection. This crosstalk degrades the receiver’s sensitivity.

1.2 OSBM modulation scheme

The author of [4] proposed an offset sideband modulation (OSBM) scheme, which can be used in downstream data transmission in GPON to reduce the electrical crosstalk between downstream and upstream signals at the end user’s side.

Downstream baseband data to be sent at the central office is used as an input to an arbitrary optical waveform generator (AOWG), which firstly converts the baseband signal to a radio frequency (RF) bandpass signal using quadrature phase-shift keying (QPSK) or quadrature amplitude modulation (QAM), and then uses the RF bandpass signal to modulate the amplitude of a laser carrier. Now the downstream data becomes an optical carrier with an offset modulated sideband. The spectrum of the OSBM optical signal is represented in Figure 1.2.

The electric field of the transmitted optical OSBM signal can be expressed as

\[ E(t) = \left( A_C + A_D d(t)e^{j\omega_{RF} t} \right) e^{j\omega_o t} \]  

(1.1)

where \( A_C \) and \( \omega_o \) are the amplitude and the frequency of the laser carrier, \( A_D \) is the
amplitude of the baseband data $d(t)$, and $\omega_{RF}$ is the offset frequency from the carrier. The data

$$d(t) = \sum_{k=-\infty}^{\infty} d_k p(t - kT)$$

(1.2)

where $d_k$ is the symbol ($\pm 1$ and $\pm j$ for QPSK), $p(t)$ is the pulse shape, and $T$ is the symbol period.

This OSBM optical signal passes through the PON and arrives at an optical detector in an end user’s receiver. A photodiode detector converts the optical input to an electrical current signal as below (assuming a unitary responsivity of the photodiode)

$$i(t) = |E(t)|^2 = |A_C|^2 + |A_D d(t)|^2 + 2A_C A_D d(t) \cos \omega_{RF} t$$

(1.3)

The spectrum of the electrical signal $i(t)$ is shown in Figure 1.3.

Figure 1.2: The spectrum of the OSBM optical signal

Figure 1.3: The spectrum of the electrical signal from the photodiode at the receiver
The bandpass portion centered at $\omega_{RF}$ of the electrical signal contains the downstream data $d(t)$ that we want. The low frequency portion are not of interest and will be filtered out later on.

The electrical signal of upstream baseband data will then not overlap and interfere with the received downstream bandpass signal if the transmitter uses an on-off keying (OOK) modulation. The benefit of such spectrum arrangement is to decrease the crosstalk between the downstream and upstream electrical signals.

1.3 An integrated-circuit transceiver proposal

As mentioned before, compact, reliable, and cost-effective integrated circuit solution is preferred for cost-sensitive GPON transceivers. Among different IC technologies, complementary-metal-oxide-semiconductor (CMOS) technology is a particularly cheap one due to its economies of scale. Therefore, an integrated-circuit solution with as much CMOS technology as possible is an attractive idea for the GPON transceiver.

An integrated-circuit transceiver of two chips was proposed in [5] for GPON using OSBM. It consists of a photonic integrated circuit (PIC), and a microelectronic integrated circuit (MIC) as shown in Figure 1.4. The PIC works as an optical-electrical interface, and MIC is a CMOS chip with a receiver and a laser driver in it.

Figure 1.4: An integrated solution of OSBM transceiver from [5] with permission
The receiver in the MIC shown in Figure 1.5 can consist of a bandpass transimpedance amplifier (TIA), and a direct down-conversion demodulator. The demodulator has a frontend composed of two mixers, a quadrature voltage controlled oscillator (VCO), and two low-pass filters. The frontend together with two following limiting amplifiers, two baseband multipliers, one subtracter, and one loopfilter form a Costas loop to recover the carrier.

![Figure 1.5: A CMOS OSBM receiver block diagram](image)

In the proposal, the baseband data symbol rate is 2.5 GSym/s, and the offset RF frequency is chosen to be 5 GHz for QPSK modulation scheme. This will result in a total data rate of 5 Gb/s. The 5 GHz RF carrier frequency is picked to avoid interference from the 2.5 Gb/s laser driver. It also offers a potential to make clock and data recovery (CDR) easier in that, if the clock of the downstream data and the RF carrier has a fixer phase relationship when OSBM signal is generated, then the clock can be recovered simply by dividing the recovered RF carrier by 2.

### 1.4 The work in my research

My research objective is a demodulator frontend which can be used in the aforementioned OSBM receiver. It consists of two mixers with RF input from 2.5 GHz to 7.5 GHz, a quadrature VCO centered at 5 GHz, and two low-pass filters filtering out the
up-conversion components out of the mixers. The block diagram of my demodulator frontend is shown in Figure 1.6

![Figure 1.6: The block diagram of a QPSK demodulator frontend](image)

Since the GPON application is inherently broadband, the mixer is required to have broadband performance, such as gain flatness and impedance matching over the wide spectrum of bandpass RF signal. Since the transimpedance amplifier proposed in [5] provides a high gain for the sake of noise performance, and GPON standard defines a wide dynamic range, the highest possible output power from the transimpedance amplifier imposes a requirement of high linearity at the input port of the mixers.

Cost effectiveness is a critical design consideration due to the cost-sensitive nature of access network. In CMOS technology, the area of a chip is the most deciding factor of the fabrication cost. Choosing a circuit topology taking up less space is required in my design.

This thesis is organized by chapter. A literature review is first presented in Chapter 2. The concept, design principle, and previous work of CMOS VCO and mixer circuits are briefly discussed.

Chapter 3 and Chapter 4 present two VCO designs. Both provide in-phase and quadrature output carriers, whose tunable frequencies are centered at 5 GHz. The former uses two cross-coupled LC cells, each containing a spiral inductor and a varactor as a resonance tank. The latter uses two delay stages consisting of only active
transistors. The phase noise, frequency tuning range, and the chip area are compared.

Two broadband mixers are discussed in Chapter 5 and Chapter 6, one with a high gain and the other with a high linearity. Broadband input and output impedance matching and gain flatness are considered for both circuits. The tradeoff between gain and linearity is balanced differently for each circuits.

In Chapter 7, a QPSK demodulator frontend is demonstrated. It integrates two broadband and high-linear mixers, one quadrature ring VCO, and two second-order low-pass filters. The measurement shows an expected demodulation function in both time domain and frequency domain.

Finally, a conclusion chapter summarizes the work in this thesis. Suggestions are then given on further research and optimization of the current design.
Chapter 2

Literature Review

2.1 Oscillator Circuits Review

An electric oscillator is a positive feedback system which converts direct current (DC) power to an alternating current (AC) waveform. It is widely used in telecommunication systems as signal source, especially as local oscillation carriers for modulation and demodulation. Some applications, like QPSK demodulation, require a pair of local oscillator (LO) signals that are in quadrature, or 90° out of phase.

Figure 2.1 shows block diagram of a feedback system, which can generally represent electric oscillators.

\[ \text{Figure 2.1: Block diagram of a feedback oscillator circuit} \]

\[ A \] is the gain of the amplifying element and \( F \) is the transfer function of the feedback path, so \( AF \) is the loop gain of the circuit.
CHAPTER 2. LITERATURE REVIEW

The oscillation will start up at a frequency where the loop gain is larger than unity in absolute magnitude, that is,

$$|AF| > 1.$$  \hspace{1cm} (2.1)

And the phase shift around the loop is zero or an integer multiple of $2\pi$, that is,

$$\angle AF = 2\pi n, \quad n \in 0, 1, 2, \cdots.$$  \hspace{1cm} (2.2)

As the oscillation amplitude increases, a mechanism in the amplifying element will reduce the gain, until $|AF| = 1$. This gain decreasing mechanism can result from the amplifier going to class B or C operation or a field effect transistor (FET) entering triode mode from saturation mode. Now the circuit oscillates with a constant output amplitude and fulfills Barkhausen criterion \[6\], which is

$$|AF| = 1$$  \hspace{1cm} (2.3)

$$\angle AF = 2\pi n, \quad n \in 0, 1, 2, \cdots.$$  \hspace{1cm} (2.4)

If exposed to interference from DC voltage ripple, variation of temperature, or noise, the working oscillator will depart from its stable condition defined by Barkhausen criterion. The oscillation amplitude or phase will wander. If the circuit can automatically return back to previous condition, the stable oscillation will be recovered and maintained. So a stable oscillation requires the magnitude of loop gain to increase when the amplitude goes down and vice versa; it also requires the oscillation frequency to increase when interference adds a lag phase and vice versa. The conditions for the oscillator to maintain stable oscillation is
\[
\frac{d |AF|}{d V_{amp}} < 0 \text{ at oscillation amplitude } V_{amp}. \quad (2.5)
\]
\[
\frac{\partial \phi}{\partial f} < 0 \text{ at oscillation frequency } f. \quad (2.6)
\]

where \( \phi \) is the phase of the output waveform.

Barkhausen criterion are widely applied in the design of popular parallel LC tank oscillators [7], Colpitts oscillators [8], crystal oscillators [9], Dielectric Resonator Oscillator (DRO) [10], ring oscillators [11] and others. This thesis will emphasize LC tank oscillators, which are most commonly used in microwave circuits, and ring oscillators, the most silicon area economical ones.

### 2.1.1 LC Oscillators

A commonly used LC oscillator circuit with cross-coupled differential pair is depicted in Figure 2.2.

![Cross-coupled LC oscillator](image_url)

Figure 2.2: Cross-coupled LC oscillator
The resonator of Figure 2.2 consists of a capacitance of $C$ and an effective inductance of $L$. The oscillation frequency will be

$$\omega_0 = \frac{1}{\sqrt{LC}}. \quad (2.7)$$

In CMOS technology, we can easily implement an on-chip LC resonator at microwave frequencies. Spiral inductors are usually fabricated in the top or top two metal layers to minimize the parasitic serial resistance. Figure 2.3 shows an equivalent circuit of spiral inductors.

![Figure 2.3: Model of CMOS spiral inductors](image)

$L_s$ is the low-frequency inductance, $R_s$ is coil’s series resistance, $C_s$ is the capacitance between the windings of the spiral, $C_1$ and $C_2$ are the capacitances between the spiral and the substrate, $C_p$ and $R_p$ together model the substrate’s capacitance and resistance.

The quality factor, $Q$, is used to characterize the loss of a reactance component or a resonant structure. It is defined as

$$Q = \frac{\omega_0}{\text{Energy loss per second}} \quad (2.8)$$

For an inductor working not close to its self resonant frequency, $Q$ can be estimated
as

\[ Q = \frac{\omega_o L_s}{R_s} \quad (2.9) \]

where \( L_s \) and \( R_s \) are inductance and resistance defined in Figure 2.3. The \( Q \) factor in CMOS technology is often under 20 and that low \( Q \) factor limits the oscillator’s performance, such as phase noise.

Let’s analyze the cross-coupled LC VCO in the perspective of feedback system, with the equivalent circuit diagram Figure 2.4, where DC biasing is not shown.

\[ A(j\omega) = A_1(j\omega) \cdot A_2(j\omega) \]

\[ = [A_1(j\omega)]^2 \quad (2.10) \]

\[ A_1(j\omega) = -g_m(R_p||j\omega L/2||1/j\omega 2C) \]

\[ = \frac{-g_m}{\frac{1}{R_p} + j(\omega 2C - \frac{2}{\omega L})} \quad (2.11) \]
\( F(j\omega) = 1 \) \hspace{1cm} (2.12)

Substituting Equations (2.10), (2.11), and (2.12) to Baukhausen criterion Equation (2.3) and (2.4), we get

\[
\omega = \frac{1}{\sqrt{LC}} = \omega_0; \quad (2.13)
\]

\[
g_m = \frac{1}{R_p} \quad (2.14)
\]

\( \omega_o \) is the stable oscillation frequency and \( g_m \) is the averaged transconductance for stable oscillation. According to startup condition, the small signal transconductance must be larger than \( \frac{1}{R_p} \) at the beginning of oscillation.

When the capacitor in the basic cross-coupled LC structure in Figure 2.2 is replaced by a tunable one, a varactor, the basic oscillator becomes voltage controlled oscillator (VCO). An NMOS transistor can be used as a varactor, with source and drain tied as one terminal while the gate is another. The voltage between these two terminals controls the capacitance under the gate. This inversion mode MOSFET (IMOS), can be enhanced by adding an n+ diffusion region underneath the gate oxide to form an accumulation mode MOSFET (AMOS) [12]. AMOS varactors can provide a larger tuning range and higher \( Q \) value. A MOS varactor for differential signal circuit can be realized by two varactors connected in series with a tuning voltage applied between them. Figure 2.5 shows two ways of the arrangement of differential AMOS varactor. In Figure 2.5a, varactor is controlled by a voltage on the gate, while in Figure 2.5b by a voltage on diffusion regions.

Based on the basic cross-coupled, LC oscillator structure, quite a few novel topologies have been developed.

Complementary LC VCO [14] [15], like Figure 2.6, uses the LC tank in between of a PMOS cross-coupled cell and an NMOS cross-coupled cell. The symmetry of the
output wave due to the symmetric circuit topology reduced phase noise by 3dB in a 5 GHz VCO. However, due to three levels of transistors, it is hard to use such topology with a very low power supply.

If two basic cross-coupled LC oscillators are incorporated and coupled, it is possible to generate an in-phase output from one oscillator and one quadrature-phase
output from another. As discussed before, one oscillator can be modeled as a positive-feedback system with amplification $A$ and feedback $F$, where $F = 1$. Then two coupled oscillators can be modeled by following block diagram Figure 2.7, where $m_1$ and $m_2$ are coupling factors.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{oscillatorDiagram.png}
\caption{Block diagram of two coupled oscillators}
\end{figure}

In steady-state, if the two oscillators synchronize to a oscillation frequency $\omega$, the output of each satisfies the following equations:

\begin{align*}
(X + m_2Y)A_1(j\omega) &= X \\
(Y + m_1X)A_2(j\omega) &= Y
\end{align*}

(2.15) 
(2.16)

where coupling coefficients $m_1 = -m_2 = m$ and amplification gain $A_1 = A_2 = A$. Equation 2.15 being divided by Equation 2.16, we get

\begin{align*}
X^2 + Y^2 &= 0 \\
(2.17)
\end{align*}

and therefore,

\begin{align*}
X &= \pm jY.
(2.18)
\end{align*}
CHAPTER 2. LITERATURE REVIEW

The stable oscillation happens at \( X = jY \) [16]. This proves the oscillatory system of Figure 2.7 indeed provides quadrature outputs \( X \) and \( Y \).

Phase noise is a critical parameter of an oscillator, especially for high-speed communication systems. It represents rapid, short-term, random fluctuations in the phase of a wave, caused by time domain instabilities (“jitter”). Hajimiri and Lee [17] have developed a linear time-variance model to explain the phase noise mechanism. They identified noise sources in LC cross-coupled oscillators as: a) parasitic series resistance from inductor; b) thermal and flicker noise from cross-coupled transistors; and c) thermal and flicker noise from tail transistor [15]. The phase noise expression is

\[
\mathcal{L}\{\Delta \omega\} = 10 \log_{10} \left( \frac{i_2 n / \Delta f}{q_{\text{max}}^2} \cdot \frac{\Gamma_{\text{rms}}^2}{2 \Delta \omega^2} \right) \tag{2.19}
\]

where \( \overline{i_n^2} / \Delta f \) is the power spectral density of the overall parallel current noise, \( \Gamma_{\text{rms}} \) is the rms value of the impulse sensitivity function (ISF) associated with that noise source, \( q \) is the maximum signal charge swing, and \( \Delta \omega \) is the offset frequency from the carrier. We can accordingly use this equation as a guideline to reduce the phase noise in our LC-oscillator design, e.g. by increasing the signal charge swing \( q \), and decreasing the ISF.

2.1.2 Ring Oscillators

A ring oscillator consists of a number of gain stages in a loop. Each stage can be an amplifier or a digital inverter. Unlike LC oscillators, ring oscillators have no resonant tank to determine the oscillation frequency. Their working frequency is controlled by the propagation delay of each stage. Stages can be single ended or differential active devices. Therefore, resonatorless ring oscillators are easier to be integrated for system-on-a-chip solutions and consume much less substrate area. Besides, as the ring oscillator is tuned in frequency by a current, its tuning range is wide and
can span orders of magnitude. Ring oscillators are widely used in phase-locked-loops (PLL) for clock and data recovery, frequency synthesis, clock synchronization in microprocessors, and many applications requiring multi-phase sampling.

The total phase shift in a loop, including DC phase shift of $180^\circ$ from each digital inverter or common-source amplifier and frequency-dependent phase shift from each $RC$ network, should be $2n\pi$ (where $n$ is an integer), to fulfill Baukhausen phase criterion. A simple example is a loop of three stages of common-source amplifiers [18] in Figure 2.8.

![Figure 2.8: Three-stage ring oscillator](image)

The total DC phase shift of this loop is $3 \times 180^\circ = 540^\circ$. We need an extra frequency-dependent phase shift of $180^\circ$ from three $R_D C_L$ networks following $M_1$, $M_2$ and $M_3$. Therefore, each $R_D C_L$ should contribute $60^\circ$. The small-signal transfer function of each stage can be approximated as

$$H(j\omega) = -\frac{A_0}{1 + \frac{j\omega}{\omega_o}}, \quad (2.20)$$

where $A_0$ is the DC gain of each stage, and $\omega_o$ is the time constant of each $R_D C_L$ stage. We need phase shift

$$\arctan\frac{\omega}{\omega_o} = 60^\circ, \quad (2.21)$$
which indicates
\[ \omega = \sqrt{3} \omega_0 = \omega_{osc}. \] (2.22)

The magnitude of this loop gain at \( \omega_{osc} \) should be greater than unity to start up oscillation:
\[ \frac{A_0^3}{\sqrt{1 + \left( \frac{\omega_{osc}}{\omega_0} \right)^2}} > 1 \] (2.23)
and hence
\[ A_0 > 2. \] (2.24)

As the oscillation amplitude increases, the amplifiers of each stage can enter triode mode, where nonlinearity limits the maximum amplitude. Like the concept of average \( g_m \) for LC oscillator at stable oscillation amplitude, a stable ring oscillator has an average loop gain of unity. We can use the propagation delay of each stage to derive oscillation frequency of large-signal operation for ring oscillators.

In Figure 2.8, assume an low-to-high transition at point A passes stage \( M_2 \) and converts to a high-to-low transition at point B through a propagation delay of \( t_p \). Similarly, another \( t_p \) is spent for point C to experience a low-to-high transition and so is a third \( t_p \) for point A’s high-to-low transition. Now it takes three \( t_p \) for a half cycle. Then the period of a full cycle will be \( 6t_p \) and, therefore, the oscillation frequency is \( \frac{1}{6t_p} \). Extending this result to a general ring oscillator of \( n \) stages, we know the large-signal operating frequency will be
\[ f_{osc} = \frac{1}{2nt_p} \] (2.25)

Digital inverters can be used as delay stages as well. The analysis principle is similar to foregoing common-source-amplifier stages. The key factor to control the oscillation frequency is, again, the propagation delay of each inverter stage.
A basic single-end, static CMOS inverter is shown in Figure 2.9a, where $C_L$ is the overall output capacitance of the gate. When oscillating, its $V_{in}$ transits from high to low and then low to high periodically, while $V_{out}$ transits in the same frequency but in opposite direction with a propagation delay. If $V_{in}$ switches from low to high instantaneously, we can use a simplified model in Figure 2.9b to explain propagation delay at $V_{out}$, where $R_n$ is the on-resistance of the NMOS transistor. So can Figure 2.9c for $V_{in}$ switching from high to low, where $R_p$ is the on-resistance of PMOS transistor.

![Figure 2.9: Static CMOS inverter: (a) Schematics; (b) Switch model for high to low transition; (c) Switch model for low to high transition.](image)

For a high-to-low transition at $V_{out}$, $R_n$ discharges $C_L$ like Figure 2.9b. The propagation delay is proportional to the time constant of the $R_nC_L$ network, $\tau_{HL} = R_nC_L$. Similar considerations are valid for low-to-high transition (Figure 2.9c), whose propagation delay is proportional to $\tau_{LH} = R_pC_L$. We can roughly estimate the propagation delay as $0.69\tau$ [19]. According to Equation (2.26) and assuming $R_n = R_p = R$, the oscillation frequency of inverter ring is

$$f_{osc} = \frac{1}{2nt_p} = \frac{1}{2n \times 0.69\tau} = \frac{0.72}{nRC_L} \quad (2.26)$$

High oscillation frequency requires small load capacitance $C_L$, small on-resistance $R$ and as less stages as possible. Let’s first look at the sources of $C_L$ from Figure 2.10.
Figure 2.10: Sources of load capacitance of inverter gate

The overall load capacitance $C_L$ of one inverter stage is a combination of drain-body junction capacitance ($C_{db} = C_{db1} + C_{db2}$) from its own stage, gate capacitance ($C_g = C_{g3} + C_{g4}$) from its fan-out stage(s), Miller capacitance converted from its own $C_{gd}$ to a capacitance between drain and ground with a value of $2C_{gd}$ [19], and interconnect wiring capacitance ($C_w$). For ring oscillators in most sub-micron CMOS technologies, $C_{db}$ and $C_g$ are major contributors for total $C_L$. Since both $C_{db}$ and $C_g$ are proportional to the widths of PMOS and NMOS transistors, keeping transistors small helps increase the oscillation frequency.

Small on-resistance of transistors can result from higher supply voltage $V_{DD}$ or wider transistor. However, the former method increases the power dissipation quadratically, since the dominant power dissipation comes from the dynamic power to charge and discharge load capacitances. Its equation is $P_{dyn} = C_L V_{DD}^2 f_{0\rightarrow1}$, where $f_{0\rightarrow1}$ is the frequency of $0\rightarrow1$ transitions. The latter method will increase the parasitic capacitances $C_{db}$ and $C_g$, contradicting the requirement of small load capacitance $C_L$.

In sum, using advanced technology with less minimum feature size, keeping parasitic capacitance small (less transistor width and shorter interconnection wiring), employing less number of stages and increasing supply voltage are ways to get higher oscillation frequency; while the trade off can be more power consumption.

In [20], a three-stage ring oscillator, with each stage as common-source differential
amplifier, worked at 5 GHz. It was implemented in 0.18 µm CMOS technology. Differential stages have the benefit of reduced sensitivity to power supply fluctuation and substrate noise, which are two major sources of jitter in high frequency oscillators. Each delay stage was actually a weighted combination of fast-propagation path and slow-propagation path. The weight assigned to each path can be tuned to control the effective delay of one stage and then control the oscillation frequency of the whole loop. This controlling idea is shown in Figure 2.11.

![Figure 2.11: Stage propagation delay tuned by weighted sum of fast and slow path from [20] with permission ©2001 IEEE](image)

A multiphase output ring oscillator can be achieved by \(\frac{360°}{\text{phase shift}}\) stages. For example in [21], four stages generated quadrature outputs. Each stage can be single-ended or differential common-source amplifier. To improve the speed limited by the long chain of four stages, the author added sub-feedback loops of only three stages per loop to increase the oscillation frequency. Figure 2.12 shows how the sub-feedback loops are constructed on the main loop. Since the effective loop delay is a weighted sum of four-stage main-loop delay and three-stage sub-feedback delay, the oscillation frequency can be tuned from \(1/(2 \times 4\tau_p)\) to \(1/(2 \times 3\tau_p)\), where \(\tau_p\) is the delay of one stage. This circuit operated from 400 MHz to 2 GHz in a 0.5 µm CMOS process.

Similar to the above design is a four-stage ring oscillator based on digital inverters to generate quadrature outputs [22]. The author used an advanced dual inverter with latch transistors to reinforce the transition and feed-forward mechanism to synchronize the latch with the inverter. It reached 1.59 GHz oscillation frequency in 0.18 µm
CHAPTER 2. LITERATURE REVIEW

Figure 2.12: Block diagram of four-stage quadrature output ring oscillator with sub-feedback loops, from [21] with permission ©1999 IEEE

CMOS technology.

Two-stage inverter-based ring VCO can also generate quadrature outputs. Each stage must be differential inputs and outputs and the outputs of the second stage must connect to the inputs of the first stage with reverse polarity as shown in Figure 2.13. This interconnection provides 180° phase shift at DC. Each stage provides another 90° frequency-dependent phase shift by the $RC$ network at the stage output node.

Figure 2.13: Block diagram of two-stage quadrature output ring oscillator

A two-stage differentially controlled ring VCO was developed to work at 0.97 GHz central frequency in 0.35 $\mu$m CMOS process [11]. It rejected common-mode interference on the control inputs by 32 dB. This idea of common-mode rejection is analogous to the differentially controlled LC VCO discussed in previous section from [23]. As the schematics of one delay stage shown in Figure 2.14, a latch consisting of two cross-coupled inverters is inserted into each delay stage as a positive feedback to achieve faster switching speed, which helps lower the phase noise. Its measured phase noise was -117 dBc/Hz at 1 MHz offset frequency.

Another two-stage ring VCO designed in 0.18 $\mu$m CMOS process reached 900 MHz
central frequency and phase noise of -106.1 dBc/Hz at 600 KHz offset frequency [24]. Its schematic of one delay stage is shown in Figure 2.15. Unlike feeding the inputs to inverters in each delay stage as the above two-stage ring VCO, this design feeds the inputs to the NMOS FETs only but uses the PMOS FETs to control the amount of current through NMOS to tune the oscillation frequency. A latch consisting of two cross-coupled inverters are inserted in each delay stage as well to lower the phase noise.

2.2 Mixer Circuits Review

An ideal mixer can be considered as a signal multiplier, which produces an output signal equal to the product of the two input signals. Mixers are often used together with an local oscillator (LO) to do up-conversion, which convert the baseband or intermediate frequency (IF) signal to radio frequency (RF), or down-conversion, which convert RF signal to IF in superheterodyne receiver or to baseband in one step in a direct-conversion receiver (homodyne receiver).

The multiplication can be realized by nonlinear effects from a diode or a transistor, where the current-vs-voltage relationship contains a quadratic term, or by
time-varying effect from a Gilbert-cell multiplier, where LO signal switches on and off the paths of RF signal. Diode-based mixers which use the non-linear effect are usually applied to very high frequency and their intermodulation products and harmonics are stronger than FET-based mixers. Besides, most nonlinear mixers exhibit conversion loss rather than gain. This thesis will focuses on CMOS FET mixers only.

2.2.1 Gilbert-cell based Mixers

The Gilbert-cell has been the most widely used structure for mixers in the analog field since 1968 [25]. It has high gain and high isolation between its ports. Figure 2.16 shows the circuit of a Gilbert cell.

The differential RF signal is applied to the gates of the bottom transistors, $M_1$ and $M_2$. These two transistors perform a voltage to current conversion, and therefore are called the transconductance stage or transconductor. The differential LO signal is applied to the upper transistors from $M_3$ to $M_6$. The upper two pairs of transistors act as current switches, which realize the multiplication function in current domain.
The multiplied current converts back to voltage through the drain resistors, $R_d$. The output signal is taken differentially between $v_{IF+}$ and $v_{IF-}$.

Based on Gilbert-cell, a variety of novel structures have been developed. The current-injection technique [26] is one of them. It can increase conversion gain and decrease 1/f noise. Its circuit is shown in Figure 2.17.

The injected current $I_x/2$ can increase the transconductance, $g_m$, of $M_1$ and $M_2$. This in turn increases the conversion gain. Current injection has another name, current bleeding. Because the current branch $I_x/2$ on each side splits transconductor’s bias current, which is $I_{SS}/2 + I_x/2$. This split makes the current through load resistor less than through the transconductor. The voltage drop across the load resistor has an upper limit to guarantee enough headrooms for $M_3$ to $M_6$ to stay in saturation mode. This DC voltage drop across the load is $V_L = I_L R_L$, where $I_L$ is the quiescent current in $R_L$. Smaller load current due to the current bleeding allows larger $R_L$ to
keep same voltage drop $V_L$. Since voltage conversion gain is $2g_m R_L/\pi$ [27], where $R_L$ is the load resistance and $g_m$ is the transconductance of the transconductors, the larger $R_L$ increases conversion gain.

Current injection also helps lower mixer’s $1/f$ noise. First, let’s look at the sources of flicker noise in Gilbert cell. The possible sources can be the output stage (the load), the RF input stage (the transconductor), or the LO switching pair stage [28]. The output stage realized by polysilicon resistors generates no flicker noise. The flicker noise in the RF input stage does not appear, to the first order, at the IF frequency or baseband range at output after frequency down conversion. Therefore, the flicker-noise performances of the mixer are primarily determined by LO switching pair devices. Since flicker noise is proportional to bias current of MOSFET [29], the reduced bias current in LO switching transistors due to current bleeding decreases LO’s and then whole mixer’s flicker noise.
2.2.2 Broadband Mixers

A broadband mixer requires input impedance matching and gain flatness along the interested frequency band, usually at least several GHz.

The input impedance at RF port of Gilbert cell is very high due to the large capacitive component of the gate of a FET. A low input reflection coefficient is desired to transfer the power to circuit and to facilitate the measurement. A wideband CMOS Gilbert-cell mixer was presented in [30], operating from 0.3 GHz to 25 GHz. LC ladder matching networks were used for input impedance matching for such a wide bandwidth. Shown in Figure 2.18, the LC ladder is actually a band-pass filter with one terminal matching characteristic impedance and the other terminal loading gate capacitance of MOSFET. However, using on-chip inductors for matching network is significantly chip-area consuming. Those four inductors consumed about four times the area than all the other active components.

Impedance matching using active components, which consumes much less area, is attractive and possible for frequency up to 10 GHz. A common-gate stage is used for broadband matching in [31]. The input impedance of a common-gate amplifier is inversely proportional to the transconductance $g_m$ of the common-gate stage. When transistor size and bias condition is properly selected, the input impedance can be close to 50 $\Omega$. Another benefit of common-gate active matching is that it can cooperate with a common-source stage to form an active balun, as shown in Figure 2.19. Such balun can be useful to convert an unbalanced RF signal to a balanced signal to feed transconductor stage in Gilbert-cell mixer.

The gain of a mixer’s transconductor and conversion gain of the whole mixer are rolling off as frequency goes up. The reason is that parasitic capacitances combine with the load resistance and transistor’s channel resistance to form RC networks at the input, intermediate and output stages. Each RC network generates a pole for the overall transfer function. Usually, the pole from the output RC network dominates.
Figure 2.18: CMOS wide-band mixer with LC-ladder impedance matching from [30] with permission ©2004 IEEE

Figure 2.19: Common-gate, common-source balun circuit
To push the output pole further away in the frequency axis, one option is to add inductor either in series or in parallel at the output. The formed LC resonance network can reduce the effective capacitance value, which in turn move the dominant pole further away. This method is called inductive peaking [32]. Based on where the additional inductor is placed, inductive peaking has three variations: shunt peaking, series peaking and shunt-series peaking. These different peaking ways are illustrated in Figure 2.20.

For shunt peaking in Figure 2.20a, the capacitive load $C_L$ has a decreasing impedance as frequency increases. The added inductor $L_1$, which is in shunt with the load capacitor, provides an impedance with an increasing magnitude as frequency goes up. This
increasing impedance offsets the decreasing impedance of the load capacitance, leaving a net impedance that remains roughly constant over a broader frequency range.

The transfer function from input current to output voltage is

\[
H(s) = (sL + R) \frac{1}{sC} = \frac{R(sL/R + 1)}{s^2LC + sRC + 1} \tag{2.27}
\]

then

\[
|H(j\omega)| = R \sqrt{\frac{(\omega L/R)^2 + 1}{(1 - \omega^2LC)^2 + (\omega RC)^2}} \tag{2.28}
\]

The term in the numerator \((\omega L/R)^2\) increases with increasing frequency. Furthermore, the \((1 - \omega^2LC)^2\) term in the denominator decreases with increasing frequency to have an effect to increase \(|H|\) as well for frequencies below the \(LC\) resonance.

For series peaking in Figure 2.20b, the transfer function is

\[
H(s) = \frac{R}{R + sL + 1/sC} \cdot \frac{1}{sC} = \frac{R}{s^2LC + sRC + 1} \tag{2.29}
\]

then

\[
|H(j\omega)| = \frac{R}{\sqrt{\omega^4L^2C^2 - 2\omega^2LC + \omega^2R^2C^2 + 1}} \tag{2.30}
\]

The term \(\omega^4L^2C^2 - 2\omega^2LC\) in the denominator has derivative as \(4\omega^3L^2C^2 - 4\omega LC\). This derivative will be negative when frequencies are below the \(LC\) resonance. So the term \(\omega^4L^2C^2 - 2\omega^2LC\) decreases with increasing frequency and then, the \(|H|\) increases with increasing frequency as long as the frequency is below the \(LC\) resonance.

The shunt-series peaking in Figure 2.20c is a combination of shunt and series peaking. This structure further extends the bandwidth of mixer.

But the inductive peaking uses on-chip inductors, which consume a lot of area. A cost-saving solution can be capacitive peaking, because an on-chip MIM capacitor takes much less area than an on-chip spiral inductor.

The extrinsic transconductance of resistor-degenerated transconductor as shown
Figure 2.21: Source degeneration of a common-source transconductor: (a) Source degeneration by a resistor; (b) Source degeneration by a parallel of resistor and capacitor.

in Figure 2.21a is [6]

\[ g_{me} = g_m \cdot \frac{1}{1 + R_s g_m} \]  

(2.31)

If a capacitor is paralleled with that degenerating resistor, as shown in Figure 2.21b, the degeneration impedance of the parallel RC becomes \( Z_s = \frac{R}{1 + j\omega RC} \), whose amplitude decreases as frequency goes up. The extrinsic transconductance of the capacitive peaked transconductor is [33]

\[ g_{me} = g_m \cdot \frac{1}{1 + Z_s g_m} = g_m \cdot \frac{1 + j\omega RC}{1 + j\omega RC + Rg_m} \]  

(2.32)

Then,

\[ |g_{me}| = g_m \sqrt{\frac{1 + \omega^2 R^2 C^2}{(1 + Rg_m)^2 + \omega^2 R^2 C^2}} \]

\[ = g_m \sqrt{1 - \frac{R^2 g_m^2 + 2Rg_m}{(1 + Rg_m)^2 + \omega^2 R^2 C^2}} \]  

(2.33)

When frequency \( \omega \) increases, the magnitude of extrinsic transconductance \( |g_{me}| \),
increases. Therefore, the conversion gain of mixer will increase with increasing frequency. In [34], such capacitive peaking is used for broadband mixer and saved a great amount of chip area comparing to the inductive-peaking counterpart.

### 2.2.3 High-linearity Mixers

The non-linearity of a Gilbert cell mainly comes from the non-linear voltage-to-current transfer function of the transconductor. In long-channel CMOS model, the transconductance is proportional to the amplitude of the RF input signal. When a degeneration resistor $R_s$ is inserted in the source of a transconductor, according to Equation (2.31), the transconductance will be approximately $1/R_s$ as long as the loop gain, $R_s g_m$, is sufficiently large. An inductor can replace the degeneration resistor to improve the linearity of the mixer as well. Inductive degeneration is preferable from a noise standpoint, since ideally, it does not contribute any noise to the system. However, using an on-chip degeneration inductor consumes much more chip area than a resistor, and thus will increase the cost of the chip.

Biasing the transconductor in the triode region can also increase the linearity of transconductance, either for long-channel CMOS devices or short-channel ones. For long channel devices, in saturation mode, the drain current has a squared dependence on the gate-source voltage $v_{GS}$ as shown in Equation (2.34). But in triode mode, the drain current is linearly dependent on $v_{GS}$ (Equation (2.35)).

\begin{align}
  i_D &= \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2 \quad \text{(Saturation)} \\
  i_D &= k'_n \frac{W}{L} (v_{GS} - V_t - \frac{v_{DS}}{2}) v_{DS} \quad \text{(Triode)}
\end{align}

where $k'_n$ is the process transconductance parameter and $\frac{W}{L}$ is the device’s aspect ratio.

The mixer in [35], designed with triode-biased CMOS transconductor of gate
length of 0.7 \mu m, reached 1 dB compression point \( P_{-1dB} \) at -2 dBm and conversion gain at 10 dB.

For short-channel devices, a triode-biased transconductor has higher linearity than when it is biased in saturation mode as well. Let’s compare current-voltage relationships for saturation region in Equation (2.36) and for triode region in Equation (2.37),

\[
\begin{align*}
    i_{DSAT} &= \kappa(V_{DSAT}) k_n' \frac{W}{L} (v_{GS} - V_t - \frac{V_{DSAT}}{2}) V_{DSAT} \quad \text{(Saturation)} \\
    i_D &= \kappa(v_{DS}) k_n' \frac{W}{L} (v_{GS} - V_t - \frac{v_{DS}}{2}) v_{DS} \quad \text{(Triode)}
\end{align*}
\]

where \( \kappa(V) = \frac{1}{1 + (V/\xi c L)} \), \( \xi_c \) is a process constant, \( V_{DSAT} \) is the drain-to-source voltage at which the transistor begins to saturate [19]. Although linear relationships exist for both cases, the triode mode offers lower transconductance than saturation mode because \( v_{DS} \) in triode mode is smaller than \( V_{DSAT} \). Usually, lower transconductance gain trades off higher linearity.

Using a bias offset technique on the transconductor helped to increase \( P_{-1dB} \) to -5.5 dBm with 3 dB voltage conversion gain in 0.18 \mu m CMOS process [36]. But the complexity of the RF stage also increased at least triply.

In [37] and [38], the author used a multiple-gated transconductor to minimize the third order intermodulation distortion. By shunting a secondary sub-threshold transistor to the main transconductor and adding a resonator for harmonic tuning, that mixer increased input third-order intercept point (IIP3) by 7 dB. But this method is for narrow band applications.

Another way to increase mixer’s linearity is to use a passive mixer rather than an active Gilber-cell mixer. Passive mixers are now widely used in ultra-wideband (UWB) applications [39]. They usually provide high linearity but with an conversion loss in stead of an conversion gain expected from active mixers. Since the DC current through the FET is zero, passive mixers have very little 1/f noise. A single-balanced
The LO signal feeds the gate of FET, which is biased at the threshold voltage. When the LO signal is positive, the FET goes to triode region, acting as a resistor and the RF voltage (at drain in this figure or at source in some other applications) is transferred to the IF port (at source in this figure). When the LO signal is negative, the FET is in cut-off region, acting as an open circuit between RF and LO ports. So the FET works as a voltage switch controlled by the LO signal. This switching realizes the multiplying function. To alleviate the LO feedthrough problem in one FET structure, a double-balanced structure can be used. As shown in Figure 2.23, a double-balanced passive mixer in 0.35 \textmu m BiCMOS process achieved +7 dBm 1dB compression point and 16.5 dBm IIP3 [40]. With the LO signal at 7dBm, that mixer had a 6.5 dB conversion loss. It had single side band noise of 7 dB and a 1/f noise corner less than 10 kHz.

Unlike the current-mode mixing in Gilbert cells, passive mixers work in voltage-mode. A single-balanced passive mixer actually provides the same conversion gain as half of a double-balanced structure if other conditions are same. But the double-balanced structure uses a differential RF input of double amplitude of each half side. Therefore, a single-balanced passive mixer has 6 dB higher conversion gain than that
Figure 2.23: Double-balanced passive mixer from [40] with permission ©2003 IEEE of a double-balanced mixer. In [41], the author developed a single-balanced mixer with conversion gain of 3 dB and IIP3 of 5 dBm in 0.18 μm CMOS process. It had a 1/f noise corner at 45 kHz. The simplified schematic is shown in Figure 2.24

Figure 2.24: Single-balanced passive mixer from [41] with permission ©2005 IEEE

Some feedforward [42], feedback [27] [43], or predistortion [44] sub-systems can be used to compensate the non-linearity of conventional mixers. But these sub-systems are relatively complex and need a lot of space and power consumption.
Chapter 3

Quadrature LC Oscillator

3.1 Introduction

A stable and low-phase-noise quadrature local oscillation (LO) source is a key component in QPSK demodulation. It feeds two mixers in a receiver to do the down conversion. LC-oscillator structures are commonly used for monolithic microwave circuit design, and are believed to have less phase noise than ring oscillators [45].

The introductory chapter discussed the basic LC-oscillator for differential output. Two basic cross-coupled LC oscillators can be incorporated and coupled to generate in-phase output from one oscillator and quadrature-phase output from another.

This chapter describes a 5 GHz quadrature LC VCO with tunable phase difference. The circuit topology and measurement results are presented.

3.2 Circuit Design

A quadrature-phase oscillation output can be generated either by adding a 90° phase shifter to a basic oscillator or by adding another oscillator while coupling it with the original one. Usually an on-chip phase shifter is designed for just one specific frequency, not wide band. So it is hard to guarantee the accuracy of phase relationship
in a whole tunable frequency range. In contrast, coupled two VCOs can always maintain a good in-phase and quadrature-phase relationship in the tunable range.

The second method was selected for this design. The circuit consists of two identical cross-coupled LC VCOs as its topology shown in Figure 3.1.

![Figure 3.1: Quadrature LC oscillator core circuit](image)

$T_{cpl,1}$ to $T_{cpl,4}$ are four coupling transistors. They force 90° phase difference among the four outputs. $T_1$ and $T_2$ are cross-coupled transistors biased by $T_{tail,1}$. They provide a negative resistance for the basic oscillator on the left. As introduced in Section 2.1.1, to start up an oscillation, the small-signal transconductance of $T_1$ and $T_2$ should be larger than the reciprocal of the inductor’s parallel equivalent resistance.

The spiral inductor $L$ was first to be determined, because its inductance and $Q$ value are the preconditions for further selection of tank varactor and cross-coupled transistors. Higher inductance and higher $Q$ value are preferred [15], because they increase inductor’s parallel-equivalent resistance $R_p$ and then the oscillation amplitude
CHAPTER 3. QUADRATURE LC OSCILLATOR

$V_{amp}$ according to Equations (3.1) and (3.2).

$$R_p = \frac{\omega L(Q^2 + 1)}{Q} \approx \omega LQ$$  \hspace{1cm} (3.1)

$$V_{amp} = I_{bias}R_p \approx I_{bias}\omega LQ$$  \hspace{1cm} (3.2)

This in turn improves the phase noise performance. The expression of phase noise in Equation (3.3)

$$\mathcal{L}\{\Delta \omega\} = 10 \log_{10} \left( \frac{\overline{i_n^2}/\Delta f}{q_{max}} \cdot \frac{\Gamma_{rms}^2}{2\Delta \omega^2} \right)$$  \hspace{1cm} (3.3)

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the overall parallel current noise, $\Gamma_{rms}$ is the rms value of the impulse sensitivity function (ISF) associated with that noise source, $q$ is the maximum signal charge swing, and $\Delta \omega$ is the offset frequency from the carrier, indicates that a larger oscillation amplitude corresponds to a larger $q$, and then a less phase noise.

A comparison of several symmetric spiral inductors of different geometric parameters on their $Q$ values, peak $Q$ frequencies, and inductances was made in Table 3.1.

Table 3.1: Comparison of symmetric spiral inductors of different geometries

<table>
<thead>
<tr>
<th>No.</th>
<th>Outer diameter (µm)</th>
<th>Number of turns</th>
<th>Turn width (µm)</th>
<th>Turn spacing (µm)</th>
<th>Peak $Q$</th>
<th>Peak $Q$ frequency (GHz)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>1</td>
<td>5</td>
<td>-</td>
<td>18.7</td>
<td>14.7</td>
<td>0.21</td>
</tr>
<tr>
<td>2</td>
<td>200</td>
<td>1</td>
<td>5</td>
<td>5</td>
<td>17.1</td>
<td>7.2</td>
<td>0.51</td>
</tr>
<tr>
<td>3</td>
<td>200</td>
<td>2</td>
<td>5</td>
<td>5</td>
<td>19.2</td>
<td>4.5</td>
<td>1.44</td>
</tr>
<tr>
<td>4</td>
<td>200</td>
<td>3</td>
<td>5</td>
<td>5</td>
<td>17.3</td>
<td>3.3</td>
<td>2.55</td>
</tr>
<tr>
<td>5</td>
<td>200</td>
<td>3</td>
<td>10</td>
<td>5</td>
<td>18.4</td>
<td>3.1</td>
<td>1.87</td>
</tr>
<tr>
<td>6</td>
<td>140</td>
<td>3</td>
<td>8.5</td>
<td>5</td>
<td>16.8</td>
<td>5</td>
<td>1.1</td>
</tr>
</tbody>
</table>

The inductors from No. 1 to No. 5 are measured reference designs from IBM’s model reference guide [46]. The inductor No.1 with an outer diameter of 100 µm has the smallest area, but its inductance is too low and its peak $Q$ frequency is far away
from my application, which requires a peak Q at 5 GHz. When the size of an inductor is increased, its inductance will increase as the trend indicated by inductors No. 2 to No. 5. But the inductors with an outer diameter of 200 µm have a relatively low peak Q frequency, and their sizes are not small. To get an inductor of needed peak Q frequency at 5 GHz, and make a balance between its Q value and its area, an spiral inductor of size 140 µm × 140 µm with 3 turns, and 8.5 µm turn width was chosen (No. 6). It is virtually a trade off between the inductors No. 1 and No. 5. It has an inductance $L$ of 1.1 nH and a peak Q of 16.8 at 5 GHz.

Since oscillation frequency $\omega = \frac{1}{\sqrt{LC}}$, a total capacitance of 0.9 pF is needed for an oscillation frequency at 5 GHz. Due to the parasitic capacitance from active devices and transmission lines, the midpoint capacitance of the needed varactor is actually less than 0.9 pF. For each basic oscillator to be coupled, a diffusion-tuned accumulation mode varactor (AMOS) was selected since it can provide larger tuning range and higher Q value in comparison with an inversion mode varactor (IMOS) as discussed in Section 2.1.1. One varactor is composed of two serially connected sub-varactors whose diffusion areas are connected while their gates are to provide differential signal outputs. One sub-varactor is constituted of 49 pieces of 2 µm x 2 µm diffusion region. The varactor as a whole has a tunable capacitance $C$ from 0.3 pF to 1.1 pF.

The parasitic resistive elements in the varactor and interconnecting wires have power dissipation, which further decreases the parallel resistance $R_p$ in the LC tank. This degradation of Q has to be considered when using $g_m = \frac{1}{R_p}$ to calculate the minimal transconductance $g_m$ of cross-coupled transistors.

The $R_p$ from the spiral inductor is

$$R_p = Q \omega L = 16.8 \times 5 \times 10^9 \times 2\pi \times 1.1 \times 10^{-9} = 581(\Omega)$$

(3.4)

A simulation of the chosen varactor showed a 400 Ω parallel parasitic resistance.
So it is reasonable to assume that the parallel parasitic resistance from the varactor and wires is of similar amount to that from the spiral inductor. Then the overall tank parallel resistance will be $R_{p,tank} = 290 \ \Omega$. Thus the minimal $g_m$ to provide negative resistance is

$$g_m = \frac{1}{R_{p,tank}} = \frac{1}{290} = 3.5 \text{ (mS)} \tag{3.5}$$

This $g_m$ should be considered as an averaged value in a stable oscillation, and should not simply be equal to the transconductance of a saturated FET because the cross-coupled transistors are only part-time working in saturation region. The FET’s minimal transconductance under saturation, $g_{m,\text{sat}}$, is estimated to be twice of the averaged $g_m$. So $g_{m,\text{sat}} = 7 \text{ mS}$.

The sizes and bias current of cross-coupled transistors can be selected to provide a transconductance at least 7 mS. In my design, the cross-coupled transistors $T_1$ to $T_4$ are 26-finger transistors with 2 $\mu$m width per finger. These transistors are biased by tail transistors, $T_{\text{tail,1}}$ and $T_{\text{tail,2}}$. An extra transconductance should be provided as buffer to make sure the oscillation and to lower the phase noise. The bias current is 6 mA per FET to provide a transconductance twice as the least needed. The design provides a saturation transconductance

$$g_{m,\text{sat}}' = \sqrt{2k_n' \frac{W}{L} I_D}$$

$$= \sqrt{2 \times 286 \times 10^{-6} \times 43 \times 6 \times 10^{-3}} \tag{3.6}$$

$$= 14 \text{ mS} > g_{m,\text{sat}}$$

where $k_n'$ is the process transconductance parameter, and in the fabrication process for this chip, it is 286 $\mu$A/V$^2$.

The phase noise originated from the tail transistor’s thermal noise at second and higher even harmonics of the oscillation frequency can be reduced if the tail transistor is decoupled by a shunt capacitor to minimize the conversion of thermal noise at
second and higher even harmonics to phase noise in the $1/f^2$ region. Besides, the
shunted capacitor reduces the duty cycle of the drain current through cross-coupled
transistors [15]. Less duty cycle leads to less amount of ISF $\Gamma_{\text{rms}}$ which appears in
the phase noise expression Equation(3.3). This results in a reduced phase noise to a
further extent. Therefore, a 3 pF metal-insulator-metal capacitor (MIM-Cap), $C_{\text{tail}}$,
was added across each tail transistor.

$T_{\text{tail,1}}$ and $T_{\text{tail,2}}$ have independent, tunable gate voltages. By adjusting them
differentially, we are altering the bias current in two branches. This can adjust the
phase error between in-phase output and quadrature output. The phase noise reaches
its minimum at the exact quadrature difference [47].

Coupling transistors $T_{\text{cpl,1}}$ to $T_{\text{cpl,4}}$ are 20-finger, 2 $\mu$m per finger transistors each.
They are biased by common-source transistors $T_5$ and $T_6$, which have 15 fingers, 2
$\mu$m per finger. Phase noise positively correlates with coupling strength; a smaller
coupling bias current leads to a lower phase noise. However, if the coupling strength
is too weak, locking of the in-phase quadrature-phase relationship disappears. By
sweeping the bias current, a balancing coupling strength was found by applying a
0.75 V gate-bias voltage to $T_5$ and $T_6$.

Finally, four buffers are added at $I^+$, $I^-$, $Q^+$, and $Q^-$ points shown in Figure 3.1. These buffers are common-source p-type transistors with 50 $\Omega$ load. Buffers
provide output-impedance matching to ease the measurement. They also ensure that
external loading does not affect the phase relationship within the oscillator. Otherwise,
the oscillation frequency will probably change for different loadings.

The layout was structured symmetrically to minimize common-mode noise. Deep
n-well structures were used commonly for active transistors to suppress crosstalk
among different circuit elements through the substrate.
3.3 Experimental Results

A photograph of the quadrature LC oscillator fabricated using IBM CMOS 0.13\(\mu\)m technology is shown in Figure 3.2. This technology has 1 polysilicon layer, 3 thin metal layers, 2 thick metal layers, and 3 RF layers. The oscillator has an area of 0.15 mm\(^2\) \((600 \mu\text{m} \times 250 \mu\text{m})\) excluding pads and 1 mm\(^2\) \((1000 \mu\text{m} \times 1000 \mu\text{m})\) including pads.

![Photograph of the fabricated CMOS Quadrature LC VCO chip](image)

DC measurements showed that the oscillator core draws 31 mA from a 1.2 V supply, while the output buffers draw 38 mA from a 2.0 V supply.

One of the quadrature oscillator outputs was connected to a spectrum analyzer (Agilent E4446A PSA) through \(\text{GSG}\) Pico-Probes from \(\text{GGB}\) industries. The DC supply and biases were supplied to chip using DC pins. Figure 3.3 shows the test setup.

The spectrum of the free-running output \(I\)– at oscillation frequency near 5 GHz is shown in Figure 3.4a. Its oscillation frequency is 4.995 GHz with a power of approximately -0.5 dBm. Because of the low-\(Q\) tank, the oscillation frequency jumps around without a locking signal as would be provided in a PLL or Costas loop.
Figure 3.3: Test setup for LC VCO spectrum, tuning range and phase noise
This will lead to an inaccuracy of the phase noise measurement. The injection lock is applied to the output pad of a signal generator with a power of 12 dBm at 10 GHz (super-harmonic injection lock). The spectrum of another output port is shown in Figure 3.4b with -1 dBm power at same frequency. Relative to the free-running case, the injection-locked spectrum has a narrower spread at the central frequency. This means the frequency drift in the free-running oscillation was suppressed by the reversely injected, low-phase-noise signal, fed from the output of Q− buffer.

![Figure 3.4: Measured spectrum for 5 GHz quadrature Ring VCO: (a) Free running; (b) Injection locked](image)

The losses associated with output probe, cable, and bias-T were totally 0.9 dB. After compensation, the output power for injection-locked case should be -0.1 dBm.

Figure 3.5 shows that the oscillation frequency ranges from 4.2 GHz to 7.2 GHz over a tuning voltage, $V_{\text{tune}}$, from 0.6 V to 2 V. This frequency range is 52% with respect to the central frequency of 5.7 GHz.

The free-running VCO phase noise was calculated from the measured injection locked phase noise [48]. The phase noise of a free-running VCO can be retrieved from the phase noise measured under injection lock by using below equation:

$$\mathcal{L}_{DUT \ free}(f_m) = \mathcal{L}_{DUT \ locked}(f_m) + \frac{\Delta f_{lock}^2}{4f_m^2} (\mathcal{L}_{DUT \ locked}(f_m) - \mathcal{L}_{inj}(f_m)) \quad (3.7)$$
where $L_{DUT\,\text{free}}(f_m)$ is the phase noise of the free-running VCO under test as a function of offset frequency $f_m$, $L_{DUT\,\text{locked}}(f_m)$ is the phase noise of the injection-locked VCO, $\Delta f_{\text{lock}}$ is the injection locking bandwidth, and $L_{\text{inj}}(f_m)$ is the phase noise of the injected reference signal [23].

The measured phase noise under injection lock is shown in Figure 3.6. At 1 MHz offset, the phase noise is -112.5 dBc/Hz.

From Equation (3.7), the phase noise of the free-running oscillator is retrieved to be -100.8 dBc/Hz at 1 MHz offset, with a locking bandwidth of 1.8 MHz, and a
reference source phase noise of -127 dBc/Hz at 1MHz offset. The simulated phase noise is -101.7 dBc/Hz at 1 MHz offset.

The waveform of the in-phase and quadrature outputs can be observed from a digital communication analyzer (Agilent 86100C DCA) with a two-input receiver module (Agilent 86118A) connected to $I-$ and $Q+$ output pads. $I+$ output pad can be connected to signal generator for injection lock. The diagram in Figure 3.7 indicates the setup which holds the phase and amplitude relationships between the two outputs while generates the required trigger signal.

![Figure 3.7: Time-domain measurement setup for the quadrature VCO](image)

The resulting waveforms for free-running operation and injection-locked operation are shown in Figure 3.8. The waveform amplitude of the free-running operation was smaller than the injection-locked one. Since the points in the measured waveforms were an averaged value after 256 points, the frequency drift in the free-running operation, i.e. the significant jitter spread the energy at any specific location and made the waveform wider.
Figure 3.8: Measured output waveforms of $Q^+$ and $I^-$ channels of 5 GHz quadrature LC VCO: (a) Free running; (b) Injection locked

3.4 Summary

A CMOS quadrature VCO, using two cross-coupled LC oscillator cells, was designed at 5 GHz. Enough coupling strength between the two oscillator cells forces a quadrature phase relationship. This designed was fabricated in CMOS 0.13$\mu$m process and the measurement result showed a tuning range of 3 GHz, which is 52% of the central frequency. Capacitor to shunt tail transistor and tunability of phase difference between in-phase and quadrature outputs were employed to reduce phase noise. The measured phase noise is -100.8 dBc/Hz at 1MHz offset. The core circuit takes 0.15 mm$^2$ area and consumes 37.2 mW power. The buffers consume 76 mW power.

The comparison and discussion of this LC QVCO is in the next chapter, together with a ring QVCO.
Chapter 4

Quadrature Ring Oscillator

4.1 Introduction

The spiral inductors in the LC oscillator discussed in last chapter take more than 80% of the chip area, which is proportional to the fabrication cost of an integrated circuit. For a cost sensitive application as GPON transceivers at the end user’s side, a voltage-controlled ring oscillator is attractive because it is inductorless. This chapter presents a quadrature ring oscillator working at the same central frequency (5 GHz) as the LC oscillator. It saves a big amount of silicon area, but the trade-off is an increased phase noise, because it does not have a resonator with good quality factor. Despite that, ring oscillators has been widely used in phase-locked-loops (PLL) [49] [50] [51] for clock and data recovery, frequency synthesis, clock synchronization in microprocessors, and many applications requiring multi-phase sampling.

4.2 Circuit Design

As the introductory chapter discussed, a higher oscillation frequency from ring oscillators requires a lower number of delay stages, smaller parasitic capacitances from devices and interconnections, and a higher supply voltage.
This design uses lowest possible number of delay stages for ring oscillators to get high oscillation frequency; only two stages are used. As discussed in Section 2.1.2, to get a 360° phase shift through the loop of a 2-stage ring oscillator, the differential input and output structure of each stage must be used. Furthermore, the two delay stages should be connected in a loop with the outputs of the second stage connected to the inputs of the first stage with reverse polarity as indicated in Figure 4.1.

The two-stage structure not only offers higher oscillation frequency, but generates quadrature phase relationship between the outputs of first stage and the outputs of the second one. The differential structure provides both the in-phase and the anti-phase local oscillation signals simultaneously to feed mixers either single-balanced or double-balanced.

Each delay stage shown in Figure 4.2 has two amplifiers of negative gain for differential inputs. Each amplifier is current controlled. Increasing or decreasing that control current can increase or decrease the oscillation frequency accordingly. A latch consisting of two cross-coupled inverters are inserted between the outputs of the two amplifiers to speed up the one-to-zero or zero-to-one transitions of the outputs of each amplifier. The latch, as a positive feedback system which shortens the transition time, can lower the phase noise and potentially increase the oscillation frequency.
Figure 4.2: A delay stage consisting of two amplifiers and two cross-coupled inverters

The circuit schematic of each stage is shown in Figure 4.3.

Figure 4.3: Circuit schematic of one delay stage for quadrature ring oscillator

$M_1$ and $M_2$ are amplifiers for input differential signals. They are 8-finger NMOS FETs with 1.87 $\mu$m width per finger. $M_7$ and $M_8$ provide the $V_c$ controlled current to the amplifiers. They are made of 21-finger PMOS FETs with 2 $\mu$m width per finger. A digital inverter $M_3$-$M_5$ cross couples to another inverter $M_4$-$M_6$, forming a latch in between of the two amplifiers. $M_3$ and $M_4$ are 4-finger NMOS FETs with 1.75 $\mu$m width per finger; $M_5$ and $M_6$ are 9-finger PMOS FETs with 2 $\mu$m width per finger.
CHAPTER 4. QUADRATURE RING OSCILLATOR

The widths of PMOS FETs are selected to be close to three times of the widths of NMOS FETs to improve the symmetry of the generated waveform, which helps lower the phase noise of the oscillator. All FETs are narrow, because the parasitic capacitances from these active devices have to be minimized for a high oscillation frequency. All transistors have gate lengths of 0.12 µm.

A relatively high supply voltage, 1.6 V, was used as $V_{DD}$. It not only boosts the oscillation frequency to the desired value, but helps lower the phase noise. The phase noise of an inverter-based ring oscillator comes from white noise and flicker noise of NFETs and PFETs [52]. The SSB phase noise due to white noise can be expressed as

$$L(f) = \frac{2kT}{I} \left( \frac{1}{V_{DD} - V_t} (\gamma_N + \gamma_P) + \frac{1}{V_{DD}} \right) \left( \frac{f_o}{f} \right)^2$$

where $f_o$ is the oscillation frequency, $f$ is the offset frequency, $I$ is the charging and discharging current to load capacitance.

Finally, buffers to $I+$, $I-$, $Q+$, and $Q-$ are added. These buffers are commonsource n-type transistors with 75 Ω loads. Buffers provide an output-impedance match to ease the measurement. They also ensure that external loading does not affect the phase relationship within the feedback system of oscillator. The whole circuit with buffers is shown in Figure 4.4. $M_9$ to $M_{12}$ are 7-finger NMOS FETs with 2 µm width per finger.

4.3 Experimental Results

This ring oscillator is integrated with some other building blocks like mixers and filters for a direct-down conversion application. IBM CMOS 0.13µm technology was used for fabrication. A photograph of a ring QVCO together with two mixers, and two LPFs is shown in Figure 4.5. The whole circuit is a QPSK demodulation frontend.
The total chip is 1 mm × 1 mm. The ring oscillator is in the middle of the chip and takes an area of 0.019 mm$^2$ (200 µm × 95 µm) excluding pads. This area is only 13% of the area used by LC oscillator (0.15 mm$^2$) described in last chapter.

DC measurement showed that the whole circuit draws 44 mA from a 1.6 V DC supply. From the result of a DC simulation, the core of the oscillator without buffers should draw 14 mA, while the output buffers draw 30 mA.

One of the quadrature oscillator outputs, $I^+$, was connected to a spectrum analyzer (Agilent E4448A PSA) through GSG Pico-Probes from GGB industries. The DC supply and control voltage were supplied to chip using DC pins. The measurement was done for both free-running oscillation and injection-locked oscillation. Figure 4.6 shows the test setup. The oscillator is free running when the signal generator (Anritsu MG3694A) is off; the oscillator is super-harmonically injection locked when the signal generator feeds a double-frequency signal, which is at 10 GHz with a power of
2 dBm to the output pads of $I^-$.  

The resulting spectrum at $V_{tune} = 0.48$ V of free-running output is shown in Figure 4.7a. The oscillation frequency is 5.01 GHz with a power of approximately -12 dBm. The spectrum of injection locked output at $V_{tune} = 0.48$ V is shown in Figure 4.7b with -9.8 dBm power at 4.99 GHz. Relative to the free-running case, the injection-locked spectrum has a narrower spread at the central frequency. This means the frequency drifting in the free-running oscillation was suppressed by the reversely injected, low-phase-noise signal fed from the output of the $I^-$ buffer.

The losses associated with output probes, cables and connectors were 1.6 dB. After compensation, the output power for injection-locked case is -8.2 dBm.

The measured harmonics up to third order of both cases are shown in Figure 4.8. The injection lock suppressed the third-order harmonic by 5 dB and suppressed the second-order harmonic by 4 dB.

Figure 4.9 shows that the oscillation frequency ranges from 2.5 GHz to 6.5 GHz over tuning voltage, $V_{tune}$, from 1.2 V to 0.35 V. This frequency range is 89% with respect to central frequency, which is actually 4.5 GHz.
Figure 4.6: Test setup for Ring VCO’s spectrum, tuning range and phase noise
Figure 4.7: Measured spectrum for 5 GHz quadrature Ring VCO: (a) Without injection lock; (b) Injection locked

Figure 4.8: Measured spectrum up to third-order harmonics of Ring VCO: (a) Without injection lock; (b) Injection locked
Figure 4.9: Measured oscillation frequency as a function of control voltage for the ring oscillator.

The phase noise of the ring oscillator was also measured by the spectrum analyzer for both cases. At 1 MHz offset, the phase noise for free running operation was -71 dBc/Hz as shown in Figure 4.10a. But due to the significant drift of oscillation frequency, the free running operation cannot provide reliable measurement for phase noise. Injection lock has to be used and then the measured phase noise should be converted from injection-locked operation to free-running operation. The measured phase noise for injection-locked case was -88 dBc/Hz at 1 MHz offset, as shown in Figure 4.10b.

The phase noise measured for the free-running VCO without injection lock suffers from the inaccuracy resulting from the frequency drift of the low-Q oscillator. This problem can be solved by retrieving the free-running phase noise from that measured under injection lock [48]. The calculation equation is [23]:

$$L_{DUT\ free}(f_m) = L_{DUT\ locked}(f_m) + \frac{\Delta f_{lock}^2}{4f_m^2} (L_{DUT\ locked}(f_m) - L_{inj}(f_m)) \quad (4.2)$$

where $L_{DUT\ free}(f_m)$ is the phase noise of the free-running VCO under test as a function of offset frequency $f_m$, $L_{DUT\ locked}(f_m)$ is the phase noise of the injection-locked VCO, $\Delta f_{lock}$ is the injection locking bandwidth, and $L_{inj}(f_m)$ is the phase
From Equation (4.2), the phase noise of the free-running oscillator is retrieved to be -81 dBc/Hz at 1 MHz offset, with a locking bandwidth of 1 MHz, and a reference source phase noise of -122 dBc/Hz at 1 MHz offset.

To verify the 90° phase shift between in-phase output and quadrature output, a digital communication analyzer (Agilent 86100C DCA) with a two-input receiver module (Agilent 86118A) was connected to $I^+$ and $Q^+$ output pads as shown in Figure 4.11. This DCA can be used as an oscilloscope with a sampling rate of 60 GHz. $I^-$ output pads were connected to signal generator, which is used for injection lock. This setup holds the phase and amplitude relationships between the two outputs while generating the required trigger signal.

The resulting waveforms for free-running operation and injection-locked operation are shown in Figure 4.12.

For the injection-locked operation, the waveform amplitude at the oscilloscope was 58 mV, which was -15 dBm. Compensating for the 6.3 dB loss from the splitter, the cables and the connectors, the output power at the $I^+$ and $Q^+$ output pads was -8.7 dBm. However, the waveform amplitude of the free-running operation was...
Figure 4.11: Time-domain measurement setup for the quadrature ring VCO
Figure 4.12: Measured output waveforms of $I^+$ and $Q^+$ channels of 5 GHz quadrature Ring VCO: (a) Without injection lock; (b) Injection locked

much smaller; only -18 dBm at the output pads after loss compensation. The points in the measured waveforms were an averaged value after 1024 points. Because of the big frequency drift from the free-running operation, the significant jitter spread the energy at any specific location and made the waveform wider. That’s why the averaged amplitude was much lower than the injection-locked operation.

4.4 Summary and discussion

A CMOS quadrature ring VCO, using two delay stages with differential inputs and outputs, was designed at 5 GHz. The parasitic capacitances from active devices and interconnection wires were minimized for higher oscillation frequency. This design was fabricated in CMOS 0.13 $\mu$m process and the measurement result showed a tuning range of 4 GHz, which is 80% of the central frequency. The measured phase noise was -81 dBc/Hz at 1MHz offset. The core circuit takes 0.019 mm$^2$ area and consumed 22.4 mW power for core circuit without buffer. It consumed 70.4 mW power with four buffers.

A comparison in Table 4.1 is made between the LC QVCO described in previous
chapter and the ring QVCO in this chapter. The comparison also includes some other published designs as references.

Table 4.1: Performance comparison of quadrature VCOs

<table>
<thead>
<tr>
<th>Ref</th>
<th>Type</th>
<th>Tuning range (GHz)</th>
<th>Tuning percentage</th>
<th>Phase noise (dBc/Hz),1MHz</th>
<th>Area w/o pads (mm²)</th>
<th>Number of inductors</th>
<th>Power w/o buffers(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prev</td>
<td>LC switched biasing</td>
<td>4.2-7.2</td>
<td>52%</td>
<td>-100.8</td>
<td>0.6x0.25</td>
<td>2</td>
<td>37.2</td>
</tr>
<tr>
<td>chap</td>
<td>LC super-harmonic</td>
<td>4.4-5.5</td>
<td>20%</td>
<td>-105</td>
<td>0.7x0.4</td>
<td>2</td>
<td>32.4</td>
</tr>
<tr>
<td>[47]</td>
<td></td>
<td>4.5-5.5</td>
<td>20%</td>
<td>-117</td>
<td>-</td>
<td>4</td>
<td>5.28</td>
</tr>
<tr>
<td>[53]</td>
<td></td>
<td>4.57-5.21</td>
<td>13%</td>
<td>-125</td>
<td>-</td>
<td>5</td>
<td>22</td>
</tr>
<tr>
<td>[54]</td>
<td></td>
<td>2.5-6.5</td>
<td>89%</td>
<td>-81</td>
<td>0.2x0.1</td>
<td>0</td>
<td>22.4</td>
</tr>
<tr>
<td>This</td>
<td>Ring</td>
<td>2.5-9</td>
<td>130%</td>
<td>-82</td>
<td>0.078x0.038</td>
<td>0</td>
<td>135</td>
</tr>
<tr>
<td>work</td>
<td>Ring</td>
<td>4.5-6.2</td>
<td>32%</td>
<td>-95.3</td>
<td>-</td>
<td>0</td>
<td>40</td>
</tr>
<tr>
<td>[55]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[56]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It is apparent that ring QVCOs take chip area one or two order of magnitude smaller than LC ones. My ring oscillator in this chapter takes 13% area of the LC one in last chapter. The trade-off of a small size for a ring oscillator is an increased phase noise, about 20 to 30 dB higher than its LC conterparts. This ring oscillator has a phase noise 20 dB higher than the LC oscillator described in the previous chapter.
Chapter 5

Broadband Mixer

5.1 Introduction

A Gilbert-cell based mixer with broadband input-impedance matching is described in this chapter.

This mixer directly down converts a broadband RF signal from 2.5 GHz to 7.5 GHz to zero-IF. A local oscillation at 5 GHz generated either from an LC-oscillator as described in Chapter 3 or from a ring oscillator as in Chapter 4 will feed this mixer. In a QPSK demodulator, two such mixers will be integrated; one for I-channel direct-down conversion and the other for Q-channel.

In the proposed GPON receiver in Figure 1.5, a transimpedance amplifier (TIA) is preceding the demodulator with an output impedance of 50 Ω. Since the mixers in the demodulator frontend are the first stages, they need a matched input impedance to limit the reflected wave back to the previous preamplifier. Low pass filters (LPFs) with 50 Ω input impedance follows the mixers. So an output impedance matching to 50 Ω is also required.

Mixers with high conversion gain and low noise figure can improve the system performance. In a direct-down-conversion applications, depressing flicker noise (1/f noise) is a good practice.
5.2 Circuit Design

The mixer consists of three stages: an input matching stage, a Gilbert-cell based mixing stage, and an output combiner stage. The input matching stage not only provides an acceptable low reflection coefficient for a broadband RF input, but also acts as a balun to convert a single-ended input RF signal to two balanced output signals with one in-phase terminal and one anti-phase terminal. The balanced RF signals are required by the following double-balanced Gilbert-cell stage. The differential outputs from the double-balanced Gilbert cell are converted back to a single-ended zero-IF signal by an output combiner. The single-ended output is easier to measure. Besides, it simplifies the following low-pass-filter design from system perspective. Otherwise, LPFs have to be developed for both differential outputs, which will increase the complexity and total cost of the system.

The input matching stage consists of a common-gate amplifier and a common-source amplifier. Figure 5.1 shows the schematics of this stage, which has been introduced in Section 2.2.2.

![Common-gate, common-source balun circuit](image)

Figure 5.1: Common-gate, common-source balun circuit

The common-gate amplifier $M_1$ provides input-impedance matching and in-phase RF output, $v_{RF^+}$; while the common-source amplifier $M_2$ provides anti-phase output,
CHAPTER 5. BROADBAND MIXER

The input impedance of this stage can be considered as a parallel of the input impedance of common-gate amplifier, seeing from the source terminal, and a resistance of $R_b$. From the model of common-gate amplifier below in Figure 5.2, the input impedance of common-gate amplifier can be obtained as

$$Z_{in-CG} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m1}} \parallel \frac{1}{j\omega C_{gs1}}$$  \hspace{1cm} (5.1)

where $g_{m1}$ is the transconductance of $M1$. Ignoring the gate-to-source parasitic capacitance $C_{gs}$, $Z_{in-CG}$ reduces to

$$Z_{in-CG} \approx \frac{1}{g_{m1}}$$  \hspace{1cm} (5.2)

Then the input impedance of the first stage can be approximated as

$$Z_{in} = \frac{1}{g_{m1}} \parallel R_b$$  \hspace{1cm} (5.3)

Since $g_{m1}$ of $M1$ is a function of its aspect ratio of channel width over channel length, a suitable size can be chosen to make $Z_{in}$ close to 50 $\Omega$. In this design, an 11-finger NMOS FET with 2 $\mu$m width per finger was selected for $M1$. $R_b$ is 600 $\Omega$, and $R_1$ is 120 $\Omega$. For the common source stage, a 16-finger NMOS FET with 2 $\mu$m width per finger was selected for $M2$ and $R_2$ is 80 $\Omega$ to provide $v_{RF}$ with a balanced

![Figure 5.2: Small signal model of Common-Gate Circuit](image-url)
amplitude and phase comparing with $v_{RF^+}$.

The differential signals $v_{RF^+}$ and $v_{RF^-}$ feed the RF ports of the following mixing stage, shown in Figure 5.3. The structure of this stage differs from the basic, conventional Gilbert cell introduced in Figure 2.16 in two ways. First, there is no current source at the bottom to provide the bias current for the two transconductors $M_3$ and $M_4$. Although lacking a current source makes transconductors not true differential amplifiers and makes common-mode rejection not happen in the mixing stage, it decreases the amount of stacking and lowers required level of $V_{DD}$. The second difference from conventional Gilbert cell is that current bleeding transistors $M_9$ and $M_{10}$ are added to split the bias currents from transconductors.

![Figure 5.3: Gilbert-cell based mixing stage](image)

The transconductors $M_3$ and $M_4$ are biased in saturation region. They are made of 10-finger NMOS FETs with 2 $\mu$m width per finger. $M_5$ to $M_8$ form the LO-controlled switches, multiplying the linear RF signal currents out of $M_3$ and $M_4$ with the LO signal. Each of these switches are NMOS FETs of 10 fingers with 2 $\mu$m width per finger. Each $R_d$ is a resistor of 400 $\Omega$.

To make $M_5$ to $M_8$ act closer to ideal switches, which helps to reduce the noise, the steering of the currents from branch $M_5$ to branch $M_6$ or vice versa in left-half circuit
should be as fast as possible. The same argument applies to right-half circuit. This can be implemented by feeding larger LO signal, decreasing the overdrive voltage of the switches, or reducing the bias current through each switch by bleeding technique.

$M_9$ and $M_{10}$ are current-bleeding devices. They split the bias currents coming from transconductors. This split makes the current through load resistors less than through the transconductor, and allows larger load resistors $R_d$ to keep same voltage drop on the loads. Since the voltage conversion gain is $2g_mR_d/\pi$ [27], where $g_m$ is the transconductance of the transconductors $M_3$ or $M_4$, a larger $R_d$ increases conversion gain.

Besides, this current bleeding also helps reduce the 1/f noise, although the influence of the 1/f noise in a broadband direct-down conversion of 2.5 GHz in the targeted application is not significant. Since the bias currents in each switch is lowered, as mentioned in Section 2.2.1, the 1/f noise from switches will be reduced by this current bleeding, because the flicker noise relates to bias current as [41]

$$V_{n,1/f}^2 = \frac{K_f I_{ds}^{af}}{C_{ox} L^2 f^{ef}}$$

(5.4)

where $K_f$ is a device-specific constant, $C_{ox}$ is the unit capacitance of oxide, $L$ is the length of the FET device, and $I_{ds}$ is the bias current. $af$ and $ef$ are indices of current and frequency. $M_9$ and $M_{10}$ are PMOS FETs with 10 fingers per device and 2 $\mu$m width per finger.

The differential outputs $v_{IF+}$ and $v_{IF-}$ are combined to form a single-ended output by a combiner stage, consisting of a differential amplifier with an active load. The circuit is shown in Figure 5.4.

The tail transistor $M_{11}$ is a 45-finger NMOS FET with 2 $\mu$m width per finger, and is biased by $V_{tail}$. $M_{12}$ and $M_{13}$ are triode-biased amplifiers of 22-finger NMOS FETs with 2 $\mu$m width per finger. The active load consists of a current mirror $M_{14}$ back to back connected to $M_{15}$. These two PMOS FETs have 32 fingers with 2 $\mu$m width.
per finger individually. In comparison with a resistor load, an active load doubles the voltage gain and increases the common-mode rejection ratio [6]. But the active PMOS load will generate 1/f noise, which is not a problem for a resistor load.

Since $M_{13}$ is working in the triode region, the output impedance can be approximated as the channel resistance of this device. When the device size and bias condition are properly selected, the output impedance can be controlled. An output buffer is not added in this case since the output reflection coefficient is acceptable. The whole circuit of the mixer with all three stages is shown in Figure 5.5.

### 5.3 Experimental Results

A photograph of the mixer fabricated in IBM CMOS 0.13 $\mu$m technology is shown in Figure 5.6. It has an area of 0.04 mm$^2$ ($200 \mu$m $\times$ 200 $\mu$m) excluding pads, or 1 mm$^2$ ($1000 \mu$m $\times$ 1000 $\mu$m) including pads.

DC measurements showed that the mixer draws 13 mA from a 1.2V DC supply.

Figure 5.7 shows the measurement setup. Two differential LO signals at 5 GHz were applied to $LO^+$ and $LO^-$ ports, an input RF signal was applied to $RF_{in}$ port,
Figure 5.5: Broadband mixer circuit with three stages

Figure 5.6: Photograph of the fabricated CMOS chip of broadband mixer
and the output port of $I$ channel was connected to a spectrum analyzer (Agilent E4448A PSA). The LO signal and the input RF signal were generated from two signal generators (Anritsu MG3694A). The DC supply and biases were supplied to chip using DC pins.

![Diagram of test setup for mixer's conversion gain and P1dB](image)

Figure 5.7: Test setup for mixer’s conversion gain and P1dB

The conversion gain at different RF frequencies is shown in Figure 5.8. The midband conversion gain around 5 GHz is 8.5 dB. This mixer has a 3 dB bandwidth of 4.5 GHz, i.e. from 2.5 GHz to 7 GHz.

Non-linearity are characterized by parameters of input 1 dB compression point (P1dB) and third-order intercept point (IP3). Figure 5.9 shows a decreasing conversion gain along with an increasing input signal power. At 6.5 GHz RF input and 1.5 GHz IF output, the input P1dB point is at -17 dBm.
Figure 5.8: Measured conversion gain as a function of RF signal frequency

Figure 5.9: Measured conversion gain as a function of the power of input signal at 6.5 GHz
The IP3 was measured by feeding the mixer with a two-tone RF signal, one tune at 5.301 GHz, and the other at 5.302 GHz. The LO was chosen at 5 GHz. Then the produced third-order intermodulation products were at 300 MHz and 303 MHz. The result shown in Figure 5.10 indicate an input IP3 (IIP3) at -9 dBm and an output IP3 (OIP3) at 0 dBm.

![IP3 Diagram]

Figure 5.10: Measured third-order intercept point

The input impedance matching was measured by a vector network analyzer (Agilent N4373A Lightwave Component Analyser). The S11 parameter is shown in Figure 5.11. The mixer has an input reflection coefficient below -10 dB from 2.5 GHz to 10 GHz. Its output reflection coefficient is not as good as input. As shown in Figure 5.12, it is only -7 dB.

The measured double sideband noise figure is 13 dB, and the simulated value is 12 dB.

The LO port to RF port feedthrough is -55 dB. The RF port to IF port feedthrough is -32 dB.
CHAPTER 5. BROADBAND MIXER

Figure 5.11: Measured input reflection coefficient of the broadband mixer

Figure 5.12: Measured output reflection coefficient of the broadband mixer
A broadband mixer targeted at 5 GHz bandwidth, with RF from 2.5 GHz to 7.5 GHz, is described in this chapter. The input impedance is well matched as required. The 3 dB bandwidth is from 2.5 GHz to 7 GHz, with 0.5 GHz at the high end not covered. Since this mixer is for direct conversion application, a Gilbert cell is used to isolate the LO to RF feedthrough to avert the risk of self-mixing, and current bleeding mechanism is adopted to minimize the flicker noise as well as boosting the conversion gain. The mixer was fabricated in CMOS 0.13 $\mu$m process. The core circuit takes 0.04 mm$^2$ area and consumes 16 mW power.

The comparison and discussion of this broadband mixer is in the next chapter, together with a high-linearity broadband mixer.
Chapter 6

Broadband Mixer with High Input Linearity

6.1 Introduction

In the GPON standard, a class B receiver should handle an input optical signal power at a minimum value of -21 dBm, and a maximum value of -1 dBm [57]. As shown in Figure 6.1, the optical signal will be firstly transduced to an electrical current signal by a photodiode, whose typical sensitivity is 0.6 A/W. Then this current signal will be converted and amplified to a voltage signal by a transimpedance amplifier (TIA). A broadband TIA for Figure 6.1 can have a transimpedance gain at around 45 dBΩ, which has been demonstrated by TIA designs in [58]. Thus, the minimum and maximum possible signal voltages out of the TIA, which also give the input voltage range to the following mixers can be calculated in Table 6.1

Table 6.1: Input Voltage Range to Mixers

<table>
<thead>
<tr>
<th></th>
<th>Optical Power by dBm</th>
<th>Current Amp after photodiode (µA)</th>
<th>Voltage Amp after TIA (mV)</th>
<th>Voltage in dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>-21</td>
<td>4.8</td>
<td>0.85</td>
<td>-48.4</td>
</tr>
<tr>
<td>MAX</td>
<td>-1</td>
<td>480</td>
<td>85</td>
<td>-8.4</td>
</tr>
</tbody>
</table>
CHAPTER 6. BROADBAND MIXER WITH HIGH INPUT LINEARITY

The input voltage level to mixers ranges from -48.4 dBm to -8.4 dBm. However, the previously designed mixer designed in Chapter 5 only has an input 1 dB compression point (P1dB) at -17 dBm. Therefore, a new broadband mixer with high input linearity has to be designed to fit the application.

As described in Chapter 2, a simple and low-cost method for higher linearity is to use resistive source degeneration. Furthermore, biasing the transconductor in triode region can enhance the linearity as well. These two methods are used in this design for higher linearity with a sacrifice of conversion gain.

6.2 Circuit Design

Similar to the mixer described in last chapter, this new mixer consists of three stages as well: an input matching stage, a Gilbert-cell based mixing stage, and an output combiner stage. The differences mainly come from some techniques used to improve linearity, and capacitive peaking to improve gain flatness.

The input matching stage consists of a common-gate amplifier and a common-source amplifier, with each amplifier resistively degenerated. Figure 6.2 shows the schematics of this stage.

The common-gate amplifier $M_1$ provides input-impedance matching and in-phase
RF output, $v_{RF^+}$; while the common-source amplifier $M2$ provides anti-phase output, $v_{RF^-}$.

The input impedance of the first stage can be approximated as

$$Z_{in} = \frac{1}{g_{m1}} + R_s || R_b$$  \hspace{1cm} (6.1)

Since $g_{m1}$ of $M1$ is a function of its aspect ratio of its channel width over channel length, a suitable size can be chosen to make $Z_{in}$ close to 50 $\Omega$. In my design, an 8-finger NMOS FET with 2 $\mu$m width per finger was selected for $M1$. $R_b$ is 220 $\Omega$, $R_s$ is 130 $\Omega$, and $R_1$ is 220 $\Omega$. For the common source stage, a 5-finger NMOS FET with 2 $\mu$m width per finger was selected for $M2$. The output $v_{RF^-}$ is taken between $R_{2b}$ of 150 $\Omega$ and $R_{2a}$ of 140 $\Omega$ to get a balanced amplitude and phase relative to $v_{RF^+}$.

The differential signals $v_{RF^+}$ and $v_{RF^-}$ feed the RF ports of the following mixing stage, shown in Figure 6.3. The structure of this stage differs from the basic, conventional Gilbert cell introduced in Figure 2.16 in three ways. First, there is no current source at the bottom to provide the bias current for the two transconductors $M_3$ and $M_4$. Although lacking a current source makes transconductors not true...
differential amplifiers and makes common-mode rejection not happen in the mixing stage, it decreases the amount of stacking and lowers required level of $V_{DD}$. The second difference from conventional Gilbert cell is that current bleeding transistors $M_9$ and $M_{10}$ are added to split the bias currents from transconductors. Thirdly, the transconductors are not biased in saturation region, but in triode region instead.

![Gilbert-cell based mixing stage with triode-biased transconductor](image)

Figure 6.3: Gilbert-cell based mixing stage with triode-biased transconductor

The triode-biased transconductors $M_3$ and $M_4$ are made of 7-finger NMOS FETs with 2 $\mu$m width per finger. $M_5$ to $M_8$ form the LO-controlled switches, multiplying the linear RF signal currents out of $M_3$ and $M_4$ with the LO signal. Each of these switches are NMOS FETs of 14 fingers with 2 $\mu$m width per finger. Each $R_d$ is a resistor of 285 $\Omega$.

To make $M_5$ to $M_8$ acting more close to ideal switches, which help to reduce the noise, the steering of the currents from branch $M_5$ to branch $M_6$ or vice versa in left-half circuit should be as short as possible. Same argument is for right-half circuit. This can be implemented by feeding larger LO signal, decreasing the overdrive voltage at which each of the switches is operating, or using current bleeding technique to reduce the bias current through each switch.

$M_9$ and $M_{10}$ are current-bleeding devices. They split the bias currents coming
from transconductors. This split makes the current through load resistors less than through the transconductor, and allows larger load resistors $R_d$ to keep same voltage drop on the loads. Since the voltage conversion gain is $2g_mR_d/\pi$ [27], where $g_m$ is the transconductance of the transconductors $M_3$ or $M_4$, a larger $R_d$ increases conversion gain.

Besides, this current bleeding also helps reduce the $1/f$ noise, although the influence of the $1/f$ noise in a broadband direct-down conversion of 2.5 GHz in the targeted application is not significant. Since the bias currents in each switch is lowered, as mentioned in Section 2.2.1, the $1/f$ noise from switches will be reduced by this current bleeding, because the flicker noise relates to bias current as [41]

$$V_{n,1/f}^2 = \frac{K_f I_{ds}^a f_{ef}}{C_{ox} L^2 f_{ef}}$$

(6.2)

where $K_f$ is a device-specific constant, $C_{ox}$ is the unit capacitance of oxide, $L$ is the length of the FET device, and $I_{ds}$ is the bias current. $af$ and $ef$ are indice of current and frequency. $M_9$ and $M_{10}$ are PMOS FETs with 13 fingers per device and 2 $\mu$m width per finger.

The differential outputs $v_{IF+}$ and $v_{IF-}$ will be combined to a single-ended output by a combiner stage, consisting of a differential amplifier with source degeneration by a parallel of one resistor and one capacitor. This technique is also called capacitive peaking, which is to help broaden the bandwidth. The circuit is shown in Figure 6.4.

The tail transistor $M_{11}$ is a 22-finger NMOS FET with 2 $\mu$m width per finger, and is biased by $V_{tail}$ to work in saturation region. $M_{12}$ and $M_{13}$ are 13-finger NMOS FETs with 2 $\mu$m width per finger. Passive loads, resistors $R_3$ and $R_4$ of 370 $\Omega$, are used in this design in place of the active PMOS load used in previous chapter, because a PMOS load will generate $1/f$ noise, while a resistor load not. The capacitive peaking consists of a 140 fF capacitor and a 280 $\Omega$ resistor.
An output buffer is following the output of this combiner. The buffer begins with a source follower working as a DC level shifter. It pulls the DC voltage, from 1.46 V out of the preceding combiner, down to 0.81 V. This new DC voltage is required to bias following common-source amplifier. The latter amplifier with a 75 Ω load provides output-impedance matching to ease the measurement. The buffer circuit is shown in Figure 6.5.
Chapter 6. Broadband Mixer with High Input Linearity

$M_{14}$ is a 13-finger NMOS FETs with $2 \, \mu m$ width per finger and $M_{15}$ NMOS FET has 24 fingers with $2 \, \mu m$ width per finger. $R_5$ is $280 \, \Omega$ and $R_6$ is a $75 \, \Omega$ resistor.

The whole circuit of the mixer with all stages is shown in Figure 6.6.

![Figure 6.6: Whole mixer circuits with three main stages and a buffer](image)

The values of the gain in each stage indicated in Figure 6.7 were simulated and listed in Table 6.2.

![Figure 6.7: Gain of each stage of a broadband mixer with high input linearity](image)

The simulation indicated that the overall conversion gain of the four stages (with buffer) is -6.7 dB with an RF signal at 5.2 GHz and IF at 0.2 GHz. The conversion gain of three main stages without buffer is -2.1 dB, and the conversion gain of the Gilbert cell stage only is 0.7 dB.
Table 6.2: Gain of each stage of the broadband mixer with high input linearity

<table>
<thead>
<tr>
<th></th>
<th>$G_{bal}$ (dB)</th>
<th>$G_{c,Glt}$ (dB)</th>
<th>$G_{cbn}$ (dB)</th>
<th>$G_{buf}$ (dB)</th>
<th>$G_{c,overall}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-1.2</td>
<td>0.7</td>
<td>-1.6</td>
<td>-4.5</td>
<td>-6.7</td>
</tr>
</tbody>
</table>

6.3 Experimental Results

There are two identical mixers in the fabricated demodulator frontend photographed in Figure 6.8. One mixer is for I channel down conversion, and the other for Q channel. IBM CMOS 0.13 $\mu$m technology was used. Each mixer takes an area of 0.04 mm$^2$ (260 $\mu$m $\times$ 150 $\mu$m) excluding pads.

![Figure 6.8: Photograph of the fabricated high-linear mixers in a QPSK demodulation frontend](image)

DC measurements showed that the two mixers together draw 48 mA from a 1.8 V DC supply. So each mixer, with buffer included, consumes 1.8 V $\times$ 24 mA = 43.2 mW power.

To measure the performance of the mixer, two differential LO signals at 5 GHz were applied to $LO^+$ and $LO^-$ ports, input RF signal was applied to the input RF port on the left, and the output port of $I$ channel was connected to a spectrum
CHAPTER 6. BROADBAND MIXER WITH HIGH INPUT LINEARITY

analyzer (Agilent E4448A PSA). The LO signal and the input RF signal were generated from two signal generators (Anritsu MG3694A). The DC supply and biases were supplied to chip using DC pins. Figure 6.9 shows the test setup.

Figure 6.9: Test setup for mixer’s conversion gain and P1dB

Since the output of the mixer goes through an on-chip 2nd-order Butterworth low-pass filter which has a cut-off frequency of 2.5 GHz, the effect of that low-pass filter has to be de-embedded to get the true performance of the mixer itself. The loss caused by the additional filter, which is a simulated result of the amplitude frequency response, was compensated. The losses associated with output probes, cables and
connectors were also measured and compensated. The conversion gain at different RF frequencies is shown in Figure 6.10. The midband conversion gain around 5 GHz is -7 dB. This mixer has a 3 dB bandwidth of 5 GHz, i.e. from 2.5 GHz to 7.5 GHz.

![Conversion Gain vs RF Frequency](image)

Figure 6.10: Measured conversion gain as a function of RF signal frequency

Non-linearity are characterized by parameters of input 1 dB compression point (P1dB) and third-order intercept point (IP3). Figure 6.11 shows a decreasing conversion gain along with an increasing input RF signal power. At 5.2 GHz input, the input P1dB point is at -5 dBm.

The IP3 was measured by feeding the mixer with a two-tone RF signal, one tune at 5.301 GHz, and the other at 5.302 GHz. The LO was chosen at 5 GHz. Then the produced third-order intermodulation products were at 300 MHz and 303 MHz. The result shown in Figure 6.12 indicate an input IP3 (IIP3) of +5.3 dBm and an output IP3 (OIP3) of -4.1 dBm. Due to a conversion loss of this mixer, the OIP3 is lower than the IIP3.

The input impedance matching was measured by a vector network analyzer (Agilent N4373A Lightwave Component Analyser). The S11 parameter is shown in Figure 6.13. The mixer has a reflection coefficient below -10 dB from 1 GHz to 12
CHAPTER 6. BROADBAND MIXER WITH HIGH INPUT LINEARITY

Figure 6.11: Measured conversion gain as a function of the power of input signal at 5.2 GHz

Figure 6.12: Measured third-order intercept point
CHAPTER 6. BROADBAND MIXER WITH HIGH INPUT LINEARITY

GHz.

Figure 6.13: Measured input reflection coefficient of the mixer with higher linearity

The measured double sideband noise figure is 25 dB, and the simulated value is 24 dB.

The LO port to RF port feedthrough is -54 dB. The RF port to IF port feedthrough is -41 dB.

A test is designed as Figure 6.14 to see the demodulation result of the designed high-linear mixer. The details of this setup including BPSK generation, chip under test, and the connections among different equipments is shown in Figure 6.15.

The baseband signal is a non-return-zero (NRZ) pseudorandom signal with a pattern period of $2^7 - 1$ bits. The data rate is 2.5 Gb/s, and the data amplitude is 0.25 V peak to peak (Vp-p). It has a waveform in Figure 6.16a, and a spectrum in Figure 6.16b.

After mixing the baseband signal with an local oscillation (LO) carrier at 5 GHz, the generated BPSK signal has a waveform in Figure 6.17a, and a spectrum in Figure 6.17b.
The BPSK signal feeds the RF input of the designed mixer, which is followed by an on-chip LC 2nd-order LPF with 3 dB cut-off frequency at 1.8 GHz. The down-converted and filtered signal has a spectrum at baseband as shown in Figure 6.18b. The time domain waveform of the demodulated signal after the chip is shown in Figure 6.18a. The baseband data represented by two voltage levels can be clearly identified, but the corner of the rectangular wave is rounded off. It has a peak-to-peak voltage of 70 mV.

To make this demodulated signal a better input for future decision circuit, an limiting amplifier can be added. This limiting amplifier not only increases the signal amplitude, but shortens the rise and fall time of the baseband signal. The waveform of the limiting-amplified baseband signal is shown in Figure 6.19a. The NRZ signal is mostly recovered with a peak-to-peak voltage of 400mV. The spectrum of this signal is shown in Figure 6.19b.

The eye diagram of the demodulated BPSK signal of 2.5 Gbps after the frontend but before the limiting amplifier is shown in Figure 6.20a. The eye diagram of the demodulated signal after the limiting amplifier is shown in Figure 6.20b.

Figure 6.14: The diagram of a test to see the BPSK demodulation result
Figure 6.15: Setup details of BPSK demodulation test
Figure 6.16: A baseband signal of 2.5 Gb/s: (a) Waveform; (b) Spectrum

Figure 6.17: A BPSK signal from 2.5 Gb/s baseband signal modulating 5 GHz carrier: (a) Waveform; (b) Spectrum
CHAPTER 6. BROADBAND MIXER WITH HIGH INPUT LINEARITY

Figure 6.18: The BPSK demodulated signal with 2.5 Gb/s baseband data: (a) Waveform; (b) Spectrum

Figure 6.19: The BPSK demodulated signal with 2.5 Gb/s baseband data after limiting amplifier: (a) Waveform; (b) Spectrum
6.4 Summary and discussion

A broadband mixer of 5 GHz bandwidth with a high linearity of P1dB at -5 dBm was designed, fabricated and measured. Both the input and output impedance are matched to 50 Ω. The gain flatness is obtained by capacitive peaking. The high linearity is achieved by resistive source degeneration. Since this mixer is for direct conversion application, a Gilbert cell is used to isolate the LO to RF feedthrough to avert the risk of self-mixing. Current bleeding is adopted to minimize the flicker noise as well as boosting the conversion gain. An integration test demonstrated the mixer’s ability to demodulate a 2.5 Gb/s broadband BPSK signal. This designed was fabricated in CMOS 0.13 μm process. The core circuit takes 0.04 mm² area. The circuit consumes 43.2 mW power with the buffer included.

A comparison in Table 6.3 is made between the high-gain mixer described in previous chapter and the high input-linearity one in this chapter. The comparison also includes some designs from published papers as references.

Comparing with previous chapter, the mixer in this chapter gets a 0.5 GHz wider bandwidth due to the capacitive peaking mechanism. In addition, this mixer trades off 16 dB conversion gain for a 12 dB increase in IP1dB. The accompanying side effect
Table 6.3: Performance comparison of broadband mixers

<table>
<thead>
<tr>
<th>References</th>
<th>Previous chap</th>
<th>This work</th>
<th>[59]</th>
<th>[30]</th>
<th>[60]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq(GHz)</td>
<td>2.5 - 7</td>
<td>2.5 - 7.5</td>
<td>1 - 5.5</td>
<td>0.3 - 25</td>
<td>2 - 11</td>
</tr>
<tr>
<td>CG(dB)</td>
<td>8.5</td>
<td>-7 (w buffer)</td>
<td>17.5</td>
<td>11</td>
<td>6.9</td>
</tr>
<tr>
<td>IP1dB(dBm)</td>
<td>-17</td>
<td>-5</td>
<td>-10.5</td>
<td>-5</td>
<td>-7</td>
</tr>
<tr>
<td>IIP3(dBm)</td>
<td>-9</td>
<td>5.3</td>
<td>0.8</td>
<td>–</td>
<td>3.5</td>
</tr>
<tr>
<td>NF(dB)</td>
<td>13</td>
<td>25</td>
<td>3.9</td>
<td>–</td>
<td>15.5</td>
</tr>
<tr>
<td>Area(mm²)</td>
<td>0.2 x 0.2</td>
<td>0.26 x 0.15</td>
<td>0.32</td>
<td>0.85 x 0.57</td>
<td>0.9 x 0.6</td>
</tr>
<tr>
<td>Number of inductors</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Power(mW)</td>
<td>16</td>
<td>43.2</td>
<td>34.5</td>
<td>71</td>
<td>25.7</td>
</tr>
</tbody>
</table>

of such tradeoff is a big deterioration of noise figure.

Comparing to other published mixers, this design is an inductorless solution, and uses an area one order of magnitude smaller. Such chip area saving is critical for cost sensitive applications like GPON transceivers for end users.

One noticeable disadvantage in this work is its high noise figure, 25 dB, which is 12 dB higher than the mixer in previous chapter. But below analysis will show that this high noise figure does not bring degradation to the system performance in an OSBM GPON receiver where the mix is used together with a high gain TIA in front.

As discussed at the beginning of this chapter, to meet the GPON standard on the maximum input optical power, one can choose a high-gain TIA together with a mixer of high input linearity like the one in this chapter. Another choice is to use a low-gain TIA followed by a mixer of an input linearity not that high. To make a fair comparison of the two cases, a parameter of the noise performance has to be deduced first.

As in Figure 6.21, the noise from a TIA can be modeled as an input-referred mean square noise current \( \overline{i_{n,TIA}^2} \), and the noise from a mixer can be modeled as an input-referred mean square noise voltage \( \overline{v_{n,mix}^2} \).

A TIA presented in [58], developed by the same research group as this work, has a transimpedance gain of 45 dBΩ. The structure of that TIA is indicated in
Figure 6.21: The noise sources in a TIA and mixer in an OSBM receiver

Figure 6.22. $I_{PD}$ is the input current from a photodiode, and $C_{PD}$ is the capacitance of the photodiode. That topology will be used for this noise analysis.

The TIA uses a feedback resistance $R_{FB}$ across the first high gain amplifier stage $-A$. Then a second 6 dB gain stage further increases the output voltage amplitude. Since the first stage gain $A$ is very high, the transimpedance gain of the first stage can be approximated as $R_{FB}$, and the input-referred noise current also mainly comes from $R_{FB}$ [18]. Therefore,

$$i_{n,TIA}^2 = \frac{4kT}{R_{FB}} \cdot B_1$$  \hspace{1cm} (6.3)

where $k$ is the Boltzmann constant, $T$ is the room temperature in Kelvin, and $B_1$ is the noise bandwidth, which is 1.6 times the 3-dB bandwidth of a one-pole system [61].

The proposed OSBM system transmits a 2.5 GSym/s baseband data on a 5 GHz offset RF carrier. So the TIA in the receiver has an input current frequency range from 2.5 GHz to 7.5 GHz. Take into consideration a low-pass filter (LPF) following the mixer.
which has a 3-dB bandwidth same as the baseband bandwidth, the noise bandwidth $B_1$ of the TIA can be approximated to be $5 \text{ GHz} \times 1.6 = 8 \text{ GHz}$.

The mixer’s input-referred noise voltage $v_{n,mix}^2$ can be derived from its noise figure (NF). As the noise model of a mixer shown in Figure 6.23, the noise factor $F$ is defined as

$$F = 1 + \frac{v_{n,mix}^2}{v_s^2} \quad (6.4)$$

where $v_s^2$ is the mean square noise voltage available to the mixer from a 50 Ω source resistor $R_s$ at temperature $T_0 = 290 \text{ K}$. The noise voltage spectrum density of $R_s$ is $4kT_0R_s$. Since the input impedance of the designed mixer matches $R_s$, the available noise voltage from $R_s$ to the mixer is

$$v_s^2 = 4kT R_s \cdot \left( \frac{1}{2} \right)^2 \cdot B_2 = k T R_s \cdot B_2 \quad (6.5)$$

where $B_2$ can be approximated to be $2.5 \text{ GHz} \times 1.6 = 4 \text{ GHz}$.

Next, this input-referred noise voltage of the mixer $v_{n,mix}^2$ should be converted to a TIA-input-referred noise current $i_{n,mix}^2$ as shown in Figure 6.24a by formula

$$v_{n,mix}^2 = \frac{v_{n,mix}^2}{Z^2} \quad (6.6)$$

where $Z$ is the transimpedance of the TIA.

Then the two TIA-input-referred mean square noise current, one from mixer, the
Figure 6.24: The TIA-input-referred mean square noise current of a TIA followed by a mixer: (a) Two separate input-referred noise current; (b) One overall input-referred noise current

other from TIA itself, can be added to get the overall input-referred noise current $\overline{i_{n,all}^2}$ as shown in Figure 6.24b. So

$$\overline{i_{n,all}^2} = \overline{i_{n,TIA}^2} + \overline{i_{n,mix}^2} \quad (6.7)$$

The overall noise performance of two types of TIA-mixer combinations can be calculated according to equations above. One combination is a 45 dBΩ TIA together with the high-input-linearity but low-gain mixer designed in this chapter; the other combination is a 25 dBΩ TIA together with the low-input-linearity but high-gain mixer designed in previous chapter.

Table 6.4: Noise calculation of two types of TIA, mixer combination

<table>
<thead>
<tr>
<th>TIA $Z$ (dBΩ)</th>
<th>$R_{FB}$ (Ω)</th>
<th>$\overline{i_{n,TIA}^2}$ (A$^2$)</th>
<th>Mixer $P_{1dB}$ (dBm)</th>
<th>Mixer NF (dB)</th>
<th>$\overline{i_{n,mix}^2}$ (V$^2$)</th>
<th>$\overline{i_{n,mix}^2}$ (A$^2$)</th>
<th>$\overline{i_{n,all}^2}$ (A$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>90</td>
<td>1.4 p</td>
<td>-5</td>
<td>25</td>
<td>$2.5 \times 10^{-7}$</td>
<td>8 p</td>
<td>9.4 p</td>
</tr>
<tr>
<td>33</td>
<td>22</td>
<td>5.7 p</td>
<td>-17</td>
<td>13</td>
<td>$1.5 \times 10^{-8}$</td>
<td>7.6 p</td>
<td>13.3 p</td>
</tr>
</tbody>
</table>
The last column of Table 6.4 gives the overall input-referred noise current for the two cases. The combination of a high-gain TIA together with a high-input-linearity but high-noise mixer has a smaller $i_{n,all}^2$ than the other combination which consists of a low-gain TIA followed by a low-input-linearity but low-noise mixer. This comparison verified that the mixer designed in this chapter doesn’t worsen the system noise performance of a proposed GPON receiver than the mixer designed in previous chapter, but actually improved it by 30%. Another benefit of using the mixer in this chapter is that the design of TIA in [58] can be kept without change.
Chapter 7

Demodulator Frontend Circuit

7.1 Introduction

A demodulator frontend chip consisting of two broadband, high-linear mixers, one quadrature Ring VCO, and two low-pass filters is described in this chapter. The design and the measurement of the fabricated chip is discussed.

7.2 Circuit Design

The block diagram of the frontend is shown in Figure 7.1

![Block diagram of a QPSK demodulator frontend](image)

Figure 7.1: The block diagram of a QPSK demodulator frontend

Mixer 1 and Mixer 2 are identical. They use the design from Chapter 5. The
CHAPTER 7. DEMODULATOR FRONTEND CIRCUIT

QVCO is a ring oscillator using the design from Chapter 4.

LPF 1 and LPF 2 are second order low-pass filters with LC ladder structure as shown in Figure 7.2.

\[ L = \frac{R_o L_k}{\omega_c} = \frac{50 \times 1.414}{2.5 \times 10^9/2\pi} = 4.45 \text{ nH} \quad (7.1) \]

\[ C = \frac{C_k}{R_o \omega_c} = \frac{1.414}{50 \times 2.5 \times 10^9/2\pi} = 1.8 \text{ pF} \quad (7.2) \]

where \( R_o \) is the source resistance of the filter which is 50 Ω, \( \omega_c \) is the cut-off frequency, and \( L_k, C_k \) are the element values in prototype.

The layout of the frontend with all the building blocks is shown in Figure 7.3.

7.3 Experimental Results

The frontend was fabricated in IBM CMOS 0.13 μm technology. A photograph of the total circuit of one ring QVCO, two mixers, and two LPFs is shown in Figure 7.4. The total chip area is 1 mm × 1 mm.

DC measurement showed that the whole circuit consumes 157 mW power, which consists of 70.4 mW from the QVCO, and 86.4 mW from the two mixers.

In the measurement setup, a QPSK signal is firstly generated as shown in the left part of the measurement setup diagram in Figure 7.5.
Figure 7.3: The layout of a QPSK demodulator frontend

Figure 7.4: Photograph of the fabricated CMOS QPSK demodulation front end
Figure 7.5: Demodulation setup to receive QPSK signal
The baseband data of I and Q channels come from two of the four channels of a pulse pattern generator (PPG)(Anritsu MP1775A). The pattern is set to be pseudorandom binary sequence (PRBS) with $2^7 - 1$ or $2^{31} - 1$ bits per pattern period. The symbol rate per channel is set at 2.5 GSym/s. The spectrum of one 2.5 Gb/s PRBS baseband NRZ signal with 0.25 Vp-p is shown in Figure 7.6.

![Figure 7.6: The spectrum of a 2.5 Gb/s PRBS baseband signal](image)

Passive mixers (ST STDB-2006-I MC) with 6 dB loss are used for frequency up-conversion. The in-phase LO is a 3-dB-divided sinusoidal signal at 5 GHz from a signal generator, and the quadrature LO is another portion of the divided signal passing through a 90° phase shifter. The generated QPSK signal has a spectrum shown in Figure 7.7.

At the receiver, an on-chip ring oscillator generates an in-phase differential LO carriers for down conversion of in-phase channel (I channel), and a quadrature differential LO carriers for down conversion of quadrature channel (Q channel). To make sure the LOs have exact same frequency as the carrier used in QPSK generation, the output port of the in-phase negative (I-) LO is injected with a portion of the carrier signal from the signal generator used at transmitter. The effect of this injection lock can be demonstrated by observing a stable and strong 5 GHz oscillating frequency in
Figure 7.7: Spectrum of a generated QPSK signal with 2.5 Gb/s data rate per channel

The input RF signal, and the LOs get mixed in two on-chip mixers. The downconverted products as well as the unwanted up-converted products pass through on-chip low-pass filters before they come to the output ports of the chip. Since the up-converted products are filtered out by the filters, the remained are the wanted demodulated signal. The spectrum of the demodulated signal of Q channel is shown

Figure 7.8: The spectrum of the signal out of in-phase positive (I+) LO port
in Figure 7.9. The signal of I channel has a same spectrum.

Figure 7.9: The spectrum of the demodulated signal in Q channel

If there is no injection lock, the LO generated from the free-running ring oscillator will jump around the center frequency. The demodulated signal spectrum under such condition is shown in Figure 7.10.

Figure 7.10: The spectrum of the demodulated signal without injection lock

The time-domain measurement was not taken since the oscilloscope was broken and sent for repair. But a time-domain simulation was done in Matlab. A matlab code
was used to simulate the performance of the designed frontend when it is integrated into a Costas loop for carrier recovery and QPSK demodulation. The simulation results include the phase error, the instantaneous frequency, and eye diagrams of demodulated signal. A discussion of the Costas loop principle, a proposal of the experiment setup, and the results of the Matlab simulation are put in Appendix A.

### 7.4 Summary

A CMOS QPSK demodulator frontend with two broadband and high-linear mixers, one quadrature VCO, and two second-order low-pass filters is designed and fabricated in CMOS 0.13 µm technology. The demodulator receives a broadband RF input which comes from a 5 GHz carrier QPSK modulated by two-channel baseband data, each with 2.5 GSym/s. Thus, such demodulator provides a demodulation for 5 Gb/s baseband data. The measurement shows that the spectrum of the received baseband data is the same as that transmitted, which indicates an expected down conversion. The whole circuit with pads takes 1 mm² area and consumed 157 mW power.
Chapter 8

Conclusions and Future Work

8.1 Summary and conclusion

A CMOS integrated transceiver is attractive for cost-sensitive and broadband GPON access network. OSBM modulation which up converts the downstream baseband data to be a sideband signal can minimize its crosstalk with the upstream baseband data. In this thesis, a QPSK demodulator frontend aiming at down converting the OSBM sideband signal back to baseband was designed, fabricated in CMOS 0.13 μm technology. The chip has been measured and verified.

The thesis’s investigation began with a comparison of the topologies of quadrature VCO. A LC oscillator and a ring oscillator both centered at 5 GHz were separately discussed. The LC oscillator uses two cross-coupled LC cells, each containing a spiral inductor and a varactor as a resonance tank. These two cells are coupled strong enough to each other to force a quadrature phase relationship. The measurement of a fabricated LC oscillator chip showed a tuning range of 3 GHz, which is 52% of the central frequency, and a phase noise of -100.8 dBC/Hz at 1MHz offset. The ring VCO, on the other hand, uses two delay stages consisting of only active transistors. The parasitic capacitances from active devices and interconnection wires were minimized for high oscillation frequency. The measurement of a ring oscillator which is a part of
a fabricated demodulator frontend showed a tuning range of 4 GHz, which is 89% of the central frequency, and a phase noise of -81 dBc/Hz at 1 MHz offset. Apparently, the LC oscillator has a 20 dB better phase noise. However, it takes huge area, i.e. 0.15 mm$^2$, comparing to 0.019 mm$^2$ of ring oscillator. Since lowering cost has high priority for FTTH/FTTP GPON tranceivers, the topology of ring oscillator was chosen for frontend integration.

Then the effort were put on the design of mixers. Two types of broadband mixers were separately presented, one with high gain and the other with high linearity. In both mixers, input and output impedance are matched to 50 ohms from 2 GHz to 8 GHz, Gilbert cell is used to isolate the LO to RF feedthrough to avert the risk of self-mixing, and current bleeding mechanism is adopted to minimize the flicker noise as well as boosting the conversion gain. The first mixer has a conversion gain of 8.5 dB and an input 1 dB compresion point at -17 dBm. The second mixer obtained high linearity by resistive source degeneration, and got better gain flatness by adding a capacitive peaking mechanism. It has a conversion gain of -7 dB with an on-chip buffer or -2.1 dB without buffer, but an input 1 dB compresion point at -5 dBm.

Lastly, a demodulator frontend integrating two broadband and high-linear mixers, one quadrature ring VCO, and two second-order low-pass filters was designed and fabricated. The demodulator can receive a broadband RF input. This input comes from a 5 GHz carrier which is QPSK modulated by two baseband-data channels, each of 2.5 GSym/s. Thus, this frontend is capable of demodulating 5 Gb/s QPSK signal.  The measurement shows that the spectrum of the demodulated baseband signal is the same as that of the data out of the pulse pattern generator, which indicates a correct down conversion. The whole frontend circuit including pads takes 1 mm$^2$ area and consumed 157 mW power.
8.2 Future work

There are many interesting aspects for future investigations based on this demodulator frontend. The phase noise of the ring oscillator could be improved by carefully studying the noise sources, and then optimizing device dimensions or circuit topology to suppress those sources.

If the phase noise performance of a VCO is crucial for an application, LC oscillator is suggested. The LC QVCO in Chapter 3 can be further optimized in term of phase noise. One possible improvement is to use complementary LC VCO [14] [15], which stacks PMOS cross-coupled transistors on top of the current tank and NMOS cross-coupled transistors to enhance the symmetry of the output wave. Some other methods to optimize the second-harmonic waveform at the common source of the NMOS cross-coupled transistors like switched biasing transistors [53], passive superharmonic coupling [54], or active superharmonic coupling [63] can improve the phase noise performance as well.

For broadband mixers in Chapter 5 and Chapter 6, the common-gate common-source active balun at the front stage could be further investigated to exploit its potential to provide noise canceling function [64] in addition to current functions of single-end to differential conversion and input matching. The linearity of the resistive-degenerated Gilbert cell can be further enhanced by a harmonic distortion canceling technique using another common-gate common-source configuration [60]. The improved linearity can save several dB conversion gain which is otherwise sacrificed by only using the resistive degeneration. The increased gain will improve the noise performance of the mixer, whose noise contribution dominates the overall noise of the OSBM receiver frontend (TIA and mixer) as indicated in the noise analysis in Table 6.4. Minimizing the noise of the mixer is an effective way to improve the receiver’s sensitivity.

Passive mixers [41] provide another structure for broadband and high linearity
mixer design. It is promising to boost the conversion gain by several dB compared to the current Gilbert-cell based design in Chapter 6 while keep the same input 1dB compression point.

The two spiral inductors used in the low-pass filters take more than 40% of the chip area. To make a CMOS transceiver more attractive from cost perspective, active inductors which are smaller than passive spiral ones in an order of magnitude are well worth trying. The 3-dB bandwidth of current LPF is 2.5 GHz for a baseband signal of 2.5 GSym/s, but the optimal ratio of 3-dB bandwidth to baseband bandwidth is 0.7 [58], which makes a better balance between noise contribution and intersymbol interference (ISI). So in future, the bandwidth of low-pass filters can be designed to be $2.5 \times 0.72 = 1.8$ GHz.

DC offset issue in this direct down conversion application is not much addressed. A future investigation on the effect of a DC offset and on a mechanism to remove that DC offset is believed to be helpful to improve the demodulation performance.

Lastly, integrating the frontend in a Costas loop to measure the QPSK demodulation performance, and further integrating the Costas loop with clock recovery and data recovery circuits to make a full receiver is a more convincing demonstration of the concept of a low-cost OSBM transceiver for FTTH/FTTP.
References


REFERENCES


REFERENCES


REFERENCES


REFERENCES


REFERENCES


[57] *Gigabit-capable Passive Optical Networks (GPON): Physical Media Dependent (PMD) layer specification*, ITU Std.


Appendix A

Costas Loop

A.1 Mathematical Basics

A four-phase Costas loop as shown in Figure A.1 is a phase-locked loop (PLL) which can be used for carrier recovery in a QPSK demodulator.

\[ s(t) = x(t) \cos(\omega_{RF} t + \theta) - y(t) \sin(\omega_{RF} t + \theta) \]  

Figure A.1: A block diagram of a four-phase Costas Loop

Suppose the input signal \( s(t) \) is
where \(x(t)\) and \(y(t)\) are baseband signal belonging to the set of \(\{\pm 1\}\), \(\omega_{RF}\) is the RF carrier frequency, and \(\theta\) is the the phase angle of the carrier.

The input signal is first down-converted to baseband by two mixers, a QVCO, and two low-pass filters. Suppose the LO signals from the QVCO are \(\cos(\omega_{RF}t + \hat{\theta})\) and \(\sin(\omega_{RF}t + \hat{\theta})\), where \(\hat{\theta}\) is the phase angle of the LO signals. The down-converted signals are

\[
\begin{align*}
s'_i(t) &= K_{d1}x(t)\cos(\theta - \hat{\theta}) - K_{d1}y(t)\sin(\theta - \hat{\theta}) \\
s'_q(t) &= -K_{d1}x(t)\sin(\theta - \hat{\theta}) - K_{d1}y(t)\cos(\theta - \hat{\theta})
\end{align*}
\]

where \(K_{d1}\) is the conversion gain of the down-conversion mixers.

Then the baseband signals in each channel are multiplied by the limiting-amplified signal from the other channel, before they get subtracted. If the limiting amplifier is modeled as a \(K_{d2}\)sgn function, where \(K_{d2}\) is the output amplitude of the limiting amplifier, then the error signal is

\[
e(t) = K_{d2}s'_i(t)\text{sgn}[s'_q(t)] - K_{d2}s'_q(t)\text{sgn}[s'_i(t)].
\]

If the phase difference between RF carrier and LO, \((\theta - \hat{\theta})\), is within \((-\frac{\pi}{4}, \frac{\pi}{4})\), then the error signal will be

\[
e(t) = K_{d2}s'_i(t)(-y(t)) - K_{d2}s'_q(t)(x(t)),
\]

which can be reduced to

\[
e(t) = 2K_{d1}K_{d2}\sin(\theta - \hat{\theta}).
\]

The filtered error signal drives the VCO to change LO frequency and phase. As the phase difference \((\theta - \hat{\theta})\) decreases to zero, the system is locked, and the carrier is recovered.
A.2 An experiment proposal

An quadrature VCO, two down-conversion mixers, and two low-pass filters following mixers are integrated in a CMOS chip described in Chapter 7. Other components including two limiting amplifiers, two multipliers, one subtracter, and one loop filter are implemented on printed circuit boards (PCBs).

Each of the limiting amplifiers is outsourced from MAXIM as shown in Figure A.2. It is an evaluation board of MAX3747A, a limiting amplifier whose bandwidth is from 155 Mbps to 3.2 Gbps, and whose differential output voltage is $800 \, \text{mV}_{P-P}$. The board has differential inputs and differential outputs. But in case of single-ended input and signal-ended output, the negative input and output ports can be simply grounded.

![Figure A.2: Picture of a limiting amplifier PCB](image)

Each multiplier is an outsourced evaluation board of AD8342 from Analog Devices. Its picture is shown in Figure A.3. It has broadband RF, LO, and IF ports from low frequency (10 MHz) to 3 GHz. The conversion gain is 3.7 dB, the IP1dB is 8.3 dBm, and the LO drive can be as small as -10 dBm. The board has single-ended input and
The subtracter and loop filter are in-house designed on a PCB board. The schematic of the design is indicated in Figure A.4. It consists of three stages. The first stage implements the subtraction function between the two signals feeding the inverting and non-inverting ports of the first operational amplifier (OP-AMP). Four resistors have resistances $R_1 = R_2 = R_3 = R_4$. The second stage is an active filter with an inverting-configurated OP-AMP. The values of $R_5$, $R_6$, $R_9$, and $C_1$ are critical because they determine not only the characteristics of the loop filter, but also the loop performance of the whole Costas loop. The selection of these values can be based on a system simulation in Matlab described in the following section. The third stage is a DC level shifter, which provides a bias voltage $V_{ref}$ for QVCO on chip. Again, the resistances $R_7 = R_8 = R_{10} = R_{11}$.

The fabricated subtractor-n-loop-filter PCB together with soldered components are shown in Figure A.5.

All components described above can be linked to form a Costas loop, which can be used as a QPSK demodulator. A proposed experiment setup to measure the Costas loop performance is shown in Figure A.6. Besides the Costas loop, a QPSK signal...
Figure A.4: The schematic of a subtracter and a loop filter on a PCB

Figure A.5: The PCB assembly of a subtractor and loop filter
APPENDIX A. COSTAS LOOP

has to be generated first. As shown in Figure A.7, the baseband data of I and Q channels come from two of four channels of a pulse pattern generator (PPG) (Anritsu MP1775A). The pattern can be set to pseudorandom binary sequence (PRBS) with $2^7 - 1$ or $2^{31} - 1$ bits per pattern period. The symbol rate per channel can be set at 2.5 GSym/s. Passive mixers (ST STDB-2006-I MC) with 6 dB loss can be used for frequency up-conversion. The in-phase LO is a 3-dB-divided sinusoidal signal at 5 GHz from a signal generator, and the quadrature LO is another portion of the divided signal passing through a 90° phase shifter. The phases of RF carrier and baseband data are synchronized by connecting the 10 MHz reference ports from signal generator to PPG. Since the carrier and the data have same clock at transmitter, the carrier recovered by Costas loop at receiver can be used to recover the clock by just dividing the carrier frequency by 2.

A.3 Matlab Simulation

The performance of the Costas loop was simulated using Matlab. The simulation code was developed by a researcher in Very-high-speed-circuit Research Group. The simulation is in time domain and includes every step in the signal flow from QPSK signal generation to the demodulation of each channel. The input to the simulator includes the data rate, frequency arrangement, modulation type, and characteristics of each component, such as the conversion gain of mixers, the transfer function of QVCO, the bandwidth and cut-off frequency of LPF, and the open-loop gain and the output resistance of the OP-AMP. The output includes deduced component values for the active loop filter, i.e. the values of R5, R6, R9, and C1 in the aforementioned subtracter and loop-filter PCB, a transient plot of the phase error between the phase of the QVCO and the phase of the carrier, a plot of the frequency of QVCO in loop, and the eye diagrams of each demodulated channel.

The symbol rate was chosen at 2.5 GSym/s, the carrier frequency at 5 GHz, and
Figure A.6: A proposal of measurement setup for Costas loop
modulation type as QPSK. Other inputs were set such as component characteristics of the on-chip frontend in Chapter 7, and those of PCB circuits described in section A.2. The loop response was tested under a phase step stimulus or a frequency step stimulus from the QVCO. The resultant transient response and the eye diagram showed that the Costas loop with designed components is able to recover a phase step within $[-46^\circ, 43^\circ]$, or a frequency step within $[-100 \text{ MHz}, 100 \text{ MHz}]$ from the VCO.

The tracking behavior of the loop after a 100 MHz frequency step of the QVCO can be observed by the instantaneous phase error between the phase of the QVCO and the phase of carrier, which is shown in Figure A.8. The VCO frequency step response can be seen in Figure A.9. The frequency step and phase error can be recovered after 15 ns by the loop.

The eye diagrams of the in-phase (I) channel and quadraute (Q) signals before they reach the limiting amplifiers ($s'_i(t)$ and $s'_q(t)$ in Figure A.1) are shown in Figure A.10, which shows widely opened eyes.
Figure A.8: The phase error in the Costas loop after a 100 MHz frequency step

Figure A.9: The VCO frequency recovery in the Costas loop after a 100 MHz frequency step
Figure A.10: The eye diagram of I and Q channels of the Costas loop after a frequency recovery of a 100 MHz VCO frequency step: (a) I channel; (b) Q channel