TOPOLOGIES AND MODELINGS OF NOVEL BIPOLAR GATE DRIVER TECHNIQUES FOR NEXT-GENERATION HIGH FREQUENCY VOLTAGE REGULATORS

by

Jizhen Fu

A thesis submitted to the
Department of Electrical and Computer Engineering
in conformity with the requirements for
the degree of Master of Applied Science

Queen’s University

Kingston, Ontario, Canada

July, 2010

Copyright © Jizhen Fu, 2010
Abstract

As is predicted by Moore’s law, the transistors in microprocessors increase dramatically. In order to increase the power density of the microprocessors, the switching frequency of the Voltage Regulator (VR) is expected to increase to MHz level. However, the frequency dependent loss will increase proportionally. In order to meet requirements of the next-generation microprocessors, three new ideas are proposed in this thesis.

The first contribution is a new bipolar Current Source Driver (CSD) for high frequency power MOSFET. The proposed CSD alleviates the gate current diversion problem of the existing CSDs by clamping the gate voltage to a flexible negative value during turn off transition. Therefore, the proposed driver turns off the MOSFET much faster. For buck converters with 12 V input at 1MHz switching frequency, the proposed driver improves the efficiency from 80.5% using the existing CSD to 82.5% at 1.2V/30A, and at 1.3V/30A output, from 82.5% to 83.9%.

The second contribution is an accurate analytical loss model of a power MOSFET with a CSD. The current diversion problem that commonly exists in CSDs is investigated mathematically. The inductor value of the CSD is optimized to achieve minimum loss for the synchronous buck converter. The experimentally measured loss matches the calculated loss very well. The efficiency with the optimal CSD inductor is improved from 86.1% to 87.6% at 12V input, 1.3V/20A output in 1MHz switching frequency and from 82.4% to 84.0% at 1.3V/30A output.

The third contribution is a new inductorless bipolar gate driver for control FET of buck converters. The most important advantage of the driver presented in this thesis is that it can turn off the power MOSFETs with a negative voltage, which will significantly reduce the turn off time and thus switching loss. In addition, the proposed bipolar gate driver has no inductor in the driver circuit; therefore it can be fully integrated into a chip. For buck converter with 5V input,
1.3V/25A load, in 2 MHz frequency, the proposed gate driver increases the efficiency from 75.8% to 77.8% and from 72.9% to 76.5% at 5V input, 1.3V/25A load, in 2.5 MHz switching frequency.
Acknowledgements

First, I would like to thank my supervisors, Dr. Yan-Fei Liu and Dr. P. C. Sen for their support, guidance and stimulation throughout this thesis project. Their vision and experience is of great help to my study for the past two years.

In addition, I would like to thank Kai Xu and his wife for their thoughtful welcome when I landed on Canada for the first time. In particular, I want to thank Dr. Zhiliang Zhang for his valuable help and encouragement during my first year in Queen’s. Discussions with Dr. Dong Wang, Liang Jia and Andrew Dickson on the fundamental theory and experimental implementation were also very inspirational. Communications with Ali Moallem, Darryl Tschirhart, Dr. Eric Meyer, and Dr. Wilson Eberle on many topics on Power Electronics were also a great help. As well, I hope to thank all the ECE staff members for their kind help.

I would thank all my new friends at Kingston and old friends back in China. For different stages of my life, I have been lucky to gain unselfish help, which makes me always willing to offer my hands whenever possible.

Financial support in the form of scholarships and teaching assistantship from Queen’s University (Queen’s Graduate Awards) is gratefully acknowledged. Travel grants from IEEE Power Electronics Society and Power Sources Manufactures Association are greatly appreciated.

Finally, special thanks are reserved for my family members: my mother, Yunxiang Zhang; my father, Hao Fu; my sister, Jianying Fu and my wife, Shuai Wan. Without their understanding and encouragement, I would not have completed this degree.
For The Ones

Who Love Me

And/Or

Who I Love
Table of Contents

Abstract............................................................................................................................................. i
Acknowledgements.........................................................................................................................iii
List of Figures .................................................................................................................................. viii
List of Tables ..................................................................................................................................... xii
Chapter 1 Introduction ..................................................................................................................... 1
  1.1 Introduction............................................................................................................................... .1
  1.2 Introduction to Switched-Mode Power Supplies ................................................................. 1
  1.3 Research Trends for Voltage Regulators (VRs) ............................................................... 3
  1.4 Losses of Power MOSFET ........................................................................................................ 6
    1.4.1 Conduction Loss ................................................................................................................. 6
    1.4.2 Switching Loss .................................................................................................................... 6
    1.4.3 Gate Drive Loss .................................................................................................................. 8
    1.4.4 Output Loss ......................................................................................................................... 9
  1.5 Introduction to Existing Gate Drivers ....................................................................................... 9
    1.5.1 Conventional Voltage Source Driver .................................................................................. 9
    1.5.2 Resonant Gate Driver ........................................................................................................ 12
    1.5.3 Existing Current Source Drivers ....................................................................................... 14
  1.6 Research Motivation ................................................................................................................ 17
  1.7 Thesis Outline .......................................................................................................................... 18
Chapter 2 A New High Efficiency Current Source Driver with Bipolar Gate Voltage ............... 20
  2.1 Introduction.............................................................................................................................. 20
  2.2 The Proposed Bipolar Current Source Driver Circuit ......................................................... 20
    2.2.1 The Proposed Bipolar Current Source Driver ................................................................. 20
    2.2.2 Detailed Turn On Operation ............................................................................................. 22
    2.2.3 Detailed Turn Off Operation ........................................................................................... 25
  2.3 Advantages of the Proposed Bipolar CSD ............................................................................. 28
    2.3.1 Significantly Reduced Turn Off Time and Thus Turn Off loss ....................................... 28
    2.3.2 Less Impact of Parasitic Inductance ................................................................................. 31
    2.3.3 Smaller Current Source Inductor ...................................................................................... 31
    2.3.4 High Stability and Noise Immunity ................................................................................. 31
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1.1 Bipolar Current Source Driver</td>
<td>102</td>
</tr>
<tr>
<td>5.1.2 Accurate Switching Loss Model and Optimal Design of a Current Source Driver</td>
<td>103</td>
</tr>
<tr>
<td>5.1.3 A New Inductorless Bipolar Gate Driver</td>
<td>104</td>
</tr>
<tr>
<td>5.2 Future Work</td>
<td>105</td>
</tr>
<tr>
<td>5.2.1 Current Source Driver Circuits</td>
<td>105</td>
</tr>
<tr>
<td>5.2.2 Inductorless Bipolar Gate Driver Circuits</td>
<td>105</td>
</tr>
<tr>
<td>References</td>
<td>106</td>
</tr>
</tbody>
</table>
List of Figures

Figure 1.1  The number of transistor integrated on the die of Intel microprocessor ......................... 4
Figure 1.2  Current and voltage prediction for Integrated Circuits ................................................... 5
Figure 1.3  Turn on and turn off waveforms of power MOSFET ..................................................... 7
Figure 1.4  Power MOSFET and common source driver  $L_s$ ........................................................... 8
Figure 1.5  Conventional VSD with power MOSFET and its associated parasitic ......................... 10
Figure 1.6  Switching waveforms of power MOSFET driven by the conventional VSD .............. 11
Figure 1.7  Equivalent circuit of the MOSFET driven by VSD during turn off transition ............ 12
Figure 1.8  Resonant transition gate drive circuit and key waveforms .......................................... 13
Figure 1.9  Resonant gate driver with two diodes .......................................................................... 13
Figure 1.10  Topology of the CSD reported in [35] ........................................................................ 15
Figure 1.11  Simplified discharging circuit of existing CSD in [35] .............................................. 15
Figure 1.12  Equivalent circuit of the CSD in [35] after $D_4$ is on ................................................ 16
Figure 1.13  Simulation waveforms of turn off transition of CSD in [35] .................................... 17
Figure 2.1  Power MOSFET driven by the proposed bipolar CSD .............................................. 21
Figure 2.2  Waveforms of the proposed bipolar CSD ...................................................................... 22
Figure 2.3  Turn on operation ........................................................................................................ 24
Figure 2.4  Turn off operation ....................................................................................................... 28
Figure 2.5  Simulation waveforms of turn off transition of the proposed CSD .......................... 29
Figure 2.6  Comparison of the simulated current fall time ............................................................ 29
Figure 2.7  Comparison of the average discharging current ....................................................... 30
Figure 2.8  New bipolar CSD with improved turn on gate current ............................................... 32
Figure 2.9  Improved dual channel Bipolar CSD with continuous inductor current mode .......... 33
Figure 2.10  Improved bipolar CSD working with continuous inductor current mode ............. 33
Figure 2.11  Improved bipolar CSD working with discontinuous inductor current mode .......... 34
Figure 2.12 Buck converter with the proposed bipolar CSD ................................................. 34
Figure 2.13 Photo of prototype with the proposed bipolar CSD ............................................. 36
Figure 2.14 Hardware implementation of the buck converter driven with the proposed CSD .... 36
Figure 2.15 Driver switch gate signals ($V_{GS1}$-$V_{GS5}$) ......................................................... 37
Figure 2.16 $V_{GS,Q1}$ and CSD inductor current $I_{Lr}$ ............................................................. 38
Figure 2.17 $V_{GS,Q1}$ and $V_{GS,Q2}$ ..................................................................................... 39
Figure 2.18 Efficiencies at 12V input, 1.2V and 1.3V output, 1MHz switching frequency ....... 39
Figure 2.19 Measured efficiency comparison at 12V input, 1.2V output, 1MHz switching frequency ...................................................................................................................... 40
Figure 2.20 Total measured loss comparison at 12V input, 1.2V output, 1MHz switching frequency ...................................................................................................................... 41
Figure 2.21 Measured efficiency comparison at 12V input, 1.3V output, 1MHz switching frequency ...................................................................................................................... 42
Figure 2.22 Total measured loss comparison at 12V input, 1.3V output, 1MHz switching frequency ...................................................................................................................... 43
Figure 3.1 Equivalent circuit of MOSFET with the proposed CSD ....................................... 46
Figure 3.2 MOSFET Switching Transition Waveforms ......................................................... 47
Figure 3.3 Turn on operation ................................................................................................. 52
Figure 3.4 Turn off operation .............................................................................................. 55
Figure 3.5 Total Loss VS. Current Source Inductor .............................................................. 58
Figure 3.6 Peak current VS. Current Source Inductor .......................................................... 58
Figure 3.7 Synchronous buck converter with the proposed CSD ........................................ 59
Figure 3.8 Photo of the buck converter driven with CSD shown in Figure 3.1 ................. 60
Figure 3.9 The waveforms of driver signals $V_{gs,Q1}$ and $V_{gs,Q2}$ ........................................ 60
Figure 3.10 Efficiencies of 1MHz, 750kHz, 500kHz for 12V input, 1.3V output ................. 61
Figure 3.11 Efficiencies of 1.2V, 1.3V, 1.5V output for 12V input, 1MHz frequency ............ 62
Figure 3.12 The current ripple of the output inductor of the buck converter .................... 63
Figure 3.13  Comparison between measured loss and calculated loss........................................... 65
Figure 3.14 Calculated loss breakdown of the synchronous buck converter ................................. 66
Figure 3.15 Polynomial fittings of the switching loss for Control FET......................................... 67
Figure 3.16 Equivalent switching circuits when drain current rises and drops......................... 67
Figure 3.17 Calculated switching loss comparison between the proposed CSD (Figure 3.1), existing CSD [44] and VSD................................................................. 69
Figure 3.18 Calculated total loss comparison between proposed CSD (Figure 3.1), existing CSD [44] and VSD ................................................................................................................................. 69
Figure 3.19 Efficiency comparison for different CSD inductors at 12V input, 1.3V output, 1MHz ............................................................................................................................... 70
Figure 3.20 Comparison between optimized CSD and DrMOS from Renesas ............................. 71
Figure 3.21 Comparison between optimized CSD and DrMOS from IR ...................................... 72
Figure 4.1 Conventional VSD with power MOSFET and its associated parasitics....................... 75
Figure 4.2 Switching waveforms of power MOSFET driven by the conventional VSD............ 75
Figure 4.3 Equivalent circuit of the MOSFET driven by VSD during turn off transition .......... 76
Figure 4.4 Topology of the proposed inductorless bipolar gate driver .......................................... 77
Figure 4.5 Driver signals and switching waveforms of $Q_1$ ............................................................ 78
Figure 4.6 Equivalent circuit for $C_1$ being charged to $V_{C1}$ ....................................................... 79
Figure 4.7 Turn on operation ......................................................................................................... 84
Figure 4.8 Equivalent circuit for $C_2$ being charged to $(V_{DS}-V_{D1})$ .................................... 85
Figure 4.9 Turn off operation.................................................................................................... 89
Figure 4.10 Comparison of the calculated switching loss between the proposed driver and conventional driver ................................................................. 91
Figure 4.11 Simulated waveforms of power MOSFET driven by conventional driver ............ 92
Figure 4.12 Simulated waveforms of power MOSFET driven by the proposed driver .......... 92
Figure 4.13 Comparison of the simulated turn off loss between the proposed driver and conventional driver .......................................................................................................................... 93
Figure 4.14 Picture of the synchronous buck converter driven with the proposed driver ....... 94
Figure 4.15 Waveforms of $V_{GS, S1}, V_{GS, S2}, V_{GS, Q2}$ ................................................................. 95

Figure 4.16 Bipolar Gate Driver signal for $Q1$: $V_{GS, Q1}$ ........................................................................... 95

Figure 4.17 The drain-to-source voltage of $Q2$: $V_{DS, Q2}$ ........................................................................ 96

Figure 4.18 Picture of the buck converter driven with conventional driver ................................................. 97

Figure 4.19 Efficiency Comparison at 2MHz between the proposed driver and conventional driver .......................................................................................................................... 97

Figure 4.20 Measured loss comparison at 2MHz between the proposed driver and conventional driver .......................................................................................................................... 98

Figure 4.21 Efficiency Comparison at 2.5MHz between the proposed driver and conventional driver .......................................................................................................................... 99

Figure 4.22 Measured loss comparison at 2.5MHz between the proposed driver and conventional driver .......................................................................................................................... 100
List of Tables

Table 2.1 Comparison of VSD, existing CSD and the proposed CSD during turn off transition.. 30

Table 2.2 Design Parameters ......................................................................................................... 35
## List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Capacitor</td>
</tr>
<tr>
<td>$C_b$</td>
<td>Bootstrap capacitance</td>
</tr>
<tr>
<td>$C_{dsi}$</td>
<td>MOSFET parasitic drain-to-source capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_f$</td>
<td>Converter powertrain output filter capacitance</td>
</tr>
<tr>
<td>$C_g$</td>
<td>MOSFET total parasitic gate capacitance</td>
</tr>
<tr>
<td>$C_{gdi}$</td>
<td>MOSFET parasitic gate-to-drain capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_{gsi}$</td>
<td>MOSFET parasitic gate-to-source capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_{issi}$</td>
<td>MOSFET parasitic input capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$C_m$</td>
<td>Magnetic core loss constant</td>
</tr>
<tr>
<td>$C_{ossi}$</td>
<td>MOSFET parasitic output capacitance, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$d$</td>
<td>MOSFET drain terminal</td>
</tr>
<tr>
<td>$d_i$</td>
<td>MOSFET drain terminal, where $i$ corresponds to the MOSFET number</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>$D_i$</td>
<td>Diode, where $i$ corresponds to the diode number</td>
</tr>
</tbody>
</table>
$D_f$  
Bootstrap diode

$f_s$  
Switching frequency

$g_{i}$  
MOSFET gate terminal, where $i$ corresponds to the MOSFET number

$g_{fs}$  
MOSFET transconductance

$i_d$  
MOSFET drain current

$i_g$  
Gate drive current

$I_o$  
Load current

$I_{off}$  
Current at turn off

$I_{on}$  
Current at turn on

$M_i$  
ith power MOSFET, ($i=1,2,3,...$)

$P_{cond}$  
Total conduction loss

$P_g$  
MOSFET gate loss

$Q_{rr}$  
Reverse recovery charge

$R_i$  
ith resistor, ($i=1,2,3,...$)

$R_{ac}$  
AC resistance

$R_{dc}$  
DC resistance

xiv
$R_{DS(on)}$ MOSFET on resistance

$R_g$ MOSFET internal gate resistance

$S$ MOSFET source terminal

$S_i$ MOSFET source, where $(i=1,2,3,\ldots)$ is the MOSFET number

$t$ time

$T_s$ Switching period

$v_{ds}$ Drain-to-source-voltage

$v_{gs}$ MOSFET gate-to-source voltage

$v_o$ Output voltage

$V_b$ Blocking capacitor voltage

$V_{cc}$ MOSFET driver supply voltage

$V_{core}$ Volume of the core

$V_{ds}$ Drain-to-source voltage

$V_F$ Diode forward voltage drop

$V_{in}$ Input voltage

$V_o$ Average output voltage

$V_{pl}$ MOSFET plateau voltage
$V_{th}$ MOSFET threshold voltage

Abbreviations

BJT Bipolar Junction Transistor

VSD Voltage Source Driver

CSD Current Source Driver

IC Integrated Circuits

MOSFET Metal Oxide Silicon Field Effect Transistor

PCB Printed Circuit Board

PWM Pulse Width Modulation

RMS Root Mean Square

SR Synchronous Rectifier

VR Voltage Regulator

ZCS Zero Current Switching

ZVS Zero Voltage Switching

Prefixes for SI Units
p  Pico \((10^{-12})\)
n  Nano \((10^{-9})\)
\(\mu\)  Micro \((10^{-6})\)
m  Milli \((10^{-3})\)
k  Kilo \((10^{3})\)
M  Mega \((10^{6})\)

SI Units

A  Amperes
F  Farads
H  Henries
Hz  Hertz
s  seconds
V  Volts
W  Watts
\(\Omega\)  Ohm
Chapter 1 Introduction

1.1 Introduction

Firstly, this chapter briefly introduces the general theory of the switched-mode power supply. Then the recent trend for a Voltage Regulator (VR) is explained. In addition, the loss mechanism of power MOSFET is addressed. The basic operation principle and limitations of the conventional Voltage Source Driver (VSD), Resonant Gate Drivers (RGDs) and existing Current Source Drivers (CSDs) are also analyzed, based on which the motivation of this thesis is illustrated. This section lays the groundwork for the material presented in Chapter 2 to 4, which focus on a new bipolar CSD, an analytic switching loss model and optimal design of the bipolar CSD and a new inductorless bipolar gate driver. Chapter 5 concludes the work of this thesis and presents the topics for future work.

1.2 Introduction to Switched-Mode Power Supplies

Due to its advantages such as high efficiency, light weight, switched-mode power supply (SMPS) finds wide applications in various environments. Nowadays, SMPS is becoming more and more important – the applications of SMPS have been widespread in every corner of our daily life: computer, automobile, telecommunication, transportation, medical equipments and etc. The SMPS related industries have taken over more than 10 Billions economies in all over the world. ([1]) In this section, the general aspects of SMPS will be explained.

Switched-mode power supply, by definition, is a power supply unit that converts the electric energy from one form to another using the semiconductor-based power converters. In SMPS, the semiconductor components are continuously controlled on and off with high frequency to implement the conversion of the electric energy.
According to the forms of the input and output voltage, SMPS can be categorized into the following four types:

1. AC to AC (also cyclo – converter)
2. AC to DC (also rectifier)
3. DC to DC
4. DC to AC (also inverter)

SMPS can also been classified into isolated topology and non-isolated topology according to the circuit topology of the SMPS. Isolated circuits, such as flyback converter, forward converter, push-pull converter and etc, normally include transformer. While non-isolated topologies are rarely consist of transformer. Examples of non-isolated topologies are buck converter, boost converter, buck-boost converter, cuk converter and so on.

Generally speaking, there are two major operating modes of the SMPS: Pulse – Width – Modulation (PWM) mode and resonant mode. For SMPS with PWM mode, the output voltage is controlled by varying the duty cycle of the converter. While for SMPS topologies that are working in resonant mode, they can be classified into variable frequency control or constant frequency control. In variable frequency control, the output voltage is regulated by adjusting the operating frequency of the converter. While for constant frequency control, the operating frequency is constant – it regulates the output voltage either by adjusting the phase shift angle between different bridges or varying the duty cycle of the switches.

In a world with ever-diminishing fossil fuels, the demands for SMPS with high efficiency become more urgent. The reason why high efficiency is so important is that the lower efficiency means more loss is dissipated, and also means that a larger volume of heat sinks are needed. Therefore, improving the electrical efficiency has become a global issue that every researcher
around the world has to face. There are some voluntary incentive programs to promote high efficiency requirements for electrical equipment under various loads level. For example, some national mandatory requirements over efficiency of the electrical equipment have been carried out in China, Australia, USA and etc. Moreover, Energy Star Group proposed “80 Plus” standard, which specifies the efficiency requirement of 80+% at three load levels – 20%, 50%, and 100% as well as an input power factor of 0.9+.

There is another important parameter of evaluating the power supply – the total harmonic distortion (THD). THD means the ratio of the RMS value of the non-fundamental harmonics to the RMS value of the fundamental component. The lower THD means better performance, because that the higher THD means that more loss is dissipated on the line impedance.

1.3 Research Trends for Voltage Regulators (VRs)

Microprocessor industry takes up a large portion of the SMPS. As is known as Moore’s law, the number of transistors per chip will be doubled every 18 months. According to Figure 1.1, since 1971 when the first microprocessor- Intel’s 4-bit 4004 chipset- was released, the number of the transistors on the microprocessor has undergoing almost the same trend as predicted by the Moore’s Law.[2]
Figure 1.1 The number of transistor integrated on the die of Intel microprocessor

Following the Moore’s law, the load current keeps increasing as there is more and more transistor on chip and more and more load are connected in paralleled to meet the demands of the customers. In order to reduce the overall power dissipation, the voltage is kept being reduced. Therefore, the recent trend for next-generation microprocessor is larger load current and lower voltage. Figure 1.2 shows the current and voltage calculation prediction chart sourced by International Technology Roadmap for Semiconductors (ITRS) 2001. The latest microprocessor from Intel - VR 11.1 is operating under 0.8V. ([3])
With the number of the transistors on the microprocessor becoming larger and larger, power density is becoming a more and more important parameter of evaluating VRs. Recently, several research fields have been undergone to increase the power density of the VRs. One interesting area is to replace the magnetic-based converter with switched capacitor (also called charge pump) which consists of an inductorless configuration [4]. However, the large current spike, high EMI noise and narrow range of the voltage regulation limit the application of the switched capacitor ([5] - [7]).

Another interesting research field, which especially attracts the attention of semiconductor industries, is to achieve the full integration of the VRs into a single integrated chip, or called system-on-a-chip (SoC). ([8] - [10]) However, due to the tight cost requirement of the commercial products, the integration of the inductor with high current handling capability becomes the bottleneck of this area, limiting the present current level of the SoC under 12Ampere. ([11])

One of the practical ways is increasing the operating frequency of the VRs into MHz range to improve the dynamic performance and reduce the size of the passive components ([12] - [13]).
As the frequency increases, frequency dependent losses such as switching loss and gate drive loss become a penalty for VRs ([14] - [17]). The loss mechanism of the power MOSFET will be explained in Section 1.4.

### 1.4 Losses of Power MOSFET

There are four major types of losses associated with MOSFETs in switching converters: 1) conduction loss, 2) switching loss, 3) gate drive loss, and 4) $CV^2$ loss due to the output capacitance. These losses are discussed in the following sub-sections.

#### 1.4.1 Conduction Loss

In the on state, MOSFETs do not behave as an ideal switch with zero impedance, but they behave like a small resistance. This resistance is typically called the $R_{DS(on)}$ of the MOSFET. Typical values of $R_{DS(on)}$ for present day MOSFETs range from about 2mΩ to 100mΩ for MOSFETs with an off state voltage stress rating of 200V, or less. The conduction loss of a MOSFET is given by Equation (1.1).

$$ P_{con} = I_{DS_{RMS}}^2 * R_{DS(on)} $$  \hspace{1cm} (1.1)

where $I_{DS_{RMS}}$ is the RMS current of the MOSFET drain current.

#### 1.4.2 Switching Loss

Switching loss is the dominant loss in a high frequency synchronous buck converter. MOSFET turn on and turn off transitions are illustrated in Figure 1.3. Switching loss occur during both turn on ($t_1$~$t_3$) and turn off ($t_5$~$t_7$) transitions where neither $V_{DS}$ nor $I_{DS}$ is zero.
Normally, the piecewise linear approximation of the MOSFET turn on and turn off waveforms is usually made for simplifying the switching loss model. ([18]) Turn on switching loss, $P_{on}$, can be expressed in Equation (1.2):

$$P_{on} = \frac{V_{DS}}{2} \cdot I_{DS} \cdot (T_3 - T_4) \cdot f_s$$  \hspace{1cm} (1.2)

where $V_{DS}$ is the block voltage and $I_{DS}$ is the load current.

Turn off loss, $P_{off}$, can also be evaluated by using Equation (1.3).

$$P_{off} = \frac{V_{DS}}{2} \cdot I_{DS} \cdot (T_7 - T_8) \cdot f_s$$  \hspace{1cm} (1.3)

However, this simplifying switching loss model does not consider the parasitic inductance of the MOSFET, among which common source inductance is the most important one. Figure 1.4 shows the power MOSFET along with the common source inductance, which is made up of the bonding wire and the trace inductance on PCB board. During turn on and turn off transition, both the gate drive circuit and main power train path share the same inductance. During current switching, this inductance will produce a large $L_{sd} \frac{di_{ds}}{dt}$ effect to slow down the turn on and turn off of the device. This effect will significantly degrade the performance at high switching
frequencies.

In order to more accurately predict the switching loss at high frequency, the analytical switching loss model was proposed in [19] analyzes the common source inductance, which is suitable for massive data processing of some applications that need good accuracy and short simulation time.

![Power MOSFET and common source driver](image)

**Figure 1.4 Power MOSFET and common source driver $L_s$**

### 1.4.3 Gate Drive Loss

In each switching period, the MOSFET parasitic gate capacitances, $C_{gs}$ and $C_{gd}$, are charged and discharged repetitively. The energy is usually dissipated through resistance in series with the gate within the gate drive circuit. MOSFET gate drive loss is given by Equation (1.4). Where $Q_g$ is the total gate charge, $f_s$ is the switching frequency and $V_{gs}$ is the amplitude of the gate drive voltage.

$$P_{\text{DRV}} = Q_g \cdot V_{gs} \cdot f_s = C_{iss} \cdot V_{gs}^2 \cdot f_s$$

(1.4)

It is noticed that gate drive loss is proportional to the switching frequency.
1.4.4 Output Loss

The output loss, $P_{out}$, is energy lost when the switch output drain-to-source capacitance is discharged during turn on as given by Equation (1.5).

$$P_{out} = \frac{1}{2} C_{oss} V_{DS}^2 f_s$$  \hspace{1cm} (1.5)

1.5 Introduction to Existing Gate Drivers

The existing gate driver can be classified as conventional Voltage Source Driver (VSD), Resonant Gate Driver (RGD) and existing Current Source Drivers (CSD). In this section, the basic operation and the limitations will be covered.

1.5.1 Conventional Voltage Source Driver

The conventional VSD is illustrated in Figure 1.5 to drive the power MOSFET, M, whose parasitics are shown in blue color: $R_G$ is the gate resistance, $C_{GS}$ is the gate-to-source capacitance, $C_{GD}$ is the gate-to-drain capacitance, $C_{DS}$ is the drain-to-source capacitance, $L_S$ is the common source inductance including the bonding wire inside the MOSFET package and PCB trace inductance and $L_D$ is the switching loop inductance. The conventional VSD has a totem pole configuration, which turns on the MOSFET by turning on the top switch of VSD, $S_T$; while turns off the MOSFET by turning on the bottom switch of VSD, $S_N$. 
Figure 1.5 Conventional VSD with power MOSFET and its associated parasitic

The switching waveforms associated with Figure 1.5 are shown in Figure 1.6, where PWM is the PWM signal input of the VSD, $V_{CGS}$ is the voltage across the $C_{GS}$ of M, $V_{DS}$ is the drain-to-source voltage across M, $i_{DS}$ is the drain-to-source current flowing through the M, $P_{on}$ is the turn on loss and $P_{off}$ is the turn off loss. It is noted that turn off loss is the dominant loss of the total switching loss $P_{switch}$ ([19] - [21]). It is also observed that, due to the effect of the parasitic inductance, $V_{DS}$ reduces sharply when $i_{DS}$ starts to increases at $t_1$ and then keeps at a plateau during $(t_1, t_2)$ since the rising rate of $i_{DS}$ is almost constant in this interval ([19], [23]).
The equivalent circuit of the MOSFET driven by the VSD during turn off transition is given in Figure 1.7. When $S_N$ in Figure 1.5 is turned on, because of the on resistance of $S_N$ (larger than 0.5Ω), the voltage appearing across the gate-to-source of power MOSFET, $V_{GS}$, is around 0.5V. Therefore, the main drawback of VSD is that $V_{GS}$ is unipolar, which means $V_{GS}$ is always bigger than zero, even during turn–off transition. It seriously limits the turn off speed, especially in the presence of the common source inductance in high frequency application as described below.
1.5.2 Resonant Gate Driver

One way to reduce the gate drive loss is Resonant Gate Drivers (RGDs) ([24] - [26]), which was originally proposed to recover part of MOSFET gate drive loss when operating at high switching frequency (above 1MHz). Initially, RGDs use a small inductance to recover part of the gate energy with reduced circulating loss. Figure 1.8 illustrates a typical resonant gate drive circuit and its corresponding waveforms.

The MOSFET $M$ is charged or discharged by resonant current $i_L$, which is provided by the resonant inductor $L$. When the gate is fully charged to $V_{cc}$, drive transistor $S_1$ is turned on so that it provides a low impedance path to the gate voltage source. At the same time, current $i_L$ in $L$ rises linearly. The turn off transition is initiated by turning $S_2$ off. When the gate capacitance is fully discharged, $S_2$ is turned on so that it shunts the gate and the source of the power MOSFET. $S_1$ and $S_2$ are turned on and off at zero voltage.
The major advantage of this approach is simplicity since only one additional inductor and a capacitor are added comparing to a conventional gate drive circuit. However, this circuit can only be beneficial for Synchronous Rectifier (SR), since the SR is designed with large gate charge and small on resistance to reduce the conduction loss of the SR during freewheeling mode.

Resonant topologies based on resonant pulse technique including full resonance and clamped resonance were proposed in [26] - [30] with the advantage of the low conduction loss. Figure 1.9 illustrates the gate driver with the resonant pulse. It consists of two control drive switches (S₁ and S₂) and two diodes (D₁ and D₂).

The major disadvantage of the resonant pulse solution is that both the turn on period and turn
off period must be longer than half of the resonant period. Therefore, the switching frequency is limited, which makes it difficult to be applied at high frequency application. Moreover, due to the diodes, the gate terminals of the power MOSFET is not effectively clamped to drive voltage when on, or ground when off, which has lower noise immunity.

Also, some RGDs can drive two MOSFETs with the transformer or coupled inductor ([30] - [31]). Nevertheless, the design of the transformer or coupled inductor is really challenging.

Most importantly, all the above RGDs only emphasize on the reduction of gate loss, but they can hardly reduce the switching loss which is the dominant loss for high frequency operations. Therefore, the efficiency improvement potentials for the RGDs are limited.

1.5.3 Existing Current Source Drivers

Current Source Drivers (CSDs) that can reduce the switching loss of the power MOSFET are reported in ([20], [32] - [37]) to improve the performance of RGDs. Either working under continuous current mode ([20], [32] -[34]) or discontinuous current mode [35] - [37], the existing CSDs can charge and discharge the power MOSFET with a nearly constant current to accelerate the switching speed. One of the representative CSDs is shown in Figure 1.10. As is reported in [35], it has the following advantages:

1. Compared with continuous current mode CSDs, it has minimized circulating current and thus minimal conduction loss due to its discontinuous current mode operating principle.
2. Independent of the duty cycle, suitable for narrow duty cycle operation.
3. Lower inductor value, easier for integrated circuit (easier for integration).
4. Soft switching of the driver switches.

However, the CSDs proposed in the previous work have the gate current diversion problem during switching transition due to impact of the common source inductance. Since the turn off loss dominates the switching loss, the turn off transition is focused on in this chapter. During the
turn off transition, the CSD in Figure 1.10 can be simplified as the circuit in Figure 1.11. The gate-to-source voltage $V_{GS}$ in Figure 1.11 is derived as below,

$$
V_{GS} = -i_G R_G + V_{CGS} - L_s \frac{di_{DS}}{dt}
$$

where $V_{CGS}$ represents the voltage across the gate-to-source capacitance of the MOSFET $Q$, $i_G$ is the effective discharge current, and $i_{DS}$ represents the drain-to-source current.

Figure 1.10 Topology of the CSD reported in [35]

Figure 1.11 Simplified discharging circuit of existing CSD in [35]
The higher the drain current falling rate $\frac{di_{DS}}{dt}$ is, the faster the turn off transition is achieved. According to the relationship in Equation (1.6), $V_{GS}$ decreases when $\frac{di_{DS}}{dt}$ increases. However, when $V_{GS}$ goes below -0.7V, the body diode of $S_4$, $D_4$, in Figure 1.10 will conduct, clamping $V_{GS}$ at -0.7V. The equivalent circuit of the CSD after $D_4$ is driven on is shown in Figure 1.12. It is noted that, compared with VSD whose gate-to-source voltage is unipolar, the $V_{GS}$ of existing CSDs is bipolar waveform, which means that CSD can achieve faster turn off speed than VSD because of the negative $V_{GS}$ (-0.7V).

![Figure 1.12 Equivalent circuit of the CSD in [35] after $D_4$ is on](image)

After $D_4$ is on, part of the inductor current $i_{Lr}$ is diverted through $D_4$, and the current diversion problem, which commonly exists in the existing CSDs, happens. Thus the falling rate of drain current, $\frac{di_{DS}}{dt}$, is limited. Therefore, the effective discharge current $i_G$ derived in Equation (1.7) is reduced, which increases the turn off transition time and weakens the effectiveness of current source driver.

$$i_G = i_{Lr} - i_{D4} \quad (1.7)$$

where $i_G$ is the gate discharge current, $i_{Lr}$ is the current flowing in the inductor, and $i_{D4}$ is the current diverted in the body diode $D_4$. It should be noted that, due to the effect of $L_s$, the gate current diversion problem becomes even worse at high load current condition.
To validate the analysis about the limitation of CSD in [35], computer simulation is conducted with SIMetrix [38]. Waveforms of $V_{CGS}$, $V_{DS}$, $i_{DS}$, $i_L$, $i_g$ and current diverted in the body diode $D_4$, $i_{D4}$, are shown in Figure 1.13. There are three intervals of turn off transition shown in Figure 1.13: turn off delay ($t_0$, $t_1$), Miller Plateau ($t_1$, $t_2$) and drain current drop ($t_2$, $t_3$).

It’s observed that, during turn off delay and Miller Plateau there is no current diversion problem as $i_{DS}$ does not change during these two intervals; while when $i_{DS}$ decreases during ($t_1$, $t_2$), a large portion of current out of 2.5A peak current source inductor current is diverted through the body diode $D_4$ because of the impact of $L_s$, which significantly limits the turn off speed.

![Figure 1.13 Simulation waveforms of turn off transition of CSD in [35]](image)

**Figure 1.13 Simulation waveforms of turn off transition of CSD in [35]**

### 1.6 Research Motivation

Currently, the switching frequency of the VR is going to move into MHz level to increase its power density; the output voltage of the VR undergoes a downward trend to reduce the overall power dissipation in the presence of ever-increasing load current.

However, conventional VSD will introduce more loss under these two trends. RGDs can recover the gate drive loss; but in high switching frequency when switching loss becomes the
dominant loss, RGDs lose their effect. Existing CSDs can turn on and turn off the power MOSFET with a nearly constant current; especially, CSDs can turn off the power MOSFET with -0.7V, which can accelerate the turn off speed and hence reduce the switching loss.

It is noted that the existing CSDs can be further improved if the gate voltage becomes more negative than -0.7V. Therefore, one research objective of this thesis is to propose a novel CSD with flexible and bipolar gate drive voltage for high frequency power MOSFET, which can significantly reduce the switching loss in high frequency applications.

When current diversion problem happens, the impact of the common source inductance still needs to be investigated. Hence, another interesting objective of research is to build up accurate mathematical modelings which can better represent the real situation of the circuits operating. Based on the analytical modeling, the performance of the CSD can be analyzed accurately and even optimized.

With the ever-urgent demands for high power density, the inductor in the CSDs has become the bottleneck to felicitate the complete integration of the VRs. Therefore, another aim is targeted at a new bipolar gate driver that has an inductorless configuration.

1.7 Thesis Outline

The thesis is organized as follows:

Chapter 1 introduces the basic theory of switched-mode power supplies and especially focuses on the research trend and challenge for future microprocessor. Then the research motivation of the thesis is presented.

Chapter 2 will present a novel bipolar current source driver that can achieve bipolar gate driver signals for high frequency power MOSFET. The limitation of the existing gate driver techniques (including conventional voltage source driver and existing current source driver) is proposed, based on which the topology and operating principle of the proposed bipolar current
source driver is proposed. The simulation results and experimentally measured efficiency are provided to support the advantages of the proposed driver.

In Chapter 3, a new analytical mathematical modeling that considers the current diversion problem is presented. The piecewise equations for the power MOSFET driven with the bipolar current source driver proposed in Chapter 2 are obtained. The optimal design of the current source inductor is also achieved to minimize the overall loss of the synchronous buck converter driven by the proposed gate driver. The experimental results show that the optimized current source driver can achieve better efficiency than the commercial Driver-MOSFET from the industry.

Chapter 4 shows the new inductorless bipolar gate driver for the control FET of the synchronous buck converter. The topology and operating principle of the proposed gate driver is presented. The analytical mathematical modeling is built to verify the advantage of the proposed gate driver compared with conventional voltage source driver. The experimental prototype further validates the efficiency improvement of the proposed gate driver in comparison with the conventional voltage source driver.

Chapter 5 summarizes the contribution of the thesis and presents the direction for future work.
Chapter 2 A New High Efficiency Current Source Driver with Bipolar Gate Voltage

2.1 Introduction

In Chapter 1, the operating principles and limitations of the conventional VSD, RGDs and the existing CSDs have been analyzed thoroughly. It is noted that the basic benefit of the existing CSDs is that they can turn off the power MOSFET with a negative voltage (around -0.7V). By comparison, the VSD can only turn off the power MOSFET with a positive voltage (around +0.5V). In other words, compared with the conventional VSDs whose gate drive signal is unipolar, the existing CSDs can achieve bipolar gate driver signal, which means much faster switching speed and smaller switching loss. In order to further improve the performance of the existing CSD, a new bipolar CSD that can turn off the power MOSFET with a flexible negative voltage (such as -3.5V) is proposed in this chapter.

The outline of this chapter is as follows: in Section 2.2 the topology and the operation principle of the proposed bipolar CSD is analyzed. The advantages of the proposed CSD is summarized and validated by the simulation results and theoretical calculations in Section 2.3. In Section 2.4, the experimental results are presented to verify the features of the proposed CSD, followed by discussions. Finally, the conclusions are drawn in Section 2.5.

2.2 The Proposed Bipolar Current Source Driver Circuit

In this section, the topology of the proposed bipolar CSD will be illustrated. In addition, the operating principle of the turn on transition and turn off transition of the CSD will be analyzed in details.

2.2.1 The Proposed Bipolar Current Source Driver

In order to alleviate the gate current diversion problem mentioned above and reduce the switching loss, a new bipolar CSD which can turn off the MOSFET with a flexible negative
voltage is proposed in this chapter. The topology of the proposed CSD is given in Figure 2.1. It is noted that as compared with the CSD in Figure 1.10, \( S_4 \) is replaced by a pair of four-quadrant switches, \( S_4 \) and \( S_5 \), whose source terminals are connected together to block the conduction of body diodes. Another key feature of the proposed CSD is to use five diodes \( D_{s1}-D_{s5} \) as an anti-diode of the \( S_4 \& S_5 \) branch to create a negative gate voltage (i.e. -3.5V in Figure 2.1) during turn off transition, which can noticeably increase the gate discharge current. It is noted that the number of the diodes used in the proposed bipolar CSD is flexible and dependent on the value of the negative voltage designed during turn off transition.

Figure 2.1 Power MOSFET driven by the proposed bipolar CSD

The waveforms of the five switches driving signals, \( V_{GS1}-V_{GS5} \), the inductor current \( i_{Lr} \), the gate charge/discharge current \( i_G \), the voltage across \( C_{GS} - V_{CGS} \), the drain-to-source current \( i_{DS} \), the drain-to-source voltage \( V_{DS} \), and the gate-to-source voltage \( V_{GS} \) are illustrated in Figure 2.2. It is noted the gate signals for \( S_4 \) and \( S_5 \) are exactly the same all through the switching cycles.
2.2.2 Detailed Turn On Operation

The operation principle of the turn on transition is illustrated as follows. Prior to $t_0$, the power MOSFET is assumed to be in the OFF state, and $S_4$ and $S_5$ are in the ON state.

A. Turn on Precharge ($t_0$, $t_1$): At $t_0$, $S_1$ is turned on, and the inductor current $i_{Lr}$ rises almost linearly in the positive direction through the current path shown in Figure 2.3 (a). The pre-charge state ends at $t_1$, which is usually set by the designer.

B. Turn on Delay ($t_1$, $t_2$): At $t_1$, $S_4$ & $S_5$ are turned off; the inductor current $i_{Lr}$ starts to charge
the gate capacitance of $Q$ - the equivalent circuit is given in Figure 2.3 (b). At this interval, the effective charge current $i_G$ equals $i_{Lr}$. This interval ends when $V_{CGS}$ reaches $V_{th}$.

C. Drain Current Rising ($t_2$, $t_3$): At $t_2$, $V_{CGS} = V_{th}$. During this interval, $V_{CGS}$ keeps increasing, and $i_{DS}$ starts to rise according to the relationship in Equation (2.1). Since $i_{DS}$ flows through $L_S$, according to Equation (1.6), the large voltage induced across $L_S$ makes $V_{GS}$ far larger than the driver supply voltage $V_c$. Therefore, $D_2$, the body diode of the driver switch $S_2$, is driven on to clamp $V_{GS}$ at $V_c+0.7$. The equivalent circuit is shown in Figure 2.3 (c). At this interval, $i_G$ drops sharply because of the voltage clamping. The subtraction of $i_{Lr}$ and $i_G$ is diverted into $D_2$.

$$i_{DS} = g_{fs}(V_{CGS} - V_{th})$$

where $g_{fs}$ is the transconductance of the power MOSFET.

D. Miller Plateau ($t_3$, $t_4$): At $t_3$, $i_{DS} = I_o$. During this interval, $V_{CGS}$ is held at the Miller Plateau voltage. $i_G$ mainly flows through the gate-to-drain capacitance of $Q$, and $V_{DS}$ decreases accordingly. It is noted that $i_G$ starts to rapidly increase since the EMF across $L_s$ falls sharply due to the unchanged $i_{DS}$, however part of the inductor current is still diverted through $D_2$. The equivalent circuit is given in Figure 2.3 (d).

E. Remaining Gate Charging ($t_4$, $t_5$): At $t_4$, $V_{DS} = 0$ and $V_{CGS}$ starts to rise again until it reaches $V_c$. $V_{GS}$ remains at $V_c+0.7$, and due to the rising of the $V_{CGS}$, $i_G$ decreases gradually. The equivalent circuit is given in Figure 2.3 (e).

F. Energy Recovery ($t_5$, $t_6$): At $t_5$, $S_2$ is turned on to recover the energy stored in the inductor to the source as well as actively clamping $Q$ to $V_c$. It is noted that the gate voltage of power MOSFET is clamped to $V_c$ through a low impedance path, which prevents the circuit being false triggered by $Cd/dt$ effect.
Figure 2.3 Turn on operation

(a) \((t_0, t_1)\): Precharge

(b) \((t_1, t_2)\): Turn on Delay

(c) \((t_2, t_3)\): Drain Current Rising

(d) \((t_3, t_4)\): Miller Plateau

(e) \((t_4, t_5)\): Remaining Gate Charging

(f) \((t_5, t_6)\): Energy Recovery
2.2.3 Detailed Turn Off Operation

The operation principle of the turn off transition is illustrated as follows. Prior to $t_7$, the power MOSFET is assumed to be in the ON state and $S_2$ is also in the ON state.

A. Turn off precharge ($t_7$, $t_8$): At $t_7$, $S_3$ is turned on, and the inductor current $i_{Lr}$ rises almost linearly in the negative direction through the current path shown in Figure 2.4 (a). The pre-charge state ends at $t_8$, which is set by the designer, and $S_2$ is turned off with ZVS at $t_8$.

B. Turn off Delay ($t_8$, $t_9$): At $t_8$, $S_2$ is turned off. In this interval, $V_{CGS}$ decreases until $V_{th} + I_o g_{fs}$ which ends the interval. The equivalent circuit is given in Figure 2.4 (b).

C. Miller Plateau ($t_9$, $t_{10}$): At $t_9$, $V_{CGS} = V_{th} + I_o g_{fs}$. In this interval, $V_{CGS}$ holds at the Miller plateau voltage, $V_{th} + I_o g_{fs}$. $i_G$ (equal to $i_{Lr}$) strictly discharges the gate-to-drain capacitance $C_{GD}$ of $Q$, and $V_{DS}$ rises until it reaches $V_{in}$ at $t_{10}$. The equivalent circuit is illustrated in Figure 2.4 (c).

D. Drain Current Drop ($t_{10}$, $t_{11}$): At $t_{10}$, $V_{DS} = V_{in}$ and $V_{CGS}$ continues to decrease from $V_{th} + I_o g_{fs}$ to $V_{th}$. $i_{DS}$ falls from $I_o$ to zero according to relationship in Equation (2.1). According to Equation (1.6), due to the induction EMF across $L_s$, the series connected diodes $D_{s1}$-$D_{s5}$ are driven on to clamp $V_{GS}$ at around -3.5V. The voltage across the current source inductor becomes -3.5V, so $i_{Lr}$ decreases at a higher rate than in the turn on transition. The equivalent circuit of this interval is given in Figure 2.4 (d). It is emphasized is that the CSD proposed in [35] only can clamp $V_{GS}$ to -0.7V. This means that the turn off speed of the CSD proposed in this chapter is much faster than that of the CSD in [35]. It is worth mentioning that $V_{DS}$ in this interval will keep rising due to effect of the $L_s$.

E. Remaining Gate Discharging ($t_{11}$, $t_{12}$): At $t_{11}$, $V_{CGS} = V_{th}$. In this interval, $V_{CGS}$ continues to decrease until it equals zero; it is noted that $V_{DS}$ continues to rise during this interval. The equivalent circuit is shown in Figure 2.4 (e).

F. Energy Recovery ($t_{12}$, $t_{13}$): At $t_{12}$, $S_3$ is turned off and $S_4$ & $S_5$ are turned on with ZVS.
The body diode of $S_1, D_3$, is forced on by $i_{Lr}$, and the CSD circuit turns into the mode of energy recovery through the path shown in Figure 2.4 (f). During this interval, the energy stored in $L_r$ is recovered to $V_c$. The interval ends at $t_{13}$ when the inductor current becomes zero.

In the analysis above, the detailed switching transition is analyzed. The current diversion problem introduced by the common source inductance is addressed. It is noted that the current diversion problem exists in both turn on and turn off transition. However, since the turn off loss is the dominant loss of the switching loss, only the current diversion in turn off transition is addressed. It could be concluded that the proposed CSD can achieve bipolar gate drive waveforms because of the diversion of the $D_{s1}$-$D_{s5}$ during turn off transition.
(a) \((t_2, t_8)\): Predischarge

(b) \((t_8, t_9)\): Turn off Delay

(c) \((t_9, t_{10})\): Miller Plateau

(d) \((t_{10}, t_{11})\): Drain Current Drop

(e) \((t_{11}, t_{12})\): Remaining Gate Discharge

(f) \((t_{12}, t_{13})\): Energy Recovery

27
Figure 2.4 Turn off operation

2.3 Advantages of the Proposed Bipolar CSD

The proposed CSD circuit in this chapter has the following advantages:

2.3.1 Significantly Reduced Turn Off Time and Thus Turn Off loss.

During turn off transition, the gate discharge current is not diverted to diode until the gate voltage reaches a much lower voltage (-3.5V) due to the increases or decreases of the current through the power MOSFET. When current decreases during turn off transition, $V_{GS}=0.5$ V for VSD because of the on resistance of the driver switch, $S_x$, in Figure 1.5; for CSD in Figure 1.10, $V_{GS}=-0.7$V because of the conduction of $D_4$; while for the bipolar CSD in Figure 2.1, $V_{GS}=-3.5$ V because of the conduction of $D_{s1}-D_{s5}$.

Simulations under the same condition for VSD, existing CSD and proposed CSD are conducted with SIMetrix. In comparison with Figure 1.13, the turn off waveforms of the proposed CSD are shown in Figure 2.5. Figure 2.6 summarizes the current fall time for the proposed CSD, existing CSD and VSD respectively. It is observed that, for the proposed CSD, it takes 8.7 ns for $i_{DS}$ to decrease from 30A to 0, which is about half of the time needed for existing CSD (15.6 ns) and one third of the time needed for VSD (20.1 ns).

The reason for the significant improvement of the proposed CSD over the existing gate drivers (VSD and existing CSDs) is because that the gate discharge current $i_G$ of the proposed CSD is greatly increased. Figure 2.7 shows the comparison of the average gate discharging current when $i_{DS}$ decreases. It is observed that the average discharge current $i_G$ of the proposed CSD is four times of that of VSD and twice of that of the existing CSD.
Figure 2.5 Simulation waveforms of turn off transition of the proposed CSD

Figure 2.6 Comparison of the simulated current fall time
In order to support the simulation results above, calculations have been done with piecewise linear approximation model [21]. According to the datasheet of power MOSEFT Si7386DP used in the simulation [39], gate mesh resistance $R_g=1.7\text{ohm}$. The voltage across the $L$, for VSD, existing CSD and the proposed CSD during $i_{DS}$ falling time are calculated and compared in 0. $i_G$ is obtained from Figure 2.7; $V_{CGS}$ is derived by Equation (2.2) according to piecewise linear approximation; $L_sdi_{DS}/dt$ is calculated through Equation (1.6).

**Table 2.1 Comparison of VSD, existing CSD and the proposed CSD during turn off transition**

<table>
<thead>
<tr>
<th>Driver Type</th>
<th>$V_{GS}$</th>
<th>$i_G$</th>
<th>$V_{CGS}$</th>
<th>$L_sdi_{DS}/dt$</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSD</td>
<td>0.5 V</td>
<td>0.16 A</td>
<td>2.7 V</td>
<td>1.93 V</td>
</tr>
<tr>
<td>Existing CSD</td>
<td>-0.7 V</td>
<td>0.25 A</td>
<td>2.7 V</td>
<td>2.98 V</td>
</tr>
<tr>
<td>The Proposed CSD</td>
<td>-3.5 V</td>
<td>0.69 A</td>
<td>2.7 V</td>
<td>5.03 V</td>
</tr>
</tbody>
</table>

From Table 2.1, it is observed that the $L_sdi_{DS}/dt$ of the proposed CSD is around twice of the
existing CSD in [35] and three times of the conventional VSD. In other words, the proposed CSD can decrease the current $i_{DS}$ at a speed of twice of the existing CSD and three times of the VSD, which matches with the simulation results in Figure 2.6.

$$V_{CGS} = \frac{V_{pl} + V_{th}}{2}$$  \hspace{1cm} (2.2)

where $V_{CGS}$ is the voltage across the gate-to-source capacitance of the MOSFET $Q$, $V_{pl}$ means the Miller plateau voltage of $Q$, and $V_{th}$ is the gate threshold voltage of $Q$.

2.3.2 Less Impact of Parasitic Inductance

Whether in the conventional VSD or the existing CSDs, the parasitic inductance, especially common source inductance, significantly reduces the switching speed and hereby increases the switching loss [34]. The proposed bipolar CSD can well alleviate the impact of parasitic inductor with $V_{GS}$ clamped to a flexible negative voltage (such as -3.5V), which can reduce the turn off time and hereby improve the efficiency.

2.3.3 Smaller Current Source Inductor

The CSD proposed in this chapter works in discontinuous current mode, which allows the current source inductor to be very small (tens of nH). It is expected that, with better on-chip inductor techniques on the way, the current source driver inductor can be fully integrated into the driver chip in the near future. ([40])

2.3.4 High Stability and Noise Immunity

The MOSFET is either actively clamped to $V_c$ during on or to zero during off, which will minimize the possibility for MOSFET to be false triggered by $Cv/dt$ effect and increase the stability of the circuit.
2.3.5 Application Extension to Other CSDs

The idea presented in this chapter can be used to further alleviate the gate current diversion problem during turn on transition. Figure 2.8 shows the topology of a new bipolar CSD with improved turn on gate current. The CSD in Figure 2.8 increases the gate current during turn on transition based on the same idea presented in this chapter. However, it is noted that, since turn on loss is relatively small compared with turn off loss, the improvement of the CSD during turn on transition in Figure 2.8 would be less significant than the improvement of the CSD during turn off transition proposed in this chapter.

Another advantage of the bipolar CSD proposed here is that it can be widely extended to all other existing CSDs to further improve the turn off speed. Figure 2.9 illustrates the improved bipolar CSD operating with continuous inductor current mode to drive both the control FET and SR of the synchronous buck converter ([33]). While another improved bipolar CSD with continuous inductor current mode is presented in Figure 2.10, which enables magnetic integration of inductor \( L_{r1} \) and \( L_{r2} \) ([34]). In Figure 2.11, a discontinuous inductor current mode CSD ([37])...
is improved using the idea presented in this chapter to achieve bipolar switching waveforms. It is noted that all the improved portion of the three CSDs are marked in blue colors.

Figure 2.9 Improved dual channel bipolar CSD with continuous inductor current mode

Figure 2.10 Improved bipolar CSD working with continuous inductor current mode
2.4 Experimental Verification and Discussion

A prototype for a synchronous buck converter shown in Figure 2.12 was built to verify the advantages of the proposed CSD circuit. The control FET of the buck converter is driven by the proposed CSD, while the SR is driven by the conventional voltage source driver as the switching loss of the SR is very small. The design parameters are given in Table 2.2.
Table 2.2 Design Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency, $f_s$</td>
<td>1MHz</td>
</tr>
<tr>
<td>Input Voltage, $V_{in}$</td>
<td>12V</td>
</tr>
<tr>
<td>Output Voltage, $V_o$</td>
<td>1.2 and 1.3V</td>
</tr>
<tr>
<td>SR Gate Drive Voltage, $V_{c2}$</td>
<td>6.5V</td>
</tr>
<tr>
<td>SR, $Q_2$</td>
<td>IRF6691</td>
</tr>
<tr>
<td>CSD Voltage, $V_{c1}$</td>
<td>5V</td>
</tr>
<tr>
<td>Control FET, $Q_1$</td>
<td>Si7386DP</td>
</tr>
<tr>
<td>Output Inductor, $L_f$</td>
<td>330nH, Vishay IHLP5050CE</td>
</tr>
<tr>
<td>Driver Switches, $S_1 - S_5$</td>
<td>FDN335N</td>
</tr>
<tr>
<td>Driver Inductor, $L_r$</td>
<td>43nH, Coilcraft B10T_L</td>
</tr>
<tr>
<td>Diodes, $D_{s1} - D_{s5}$</td>
<td>MBR0520</td>
</tr>
</tbody>
</table>

The photo of the prototype is illustrated in Figure 2.13. It uses 6-layer, 4-oz copper PCB. Figure 2.14 illustrates the hardware implementation of the proposed CSD. Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. Driver switches $S_1$-$S_5$ are driven with the level shift circuits.
Figure 2.13 Photo of prototype with the proposed bipolar CSD

Figure 2.14 Hardware implementation of the buck converter driven with the proposed CSD

Figure 2.15 shows switch gate signals, $V_{GS1}-V_{GS5}$ and associated modes for turn on and turn off transition respectively.
Figure 2.15 Driver switch gate signals ($V_{GSI}$-$V_{GSS}$)

Figure 2.16 illustrates that driver inductor current $i_L$ and the gate-to-source voltage $V_{GS.Q1}$ of control FET. It can be observed that $Q_1$ is charged and discharged with nearly constant current and $V_{GS.Q1}$ is clamped to about -3.5V during turn off transition. Most importantly there is no Miller Plateau observed in $V_{GS.Q1}$. It is noted that the effective charge current, $i_{G.e}$, is hard to measure without disturbing the circuit operation. Therefore, the measured waveform of $i_{G.e}$ is not provided in this chapter.
The gate to source voltage waveforms for control FET and SR are shown in Figure 2.17. It is observed that the dead time between $V_{GS, Q1}$ and $V_{GS, Q2}$ is minimized to avoid body diode conduction without causing shoot through problem.
Figure 2.17 $V_{gs\_Q1}$, $V_{gs\_Q2}$

Figure 2.18 summarizes the measured efficiencies (including gate drive loss) of the proposed CSD in 1.2V and 1.3V output in 1MHz switching frequency with 12V input.

![Efficiency Chart](image)

**Measured Efficiencies @Vo=1.2V&1.3V**

- 1.3V output:
  - 78.8%
  - 84.0%
  - 85.8%
  - 86.8%
  - 86.1%
  - 89.3%
  - 83.9%

- 1.2V output:
  - 76.0%
  - 84.0%
  - 85.5%
  - 85.4%
  - 84.7%
  - 82.5%

Figure 2.18 Efficiencies at 12V input, 1.2V and 1.3V output, 1MHz switching frequency
Figure 2.19 shows the efficiency comparison among the proposed bipolar CSD, existing CSD proposed in [35] and the conventional VSD at 12V input, 1.2V output and 1MHz switching frequency. It is noted that the proposed bipolar CSD increases the efficiency of VSD from 73.1% to 82.5% by 9.4% at 1.2V/30A output and improves the efficiency of the existing CSD from 80.5% to 82.5% by 2% at 30A output.

![Figure 2.19 Measured efficiency comparison at 12V input, 1.2V output, 1MHz switching frequency](image)

Figure 2.19 Measured efficiency comparison at 12V input, 1.2V output, 1MHz switching frequency

Figure 2.20 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, existing CSD proposed in [35] and the conventional VSD at 12V input, 1.2V output and 1MHz switching frequency. It is noted that compared with existing CSD, the proposed CSD saves a 1.08W loss at 30A load. While compared with the conventional VSD, the proposed CSD achieves a loss reduction of 5.61W at 30A load.
Figure 2.20 Total measured loss comparison at 12V input, 1.2V output, 1MHz switching frequency

Figure 2.21 shows the efficiency comparison among the proposed bipolar CSD, existing CSD proposed in [35] and the conventional VSD at 12V input, 1.3V output and 1MHz switching frequency. It is noted that, compared to the conventional VSD, the proposed bipolar CSD increases the efficiency of VSD from 77.5% to 83.9% by 6.4% and improves the efficiency of the existing CSD from 81.9% to 83.9% by 2% at 30A output.
Figure 2.21 Measured efficiency comparison at 12V input, 1.3V output, 1MHz switching frequency

Figure 2.22 compares the total measured loss (including gate drive loss) among the proposed bipolar CSD, existing CSD proposed in [35] and the conventional VSD at 12V input, 1.3V output and 1MHz switching frequency. It is observed that the proposed bipolar CSD achieves a loss reduction of 3.84W at 30A load compared with VSD. Even compared with CSD in [35], the proposed bipolar CSD save a loss of 1.14W. It is also observed that the proposed CSD achieves higher efficiency improvement at high load current. This is because the proposed CSD significantly alleviates the gate current diversion problem at high current load.
2.5 Conclusions

In this chapter, a new bipolar Current Source Driver which can achieve much faster switching speed is proposed. The gate current diversion problem that exists in the existing CSDs is analyzed. Compared with previous gate drivers (VSD and existing CSDs), the proposed CSD can turn off the power MOSFET with a flexible negative voltage (such as -3.5V) to accelerate the turn off speed. The experimental results demonstrate the significant efficiency improvement over the conventional VSD with a 5.62W loss reduction at 1.2V/30A output and a 3.84W loss reduction at 1.3V/30A with 12V input in 1MHz switching frequency. The comparison between the proposed CSD and the existing CSD in [35] demonstrates the CSD proposed in this chapter is a better alternative for next generation VRs. More importantly, the basic idea presented in this chapter can be also extended to other existing CSD drivers to further improve their performance with high output current.

Figure 2.22 Total measured loss comparison at 12V input, 1.3V output, 1MHz switching frequency
Chapter 3 Accurate Switching Loss Model and Optimal Design of a Current Source Driver Considering the Current Diversion Problem

3.1 Introduction

As is illustrated in the previous chapters, the basic benefits of the existing CSDs compared with VSD and RGDs is that the gate drive waveforms of CSDs are bipolar ([41] - [42]), which means that CSDs can turn off the power MOSFET with a negative voltage (-0.7V). In Chapter 2, a new bipolar CSD that can turn off the power MOSFET with a flexible negative voltage (such as -3.5V) is presented. Therefore, compared to previous gate drivers (VSD, RGDs and existing CSDs), the proposed CSD in Chapter 2 can significantly reduce the turn off loss, which is the dominant loss of the switching loss.

However, during switching transitions the current in the current source inductor is diverted, which reduces the effective current to charge or discharge the MOSFET. This is known as the current diversion problem, which commonly exists in CSDs. In order to maintain the superior performance of CSDs compared with VSD and RGDs, the current diversion problem needs to be analyzed mathematically in order to predict and optimize the performance of CSD more accurately.

An analytical loss model, which thoroughly analyzes the impact of the parasitic inductance in CSDs, is presented in [20] to evaluate the performance of the CSDs. In addition, a generalized way to optimize the overall performance of the buck converter driven by a CSD is analyzed in the proposed model. A piecewise model that enables easy calculation and estimation of the switching loss is also proposed in [21]. However, the current diversion problem, which reduces the effective gate current and the switching speed, has not been analyzed in the mentioned models.

A new analytical switching loss model for the power MOSFETs driven by the bipolar CSD
reported in Chapter 2 is presented in this chapter. The gate current diversion problem, which commonly exists in existing CSDs, is analyzed mathematically. In addition, a new accurate switching loss model which considers every switching interval piecewisely is proposed. The optimal design of the CSD inductor based on the proposed loss model is also achieved to minimize the total power loss for the buck converter. The experimental result is also provided to verify the proposed switching loss modeling and optimal design.

The proposed switching loss model that analyzes the current diversion problem is presented in Section 3.2 of this chapter. Section 3.3 explains the procedures to obtain the optimal driver inductor of a CSD. The experimental results and related discussions are shown in Section 3.4 to validate the proposed loss model and optimal design. Finally, the conclusions are drawn in Section 3.5.

3.2 The Proposed Switching Loss Model Considering the Current Diversion Problem

The following sub-parts will present the operation principles of the CSD and a new switching loss model which considers the gate current diversion problem.

The equivalent circuit of the MOSFET driven by proposed CSD is shown in Figure 3.1, where the power MOSFET $Q$ is represented by a typical capacitance model, $L_S$ is the common source inductance including the PCB track and the bonding wire inside the MOSFET package and $L_D$ is the switching loop inductance. For the purpose of the transient analysis, the following assumptions are made [43]:

1) $i_{DS} = g_{fs}(v_{CGS}-V_{th})$ and MOSFET is ACTIVE, provided $v_{CGS} > V_{th}$ and $v_{DS} > i_{DS}R_{DS(on)}$

2) For $v_{CGS} < V_{th}$, $I_{DS} = 0$, and MOSET is OFF

3) When $g_{fs}(v_{CGS}-V_{th}) > v_{DS} / R_{DS(on)}$, the MOSFET is fully ON
Where $i_{DS}$ is the drain current of the $Q$, $g_{fs}$ is the transconductance, $v_{DS}$ is the voltage across the drain-source capacitance of the $Q$, $v_{CGS}$ is the voltage across the gate-source capacitance of the $Q$, $V_{th}$ is the threshold voltage of $Q$, $R_{DS(on)}$ is the drain-source on-state resistance. During the Active State when switching loss happens,

$$i_{DS} = g_{fs} (v_{CGS} - V_{th})$$

(3.1)

According to Figure 3.1, $i_G$ is the effective current to charge or discharge $Q$ as shown below,

$$i_G = (C_{GS} + C_{GD}) \frac{dv_{GS}}{dt} - C_{GD} \frac{dv_{DS}}{dt}$$

(3.2)

$v_{DS}$ is given as,

$$v_{DS} = V_{in} - L_D \frac{di_{DS}}{dt} - L_S \frac{d(i_{DS} + i_G)}{dt}$$

(3.3)

![Current Source Driver](image)

**Figure 3.1** Equivalent circuit of MOSFET with the proposed CSD

The detailed switching waveforms are illustrated in Figure 3.2, where $v_{gs1}$-$v_{gs5}$ are the gate drive signals for driver switches $S_1$-$S_5$ in Figure 3.1, $i_{Lr}$ is the driver inductor current of $L_r$; $v_{GS'}$, as shown in Equation (3.4), is the gate source voltage of $Q$ including the effect of the common source inductance and the gate resistance, $p_{sw}$ is the switching loss of the $Q$. 

46
$$v_{GS} = -i_G R_g + V_{CGS} - L_s \frac{d}{dt} (i_{DS} + i_G)$$ (3.4)

Figure 3.2 MOSFET Switching Transition Waveforms

The operation principle of the turn on transition is illustrated as follows. Prior to \( t_0 \), the power MOSFET is clamped in the OFF state by \( S_4 \) and \( S_5 \).
3.2.1 Turn On Transition:

A. Precharge \([t_0, t_1]\): At \(t_0\), \(S_1\) is turned on, and the inductor current \(i_{Lr}\) rises almost linearly and the interval ends at \(t_1\) which is preset by the designer. The equivalent circuit is given in Figure 3.3 (a). The inductor current \(i_{Lr}\) is given in Equation (3.5).

\[
i_{Lr} \approx \frac{V_C \cdot (t - t_0)}{L_r}
\]  

B. Turn on Delay \([t_1, t_2]\): At \(t_1\), \(S_4 \& S_5\) are turned off; the inductor current \(i_{Lr}\) starts to charge the gate capacitance of \(Q\) – the equivalent circuit is given in Figure 3.3 (b). At this interval, the effective charge current \(i_G\) equals \(i_{Lr}\). The initial condition of this interval is \(i_{Lr,t1} = i_{Lr}(t_1-t_0)\), and \(v_{CGS,t1}=0\). This interval ends when \(v_{CGS}\) reaches \(V_{th}\). The differential equations for the circuit are given in Equation (3.6), where \(R_{on}=R_{dson,S2}+R_{Lr}+R_g\), \(R_{dson,S2}\) is the on-resistance of \(S_2\), \(R_{Lr}\) is the DCR of \(L_r\) and \(R_g\) is the gate-resistance of the power MOSFET.

\[
V_c = (L_r + L_s) \frac{d}{dt}(i_{Lr}) + i_{Lr}R_{on} + v_{CGS}, \quad i_{Lr} = (C_{GS} + C_{GD}) \frac{d}{dt}(v_{CGS})
\]  

(3.6)

Mathematically, there are three possible forms for the equation of the inductor current: over damped, critically damped and under damped – for practical situations, \(\omega_0 > \alpha_0\), the equations for \(i_G\), \(i_{Lr}\) and \(v_{CGS}\) are given in Equation (3.7) ~ (3.8).

\[
v_{CGS} = [A_0 \cos(\sqrt{\omega_0^2 - \alpha_0^2} \ t) + B_0 \sin(\sqrt{\omega_0^2 - \alpha_0^2} \ t)]e^{-\alpha_0 t} + C_0
\]  

(3.7)

\[
i_G = i_{Lr} = (C_{GS} + C_{GD})[-A_0 \sqrt{\omega_0^2 - \alpha_0^2} \cos(\sqrt{\omega_0^2 - \alpha_0^2} \ t) + B_0 \alpha_0 \sin(\sqrt{\omega_0^2 - \alpha_0^2} \ t)]
\]

\[
+ (A_0 \alpha - B_0 \sqrt{\omega_0^2 - \alpha_0^2}) \cos(\sqrt{\omega_0^2 - \alpha_0^2} \ t)\ e^{-\alpha_0 t}
\]  

(3.8)

Where \(\alpha_0 = \frac{R_{on}}{2(L_r + L_s)}\), \(\omega_0 = \sqrt{(L_r + L_s)(C_{GS} + C_{GD})}\),

\[
A_0 = -[2\alpha_0 i_{Lr,t1} + (V_C - 2i_{Lr,t1}R_{on})/(L_r + L_s)]/[(C_{GS} + C_{GD})\omega_0^2],
\]

\[
B_0 = (i_{Lr,t1} + (C_{GS} + C_{GD})\alpha_0 A_0)/[(C_{GS} + C_{GD})\omega_0^2], \quad C_0 = -A_0
\]
C. Drain Current Rising \([t_2, t_3]\): At \(t_2\), \(v_{CGS} = V_{th}\). During this interval, \(v_{CGS}\) keeps increasing, and \(i_{DS}\) starts to rise according to the relationship in Equation (3.1). Since \(i_{DS}\) flows through \(L_S\), according to Equation (3.4), the large voltage induced across \(L_S\) makes \(v_{GS}\) far larger than the driver supply voltage \(V_c\). Therefore, \(D_2\), the body diode of the driver switch \(S_2\), is driven on to clamp \(v_{GS}\) at \(V_c+0.7\). The equivalent circuit is shown in Figure 3.3 (c). At this interval, \(i_G\) drops sharply because of the voltage clamping. The subtraction of \(i_{Lr}\) and \(i_G\) is diverted into \(D_2\). The initial condition of this interval is \(i_{G,t_2} = i_G(t_2-t_1)\), \(i_{DS,t_2} = 0\), and \(v_{CGS,t_2} = V_{th}\). The interval ends at \(t_3\) when \(i_{DS}\) equals the load current, \(I_o\). The equations for \(i_G\), \(i_{Lr}, v_{CGS}\) and \(v_{DS}\) are given in Equation (3.9)–(3.13).

\[
v_{CGS} = A_1 e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}) t} + B_1 e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) t} + C_1
\]

(3.9)

\[
i_{DS} = g_f(v_{CGS} - V_{th})
\]

\[
= g_f(A_1 e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}) t} + B_1 e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) t} + C_1 - V_{th})
\]

(3.10)

\[
i_G = A_i(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}) e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}) t} + B_i(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) t}
\]

(3.11)

\[
i_{Lr} = (I_{G,t_2} + 0.7/R_g) e^{(-R_{f}/L_r)t} - 0.7/R_g
\]

(3.12)

\[
v_{DS} = V_{in} - L_D \frac{d}{dt}(i_G) - (L_S + L_D) \frac{d}{dt}(i_{DS})
\]

(3.13)

Where \(\omega_1 = 1/\sqrt{L_S (C_{GS} + C_{GD})}\), \(\alpha_i = [R_g (C_{GS} + C_{GD}) + L_S g_{f,s}]/[L_S (C_{GS} + C_{GD})]\), \(C_1 = 0.7 + V_c\), \(A_i = [(V_{th} - 0.7 - V_c)(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}) - I_{G,t_2}]/[2\sqrt{\alpha_1^2 - \omega_1^2}]\), \(B_i = V_{th} - A_i - C_1\).

D. Miller Plateau \([t_3, t_4]\): At \(t_3\), \(i_{DS} = I_o\). During this interval, \(v_{CGS}\) is held at the Miller Plateau voltage. \(i_G\) mainly flows through the gate-to-drain capacitance of \(Q_i\), and \(v_{DS}\) decreases accordingly. It is noted that \(i_G\) starts to rapid increase since the EMF across \(L_s\) falls sharply due to
the unchanged $i_{DS}$, however part of the inductor current is still diverted through $D_2$. The equivalent circuit is given in Figure 3.3 (d). The initial values of the interval are $i_{G,t3}=i_G(t_3-t_2)$, $v_{CGS,t3}=v_{CGS}(t_3-t_2)$, and $v_{DS,t3}=v_{DS}(t_3-t_2)$. The interval ends when $v_{DS}$ equals zero at $t_4$. The equations for $i_G$, $v_{CGS}$ and $v_{DS}$ are given in Equation (3.14) ~ (3.16). $i_{Lr}$ remains the same as the previous interval.

$$v_{CGS} = V_{CGS,t3}$$ (3.14)

$$i_G = \left[I_{G,t3} - (V_c + 0.7 - V_{CGS,t3})/R_g \right] e^{(-R_g/L_s) t} + (V_c + 0.7 - V_{CGS,t3})/R_g$$ (3.15)

$$v_{DS} = \left[ (I_{G,t3} - (V_c + 0.7 - V_{CGS,t3})/R_g \right] e^{(-R_g/L_s) t} - \frac{(I_{G,t3} - (V_c + 0.7 - V_{CGS,t3})/R_g \right]}{C_{GD} R_g / L_s} + (V_{DS,t3} - (V_c + 0.7 - V_{CGS,t3})/R_g)$$ (3.16)

E. Remaining Gate Charging [$t_4$, $t_5$]: At $t_4$, $v_{DS} = 0$ and $v_{CGS}$ starts to rise again until it reaches $V_c$. $v_{GS}$ remains at $V_c + 0.7$, and due to the rising of the $v_{CGS}$, $i_G$ decreases gradually. The equivalent circuit is given in Figure 3.3 (e). The initial values of this interval are: $i_{G,t4}=i_G(t_4-t_3)$, $v_{CGS,t4}=v_{CGS,t3}$, and $v_{DS,t4}=v_{DS}(t_4-t_3)$. This interval ends at $t_5$ when $v_{CGS}=V_c$. The equations for $i_G$, $v_{CGS}$ and $v_{DS}$ are given in Equation (3.17) ~ (3.19) and $i_{Lr}$ is the same as the previous interval.

$$v_{CGS} = \left[A_2 \cos(\sqrt{\omega_2^2-\omega_1^2} t) + B_2 \sin(\sqrt{\omega_2^2-\omega_1^2} t) \right] e^{-\omega_1 t} + C_2$$ (3.17)

$$i_G = (C_{GS} + C_{GD}) \left[ (-A_1 \sqrt{\omega_1^2-\omega_2^2} + B_1 \omega_1) \sin(\sqrt{\omega_2^2-\omega_1^2} t) + (-A_1 \omega_1 - B_1 \sqrt{\omega_2^2-\omega_1^2}) \cos(\sqrt{\omega_2^2-\omega_1^2} t) \right] e^{-\omega_1 t}$$ (3.18)
\[ V_{DS} = V_{DS,t4} - \frac{(V_{CGS,t4} - V_{DS,t4})(V_{DS,t4} - I_o R_{on@V_c})}{V_c - V_{CGS,t4}} \] (3.19)

Where \( A_2 = V_{CGS,t4} - C_2 \), \( B_2 = [I_{G,t4} / (C_{GS} + C_{GD}) - A_i \alpha_i]/\sqrt{\alpha_i^2 - \omega_1^2} \), \( C_2 = V_C + 0.7 \) and \( R_{on@V_c} \) is the on-resistance of the MOSFET when \( V_{CGS} = V_C \).

F. Energy Recovery \([t_5, t_6]\): At \( t_5 \), \( S_2 \) is turned on to recover the energy stored in the inductor to the source as well as actively clamping \( Q \) to \( V_C \). The initial value of this interval is \( i_{LR,t5} = i_{LR}(t_5, t_2) \), and this interval ends when \( i_{LR} \) becomes zero. The equivalent circuit is illustrated in Figure 3.3 (f). The equation for \( i_{LR} \) is in Equation (3.20).

\[
i_{LR} = \left[ I_{G,t5} + (V_c + 0.7)/(R_{on,S2} + R_p) \right] e^{-(R_{on,S2}+R_p)/Lp} - (V_c + 0.7)/(R_{on,S2} + R_p)
\] (3.20)
Figure 3.3 Turn on operation
Prior to \( t_7 \), the power MOSFET is clamped in the ON state by \( S_2 \).

### 3.2.2 Turn Off Transition:

A. Predischarge \([t_7, t_8]\): At \( t_7 \), \( S_3 \) is turned on, and the inductor current \( i_{Lr} \) rises almost linearly and the interval ends at \( t_8 \) which is preset by the designer. The equivalent circuit is shown in Figure 3.4 (a). The equation for \( i_{Lr} \) is given in Equation (3.21).

\[
i_{Lr} \approx -\frac{V_c \cdot (t - t_7)}{L_r}
\]  

(3.21)

B. Turn off Delay \([t_8, t_9]\): At \( t_8 \), \( S_2 \) is turned off. In this interval, \( v_{CGS} \) decreases until \( V_{th} + I_o \cdot g_{fb} \) which ends the interval. The equivalent circuit is given in Figure 3.4 (b). The initial condition of this interval is \( i_{G,8} = i_{Lr,8} = i_{Lr}(t_8), v_{CGS,8} = V_c \). The way to solve the equations for \( i_G \), \( i_{Lr} \) and \( v_{CGS} \) are the same as Turn on Delay interval.

C. Miller Plateau \([t_9, t_{10}]\): At \( t_9 \), \( v_{CGS} = V_{th} + I_o \cdot g_{fb} \). In this interval, \( v_{CGS} \) holds at the Miller plateau voltage, \( V_{th} + I_o \cdot g_{fb} \), \( i_G \) (equal to \( i_{Lr} \)) strictly discharges the gate-to-drain capacitance \( C_{gd} \) of \( Q \), and \( v_{DS} \) rises until it reaches \( V_{in} \) at \( t_{10} \). The equivalent circuit is illustrated in Figure 3.4 (c). The equations of this interval can be obtained in the same way as the Miller Plateau in turn on interval.

D. Drain Current Drop \([t_{10}, t_{11}]\): At \( t_{10} \), \( v_{DS} = V_{in} \) and \( v_{CGS} \) continues to decrease from \( V_{th} + I_o \cdot g_{fb} \) to \( V_{th} \). \( i_{DS} \) falls from \( I_o \) to zero according to relationship in Equation (3.1). According to Equation (3.4), due to the induction EMF across \( L_s \), the series connected diodes \( D_{s1}-D_{s5} \) are driven on to clamp \( v_{GS} \) at around -3.5V. The voltage across the current source inductor becomes -3.5V, so \( i_{Lr} \) decreases at a higher rate than in the turn on transition. The equivalent circuit of this interval is given in Figure 3.4 (d).

By comparison, the CSD proposed in [44] only can clamp \( v_{GS} \) to -0.7V during this interval. This means that the turn off speed of the CSD proposed in this chapter (Figure 3.1) is more than
three times that of the CSD in [44]. It is worth mentioning that \( v_{DS} \) in this interval will keep rising due to effect of the \( L_s \). Therefore, the derivation of the equations in this interval needs to solve the 3rd order differential equations in Equation (3.22).

\[
\begin{align*}
L_s \frac{d}{dt} (i_{DS} + i_G) + v_{CGS} + i_G R_g + V_f &= 0 \\
i_{DS} &= g_{ps} (v_{CGS} - V_{th}) \\
i_G &= (C_{GS} + C_{GD}) \frac{d}{dt} (v_{CGS}) - C_{GD} \frac{d}{dt} (v_{DS}) \\
L_s \frac{d}{dt} (i_G) + (L_D + L_s) \frac{d}{dt} (i_{DS}) + v_{DS} - V_{as} - 0.7 &= 0
\end{align*}
\]

(3.22)

E. Remaining Gate Discharging \([t_{11}, t_{12}]\): At \( t_{10} \), \( v_{CGS} = V_{th} \). In this interval, \( v_{CGS} \) continues to decrease until it equals zero; it is noted that \( v_{DS} \) continues to rise during this interval. The equivalent circuit is shown in Figure 3.4 (e). The equations in this interval have the same form as the equations in Remaining Gate Charging Interval.

F. Energy Recovery \([t_{12}, t_{13}]\): At \( t_{11} \), \( S_4 & S_5 \) are turned on to recover the energy stored in the inductor to the source as well as actively clamping \( Q \) to ground. The equivalent circuit is given in Figure 3.4 (f). This interval is the same as the Energy Recovery at this turn on transition.
Figure 3.4 Turn off operation

(a) \((t_7, t_8):\) Predischarge

(b) \((t_8, t_9):\) Turn off Delay

(c) \((t_9, t_{10}):\) Miller Plateau

(d) \((t_{10}, t_{11}):\) Drain Current Drop

(e) \((t_{11}, t_{12}):\) Remaining Gate Discharge

(f) \((t_{12}, t_{13}):\) Energy Recovery
3.2.3 Total Loss for the Power MOSFET Driven with the Proposed CSD:

1. The switching loss of power MOSFET $P_{sw}$, which consists of turn on loss $P_{sw\_on}$ and turn off loss $P_{sw\_off}$, is derived according to in Equation (3.23), where $f_s$ is the switching frequency.

$$P_{sw} = \int_{t_2}^{t_4} (i_{DS} \cdot v_{DS} \cdot f_s) dt + \int_{t_6}^{t_8} (i_{DS} \cdot v_{DS} \cdot f_s) dt$$  \hspace{1cm} (3.23)

2. The gate driver loss $P_{dr}$ is the sum of conduction loss $P_{dr\_cond}$, gate drive loss $P_{dr\_gate}$ and output loss $P_{dr\_out}$ as given in Equation (3.24); while $P_{dr\_cond}$, $P_{dr\_gate}$ and $P_{dr\_out}$ are shown in Equation (3.25) ~ (3.27), where $R_{DS\_dr}$ is the on-resistance of the driver switch, $V_{D\_dr}$ is the gate driving voltage, $Q_{G\_dr}$ is the gate charge of the driver switch and $C_{OSS\_dr}$ is the output capacitance of the driver switch.

$$P_{dr} = P_{dr\_cond} + P_{dr\_gate} + P_{dr\_out}$$  \hspace{1cm} (3.24)

$$P_{dr\_cond} = \int_{t_0}^{t_9} (3 \cdot i_{Lr}^2 \cdot R_{DS\_dr}) dt + \int_{t_9}^{t_10} (i_{Lr}^2 \cdot R_{DS\_dr}) dt$$
$$+ \int_{t_7}^{t_8} (2 \cdot i_{Lr}^2 \cdot R_{DS\_dr}) dt + \int_{t_8}^{t_12} (i_{Lr}^2 \cdot R_{DS\_dr}) dt + \int_{t_12}^{t_13} (2 \cdot i_{Lr}^2 \cdot R_{DS\_dr}) dt$$  \hspace{1cm} (3.25)

$$P_{dr\_gate} = 5 \cdot V_{D\_dr} \cdot Q_{G\_dr} \cdot f_s$$  \hspace{1cm} (3.26)

$$P_{dr\_out} = \frac{5}{2} \cdot V_{dss}^2 \cdot C_{OSS\_dr} \cdot f_s$$  \hspace{1cm} (3.27)

3. Conduction loss $P_{cond}$ is calculated in Equation (3.28), where $I_o$ is the drain-to-source current when the power MOSFET is on, $R_{dr\_on}$ is the on-resistance of the MOSFET, $T_{on}$ is the on time and $T_s$ is the switching period.

$$P_{cond} = I_o^2 \cdot R_{dr\_on} \cdot \frac{T_{on}}{T_s}$$  \hspace{1cm} (3.28)

4. The output loss, $P_{out}$ is calculated in Equation (3.29), where $V_{in}$ is the drain-to-source voltage across the MOSFET when it is off, $C_{oss}$ is the output capacitance of the MOSFET.

$$P_{out} = \frac{V_{in}^2}{2 \cdot C_{oss} \cdot f_s}$$  \hspace{1cm} (3.29)

5. The total loss for the power MOSFET driven with the proposed CSD, $P_{sum}$, is given in Equation (3.30).

$$P_{sum} = P_{dr} + P_{sw} + P_{cond} + P_{out}$$  \hspace{1cm} (3.30)

3.3 Optimal Design of Current Source Driver

According to Equation (3.5) and (3.21), the RMS current of the CSD during precharge and predischarge interval, $I_{Lr\_RMS}$, is calculated in Equation (3.31).
\[ I_{L_{r\_RMS}} \approx \frac{V_c \cdot T_{pre}}{L_c} \sqrt{\frac{T_{pre} f_s}{3}} \quad (3.31) \]

The conduction loss at these two intervals is proportional to the precharge time \( T_{pre} \), and it is the same for gate energy recovery interval since during charging and discharging the current in the CSD inductor roughly remains constant. Therefore, \( T_{pre} \) should be set as short as possible within the practical limits of the driver to minimize the conduction loss. Taken the logic limits into consideration, \( T_{pre} \) is set to be 20 nanoseconds. And it needs to be pointed out that the design procedure presented here is also applicable to other conditions.

In order to maximize the overall efficiency of the buck converter with the proposed CSD, \( P_{sum} \) should be minimized. Since the conduction loss and output loss for power MOSFET are relatively constant for the given duty cycle and load current, the optimal design of the CSD involves a tradeoff between driver loss and switching loss, and there is an optimal inductor current, \( I_{L_{r\_opt}} \), where \( P_{sum} \) reaches the minimum value. With \( T_{pre} \) fixed to 20ns and according to Equation (3.31), it can be inferred that there also exists an optimal current source inductor, \( L_{r\_opt} \), as given in Equation (3.32).

\[ L_{r\_opt} = \frac{V_c \cdot T_{pre}}{I_{L_{r\_opt}}} \quad (3.32) \]

To validate the analysis, the following conditions are assumed: \( V_{in}=12V, V_o=1.3V, I_o=30A, V_c=5V, f_s=1MHz, Q: \) SI7386DP. Typically, the parasitic inductance value for Power PAK SO-8 package is tested by the semiconductor manufacturers in [45] - [46] and range from approximately 250pH-1nH. In the models of this chapter, \( L_s=1nH, L_D=1nH \) are assumed.

Figure 3.5 illustrates the numerical plot of the equation \( P_{sum} \) versus different CSD inductor values within practical range using MathCAD. It is noted that, in comparison with the driver loss, the switching loss is the dominant loss of the power MOSFET. It is observed that the optimal
current source inductor is around 25nH, where $P_{\text{sum}}$ is the minimum. As is shown in Figure 3.6, the peak inductor current at this moment equals 4A.

Figure 3.5 Total Loss VS. Current Source Inductor

Figure 3.6 Peak current VS. Current Source Inductor
3.4 Experimental Results and Discussions

3.4.1 Hardware Setup

A prototype of a synchronous buck converter as shown in Figure 3.7 was built to verify the proposed switching loss model and the optimal design of the current source inductor. The control FET of the converter is driven with the proposed CSD, while the SR is driven with a conventional voltage source driver since the switching loss for SR is very small.

![Figure 3.7 Synchronous buck converter with the proposed CSD](image)

The PCB consists of 6 layer 4 oz copper, and the picture of the prototype is shown in Figure 3.8. The components used in the circuit are: \( Q_1 \): Si7386DP; \( Q_2 \): IRF6691; output filter inductance: \( L_f = 330 \, \text{nH} \) (IHLP-5050CE-01); current-source inductor: \( L_r = 23 \, \text{nH} \) (Coilcraft 2508-23N_L); drive switches \( S_1 \sim S_5 \): FDN335; Anti-diodes \( D_{s1} \sim D_{s5} \): MBR0520. Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. For common practice, the driver voltages for the control FET and SR are both set to be 5V. The operating conditions are: input voltage \( V_{in} \): 12V; output voltage \( V_o \): 1.2V–1.5V; switching frequency \( f_s \): 500kHz–1MHz.
Figure 3.8 Photo of the buck converter driven with CSD shown in Figure 3.1

The gate driver signals for $V_{gs,Q1}$ and $V_{gs,Q2}$ are shown in Figure 3.9. It is observed that during turn off transition, $V_{gs,Q1}$ is clamped to about -3.5V. The current waveform of the CSD inductor is impossible to obtain without breaking the setup of the prototype.

Figure 3.9 The waveforms of driver signals $V_{gs,Q1}$ & $V_{gs,Q2}$

Figure 3.10 shows the efficiencies of 1.3V output at 1MHz, 750 kHz, and 500 kHz respectively. It is observed that at 30A load current, when frequency decreases from 1MHz to 500
kHz, the overall efficiency increases from 84.0% to 86.8%, thanks to the reduction of the frequency-dependent loss.

Figure 3.10 Efficiencies of 1MHz, 750kHz, 500kHz for 12V input, 1.3V output

Figure 3.11 summarizes the efficiencies of the CSD with the optimal inductor for 1.2V, 1.3V and 1.5V output respectively at 1MHz switching frequency. It can be observed that at 30A load current, when output voltage increases from 1.2V to 1.5V, the efficiency increases from 82.8% to 85.1%; and the highest efficiency at 1.5V output is 89.8% for a 15A load.
3.4.2 Verification and Discussions of the Proposed Switching Loss Model

1. Verification of the Proposed Switching Loss Model
In addition to the loss for control FET illustrated in Section 3.2, the loss of the buck converter in Figure 3.7 also includes the following major losses, output inductor loss and SR loss.

(1) Loss for output inductor
Under continuous current mode, there is always current flowing through the output inductor. Therefore, the parasitic resistance of the output inductor, often called DCR, introduces conduction loss. The accurate calculation of this portion of loss should consider the ripple of the inductor current as shown in Figure 3.12.

Figure 3.11 Efficiencies of 1.2V, 1.3V, 1.5V output for 12V input, 1MHz frequency
The RMS of the inductor current, \( I_{\text{in,RMS}} \) is calculated in Equation (3.33) \[19\]. And the conduction loss for inductor is calculated in Equation (3.34), where \( I_o \) is the load current of the buck converter, \( V_o \) is the output voltage, \( V_{in} \) is the input voltage, \( T_s \) is the switching period, \( L_o \) is the value of the output inductor and DCR is the parasitic resistance of the output inductor.

\[
I_{\text{in,RMS}} = \sqrt{\frac{\int_0^{DT_s} i_o^2 dt + \int_0^{T_s} i_o^2 dt}{T_s}} = \sqrt{\frac{I_o^2 + V_o (V_{in} - V_o) T_s}{12 L_o V_{in}}}
\]

(3.33)

\[
P_{in} = I_{\text{in,RMS}}^2 \cdot \text{DCR} = \left[ I_o^2 + \frac{V_o (V_{in} - V_o) T_s}{12 L_o V_{in}} \right] \cdot \text{DCR}
\]

(3.34)

(2) Loss for SR of the buck converter

The loss for SR consists of conduction loss, gate driver loss, reverse recovery loss and switching loss.

The gate driver loss \( P_{dr,SR} \) is given in Equation (3.35), where \( Q_{g,SR} \) is the total gate charge for SR, \( V_{c,SR} \) is the gate drive voltage for SR and \( f_s \) is the switching frequency.

\[
P_{dr,SR} = Q_{g,SR} \cdot V_{c,SR} \cdot f_s
\]

(3.35)

Conduction loss \( P_{\text{cond,SR}} \) is calculated in Equation (3.36), where \( R_{\text{dr(on)},SR} \) is the on-resistance of the SR, \( T_{\text{on,SR}} \) is the on-time of the SR and \( T_s \) is the switching period.

\[
P_{\text{cond,SR}} = I_{\text{in,RMS}}^2 \cdot R_{\text{dr(on)},SR} \cdot \frac{T_{\text{on,SR}}}{T_s}
\]

(3.36)
Reverse recovery loss for SR $P_{RR,SR}$ is calculated in Equation (3.37), where $V_{in}$ is the drain-to-source voltage across the SR when it is off, $Q_{RR,SR}$ is the body diode’s reverse recovery charge of the SR.

$$P_{RR,SR} = V_{in}^2 \cdot Q_{RR,SR} \cdot f_s$$  \hspace{4cm} (3.37)

The switching loss of the SR $P_{SW,SR}$ is made up of the turn on loss $P_{SW(on),SR}$ and turn off loss $P_{SW(off),SR}$ of SR, as shown in Equation (3.38).

$$P_{SW,SR} = P_{SW(on),SR} + P_{SW(off),SR}$$  \hspace{4cm} (3.38)

The equations for $P_{SW(on),SR}$ and $P_{SW(off),SR}$ are shown in Equation (3.39) and Equation (3.40) provided in [18], where $V_{th,SR}$ is the gate threshold voltage of the SR, $g_{fs,SR}$ is the transconductance of the SR, $R_{dr,SR}$ is the on-resistance of the driver, $R_{g,SR}$ is the gate resistance of the SR, $C_{iss,SR}$ is the input capacitance of the SR, $V_{f,SR}$ is the forward voltage drop of the SR, $V_{spe,SR}$ is the specified gate voltage of the SR according to the datasheet, $R_{ds(on),SR}$ is the on-resistance of the SR when gate drive voltage equals $V_{spe,SR}$.

$$P_{SW(on),SR} = \ln \left( \frac{V_{c,SR} - V_{th,SR}}{V_{c,SR} - V_{th,SR} - I_o / g_{fs,SR}} \cdot \left( R_{dr,SR} + R_{g,SR} \right) \cdot C_{iss,SR} \cdot V_{f,SR} \right) + \ln \left( \frac{V_{c,SR} - V_{th,SR} - I_o / g_{fs,SR}}{2} \cdot V_{f,SR} + I_o \cdot 1.1 \cdot R_{ds(on),SR} \right) \cdot I_o \cdot f_s$$  \hspace{4cm} (3.39)

$$P_{SW(off),SR} = \ln \left( \frac{V_{th,SR} + I_o / g_{fs,SR}}{V_{th,SR}} \cdot \left( R_{dr,SR} + R_{g,SR} \right) \cdot C_{iss,SR} \cdot V_{f,SR} \right) + \ln \left( \frac{0.9 \cdot V_{spe,SR}}{V_{th,SR} + I_o / g_{fs,SR}} \cdot \left( V_{f,SR} + I_o \cdot 1.1 \cdot R_{ds(on),SR} \right) \cdot I_o \cdot f_s \right)$$  \hspace{4cm} (3.40)

(3) Comparison between the calculated total loss and experimentally measured loss

In order to validate the accuracy of the proposed switching loss model, the calculated total loss of the synchronous buck converter as a function of load current is compared to the experimentally measured loss in Figure 3.13. It is observed that the calculated loss by the loss model proposed in this chapter matches the actual loss of the synchronous buck converter very
well. The difference between the calculated loss and experimentally measured loss is less than 10% across all load levels from 5A to 30A.

![Comparison between Measured Loss and Calculated Loss](image)

Figure 3.13  Comparison between measured loss and calculated loss
(Top numbers: calculated loss; bottom numbers: measured loss)

2. Loss Breakdown of the Synchronous Buck Converter
The loss breakdown of the calculated loss of the synchronous buck converter is illustrated in Figure 3.14. It is observed that for Control FET of the synchronous buck converter, switching loss is the dominant loss, taking up 2.83W out of the 7.56W of total loss (37%); while for SR, the conduction loss is the dominant loss which is taking up 20% of the total loss.
3. Switching Loss of Control FET Vs. Load Current

The calculated switching loss of the control FET is plotted as a function of the load current in Figure 3.15 to study their relationship. First order linear fitting and second order linear fitting are made respectively to the points obtained from the proposed switching loss model [47]. It is observed that the coefficient of determination, $R^2$, for second order polynomial fitting is 0.99, which is larger than the $R^2$ for first order polynomial fitting (0.83). Since the larger $R^2$ is, the better the fitting represents the data, so it is inferred that second order linear fitting matches the calculated switching loss points for control FET better. In other words, the switching loss for control FET almost increases proportionally to $I_o^2$.  

![Figure 3.14 Calculated loss breakdown of the synchronous buck converter](image)

**Calculated Loss Breakdown of Synchronous Buck Converter**

- Vin=12V, Vo=1.3V, Io=30A,
- Lo=330nH, Fs=1MHz
The physics behind the quadratic relationship between the switching loss of control FET and load current is the gate-to-source voltage clamping due to the gate current diversion during drain current rising and drain current drop intervals, as analyzed in Section 3.2. The equivalent switching circuits in these two intervals are shown in Figure 3.16.

The KVL equation for drain current rising is given in Equation (3.41), while the equation for drain current drops is given in Equation (3.42), where $T_r$ is the current rising time and $T_f$ is the...
current falling time, $V_{on}$ and $V_{off}$ is the clamped gate-to-source voltage due to the gate current diversion during drain current rises or drops.

$$L_S \frac{d}{dt}(i_{DS}) = L_S \frac{\Delta i_{DS}}{\Delta t} = L_S \frac{I_s}{T_r} = V_{on} - i_G R_g - V_{CGS}$$  

(3.41)

$$L_S \frac{d}{dt}(i_{DS}) = L_S \frac{\Delta i_{DS}}{\Delta t} = L_S \frac{I_o}{T_f} = -i_G R_g + V_{CGS} - V_{off}$$  

(3.42)

It is inferred, from Equation (3.41) and (3.42), that both $T_r$ and $T_f$ are proportional to load current $I_o$. Therefore, the switching loss of control FET, $P_{sw\_control}$ as approximated in Equation (3.43) is almost proportional to $I_o^2$.

$$P_{sw} = P_{sw\_on} + P_{sw\_off} = \frac{V_{ds\_rising} I_s T_r}{2} + \frac{V_{ds\_drop} I_o T_f}{2}$$  

(3.43)

$$\approx \frac{1}{2} \left( \frac{V_{on} - i_G R_g - V_{CGS}}{L_S} + \frac{V_{off}}{L_S} \right) I_o^2$$

It is noted that the relationship between the switching loss of control FET and load current for conventional VSD is also the quadratic except for the coefficients for VSD is larger than those for CSD - it is observed from Equation (3.43) that during drain current drop interval, the clamped gate-to-source voltage, $V_{off}$ affects the turn off loss to a great extent. The more negative $V_{off}$ is, the smaller the turn off loss is introduced. The $V_{off}$ for the proposed CSD in Figure 3.11 is -3.5V, and $V_{off}$ for existing CSD in [44] is -0.7V, while for conventional VSD, $V_{off}$ is roughly +0.5V. Therefore, the proposed CSD in Figure 3.11 is supposed to have smaller switching loss than existing CSD in [44]; both CSDs introduce smaller switching loss than conventional VSD.

4. Comparison of the Calculated Loss among the Proposed CSD, Existing CSD and VSD

The calculated switching loss comparison among the proposed CSD in Figure 3.11, existing CSD in [44] and conventional VSD is shown in Figure 3.17. It is noted that the proposed CSD in Figure 3.11 has the smallest total switching loss due to the negative gate-to-source voltage during turn off transition. The calculated total loss comparison between these three drivers is illustrated in Figure 3.18. It is observed that because of the switching loss reduction, the proposed CSD has much smaller total loss than the conventional VSD and existing CSDs.
Switching Loss Comparison between Proposed CSD, Existing CSD and VSD

<table>
<thead>
<tr>
<th>Load Current (A)</th>
<th>Proposed CSD</th>
<th>Existing CSD</th>
<th>Conventional VSD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.092</td>
<td>0.48</td>
<td>0.14</td>
</tr>
<tr>
<td></td>
<td>0.326</td>
<td>0.711</td>
<td>0.711</td>
</tr>
<tr>
<td></td>
<td>0.91</td>
<td>1.77</td>
<td>2.479</td>
</tr>
<tr>
<td></td>
<td>1.469</td>
<td>4.328</td>
<td>3.428</td>
</tr>
<tr>
<td></td>
<td>2.411</td>
<td>5.221</td>
<td>3.86</td>
</tr>
</tbody>
</table>

Calculate Switching Loss of Proposed CSD
Calculate Switching Loss of Existing CSD
Calculate Switching Loss of Conventional VSD

Figure 3.17 Calculated switching loss comparison between the proposed CSD (Figure 3.1), existing CSD [44] and VSD

Calculated Loss Comparison among Proposed CSD, Existing CSD and VSD

<table>
<thead>
<tr>
<th>Load Current (A)</th>
<th>Proposed CSD</th>
<th>Existing CSD</th>
<th>Conventional VSD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.15</td>
<td>1.19</td>
<td>1.17</td>
</tr>
<tr>
<td></td>
<td>1.73</td>
<td>2.00</td>
<td>2.00</td>
</tr>
<tr>
<td></td>
<td>2.67</td>
<td>3.30</td>
<td>3.30</td>
</tr>
<tr>
<td></td>
<td>3.98</td>
<td>5.05</td>
<td>5.05</td>
</tr>
<tr>
<td></td>
<td>5.22</td>
<td>6.33</td>
<td>6.33</td>
</tr>
<tr>
<td></td>
<td>7.56</td>
<td>8.59</td>
<td>8.59</td>
</tr>
</tbody>
</table>

Figure 3.18 Calculated total loss comparison between proposed CSD (Figure 3.1), existing CSD [44] and VSD
3.4.3 Verification of the Optimal Design of the CSD Inductor

To validate the optimal design of the CSD inductor, an apple-to-apple comparison between the synchronous buck converters with a 25nH and a 43nH CSD inductor is made. Figure 3.19 illustrates the efficiency comparison for two prototypes at 1.3V/1MHz output. It is noted that, comparing to the CSD with 43nH, the CSD with the optimal CSD inductor increases the efficiency at all load currents, improving from 86.1% to 87.6% by 1.5% at 20A load, and from 82.4% to 84.0% by 1.6% at 30A load.

![Efficiency Comparison for Different CSD Inductors](image)

Figure 3.19 Efficiency comparison for different CSD inductors at 12V input, 1.3V output, 1MHz

3.4.4 Comparison between CSD and Commercial Products

The integrated Driver-MOSFET (DrMOS) provides the optimal solution for multiphase synchronous buck converter for its high power density and reduced design time. Compared with DrMOS from industries, the synchronous buck converter driven with the optimized proposed CSD can achieve better performance.

Figure 3.20 illustrates the loss comparison between optimized CSD and DrMOS from Renesas [48]. It is noted that optimized CSD has smaller loss across all load levels (5A~30A load).
and at 30A/1.3V load in 500kHz switching frequency, the optimized CSD can save nearly half Watt loss (0.46W). In addition, from the standpoint of the thermal performance, the optimized CSD is better than DrMOS, since the typical package for DrMOS is 8 mm by 8 mm by 0.95 mm – in such a small package, even for the same amount of loss, the DrMOS has higher temperature than the optimized CSD.

![Figure 3.20 Comparison between optimized CSD and DrMOS from Renesas](image)

While the loss comparison between optimized CSD and DrMOS-IP2005 [48] from International Rectifier is shown in Figure 3.21, from which it is observed that optimized CSD can save nearly a quarter Watt (0.24W) at 1.3V/30A load in 1MHz switching frequency.
3.5 Conclusions

In this chapter, a new accurate switching loss model which considers the current diversion is presented for power MOSFET driven by a Current Source Driver (CSD), and analytical equations for each interval are derived. Based on the proposed model, the optimal current source inductor is obtained to achieve the maximum overall efficiency of the synchronous converter. The experimental results verify the proposed switching loss model. The variation between the calculated loss and the experimentally measured loss is within 0.2W from 5A load to 30A load. The optimal design of the CSD inductor is also validated by the experimental results. Compared with the previous work, the CSD with optimal inductor improves the efficiency by 1.6% at 1.3V output 30A load in 1MHz switching frequency. The buck converter with optimized CSD can achieve better performance than DrMOSs from Renesas and International Rectifier.
Chapter 4 A New Inductorless Bipolar Gate Driver for Control FET of High Frequency Buck Converters

4.1 Introduction

Recently, there is a trend to increase the switching frequency of voltage regulators (VRs) above 1MHz ([3], [50] - [52]). The primary barrier to increase switching frequency for conventional VSD is the frequency-dependent losses, such as switching loss, gate drive loss and MOSFE output capacitance loss. RGDs are able to recover part of the gate drive loss ([25] - [30]). However, they cannot reduce the switching loss, which is the dominant part of the overall frequency-dependent loss.

CSDs can reduce the switching loss with a constant current to charge and discharge the power MOSFET. Particularly, it is noted that the basic benefit of the CSDs during turn off transition is to turn off the power MOSFET with a negative voltage. Compared with the previous gate drivers, the bipolar CSD presented in Chapter 2 can achieve much faster turn off speed by turning off the power MOSFET with a flexible negative voltage (such as -3.5V).

However, as the number of the transistor on the microprocessor expands exponentially, the demand of higher power density for VRs becomes more and more urgent. Under this circumstance, the inductor required in the CSDs becomes the bottle neck to facilitate the complete integration of the driver, either in the way of System in a Package (SIP) or System on a Chip (SoP), since it is very hard for CSD inductor to be integrated into the driver chip. Therefore, a new gate driver, which can achieve bipolar gate driver but do not have an inductor, is needed. Hence, a novel inductorless bipolar gate driver is presented in this chapter to reduce the turn off time and switching loss of the power MOSFETs. The proposed gate driver can turn off the power MOSFETs with a negative voltage, which will significantly increase the turn off speed and
reduce the turn off loss. What is more, the proposed gate driver can be fully integrated into a chip since no inductor is needed in the driver circuit.

Section 4.2 presents the topology of the proposed inductorless bipolar gate driver along with its operating principles; in addition, the analytical equations are derived in this Section as well. Section 4.4 illustrates the advantages of the proposed gate driver; calculated switching loss from the modeling and simulated turn off transition from computer simulation are also presented to validate the benefits of the proposed gate driver. Section 4.5 shows the experimental results and associated discussions that verify the advantages of the proposed gate driver over the conventional driver. Finally, the conclusions are drawn in Section 4.6.

4.2 Operation Principle of the Proposed Inductorless Bipolar Gate Driver

The conventional VSD is illustrated in Figure 4.1 to drive the power MOSFET, \( M \), whose parasitics are shown in blue color: \( R_G \) is the gate resistance, \( C_{GS} \) is the gate-to-source capacitance, \( C_{GD} \) is the gate-to-drain capacitance, \( C_{DS} \) is the drain-to-source capacitance, \( L_S \) is the common source inductance including the bonding wire inside the MOSFET package and PCB trace inductance and \( L_D \) is the switching loop inductance. The conventional VSD has a totem pole configuration, which turns on the MOSFET by turning on the top switch of VSD, \( S_T \); while turns off the MOSFET by turning on the bottom switch of VSD, \( S_B \).
The switching waveforms associated with Figure 4.1 are shown in Figure 4.2, where PWM is the PWM signal input of the VSD, \( V_{CGS} \) is the voltage across the \( C_{GS} \) of \( M \), \( V_{DS} \) is the drain-to-source voltage across \( M \), \( i_{DS} \) is the drain-to-source current flowing through the \( M \), \( P_{on} \) is the turn on loss and \( P_{off} \) is the turn off loss. It is noted that turn off loss is the dominant loss of the total switching loss \( P_{switch} \). It is also observed that, due to the effect of the parasitic inductance, \( V_{DS} \) reduces sharply when \( i_{DS} \) starts to increases at \( t_1 \) and then keeps at a plateau during \((t_1, t_2)\) since the rising rate of \( i_{DS} \) is almost constant in this interval.

Figure 4.2 Switching waveforms of power MOSFET driven by the conventional VSD
The equivalent circuit of the MOSFET driven by the VSD during turn off transition is given in Figure 4.3. When $S_N$ in Figure 4.1 is turned on, because of the on resistance of $S_N$ (larger than $0.5\Omega$), the voltage appearing across the gate-to-source of power MOSFET, $V_{GS}$, is around $0.5V$. Therefore, the main drawback of VSD is that $V_{GS}$ is unipolar, which means $V_{GS}$ is always bigger than zero, even during turn–off transition. It seriously limits the turn off speed, especially in the presence of the common source inductance in high frequency application as described below.

![Figure 4.3 Equivalent circuit of the MOSFET driven by VSD during turn off transition](image)

An inductorless bipolar gate driver is proposed to drive the control FET of the synchronous buck converter as is shown in Figure 4.4. The synchronous rectifier is still driven by the conventional unipolar gate driver as its switching loss is very small. The proposed gate driver consists of two driver switches ($S_1$ and $S_2$), two capacitors ($C_1$ and $C_2$), and one schottky diode ($D_1$).
Figure 4.4 Topology of the proposed inductorless bipolar gate driver

The key waveforms of the proposed gate driver are shown in Figure 4.5. $V_{GS,Q1}$ and $V_{GS,Q2}$ are the driver signals for driver switches $S_1$ and $S_2$; $V_{CGS,Q1}$ and $V_{CGS,Q2}$ are the gate-source voltages of $Q_1$ and $Q_2$ respectively; $V_{DS,Q1}$ is the drain-source voltage of $Q_1$; $I_{DS,Q1}$ is drain-source current of $Q_1$; $V_{SW}$ is the switching point of the synchronous buck converter.

The main feature of the proposed gate driver is that it can turn on $Q_1$ with a positive voltage, and turn it off with a negative voltage. As a result, it is termed as “bipolar gate driver”, which is opposed to the “unipolar gate driver”. The detailed operations for $C_1$ and $C_2$ to build up voltage will be explained in Section 4.3.
4.3 Analysis and Modeling of Switching Intervals with the Proposed Inductorless Bipolar Gate Driver

In this section, the detailed operation of the proposed inductorless bipolar gate driver will be covered. In addition, the piecewise modeling is made to derive the equations for the \( V_{gs}, I_{ds} \) and \( V_{ds} \). Based on the modeling and equations, the calculated switching loss comparison between the proposed inductorless bipolar gate driver and conventional gate driver is made to validate the
advantage of the proposed gate driver. Simulation results are also provided to support the advantage of the proposed gate driver. Time period \([t_0, t_5]\) is the turn on transition of \(Q_1\), while the turn off transition is the interval between \([t_6, t_{11}]\).

Before \(t_0\), assume \(Q_1\) is in the OFF state and \(Q_2\) is in the ON state. Therefore, \(V_{SW}\) is almost clamped to GND by \(Q_2\). \(C_1\) is charged to \(V_{C1}\) through the path shown in Figure 4.6 and the voltage across \(C_2\) keeps unchanged.

![Figure 4.6 Equivalent circuit for \(C_1\) being charged to \(V_{C1}\)](image)

At \(t_0\), \(S_2\) is turned off. After a short period of dead time \([t_0, t_1]\), the turn on transition of \(Q_1\) begins at \(t_1\). The turn on transition is made up of four intervals: turn on delay \([t_1, t_2]\), current rising \([t_2, t_3]\), Miller Plateau \([t_3, t_4]\) and the remaining gate charge \([t_4, t_5]\).

### 4.3.1 Turn On Transition:

A. Turn on Delay \([t_1, t_2]\): at \(t_1\), \(S_1\) is turned on, and gate drive voltage \(V_{C1}\) is applied across the gate and the source of the power MOSFET. The gate charge current \(i_G\) charges the input capacitance \(C_{ISS1}\) of the power MOSFET, which is the combination of the gate-to-source capacitance \(C_{GSI}\) and the gate-to-drain capacitance \(C_{GDI}\). This interval ends when \(v_{CGSI} = V_{TH}\) at...
The equivalent circuit of this interval is shown in Figure 4.7 A.

The KVL equations for this interval are given in Equation (4.1). The characteristic equation is of the form in Equation (4.2) with poles at $p_1$ and $p_2$ as given in Equation (4.3). The parameters in Equation (4.4) and Equation (4.5) are the neper frequency $\alpha_1$, and the resonant frequency $\omega_1$, where $R_{on1}=R_{ds(on)S1}+R_g$, where $R_{ds(on)S1}$ is the on-resistance of $S_1$ and $R_g$ is the gate resistance of the power MOSFET.

$$V_C1 = L_{S1} \frac{d}{dt}(i_{G1}) + i_{G1}R_{on1} + V_{CGS1}, \ i_{G1} = (C_{GS1} + C_{GD1}) \frac{d}{dt}(V_{CGS1})$$

$$s^2 + \left(\frac{R_{on1}}{L_{S1}}\right)s + \left(\frac{1}{L_{S1}(C_{GS1} + C_{GD1})}\right) = (s + p_1)(s + p_2)$$

$$p_1 = -\frac{R_{on1}}{2L_{S1}} + \sqrt{\left(\frac{R_{on1}}{2L_{S1}}\right)^2 - \frac{1}{L_{S1}(C_{GS1} + C_{GD1})}} = -\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2}$$

$$p_2 = -\frac{R_{on1}}{2L_{S1}} - \sqrt{\left(\frac{R_{on1}}{2L_{S1}}\right)^2 - \frac{1}{L_{S1}(C_{GS1} + C_{GD1})}} = -\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2}$$

$$\alpha_1 = \frac{R_{on1}}{2L_{S1}}$$

$$\omega_1 = \frac{1}{\sqrt{L_{S1}(C_{GS1} + C_{GD1})}}$$

Mathematically, there are three possible forms for the equation of $v_{CGS1}$, the voltage across $C_{GS1}$: over damped, critically damped and under damped.

If $\alpha_1 < \omega_1$, the equation for $v_{CGS1}$ is sinusoidal as given in Equation (4.6) and the equation for $i_{G1}$ is given in Equation (4.7).

$$v_{CGS1} = [A_1 \cos(\omega_1^2 - \alpha_1^2)t + B_1 \sin(\omega_1^2 - \alpha_1^2)t] e^{-\alpha_1 t} + C_1$$

$$i_{G1} = (C_{GS1} + C_{GD1})[(-A_1 \sqrt{\omega_1^2 - \alpha_1^2} + B_1 \alpha_1) \sin(\omega_1^2 - \alpha_1^2)t)$$

$$+ (-A_1 \alpha_1 - B_1 \sqrt{\omega_1^2 - \alpha_1^2}) \cos(\sqrt{\omega_1^2 - \alpha_1^2}t)] e^{-\alpha_1 t}$$

where $A_1 = -V_{C1}/[L_{S1}(C_{GS1} + C_{GD1})\omega_1^2]$, $B_1 = \sqrt{\omega_1^2 - \alpha_1^2} \alpha_1 V_{C1}/((C_{GS} + C_{GD})(\alpha_1^2 - \omega_1^2)\omega_1^2 L_{S1})$, $C_1 = -A_1$
If $\alpha_1 > \omega_1$, the equation for $v_{CGS1}$ is exponential as given in Equation (4.8) and the equation for $i_{G1}$ is given in Equation (4.9).

$$v_{CGS1} = A_2 e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})t} + B_2 e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t} + C_2$$  \hspace{1cm} (4.8)

$$i_{G1} = (C_{GS1} + C_{GD1})[A_1(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})e^{(-\alpha_1 + \sqrt{\alpha_1^2 - \omega_1^2})t} + B_1(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})e^{(-\alpha_1 - \sqrt{\alpha_1^2 - \omega_1^2})t}]$$  \hspace{1cm} (4.9)

Where

$$A_1 = -V_C([\alpha_1^2 - \omega_1^2] + \alpha_1 \sqrt{\alpha_1^2 - \omega_1^2})/[2L_S (C_{GS1} + C_{GD1}) \omega_1^2(\alpha_1^2 - \omega_1^2)]$$

$$B_1 = -V_C([\alpha_1^2 - \omega_1^2] - \alpha_1 \sqrt{\alpha_1^2 - \omega_1^2})/[2L_S (C_{GS1} + C_{GD1}) \omega_1^2(\alpha_1^2 - \omega_1^2)]$$

$$C_2 = V_C/[2L_S (C_{GS1} + C_{GD1}) \omega_1^2]$$

From practical standpoint, the driver resistance $R_{on1}$ is typically 3Ω, therefore in most cases $\alpha_1 > \omega_1$, and the equations for $v_{CGS1}$ and $i_{G1}$ have the real roots.

B. Drain Current Rising [$t_2$, $t_3$]: At $t_2$, $v_{CGS1} = V_{TH}$. During this interval, $v_{CGS1}$ keeps increasing, and the drain current $i_{DS1}$ starts to rise according to the relationship in Equation (4.10).

$$i_{DS1} = g_{m1}(v_{CGS1} - V_{TH})$$  \hspace{1cm} (4.10)

The equivalent circuit is shown in Figure 4.7 B. At this interval, $i_{DS1}$ rises from 0 to $I_o$, the load current. Since $i_{DS1}$ flows through $L_{S1}$, the large voltage is induced across $L_{S1}$, making $i_{G1}$ drop sharply. The initial condition of this interval is $I_{G1,t_2} = i_{G1}(t_2-t_1)$, $I_{DS1,t_2}=0$, and $V_{CGS1,t_2}=V_{TH1}$. The interval ends at $t_3$ when $i_{DS1}$ equals the load current, $I_o$. The equations $v_{CGS1}$ and $v_{DS1}$ are given in Equation (4.11), which has the same form of the solutions as Equation (4.1).

The neper frequency $\alpha_2$ is given in Equation (4.12) and the resonant frequency $\omega_2 = \omega_1$.

$$V_{C1} = L_{S1} \frac{d}{dt}(i_{G1} + i_{DS1}) + i_{G1} R_{on1} + v_{CGS1}$$

$$i_{G1} = (C_{GS1} + C_{GD1}) \frac{d}{dt}(v_{CGS1})$$

$$i_{DS1} = g_{m1}(v_{CGS1} - V_{TH})$$  \hspace{1cm} (4.11)
\[ \alpha_2 = \frac{(C_{GS1} + C_{GD1})R_{on} + L_{s1}g_{f1}}{2L_{s1}(C_{GS1} + C_{GD1})} \]  
(4.12)

If \( \alpha_2 < \omega_1 \), the equation for \( v_{CGS1} \) is sinusoidal as given in Equation (4.13) and the equations for \( i_{G1} \), \( i_{DS1} \) and \( v_{DS1} \) are given in Equation (4.14) ~ (4.16) respectively.

\[ v_{CGS1} = [A_3 \cos(\sqrt{\omega_1^2 - \alpha_2^2} t) + B_3 \sin(\sqrt{\omega_1^2 - \alpha_2^2} t)]e^{-\alpha_2 t} + C_3 \]  
(4.13)

\[ i_{G1} = (C_{GS1} + C_{GD1})[(-A_3 \sqrt{\omega_1^2 - \alpha_2^2} + B_3 \alpha_2) \sin(\sqrt{\omega_1^2 - \alpha_2^2} t) \]
\[ + (-A_2 \alpha_2 - B_3 \sqrt{\omega_1^2 - \alpha_2^2}) \cos(\sqrt{\omega_1^2 - \alpha_2^2} t)]e^{-\alpha_2 t} \]  
(4.14)

\[ i_{DS1} = g_{f1}([A_3 \cos(\sqrt{\omega_1^2 - \alpha_2^2} t) + B_3 \sin(\sqrt{\omega_1^2 - \alpha_2^2} t)]e^{-\alpha_2 t} + C_3 - V_{TH1}) \]  
(4.15)

\[ v_{DS1} = V_{in} -(L_{s1} + L_{d1}) \frac{di_{DS1}}{dt} - L_{s1} \frac{di_{G1}}{dt} \]  
(4.16)

Where

\[ A_3 = -(2L_s(\alpha_2 I_{G-r2} + V_C1)\left[ L_{s1}(C_{GS1} + C_{GD1})\omega_1^2 \right] \]

\[ B_3 = \sqrt{\omega_1^2 - \alpha_2^2} (2L_s \alpha_2^2 I_{G-r2} - L_{s1} \omega_1^2 I_{G-r2} + V_C1 \alpha_2) \left[ L_{s1}(C_{GS1} + C_{GD1})\omega_1^2 (\alpha_2^2 - \omega_1^2) \right] \]

\[ C_3 = [2L_{s1} \alpha_2 I_{G-r2} + L_{s1} (C_{GS1} + C_{GD1}) \omega_1^2 V_{TH1} + V_C1] \left[ L_{s1}(C_{GS1} + C_{GD1})\omega_1^2 \right] \]

If \( \alpha_2 > \omega_1 \), the equation for \( v_{CGS1} \) is exponential as given in Equation (4.8) and the equation for \( i_{G1} \), \( i_{DS1} \) and \( v_{DS1} \) are given in Equation (4.18) ~ (4.20) respectively.

\[ v_{CGS1} = A_4 e^{(-\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2})t} + B_4 e^{(-\alpha_2 - \sqrt{\alpha_2^2 - \omega_1^2})t} + C_4 \]  
(4.17)

\[ i_{G1} = (C_{GS1} + C_{GD1})[A_4(-\alpha_2 + \sqrt{\alpha_2^2 - \alpha_2^2})e^{(-\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2})t} \]
\[ + B_4(-\alpha_2 - \sqrt{\alpha_2^2 - \alpha_2^2})e^{(-\alpha_2 - \sqrt{\alpha_2^2 - \omega_1^2})t}] \]  
(4.18)

\[ i_{DS1} = g_{f1}([A_4 e^{(-\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2})t} + B_4 e^{(-\alpha_2 - \sqrt{\alpha_2^2 - \omega_1^2})t} + C_4 - V_{TH1}) \]  
(4.19)

\[ v_{DS1} = V_{in} -(L_{s1} + L_{d1}) \frac{di_{DS1}}{dt} - L_{s1} \frac{di_{G1}}{dt} \]  
(4.20)

where

\[ A_4 = -(L_{s1} \alpha_2 I_{G-r2} + V_C1 + \sqrt{\alpha_2^2 - \omega_1^2} I_{G-r2} L_{s1}) \left[ \sqrt{\alpha_2^2 - \omega_1^2} \alpha_2 + \alpha_2^2 - \omega_1^2 \right] \left[ 2L_{s1}(C_{GS1} + C_{GD1})\omega_1^2 \sqrt{\alpha_2^2 - \omega_1^2} \right] \]
\[ B_4 = -\left(\alpha_2^2 - \omega_1^2 - \sqrt{\alpha_2^2 - \alpha_1^2} \right) (L_2 \alpha_2 I_{G_{t2}} - \sqrt{\alpha_2^2 - \alpha_1^2} I_{G_{t2}} L_{S1} + V_{C_1}) \left[ 2L_{S1} (C_{GSI} + C_{GDI}) (\alpha_2^2 - \omega_1^2) \right] \]

\[ C_4 = (2L_{S1} \alpha_2 I_{G_{t2}} + L_{S1} (C_{GSI} + C_{GDI}) \alpha_1^2 V_{TH1} + V_{C_1}) \left[ L_{S1} (C_{GSI} + C_{GDI}) \alpha_1^2 \right] \]

Since the driver is proposed for control FET of the buck converter, which has very small input capacitance \((C_{ISS}=C_{GSI}+C_{GDI})\), typically 1nC for control FET of the buck converter), therefore in most cases \(\alpha_2 > \omega_1\).

C. Miller Plateau \([t_3, t_4]\): At \(t_3\), \(i_{DS1} = I_o\). During this interval, \(v_{CGS1}\) is held at the Miller Plateau voltage \(V_{PL1} = V_{TH1} + I_o / g_{m1} I_{G1}\) mainly flows through the gate-to-drain capacitance of \(Q\), and \(v_{DS1}\) decreases accordingly. It is noted that \(i_{G1}\) starts to rapid increase since the EMF across \(L_s\) falls sharply due to the unchanged \(i_{DS1}\). The equivalent circuit is given in Figure 4.7 C. The initial values of the interval are \(I_{G1,t3}=I_{G1}(t_3-t_2)\), \(V_{CGS1,t3}=V_{CGS1}(t_3-t_2)\), and \(V_{DS1,t3}=V_{DS1}(t_3-t_2)\). The equations for \(v_{CGS1}, i_{G1}\) and \(v_{DS1}\) are given in Equation (4.21) ~ (4.23). The interval ends when \(v_{DS1}\) equals zero at \(t_4\).

\[ v_{CGS1} = V_{CGS1,t3} = V_{PL1} \quad (4.21) \]

\[ i_{G1} = \left[ I_{G1,t3} - (V_{C1} - V_{CGS1,t3}) / R_{out} \right] e^{(-R_{out} / C_{GDI}) t} + (V_{C1} - V_{CGS1,t3}) / R_{out} \quad (4.22) \]

\[ v_{DS1} = V_{DS1,t3} - \int \frac{\left[ I_{G1,t3} - (V_{C1} - V_{CGS1,t3}) / R_{out} \right] e^{(-R_{out} / C_{GDI}) t} + (V_{C1} - V_{CGS1,t3}) / R_{out} dt}{C_{GDI}} \quad (4.23) \]

D. Remaining Gate Charging \([t_4, t_5]\): At \(t_4\), \(V_{DS1} = 0\) and \(V_{CGS1}\) starts to rise again until it reaches \(V_{c1}\). Due to the rising of the \(v_{CGS1}\), \(i_{G1}\) decreases gradually. The equivalent circuit is given in Figure 4.7 D. The initial values of this interval are: \(I_{G1,t4}=I_{G1}(t_4-t_3)\), \(V_{CGS1,t4}=V_{CGS1,t3}\), \(V_{DS1,t4}=V_{DS1}(t_4-t_3)\). The equations for \(i_{G1}\) have the same format as the turn on delay interval except for different initial conditions.
A. \((t_1, t_2)\): Turn on Delay

B. \((t_2, t_3)\): Drain current Rising

C. \((t_3, t_4)\): Miller Plateau

D. \((t_4, t_5)\): Remaining Gate Charges

Figure 4.7 Turn on operation

During \([t_5, t_6]\), \(Q_1\) is clamped to ON state by \(S_1\). It is noted that \(V_{SW}\) equals \(V_{IN}\) during \([t_4, t_8]\). In this interval the voltage across \(C_2\) is recharged to \((V_{IN} - V_{D1})\), where \(V_{D1}\) is forward voltage drop of the schottky diode \(D_1\), while the voltage across \(C_1\) keeps unchanged. The equivalent circuit for \(C_2\) to be charged to \((V_{IN} - V_{D1})\) is shown in Figure 4.8.
Figure 4.8 Equivalent circuit for $C_2$ being charged to $(V_{IN} - V_D)$

At $t_6$, $S_1$ is turned off. After a short period of deadtime ([$t_6$, $t_7$]), $S_2$ is turned on at $t_7$. Of particular concern is that the voltage across $C_2$ is inversely applied to the gate-source capacitance of $Q_1$, which means $Q_1$ is turned off with a negative voltage $-(V_{IN} - V_D)$. By contrast, the conventional unipolar gate driver in Figure 4.4 only can turn off $Q_2$ with zero voltage. The turn off transition is also made up of four intervals: turn off delay ([$t_7$, $t_8$]), Miller Plateau ([$t_8$, $t_9$]), current dropping ([$t_9$, $t_{10}$]) and the remaining gate discharge ([$t_{10}$, $t_{11}$]).

4.3.2 Turn Off Transition:

A. Turn off Delay [$t_7$, $t_8$]: at $t_7$, $S_2$ is turned on, and a negative voltage $-(V_{IN} - V_D)$ is applied across the gate and the source of the power MOSFET. The gate charge current $i_G$ discharge the input capacitance $C_{ISS1}$ of the power MOSFET. The initial condition is $V_{CGS1}=V_{C1}$, $i_{G1}=0$. This interval ends when $v_{CGS1}= V_{TH} + I_D/g_{fs1}$ at $t_8$. The equivalent circuit of this interval is shown in Figure 4.9 A.

The equations for this interval have the same format as the turn on delay interval except for
different initial conditions. They also have three possible solutions: over damped, critically damped and under damped. The neper frequency $\alpha_3$, and the resonant frequency $\omega_3$ are given in Equation (4.24) and (4.25) respectively, where $R_{off1}=R_{dr(on)S2}+R_g$, where $R_{dr(on)S2}$ is the on-resistance of $S_2$.

$$\alpha_3 = \frac{R_{off1}}{2L_{S1}} \quad (4.24)$$

$$\omega_3 = \omega_1 \quad (4.25)$$

If $\alpha_3 < \omega_3$, the equation for $v_{CGS1}$ is sinusoidal as given in Equation (4.26) and the equation for $i_{G1}$ is given in Equation (4.27).

$$v_{CGS1} = [A_4 \cos(\sqrt{\omega_3^2 - \alpha_3^2}) t + B_5 \sin(\sqrt{\omega_3^2 - \alpha_3^2}) t] e^{-\alpha_3 t} + C_5 \quad (4.26)$$

$$i_{G1} = (C_{GS1} + C_{GD1}) [(-A_5 \sqrt{\omega_3^2 - \alpha_3^2} + B_5 \alpha_3 \sin(\sqrt{\omega_3^2 - \alpha_3^2}) t) + (-A_5 \alpha_3 - B_5 \sqrt{\omega_3^2 - \alpha_3^2} \cos(\sqrt{\omega_3^2 - \alpha_3^2}) t)] e^{-\alpha_3 t} \quad (4.27)$$

Where

$$A_5 = \frac{(V_{C1} + V_{IN} - V_{D1})}{[L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2]}$$

$$B_5 = -\sqrt{\omega_3^2 - \alpha_3^2} \alpha_3 (V_{C1} + V_{IN} - V_{D1}) / [(C_{GS1} + C_{GD1}) (\alpha_3^2 - \omega_3^2) \omega_3^2 L_{S1}], \ C_5 = -A_5$$

If $\alpha_3 > \omega_3$, the equation for $v_{CGS1}$ is exponential as given in Equation (4.28) and the equation for $i_{G1}$ is given in Equation (4.29).

$$v_{CGS1} = A_6 e^{(-\alpha_3 + \sqrt{\alpha_3^2 - \omega_3^2}) t} + B_6 e^{(-\alpha_3 - \sqrt{\alpha_3^2 - \omega_3^2}) t} + C_6 \quad (4.28)$$

$$i_{G1} = (C_{GS1} + C_{GD1}) [A_5 (-\alpha_3 + \sqrt{\alpha_3^2 - \omega_3^2}) e^{(-\alpha_3 + \sqrt{\alpha_3^2 - \omega_3^2}) t} + B_5 (-\alpha_3 - \sqrt{\alpha_3^2 - \omega_3^2}) e^{(-\alpha_3 - \sqrt{\alpha_3^2 - \omega_3^2}) t}] \quad (4.29)$$

Where

$$A_6 = (V_{C1} + V_{IN} - V_{D1}) [(\alpha_3^2 - \omega_3^2) + \alpha_3 \sqrt{\alpha_3^2 - \omega_3^2}] / [2L_{S1} (C_{GS1} + C_{GD1}) \omega_3^2 (\alpha_3^2 - \omega_3^2)]$$

$$B_6 = (V_{C1} + V_{IN} - V_{D1}) [(\alpha_3^2 - \omega_3^2) - \alpha_3 \sqrt{\alpha_3^2 - \omega_3^2}] / [2L_{S1} (C_{GS1} + C_{GD1}) \omega_3^2 (\alpha_3^2 - \omega_3^2)]$$

$$C_6 = -(V_{C1} + V_{IN} - V_{D1} - L_{S1} (C_{GS1} + C_{GD1}) \omega_3^2 V_{C1}) / [2L_{S1} (C_{GS1} + C_{GD1}) \omega_3^2]$$

86
From practical standpoint, the driver resistance $R_{on}$ is typically $3\Omega$, therefore in most cases $\alpha_3 > \omega_3$, and the equations for $v_{CGS1}$ and $i_{G1}$ have the real roots.

B. Miller Plateau [$t_8$, $t_9$]: At $t_8$, $V_{CGS1} = V_{TH} + I_o/g_{fs1}$. During this interval, $v_{CGS1}$ is held at the Miller Plateau voltage $V_{PL1} = V_{TH} + I_o/g_{fs1}$. $i_{G1}$ mainly flows through the gate-to-drain capacitance of $Q$, and $v_{DS1}$ increases accordingly. The equivalent circuit is given in Figure 4.9 B. The initial values of the interval are $I_{G1,t8} = I_G(t_8-t_7)$, and $V_{DS1,t8} = V_{TH} + I_o/g_{fs1}$. The on resistance of the power MOSFET when $v_{CGS} = V_{PL1}$. The equations for $v_{CGS1}$, $i_{G1}$ and $v_{DS1}$ are given in Equation (4.30) ~ (4.32). The interval ends when $v_{DS1}$ equals $V_{IN}$ at $t_4$.

$$v_{CGS1} = V_{CGS,t8} = V_{PL1}$$ (4.30)

$$i_{G1} = [I_{G1,t8} + (V_{PL1} + V_{IN} - V_{D1})/R_{off1}]e^{(-r_{off1}/t_{on})t} - (V_{PL1} + V_{IN} - V_{D1})/R_{off1}$$ (4.31)

$$v_{DS1} = v_{DS1,t8} - \int [I_{G1,t8} + (V_{PL1} + V_{IN} - V_{D1})/R_{off1}]e^{(-r_{off1}/t_{on})t} - (V_{PL1} + V_{IN} - V_{D1})/R_{off1} dt$$ (4.32)

C. Drain Current Drop [$t_9$, $t_{10}$]: At $t_9$, $V_{DS1} = V_{IN}$. During this interval, $v_{CGS1}$ decreases, and the drain current $i_{DS1}$ starts to drop according to the relationship in Equation (4.10).

The equivalent circuit is shown in Figure 4.9 C. At this interval, $i_{DS1}$ drops from $I_o$ to 0. Since $i_{DS1}$ flows through $L_{S1}$, the large voltage is induced across $L_{S1}$, making $i_G$ drop sharply. The initial condition of this interval is $I_{G1,t9} = I_G(t_9-t_8)$, $I_{DS1,t9} = I_o$, and $V_{CGS1,t9} = V_{PL1}$. The interval ends at $t_{10}$ when $i_{DS1}$ equals zero. The neper frequency $\alpha_4$ is given in Equation (4.33) and the resonant frequency $\omega_4 = \omega_1$.

$$\alpha_4 = \frac{(C_{GS1} + C_{GD1})R_{off1} + L_{S1}g_{fs1}}{2L_{S1}(C_{GS1} + C_{GD1})}$$ (4.33)

If $\alpha_4 < \omega_4$, the equation for $v_{CGS1}$ is sinusoidal as given in Equation (4.34) and the equations for $i_{G1}$, $i_{DS1}$ and $v_{DS1}$ are given in Equation (4.35) ~ (4.37) respectively.

$$v_{CGS1} = [A_t \cos(\sqrt{\alpha_4^2 - \omega_4^2} t) + B_t \sin(\sqrt{\alpha_4^2 - \omega_4^2} t)]e^{-\alpha_4 t} + C_t$$ (4.34)
\[ i_{G1} = (C_{GS1} + C_{GD1}) \left[ (-A_x \sqrt{\omega_1^2 - \omega_4^2} + B_x \omega_4) \sin(\sqrt{\omega_1^2 - \omega_4^2} t) \right. \]
\[ \left. + (-A_2 \omega_4 - B_2 \sqrt{\omega_1^2 - \omega_4^2} \cos(\sqrt{\omega_1^2 - \omega_4^2} t)) e^{-a_4 t} \right] \]  
(4.35)

\[ i_{DS1} = g_{p1} \left[ (A_x \cos(\sqrt{\omega_1^2 - \omega_4^2} t) + B_x \sin(\sqrt{\omega_1^2 - \omega_4^2} t)) e^{-a_4 t} + C_7 - V_{TH1} \right] \]  
(4.36)

\[ v_{DS1} = V_{IN} - (L_{S1} + L_{D1}) \frac{di_{DS1}}{dt} - L_{S1} \frac{di_{G1}}{dt} \]  
(4.37)

Where

\[
A_x = -(2L_{S1} \omega_4 I_{G_{-r9}} - V_{C1} - V_{IN} + V_{DL}) / (L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2) \\
B_x = -\sqrt{\omega_1^2 - \omega_4^2} (2L_{S1} \omega_4 I_{G_{-r9}} + L_{S1} \omega_4 I_{G_{-r9}} + V_{PL1} \omega_4 + \alpha_4 V_{IN} - \alpha_4 V_{DL}) / (L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2 (\omega_4^2 - \omega_1^2)) \\
C_7 = (2L_{S1} \omega_4 I_{G_{-r9}} + L_{S1} (C_{GS1} + C_{GD1}) \omega_4^2 V_{TH1} + V_{PL1} + V_{IN} - V_{DL}) / (L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2) \\
\]

If \( \alpha_4 > \omega_4 \), the equation for \( v_{GS1} \) is exponential as given in Equation (4.38) and the equation for \( i_{G1} \), \( i_{DS1} \) and \( v_{DS1} \) are given in Equation (4.39) ~ (4.41) respectively.

\[ v_{GS1} = A_8 e^{(-\alpha_4 + \sqrt{\omega_1^2 - \omega_4^2}) t} + B_8 e^{(-\alpha_4 - \sqrt{\omega_1^2 - \omega_4^2}) t} + C_8 \]  
(4.38)

\[ i_{G1} = (C_{GS1} + C_{GD1}) [A_8 (-\alpha_4 + \sqrt{\omega_1^2 - \omega_4^2}) e^{(-\alpha_4 + \sqrt{\omega_1^2 - \omega_4^2}) t} + B_8 (-\alpha_4 - \sqrt{\omega_1^2 - \omega_4^2}) e^{(-\alpha_4 - \sqrt{\omega_1^2 - \omega_4^2}) t}] \]  
(4.39)

\[ i_{DS1} = g_{p1} \left[ (A_8 e^{(-\alpha_4 + \sqrt{\omega_1^2 - \omega_4^2}) t} + B_8 e^{(-\alpha_4 - \sqrt{\omega_1^2 - \omega_4^2}) t} + C_8 - V_{TH1} \right] \]  
(4.40)

\[ v_{DS1} = V_{IN} - (L_{S1} + L_{D1}) \frac{di_{DS1}}{dt} - L_{S1} \frac{di_{G1}}{dt} \]  
(4.41)

where \( A_8 = \frac{(-L_{S1} \omega_4 I_{G_{-r9}} + V_{PL1} + V_{IN} - V_{DL} - \sqrt{\omega_4^2 - \omega_1^2} I_{G_{-r9}} L_{S1}) \sqrt{\omega_4^2 - \omega_1^2} \alpha_4 + \alpha_4^2 - \omega_4^2}{2L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2 \sqrt{\omega_4^2 - \omega_1^2}} \)

\[ B_8 = \frac{(-\omega_4^2 + \omega_1^2 - \sqrt{\omega_4^2 - \omega_1^2} \alpha_4) (L_{S1} \omega_4 I_{G_{-r9}} - \sqrt{\omega_4^2 - \omega_1^2} I_{G_{-r9}} L_{S1} + V_{PL1} + V_{IN} - V_{DL})}{2L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2} \]

\[ C_8 = \frac{(2L_{S1} \alpha_4 I_{G_{-r9}} + L_{S1} (C_{GS1} + C_{GD1}) \omega_4^2 V_{PL1} - V_{PL1} - V_{IN} + V_{DL})}{L_{S1} (C_{GS1} + C_{GD1}) \omega_1^2} \]

Since the driver is proposed for control FET of the buck converter, which has very small
input capacitance \( C_{\text{ISS}}=C_{GSI}+C_{GD1}, \) typically 1nC for control FET of the buck converter, therefore in most cases \( \alpha_4 > \omega_4. \)

D. Remaining Gate Charging \([t_{10}, t_{11}]):\) At \( t_{10}, i_{DS1} = 0 \) and \( v_{CGS1} \) keeps decreasing until it reaches \(- (V_{IN}-V_{D1}).\) Due to the decreasing of the \( v_{CGS1}, i_{G1} \) decreases gradually to zero. The equivalent circuit is given in Figure 4.9 D. The initial values of this interval are: \( i_{G1,t_{10}}=i_{G1}(t_{10}-t_9), \) \( v_{CGS1,t_{10}}=V_{TH1}.\) This interval ends at \( t_5 \) when \( v_{CGS1}=- (V_{IN}-V_{D1}).\) The equations for \( i_{G1}, v_{CGS1} \) have the same format as the turn on delay interval except for different initial conditions.

After \( t_{11}, Q_1 \) is clamped to OFF state by \( S_2 \) until next switching cycle comes.
4.4 Benefits of the Proposed Inductorless Bipolar Gate Driver

The proposed inductorless bipolar gate driver has two main advantages compared with the previous gate drivers:

1. Much faster turn off speed and smaller turn off loss

   According to the modeling of the switching transition for the proposed bipolar gate driver in Section 4.2, the switching loss of power MOSFET $P_{sw1}$, which consists of turn on loss $P_{sw1_{on}}$ and turn off loss $P_{sw1_{off}}$, is derived according to in Equation (4.42), where $f_s$ is the switching frequency.

\[
P_{sw1} = P_{sw1_{on}} + P_{sw1_{off}} = \int_{t_2}^{t_4} (I_{DS1} \cdot V_{DS1} \cdot f_s)dt + \int_{t_8}^{t_{10}} (I_{DS1} \cdot V_{DS1} \cdot f_s)dt
\]  

Equation (4.42)

The gate driver loss $P_{dr1}$ is given in Equation (4.43). It is observed that compared with conventional driver, the proposed bipolar gate driver introduces more gate driver loss. However, since the gate driver loss is much smaller than the switching loss, therefore, the proposed gate driver still achieves much better overall performance compared with the conventional driver.

\[
P_{dr1} = Q_g(V_{c1} + V_{IN} - V_{D1})f_s
\]  

Equation (4.43)

Figure 4.10 shows the comparison of the calculated switching loss between the proposed driver and conventional driver. The condition for the modeling is: $V_{DS}=5V$, $I_{DS}=5A$~$25A$, $f_s=2MHz$, $L_s=2nH$; the power MOSFET used for the modeling is Si7386DP from Vishay. It is observed that as the drain current increases from 5A to 25A, the loss reduction of the proposed inductorless bipolar gate driver over the conventional driver increases from 0.07W to 1.1W. Therefore, the proposed bipolar gate driver is even more advantageous in high current applications.
Figure 4.10 Comparison of the calculated switching loss between the proposed driver and conventional driver

In order to verify the function and advantage of the proposed bipolar gate driver, the simulation of the power MOSFET driven by the proposed driver is made in Simetrix. The condition for the modeling is: $V_{DS}=12\,V$, $I_{DS}=25\,A$, $f_s=2\,MHz$, $L_s=2\,nH$; the power MOSFET used for the simulation is Si7386DP. The performance of the conventional driver is also simulated for comparison. Figure 4.11 shows the turn off waveforms for conventional driver, while Figure 4.12 presents the turn off waveforms for the proposed driver. It is noted that the turn off time for conventional driver is 16\,ns, while for the proposed driver, the turn off time is 6\,ns, almost one third of the conventional driver, which means the proposed bipolar gate driver can turn off the power MOSFET much faster.
Figure 4.11 Simulated waveforms of power MOSFET driven by conventional driver

Figure 4.12 Simulated waveforms of power MOSFET driven by the proposed driver

Figure 4.13 shows the comparison of the simulated turn off loss between the proposed gate driver and conventional driver at 12V input, 25A drain current in 2MHz switching frequency. It is observed that the turn off loss of the power MOSFET driven by the proposed driver is reduced.
from 2.96W to 1.50W.

2. Inductorless configuration and easiness to be fully integrated

Since the proposed bipolar gate driver has no inductor in the driver circuits, therefore, it is much easier to be fully integrated into chips, which will further increase the power density of the VRs.

4.5 Experimental Results and Discussions

4.5.1 Experimental Verification

A prototype of a synchronous buck converter was built to verify the feasibility of the proposed inductorless bipolar gate driver as well as the switching loss model. The control FET of the converter is driven with the proposed bipolar gate driver, while the SR is driven with a conventional unipolar gate driver since the switching loss for SR is very small. The picture of the prototype is shown in Figure 4.14. The operating conditions are: input voltage $V_{IN}$: 5V; output voltage $V_O$: 1.3V; switching frequency $f_s$: 2MHz~2.5MHz.
The PCB consists of 6 layer 4 oz copper. The components used in the circuit are: $Q_1$: SIR462DP; $Q_2$: IRF6691; output filter inductance: $L_f=100\text{nH}$; drive switches $S_1$-$S_2$: FDN359; $D_1$:MBR0520. Altera Max II EPM240 CPLD is used to generate the PWM signals with accurate delays since the CPLD can achieve time resolution as high as 1/3 ns per gate. The driver voltages for the control FET and SR are both set to be 7V, to make fair comparison with the conventional driver used in Figure 4.18.

Figure 4.15 shows the driving signals for switches $S_1$, $S_2$ and $Q_2$. It is observed that it is necessary to maintain enough deadtime between $V_{GS,S1}$, $V_{GS,S2}$ to avoid shoot through problem of the driver switches, $S_1$, $S_2$. 

Figure 4.14 Picture of the synchronous buck converter driven with the proposed driver
As is shown in Figure 4.16, $V_{GS,Q1}$ equals +7V during turn on transition and is -5V during turn off transition, which validates the feasibility of the proposed inductorless bipolar gate driver.
Figure 4.17 illustrates the drain-source voltage across $Q_2$ at 1.3V/25A load under 2MHz operating frequency. It is noted that because the circuit works in 2MHz frequency, the impact of the parasitic inductance becomes more obvious, therefore there are some ringing during the turn on and turn off transitions.

![Figure 4.17 The drain-to-source voltage of $Q_2$: $V_{DS\_Q2}$](image)

To make a fair comparison with the proposed gate driver, a benchmark of synchronous buck converter driven by conventional driver was built. In Figure 4.18, advanced synchronous rectified buck MOSFET drivers ISL6594D from Intersil is used to drive the synchronous buck converter. The driver voltage for control FET and SR are both set to be 7V since the minimum voltage for ISL6594D is 6.8V.
Figure 4.18 Picture of the buck converter driven with conventional driver

Figure 4.19 compares the efficiencies of the proposed scheme and conventional driver at 1.3V output in 2MHz operating frequency. It is observed that the efficiency improvement of the buck converter is achieved by the proposed bipolar gate driver; especially at 25A load, the proposed driver increases the efficiency from 75.8% to 77.8%.

![Efficiency Comparison Graph](image)

Figure 4.19 Efficiency Comparison at 2MHz between the proposed driver and conventional driver
Figure 4.20 illustrates the measure loss comparison between conventional driver and the proposed inductorless bipolar gate driver at 1.3V output in 2MHz switching frequency. It is observed that as the load increases, the proposed driver can achieve a higher loss reduction; specifically at 25A, the proposed driver can reduce the loss by 0.91W (10.46-9.55W).

![Measured Loss Comparison@Vo=1.3V, Fs=2MHz](image)

Figure 4.20 Measured loss comparison at 2MHz between the proposed driver and conventional driver

Figure 4.21 illustrates the efficiencies comparison of the proposed scheme and conventional driver at 1.3V output in 2.5MHz operating frequency. It is noted that the proposed gate driver can achieve better performance than the conventional driver for all load levels. At 5V input, 1.3V/15A load, the efficiency is improved from 79.2% to 81.9%; while for 25A load, the efficiency is boosted from 72.9% to 76.5%. Therefore, as the load increases, the improvement becomes more obvious, which further proves that the proposed bipolar gate driver is a better choice in high frequency and high current application.
Figure 4.21 Efficiency Comparison at 2.5MHz between the proposed driver and conventional driver.

Figure 4.22 shows the measure loss comparison between conventional driver and the proposed inductorless bipolar gate driver at 1.3V output in 2.5MHz switching frequency. It is observed that as the load increases, the proposed driver can achieve a higher loss reduction; specifically at 25A, the proposed driver can reduce the loss by 1.88W (11.95-10.07W).

It is also observed from Figure 4.20 and Figure 4.22 that, the loss reduction achieved by the proposed driver becomes more significant when the switching frequency increases.
4.5.2 Comparison between the Proposed CSD and the Proposed Inductorless Bipolar Gate Driver

The proposed CSD in Chapter 2 is independent of the input voltage of the buck converter; therefore it can be widely used in all different applications. Especially for current VRs with 12V input, the proposed CSD is a good alternative to the present VSD to improve the performance of the VRs.

While the bipolar gate voltage of the proposed inductorless bipolar gate driver is dependent on the input voltage buck converter, therefore it is more suitable for low input voltage buck converter. Especially, the two stage buck converter is becoming more and more popular [53]. The proposed inductorless bipolar gate driver can be used to drive its second stage buck converter which is working with 5V input at above MHz switching frequency.

![Measured Loss Comparison@Vo=1.3V, Fs=2.5MHz](image)

Figure 4.22 Measured loss comparison at 2.5MHz between the proposed driver and conventional driver

<table>
<thead>
<tr>
<th>Load Current (A)</th>
<th>Conventional Driver</th>
<th>Proposed Bipolar Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>2.19</td>
<td>2.15</td>
</tr>
<tr>
<td>10</td>
<td>3.33</td>
<td>2.85</td>
</tr>
<tr>
<td>15</td>
<td>5.16</td>
<td>4.41</td>
</tr>
<tr>
<td>20</td>
<td>7.55</td>
<td>6.57</td>
</tr>
<tr>
<td>25</td>
<td>11.95</td>
<td>10.07</td>
</tr>
</tbody>
</table>
4.6 Conclusions

A new inductorless bipolar gate driver is proposed in this chapter. Compared with the conventional driver, the proposed driver can turn off the power MOSFET with a negative voltage, which could significantly reduce the turn off loss and thus the switching loss. Also the proposed driver could be fully integrated into a chip as it has no inductor in the circuit. Mathematical modeling and computer simulation are conducted to illustrate the advantages of the proposed gate driver over the conventional driver. The experimental results verify the functionality and advantage of the proposed driver. At 5V input, 1.3V/25A load, in 2 MHz switching frequency, the proposed driver increases the efficiency from 75.8% to 77.8%. At 5V input, 1.3V/25A load, in 2.5MHz switching frequency, the efficiency is boosted from 72.9% to 76.5% by the proposed driver. Therefore, the proposed bipolar gate driver is a better choice in high frequency and high current application.
Chapter 5 Conclusions and Future Work

5.1 Conclusions

In order to reduce the switching loss of the high frequency of the VRs, this thesis proposed two novel topologies of bipolar gate driver and associated mathematical modelings which could help to predict, improve and optimize the performance of the new bipolar gate drivers. By utilizing both the proposed novel bipolar gate drivers, significant overall efficiency improvement can be realized for buck regulators in high frequency applications.

5.1.1 Bipolar Current Source Driver

The first contribution of this thesis is a new bipolar current source driver (CSD) for synchronous buck converter. The main feature of the proposed gate driver is that it can turn off the power MOSFET with a flexible negative voltage (such as -3.5V), which will achieve much faster turn off speed and thus much smaller switching loss than the conventional voltage source driver (VSD) and existing CSDs. By comparison, the conventional VSD turns off the power MOSFET with a positive voltage around +0.5V; existing CSDs can turn off the power MOSFET with -0.7V. Another benefits of the proposed gate driver is that the idea presented in this thesis can also be extended to other Current Source Driver circuits to further improve the efficiency with high output currents.

Computer Simulation demonstrated a significant reduction of the turn off time of the proposed CSD compared with conventional VSD and existing CSDs. Experimental results verified the overall efficiency improvement of synchronous buck converter driven by the proposed gate driver compared with the previous drivers. For buck converters with 12 V input at 1MHz switching frequency, the proposed driver improves the efficiency from 80.5% using the existing CSD to 82.5% (an improvement of 2%) at 1.2V/30A, and at 1.3V/30A output, from 82.5% using the existing CSD to 83.9% (an improvement of 1.4%).
The content of this chapter is subject to patent pending for U.S. patent. The work has been published or submitted in the following IEEE journal and conference:


**5.1.2 Accurate Switching Loss Model and Optimal Design of a Current Source Driver**

The second contribution of this thesis is a new accurate switching loss model on the bipolar CSD proposed in Chapter 2. The gate current diversion problem, which commonly exists in existing CSDs, is analyzed mathematically. Based on the proposed loss model, the optimal design of the CSD inductor is also achieved to minimize the total power loss for the buck converter.

The experimental result verifies the proposed switching loss modeling and optimal design. The experimentally measured loss matches the calculated loss very well; the error between the calculated loss and measured loss is less than 10% from 5A load to 30A load. Compared with previous work, the efficiency with the optimal CSD inductor is improved from 86.1% to 87.6% at 12V input, 1.3V/20A output in 1MHz switching frequency and from 82.4% to 84.0% at 12V input, 1.3V/30A output at 1MHz switching frequency. Even compared with the commercial DrMOSs from Renesas and International Rectifier, the buck converter with the optimal CSD can achieve better performance.

The work in this chapter has been accepted or submitted in the following IEEE journal and conference:


5.1.3 A New Inductorless Bipolar Gate Driver

The third contribution of this thesis is a new inductorless bipolar gate driver for control FET of synchronous buck converters. Compared with the conventional unipolar gate driver, the most important advantage of the new gate driver presented in this chapter is that it can turn off the power MOSFETs with a negative voltage, which will significantly reduce the turn off time and thus switching loss of the power MOSFETs. In addition, the proposed bipolar gate driver does not need inductor; therefore it can be fully integrated into a chip. Analytical mathematical modeling is built to analyze the performance of the proposed inductorless bipolar gate driver compared with conventional unipolar gate driver.

It is demonstrated through computer simulation and mathematical modeling that the proposed inductorless bipolar gate driver can achieve much faster turn off speed compared with conventional unipolar gate driver. The experimental results verify the functionality and advantage of the proposed driver. At 5V input, 1.3V/25A load, in 2 MHz switching frequency, the proposed driver increases the efficiency from 75.8% to 77.8%. At 5V input, 1.3V/25A load, in 2.5MHz switching frequency, the efficiency is boosted from 72.9% to 76.5% by the proposed driver. Therefore, the proposed bipolar gate driver is a better choice in high frequency and high current application.

The work will be published or submitted in the following IEEE conference and journal:


### 5.2 Future Work

This sub-section outlines possible future work for the thesis topics.

#### 5.2.1 Current Source Driver Circuits

In the experimental verification, the proposed CSDs in Chapters 2 and 3 have been implemented with discrete components. To increase the practicability of CSDs, the drivers need to be integrated into single discrete driver chipset. The CSDs chips have already been designed into a monolithic chip, so the future work will involve the debugging and testing of the CSD chip.

#### 5.2.2 Inductorless Bipolar Gate Driver Circuits

The negative turn off voltage of the proposed inductorless bipolar gate driver in Chapter 4 is dependent on the input voltage; therefore its application is within low voltage environment. In order to further extend the application of the proposed gate driver, new inductorless bipolar gate drivers with variable negative turn off voltage can be investigated on.
References


[38] SIMetrix, SIMetrix Technologies, http://www.simetrix.co.uk/


