NOVEL DIGITAL CONTROLLER
FOR
MULTI FULL-BRIDGE DC/DC CONVERTER

by

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Abstract

Distributed generation that utilizes 5-10kW Solid Oxide Fuel Cells requires power electronics to optimize the overall system efficiency while reducing the cost. The Adaptive Energy Zero-Voltage-Switching Phase-Shift-Modulated Full-Bridge (AE-ZVS-PSM-FB) topology meets these criteria under all loading conditions, but suffers from complexity associated with an analog control implementation. This thesis presents a novel Look-Up-Table (LUT) based digital controller required for such converter. The applied design approach also reduces the design time and controller requirements, which in turn decreases the overall system cost.

Steady-state analysis for the AE-ZVS-PSM-FB converter is performed using a piece-wise equivalent circuit model. This analysis is used to verify the LUT concept that forms the basis for the proposed LUT-based digital controller. The proposed LUT-based digital control algorithm is developed and verified using Field Programmable Gate Array (FPGA) Logic platform. Design procedures and operational function under steady state and step change conditions are presented.

Simulation results demonstrate the LUT concept in the AE-ZVS-PSM-FB converter, and the simplicity of the proposed LUT-based digital controller in producing the expected switching sequence. Simulation results were also produced showing successful dynamic response of LUT-based digital controller interconnected with the converter under different operating conditions. A Xilinx FPGA demonstration board was used to generate experimental switching sequence results to demonstrate the simplicity of the proposed controller.
Acknowledgements

I wish to thank my supervisor Dr. Praveen Jain for his guidance and direction throughout the course of my studies. His confidence in me and his support allowed me to realize my full potential throughout this entire process. I would also like to thank my peers in the Queen’s Power Electronics Applied Research Lab. A special debt of gratitude is owed to Andrew Mason, Darryl Tschirhart, Wilson Eberle, George Prpich, Davood Yazdani and Sayed Ali Khajehoddin for their help, advice and support during my work. The work of our Lab Engineer, Djilali Hamza, for his help with my simulation and test equipment is greatly appreciated.

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<tr>
<td>( t )</td>
<td>denotes a value which has been referred to the primary side</td>
</tr>
<tr>
<td>( \theta )</td>
<td>leg-to-leg phase shift within a bridge</td>
</tr>
<tr>
<td>( \varphi )</td>
<td>bridge-to-bridge phase shift (in degrees)</td>
</tr>
<tr>
<td>( C_{\text{aux}} )</td>
<td>Auxiliary capacitor</td>
</tr>
<tr>
<td>( C_{\text{dc}} )</td>
<td>DC blocking capacitor</td>
</tr>
<tr>
<td>( C_{\text{sb}} )</td>
<td>snubber capacitor in parallel with MOSFET</td>
</tr>
<tr>
<td>( \text{Clk} )</td>
<td>Clock signal</td>
</tr>
<tr>
<td>( \text{Cnt} )</td>
<td>Counter signal</td>
</tr>
<tr>
<td>( C_{\text{O}} )</td>
<td>output capacitor</td>
</tr>
<tr>
<td>( D_x )</td>
<td>diode rectifier</td>
</tr>
<tr>
<td>( D )</td>
<td>duty cycle</td>
</tr>
<tr>
<td>( D_{\text{op}} )</td>
<td>Optimal duty cycle</td>
</tr>
<tr>
<td>( D_{\text{eff}} )</td>
<td>effective duty cycle</td>
</tr>
<tr>
<td>( E_{\text{SWon}} )</td>
<td>switching energy dissipated due to turn-on of a MOSFET</td>
</tr>
<tr>
<td>( E_{\text{SWoff}} )</td>
<td>switching energy dissipated due to turn-off of a MOSFET</td>
</tr>
<tr>
<td>( f_s )</td>
<td>switching frequency in Hertz</td>
</tr>
<tr>
<td>( I_{\text{ds}} )</td>
<td>drain-source current of a MOSFET</td>
</tr>
<tr>
<td>( I_p )</td>
<td>transformer primary current</td>
</tr>
<tr>
<td>( I_s )</td>
<td>transformer secondary current</td>
</tr>
<tr>
<td>( I_{\text{pk}} )</td>
<td>transformer peak primary current</td>
</tr>
<tr>
<td>( I_1 )</td>
<td>transformer primary current at end of freewheeling interval</td>
</tr>
<tr>
<td>( I_2 )</td>
<td>transformer primary current at start of leading leg commutation</td>
</tr>
<tr>
<td>( I_{\text{aux}} )</td>
<td>auxiliary current</td>
</tr>
<tr>
<td>( I_{\text{auxPK}} )</td>
<td>peak auxiliary current</td>
</tr>
<tr>
<td>( I_{\text{out}} )</td>
<td>DC output load current</td>
</tr>
<tr>
<td>( L_{\text{Lk}} )</td>
<td>transformer leakage inductance</td>
</tr>
<tr>
<td>( L_{\text{aux}} )</td>
<td>auxiliary inductor</td>
</tr>
<tr>
<td>( L_O )</td>
<td>output inductor</td>
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L_p  equivalent inductance of load as seen by primary-side bridge
N    number of parallel ZVS-PSM full bridges
N_p  number of transformer primary turns
N_s  number of transformer secondary turns
P_{out}  output power
P_{SW} instantaneous switching power loss in a MOSFET
Q    FPGA output switch signal
S    MOSFET switch
T    transformer
T_s  switching period
t_d  deadtime
t_{ri} rise time of current at switch turn-on
t_{fv} fall time of voltage at switch turn-on
t_{rv} rise time of voltage at switch turn-off
t_{fi} fall time of current at switch turn-off
V_p  transformer primary voltage
V_s  transformer secondary voltage
V_{gs} gate-source voltage of a MOSFET
V_{gs(th)} gate-source voltage (threshold) of a MOSFET
V_{ds} drain-source voltage of a MOSFET
V_F  diode forward conduction voltage drop
V_{in} DC input voltage
V_{in_min} minimum input voltage
V_{in_max} maximum input voltage
V_{out} DC output voltage
V_{aux} auxiliary circuit voltage
AE-ZVS-PS-FB adaptive energy zero voltage switching phase shift full bridge
CO2  carbon dioxide, commonly referred to as greenhouse gas
DG  distributed generation
DOE  U.S. Department of Energy
DSP  Digital signal processing
<table>
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<td>Field programmable gate array</td>
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<tr>
<td>IESO</td>
<td>Independent energy system operator</td>
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<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>SECA</td>
<td>Solid State Energy Conservation Alliance</td>
</tr>
<tr>
<td>SOFC</td>
<td>Solid oxide fuel cell</td>
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<td>ZVS</td>
<td>Zero voltage switching</td>
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Chapter 1: Introduction

1.1 General Introduction

In recent years the power industry has seen a rise in energy prices coupled with an increasing demand for reliable power. These pressures are pushing power design at all levels to create devices with higher efficiency, lower cost, reduced emissions (CO$_2$), increased reliability and enhanced adaptability for different power settings.

In 2006 the Independent Electricity System Operator’s (IESO) 10-year outlook identified the Ontario Government’s goal of increasing conservation by 5% by 2010 as a significant change in the Ontario power demand and supply interaction. In order to achieve this goal, the IESO aims to vigorously pursue demand reduction and supply diversification in Ontario [1]. However, this progress is currently impeded by the cost of creating large amounts of new generating capacity; for examples $4.25 billion would be required to refurbish Bruce A Nuclear Plant [2]. For the province to achieve the outlined goals, the focus of investments and research must be placed on supply systems that are efficient and reliability, while maintaining a minimum impact financially and environmentally.

One form of power generation that achieves these goals is Distributed Generation (DG) of electricity [3]. Unlike typical centralized power plants, such as nuclear or large-scale fossil fuel plants, DG systems can be located locally and operate independent of the electrical grid. During blackouts, especially large scale blackouts such as the one that occurred on August 14$^{th}$, 2003 [4], DG systems could disengage themselves from the grid
and continue to provide reliable power, which has many added benefits from social, economic and environmental standpoints. Being located locally could also allow DG systems to achieve higher overall system efficiencies by utilizing waste heat produced during power generation. In power generation, most energy that is not converted into usable electrical power is lost to waste heat; however, in co-generation application, this waste heat is captured and used in heating and cooling applications such as steam heating, industrial processes or air conditioning. By operating DG systems in a co-generation application the overall efficiency could reach up to 90%, whereas typical centralized power plants operate at roughly 43% to 54%, depending on the fuel source [5]. A higher efficiency system could result in lowered CO$_2$ emissions and reduced fuel demand. Reduction in fuel demand may lower the operating cost of the system while lower CO$_2$ emissions can reduce any burden associated with Carbon Tax or Carbon Cap-and-Trade expenses. Finally, DG power systems can provide power generation at the distribution grid levels that avoid any additional demand on the already overburdened transmission capacity [6].

The main motivation of this thesis was derived from the benefits of distributed generation, specifically in Solid-Oxide Fuel Cells (SOFC). The production of clean and efficient power in a distributed generation system using the SOFC is significant, especially when operated in a co-generation application. The multi full-bridge DC/DC converter analyzed in this thesis is used in the first of two stages of power conversion for SOFC and has the ability to achieve ZVS under light and no-load conditions. This operation capability under those loading conditions contributes to the overall system advantage. The major drawback of the multi-full bridge converter is the high complexity
of the analog controller. This thesis presents a simple look-up table based digital
controller that utilizes the benefits of co-generation SOFC and multi full-bridge DC/DC
converters with minimal trade-offs. This controller is the first look-up table based digital
control design for the multi full-bridge converter and utilizes the constraints of second
stage of the SOFC power conversion as an advantage for simplification. The base
objective and motivation is elaborated more in the following sections of this chapter and
throughout the thesis.

1.2 Distributed Generation: Solid Oxide Fuel Cell

There are many different sources of Distributed Generation that could be utilized
in a co-generation application, and example of one such source being the fuel cell. A fuel
cell produces electricity and heat through an electrochemical reaction that combines
hydrogen and oxygen with the only major by-product being clean water [6]. A leading
candidate for DG application in residential or small commercial developments is the
Solid Oxide Fuel Cell (SOFC), which, with some minor modifications can accept natural
gas as a fuel, which commonly exists as a residential distribution system. Pure hydrogen
driven fuel cells lack infrastructure for a large-scale hydrogen distribution system.

Although the SOFC can achieve high efficiency and versatility associated with
DG systems, there is a drawback associated with effectively converting the output power
from the SOFC in an efficient, low-cost manner that does not greatly reduce the initial
benefits. At Siemens Westinghouse and Fuel Cell Technologies, there is a 7.5 kW, 44
cell unit under development [7]. Each cell within the unit has a total output voltage of
0.55V DC, but due to a large physical size required to keep manufacturing costs low, a
minimal number of units may be stacked together to increase the overall unit output.
voltage, with a common output voltage of 24 DC under full load for this unit. Figure 1.1 shows the output characteristics for the unit.

![Graph showing output characteristics for 7.5kW SOFC](image)

Figure 1.1: Output Characteristics for 7.5kW SOFC

This low DC output voltage from the SOFC must be converted to 60Hz, 110V AC voltage for use in conventional buildings. Typically power conversion for this application is done in two stages [3-7] as shown in Figure 1.2. The first stage converts the SOFC’s output voltage to a much higher DC output voltage that can be converted into the applicable AC voltage by the second stage inverter [8].

![Diagram of typical power conditioning system](image)

Figure 1.2: Typical Power Conditioning System
Since the initial input to the power conversation system from the SOFC has a very high current at full load (in excess of 300A), an effective efficient DC/DC converter design is required. High current within the first stage of the power conversion can cause extreme conduction losses if it is not mitigated. This impact is also compounded by the cost-sensitivity of SOFC power conditioning applications. The Solid State Energy Conversation Alliance (SECA), founded by the U.S. Department of Energy (DOE) has set $40/kW target for SOFC power conditioning systems [6]. This has a direct impact on the DC/DC converter design as it contains a bulk of the two-stage power conditioning system cost, which is the result of a large transformer needed for the voltage conversion and high number of components due to the paralleling necessary to mitigate the high input current stresses. Thus, particular attention is given to the overall DC/DC converter design; especially from a design cost and component count viewpoint.

1.3 DC/DC Efficiency Improvement

Boosting the efficiency, reliability and flexibility of the DC/DC power converter while maintaining or decreasing cost, may provide a solution to the general conservation goal. Currently there exist many design principles that may be adapted for use in achieving these goals. Operating a converter using a constant switching frequency allows the magnetic components, along with the filter design, to be optimized, which increases the overall efficiency of these components while decreasing their size. [14] [15] [16]. Efficiency in a power system may also be improved by ensuring that the switching duty cycle is operated as close to 50% as possible, which reduces the stress on components within the system. In [17], a duty cycle that is significantly less then 50% was linked to
decreased efficiency and poor transient response performance in comparison to operation at 50% duty cycle. A small duty cycle also puts limitations on switching frequency in a power conditioning system since malfunction can happen due to the extremely short conduction times [18].

One concept that can be beneficial for boosting efficiency within power system design is operating at a higher switching frequency. This diminishes the cost and size of the power converter while improving the reliability and efficiency of the system, although these benefits can be nullified if effects of increased frequency-dependent losses, switching losses, output capacitance losses and gate losses are not counteracted.

1.4 The Case for Higher Switching Frequency

It is well documented that converters designed with higher switching frequencies can reduce the size and weight of transformers and filter components along with improving transient response [10]. The increased transient response is due to higher switching frequency, which enables the converter to respond more rapidly to changes in line and load conditions. The improved transient response leads to smaller voltage sags as observed by equipment connected to the power system, and therefore increases the reliability of the overall power generation. At a higher switching frequency, the size of the magnetic components required may be decreased leading to a reduction in raw material costs, along with the converter occupying less physical volume. These factors may improve the economics of many power electronics applications, particularly when viewed from a whole-system conservation point of view.

Although higher switching frequency leads to benefits in cost and reliability, these benefits can quickly be negated by the decrease in efficiency due to increased switching
losses. Switching losses occur when there is simultaneous overlap between the switch voltage and the switch current while the switch is either turning on or turning off. The phenomenon when neither the switch voltage nor the switch current is reduced to zero before the switching interval, is often referred to as “hard switching”. The power loss that occurs during hard switching can significantly increase the losses within the circuit, and therefore decrease the overall efficiency [10].

An example using Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switches (hereafter, “MOSFET” and “switch” are used interchangeably) will demonstrate the effects of hard switching. Figure 1.3 illustrates the simultaneous overlap during the switch turn on interval between the switch voltages and switch current waveforms during hard switching.

![Figure 1.3: MOSFET Turn On Waveforms during Hard Switching](image)

Prior to $V_{gs}$ reaching turn on ($t_0$) threshold ($V_{gs(th)}$), $V_{ds}$ for the MOSFET equals $V_{in}$. When $V_{gs}$ reaches the threshold voltage at $t_1$, the switch current, $I_{ds}$, begins to ramp up from zero to $I_{out}$, the conduction current level. At this time ($t_2$), $V_{ds}$ is driven from $V_{in}$
to zero over the time period $t_2$ to $t_3$. Between $t_1$ and $t_3$, both the switch voltage $V_{ds}$ and switch current $I_{ds}$ are overlapping. The product of these two values produces the switching loss $P_{SW}$. A similar loss may be observed for the MOSFETs turn off interval as seen in Figure 1.4.

The switching loss for the turn off interval occurs in an analogous fashion to the turn on interval. The switch voltage $V_{ds}$ ramps up from zero to $V_{in}$ while the switch current $I_{ds}$ is constant at $I_{out}$. The switch current $I_{ds}$ then ramps down from $I_{out}$ to zero; again, the product of this overlap of $V_{ds}$ and $I_{ds}$ produces the switching loss $P_{SW}$ during the turn off transition.

The energy dissipated in the MOSFET during the turn on and off transition can be represented by the areas $E_{SWon}$ and $E_{SWoff}$ from Figure 1.2 and Figure 1.3 respectively. As a result, the average switching power loss, $P_{SW}$, in the switch due to the turn on and off transition can be approximated by (1-1) [10].
\[
P_{SW} = \frac{1}{2}V_{in}I_{out}f_s(t_{ri} + t_{fv} + t_{fi} + t_{rv})
\]

Where

\[
\text{Current Rise Time} = t_{ri} = t_2 - t_1
\]

\[
\text{Voltage Fall Time} = t_{fv} = t_3 - t_2
\]

\[
\text{Voltage Rise Time} = t_{rv} = t_4 - t_6
\]

\[
\text{Current Fall Time} = t_{fi} = t_8 - t_7
\]

It can be seen from (1-1) that high switching frequencies result in an increased switching loss; and that loss is responsible for countering afore mentioned advantages of a higher switching frequency. To realize the benefits of a high switching frequency switching loss must be eliminated and a common and effective approach for achieving this involves the implementation of Zero Voltage Switching (ZVS) [19], [20], [21]. ZVS is a technique that removes switching loss by ensuring that during the switch transition, the switch voltage \(V_{SW}\) is roughly equal to zero. Achieving ZVS produces higher efficiency through the removal of switching loss, and also allows the benefits of higher switching frequency to be realized.

1.5 The ZVS-Clamped Voltage Family of Converters

While zero voltage switching can be achieved with many different circuit configurations and switching sequences [21][19], a commonly used family of converters is the ZVS-Clamped Voltage family of converters [10]. The proposed controller design, presented later in Chapter 3, is applied to a subsidiary of this family and is the reason for its presentation here. This converter family has also been referred to as pseudo-resonant
converters [22] and resonant transition converters [19]. Zero voltage switching is observed in two forms, zero voltage during turn on and zero voltage during turn off.

### 1.6 Mechanisms of ZVS in ZVS-Clamped Voltage Converters

To achieve ZVS for turn on, a lagging current is used to discharge the voltage of the parallel snubber capacitor (\(C_{sb}\)) before the switch is turned on. The lagging current is naturally present in this family of converters due to the leakage inductance found in the circuit’s transformer. When the voltage in the snubber capacitor has been driven to zero, the current flow transfers to the anti-parallel diode connected to the switch. At this point, the switch can safely be activated under zero voltage conditions. It should be noted that the voltage is not actually zero at turn on, but instead is equal to the negative of the anti-parallel diode voltage drop, \(V_F\); however, this value is commonly considered too small to have an impact on switching losses and is therefore neglected.

ZVS turn-off is also naturally achieved in this family of converters. Again, the parallel snubber capacitor \(C_{sb}\) plays a key role in achieving ZVS. The snubber capacitor limits the rate of voltage rise across the switch during the turn-off cycle and is kept low long enough to allow the switch current to decrease to zero. While there is some overlap between the rising switch voltage and dropping switch current, the suppressed rise in voltage that is observed by the switch is small enough to have an insignificant impact on the total switching losses and therefore is assumed that ZVS is achieved.
Figure 1.5 shows ZVS turn-on and turn-off for an ordinary single leg of a ZVS-Clamped Voltage converter. This single leg is feeding a load with a series connection to \( L_p \), an equivalent inductance of the load as seen by the primary. \( L_p \) is a combination of any discrete inductances along with leakage and magnetic inductances from the transformer. Each switch has a connected anti-parallel diode (\( D_A \) and \( D_B \)) along with equivalent parallel capacitors (\( C_{sbA} \) and \( C_{sbA}^- \)) representing any discrete or parasitic
components. Figure 1.6 shows the voltage and current waveforms for the switching intervals.

During time $t_0-t_1$, switch $S_A$ is conducting $I_p$ to the load; switch $S_B$ has the same voltage as the parallel snubber capacitor $C_{sbB}$. At $t_1$, the switch $S_A$ turns off. ZVS turn-off is achieved for switch $S_A$ because the snubber capacitor $C_{sbA}$ reduces the rising voltage rate so that the current in $S_A$ has sufficient amount of time to decrease to zero. $I_p$ continues to flow in the same direction during the interval $t_1-t_2$ due to the equivalent inductance $L_p$. This current must be carried by $C_{sbA}$ and $C_{sbB}$. It is assumed that both have equal values, so $C_{sbA}$ charging and $C_{sbB}$ discharging will be at the same rate. At $t_2$, the voltage across $C_{sbB}$ reaches zero and that snubber capacitor is completely discharged. During the interval $t_2-t_3$, the current $I_p$ continues to flow in the same direction due to the energy stored in the inductance $L_p$, and that current flow is now transferred to the anti-
parallel diode $D_B$. The voltage seen by switch $S_B$ is the negative of the forward diode voltage drop of $D_B$, however, as mentioned earlier, this voltage is insignificant for switching losses.

At $t_3$, it is assumed that the voltage across switch $S_B$ is equal to zero due to the conduction of $D_B$. Switch $S_B$ can now be activated under ZVS conditions. During the interval $t_3-t_4$, switch $S_B$ begins conducting the current $I_p$. At $t_4$, the current $I_p$ passing through switch $S_B$ crosses zero. During the interval $t_4-t_5$, the current $I_p$ begins conducting in the opposite direction and the process is set to repeat for switch $S_B$ ZVS turn-off and switch $S_A$ ZVS turn-on ($t_5-t_{10}$), as shown in Figure 1.5. The ZVS for turn-on and turn-off of switch $S_A$ and $S_B$ is identified in the figure.

### 1.7 The Zero-Voltage-Switching Phase-Shift-Modulated Full-Bridge (ZVS-PSM-FB) Converter

The proposed digital controller presented in this thesis is built upon a derivative of the ZVS-PSM-FB converter [20], which is a subfamily of the ZVS-Clamped Voltage Circuit. This section outlines the basic circuit description, including advantages, principle of operation, and the evolution of the circuit to solve the drawbacks associated with the ZVS-PSM-FB converter. The converter used for the digital control design [15] is also presented and describes the ability of the converter to overcome many of the disadvantages of the ZVS-PSM-FB converter thus making it the strongest evolution so far in the sub family.
1.7.1 Circuit Description

The ZVS-PSM-FB converter has two legs of series-connected MOSFETS in a full bridge configuration shown in Figure 1.7. Switch $S_1$ and $S_4$ form Leg$_A$, while switch $S_2$ and $S_3$ form Leg$_B$. The output of the full bridge is connected to a series inductor and high frequency transformer $T_1$. The series inductor in many designs is not a discrete component, but instead, is a representation of the leakage inductance of the transformer $T_1$. There are cases where a discrete inductance is added to the design to increase the overall inductance value, but this is not considered in this description. The output DC voltage $V_{out}$ is achieved by rectifying and filtering the transformer secondary voltage using an output filter comprised of an inductor $L_O$ and capacitor $C_O$ along a diode full bridge rectifier connected to the output of transformer $T_1$. A DC blocking capacitor $C_{dc}$ is used for blocking any DC components of the primary current, $I_p$.

![Figure 1.7: Zero-Voltage-Switching Phase-Shift-Modulated Full-Bridge Converter](image)

The converter achieves zero switching losses under heavy loading conditions at a high switching frequency with a low component count. As a result, the advantage in utilizing this converter is its low-cost, small size and high efficiency; however, a
limitation of this converter is the loss of ZVS under light loading conditions as explained below.

### 1.7.2 Principle of Operation

As mentioned previously, there is an advantage in operating switches consistently at a relative 50% duty cycle. The ZVS-PSM-FB converter takes advantage of this by utilizing leg-to-leg phase shifting. The legs are operated in a similar manner as the other, with each switch on a leg active for a relative 50% duty cycle. There is a slight delay between one switch on a leg deactivating and the other switching activating and this is desirable in order to leave the required dead time to achieve ZVS (as described in Section 1.7). As result, the actually duty cycle of each switch is less then 50% duty cycle.

Output voltage regulation is achieved by creating a voltage pulse across the transformer. The voltage pulse is present when either switch $S_1$ and $S_3$ are active (positive power flow), or when $S_2$ and $S_4$ are active (negative power flow). The voltage pulse can be adjusted by varying the phase shift ($\Phi$) between the two legs of the converter and thus output voltage regulation can be obtained. Figure 1.8 shows the voltage and current waveforms to illustrate this concept.
As described in section 1.7, ZVS turn-off can be achieved in all switches using snubber capacitors ($C_{sb1}$-$C_{sb4}$) to reduce the rise-rate of the switch voltage when the switch is deactivated. Similarly, ZVS turn-on is achieved through the description in section 1.7 using the energy stored in the leakage inductance of the transformer, $L_{lk}$ to discharge the snubber capacitor voltages before turn on. The time needed to discharge the snubber capacitors and achieve ZVS turn-on is the reason why the duty cycle of each individual switch is less than 50%. When the converter is operating under normal full load conditions, the $L_{lk}$ inductor is able to store enough energy to discharge the snubber capacitors. However, under light load conditions, the inductance $L_{lk}$ cannot store sufficient energy to fully discharge the snubber capacitors before the switch is activated.
As a result, ZVS turn-on is lost for all switches thus in many applications limiting the this converter to heavy load, low input voltage conditions.

1.8 The Evolution of the ZVS-PSM-FB converter

Many solutions have been proposed to solve the drawback of the ZVS-PSM-FB converter, with most focussing on the use of auxiliary circuit connections [16-23]. All of these proposed solutions increase the amount of energy available to discharge the snubber capacitor voltage before switch activation while adhering to the basic operating principles. This section will discuss three types of proposed solutions; auxiliary circuits using passive elements, auxiliary circuits using active elements and an adaptive energy storage technique. The final proposed solution presented is the basis of the digital controller presented in this thesis and is seen as the strongest solution to the drawback of the ZVS-PS-FB converter.

1.8.1 Auxiliary Circuit Using Passive Elements

Passive elements refer to components that require no external control and generally consist of a combination of inductors, capacitors and diodes. These passive components induce and store a flow of circulating current through the auxiliary circuit, which is produced by the normal operation of the ZVS-PSM-FB converter’s switching pattern. The auxiliary circuits commonly used may consist of resonant [28] or non-resonant networks [23][29]. The auxiliary circuits utilize a circulating current to ensure that there is no energy differential needed to properly discharge the snubber capacitors and achieve ZVS.
An example of auxiliary circuits using passive components is presented in [23], and is illustrated in Figure 1.9. In this paper, inductors (\(L_{\text{auxA}}\) and \(L_{\text{auxB}}\)) are installed at the midpoint of each leg and connected in parallel to the midpoint of a capacitor leg (comprising of \(C_{\text{aux1}}\) and \(C_{\text{aux2}}\)). The capacitor leg is used to split the input voltage and ensure the inductors only carry an AC current, which is used to extend the ZVS range to no-load conditions. Both auxiliary inductors have a \(\frac{V_{\text{in}}}{2}\) voltage applied to them when the top switch of a leg is active, and a voltage of \(\frac{-V_{\text{in}}}{2}\) applied when the bottom switch is active. This produces a sawtooth circulating current independent of the load through the auxiliary circuit.

![Figure 1.9: Passive Element Auxiliary Circuit used in a ZVS-PSM-FB Converter](image)

The advantage of this solution is that no external switching scheme is needed to achieve the level of circulating current needed for all load conditions, making this a cost-effective method to implement. Also, with no external switching scheme, this circuit can be used in all switching frequency levels of conventional ZVS-PSM-FB converters. This
is particularly advantageous when comparing passive components to MOSFET switches, which generally cannot handle high frequency switch. The significant drawback associated with this circuit is a result of the use of an opposing 50% duty cycle for each switch on a leg. Therefore, the circulating current produced by the auxiliary circuit is constantly present throughout the operation of the converter and leads to higher conduction losses in the primary switches and auxiliary components throughout the entire switching period that could offset the gains in efficiency from ZVS.

1.8.2 Auxiliary Circuit Using Active Elements

Active auxiliary circuits utilize passive components that require external switches to provide the circulating current needed for the achievement of ZVS. Many examples of such circuits have been proposed in [30][25][24], with the circuit proposed by Cho (1994) shown in Figure 1.10

Figure 1. 10: Active Element Auxiliary Circuit used in a ZVS-PSM-FB Converter
Active auxiliary circuits address the drawback of the passive auxiliary circuits by reducing the amount of time during the switching cycle that the circulating current is present. In this scenario the auxiliary switches are activated for a short duration just prior to and during the switching leg commutation. By turning the auxiliary switches on for a small period of the half cycle of the converter, this helps reduce unnecessary circulating current from flowing through the primary circuit switches. During line and load conditions where the energy stored in the leakage inductance may be used to achieve ZVS (i.e. heavy load and low line conditions), the auxiliary circuit can be deactivated to eliminate any losses that may have been produced by its operation. During light load conditions when there is insufficient energy to achieve ZVS, the auxiliary inductors can induce the needed circulating current to make up that energy shortfall along with reducing the power consumption and current stresses in the main circuit.

Although the active auxiliary circuit does solve the high circulating current drawback of the passive component auxiliary circuit, it does come with a trade-off. Since the active auxiliary circuits require added controls for the extra switching operations, there is a higher level of complexity than passive auxiliary circuits and coupled with the added component count (increased overall cost) many of the benefits of the active auxiliary circuit are offset.

Beyond the added complexity and larger component count, the key limiting factor of the active auxiliary circuit is the small fraction of time that the auxiliary switches are operated. Limits in turn-on and turn-off time for the MOSFET switches used in the auxiliary circuit can limit the overall converter switching frequency and therefore limit the benefits of a higher switching frequency. This problem may be solved using high
current MOSFET drivers. However, in order to minimize turn-off switching losses these components would be required for the main MOSFET drivers and as a result would increase the overall system cost.

### 1.8.3 Adaptive Energy Storage

A novel design has been introduced by [8] that enables no-load ZVS without suffering from many of the key limitations observed in passive and active auxiliary circuits. The circuit design presented, an Adaptive Energy-Zero Voltage Switching-Phase Shifted-Full Bridge (AE-ZVS-PS-FB) converter, utilizes a technique referred to as adaptive energy storage, which stores only the required amount of energy required to achieve ZVS for a given line and load condition.
Figure 1.11 shows the topology of the AE-ZVS-PS-FB converter. The circuit utilizes two identical ZVS-PSM-FB converters that share an equivalent power load. Each bridge delivers half the overall power by possessing the same leg-to-leg phase shift to achieve equal output voltage regulation. The leg-to-leg phase shift ($\Phi$) is also used to achieve ZVS under certain line and load conditions. To achieve ZVS over all line and load conditions, the bridges are connected through the midpoints of each leg by auxiliary
inductors, L_{auxA} and L_{auxB}. Circulating current required for ZVS in light load conditions is produced in the auxiliary inductors by phase shifting between the bridges for a predetermined period. The bridge-to-bridge phase shift (\( \phi \)) is based upon the line and load conditions present in the circuit. Under these certain load conditions in which the leg-to-leg phase shift may achieve ZVS using the leakage inductance of each individual bridge’s transformer, \( \phi \) is set to zero. The phase shift \( \phi \) has a range of circa 0° to 180° and with properly selected auxiliary inductors may achieve ZVS from no-load, high input voltage operating condition to full-load, low input voltage operating conditions. Figure 1.12 shows the experimental efficiency results in comparison to the auxiliary circuit using passive components.

![Figure 1.12: Experimental Efficiency vs. Load for AE-ZVS-PS-FB converter and reference (Passive Component) topology: Vin=20V][8]

The converter achieves ZVS efficiently with no frequency limitations and slight MOSFET conduction losses due to circulating current. In applications where the power level is sufficiently large, the circuit’s ability to split the power flow evenly between the
two bridges can make it cost effective thus allowing the AE-ZVS-PS-FB converter to possess an advantage over active and passive auxiliary circuits. For this reason, the AE-ZVS-PS-FB converter was selected as the base circuit for the proposed digital controller presented in this thesis.

1.9 Drawbacks of the AE-ZVS-PS-FB Converter

Compared to previous ZVS-PS-FB converters, the Adaptive Energy ZVS-PS-FB (AE-ZVS-PS-FB) converter possesses two key limitations. The first limitation is the high component count which leads to increased size and cost. However, when comparing higher level of low power transfer capabilities with the other topologies this drawback is far less significant. Further, at higher low power levels (10kW), the AE-ZVS-PS-FB converter is a better topology then the ZVS-PSM-FB.

The second limitation, and key focus of this research, is the increased control complexity under analog implementation. As with the active auxiliary circuit, the AE-ZVS-PS-FB converter has twice as many controlled devices (MOSFETs) as the ZVS-PSM-FB converter. In addition to increased number of controlled components, there exists an increased level of complexity with the control circuit required for operation. The basis of this complexity comes from the requirement to achieve two separate phase shifts within the converter during operation. The role of the control circuit is to ensure that all switches have a constant switching frequency that output voltage is regulated, and that significant energy is stored to ensure ZVS will occur. As noted in [15], these objectives may be complicated and difficult to implement using an analog control scheme. [15] discusses the possibility of using a digital controller to offset these difficulties and ensure that the benefits of the AE-ZVS-PS-FB converter are fully utilized. The proceeding
section will discuss the benefits of digital control in switch mode power converters and it is these benefits that form the basis of the digital controller proposed in this thesis.

### 1.10 The Case for Digital Controller in Switch Mode Power Converters

Digital control of switching power converters is becoming more common for all power levels. Many publications [24-32] show comparable performance for both digitally controlled converters and analog controllers. This section will outline some of the advantages of the digital control and present instances that demonstrate the benefits applied to switch mode power converters.

The advantages of digital control over analog control in switch mode power converters vary depending on the application for which they are used. One key advantage is the flexibility that digital control provides [24, 28, 31]. If an analog controller must be replaced or tuned due to different control techniques or operating conditions, it would need to be rebuilt. The digital control on the other hand can utilize the existing hardware through a reprogramming of its control algorithm. This flexibility enables improvements in soft control techniques (new control algorithms) to be applied on a continuous basis without the need for costly prototypes. Another added benefit of flexibility is that it allows control techniques to be adjusted depending on the operating conditions of the converter to which they are applied. This is also referred to as reproducibility in [31].

The increased flexibility to quickly adjust to different operating conditions and implement advances in digital control theory represents distinct advantages over analog control. In the past, the costs for digital control development were higher than those for
analog systems since high performance microcontrollers were expensive to implement. However, recent advances in modern microcontrollers, as noted in [32], have since been able to produce high performance microcontrollers at a relatively low cost. As digital controllers continue to gain momentum in power converters, this cost will continue to decrease in comparison to the more mature analog technology. Analog controllers are implemented with hardware components only and therefore require a long design time [29, 32]. Comparatively, digital controllers are implemented through software development which reduces the effects of design errors and iterations since costly, time-consuming prototypes are not required.

As modern advances in digital technology advance, drawbacks of analog control become more apparent. One such drawback is the sensitivity of analog controls to noise and environmental effects when compared to digital controls [28, 32, 33]. Microprocessors are generally less sensitive to environmental and noise variations that cause disruptions or limitations in analog control design. Another benefit of digital control is the ability to provide self diagnostics and monitoring. This allows deficiencies in control architecture to be uncovered more easily, or adjustments to be made for fine-tuning and adaptation purposes. Self-diagnostic and monitoring are also related to the advantages of flexibility discussed earlier in this section.

In DC/DC converters, the non-linear dynamics make the design of an optimal compensation circuit for the closed-loop operation difficult. The difficulties stem from the inherent inaccuracies in theoretical converter operations which could be due to many aspects; parasitic resistances, stray capacitances or leakage inductances of the converter components. Digital control has the ability to employ intelligent control schemes to
reduce the impact of these inaccuracies. In [41], fuzzy logic control theory is used to simplify the design of the compensation for DC/DC converters. One key aspect of this application is the use of a database of stored values (or a Look-Up Table) to decrease the control design complexity during design. This aspect is a key component of the digital controller proposed in this thesis.

Some mentionable results from advanced digital controls have been published recently [37][42]. In [37], the dead-zone digital controller was used to improve the dynamic response of Power Factor Correction (PFC) systems. Specific improvements presented include faster voltage transient responses and significantly reduced voltage overshoots and dips compared to previous systems. High-speed dynamic response is again presented in [42] along with tight output voltage regulation for a high-frequency DC/DC switching converter.

### 1.10.1 Digital control applications in ZVS-PSM-FB Converters

The literature describes digital controllers that have been developed for ZVS-PSM-FB converters. Kocybik, et al. [34] illustrates a system in which the key benefit is the opportunity to realize non-linear, predictive and adaptive control strategies, with emphasis on the ability to achieve non-linear control. In [34], the large signal analysis of the ZVS-PSM-FB is also presented, as is the non-linear dependence on input and output voltage. Realizing the control law based on this non-linear dependence would be complex with an analog control, but not true with a digital control. The control law equations developed could be programmed into the software when using digital control. The research also presented improved dynamic performance for this converter and used these results as strong validation for the use of digital control technology. Kocybik, et al.
[34] describes a scenario in which a limitation with real-time solving digital control is realized. If the control law of the converter is overly complex, the digital controller may not be able to solve the control equations in the time available due to the switching frequency of the converter. This problem was later addressed by using a look-up table (LUT) that is populated with all the possible equation outcomes. The time required to search the look-up does not vary much for different values in the LUT. As long as the look-up time is sufficiently lower than the switching period of the converter, the proper control law will be applied. The control scheme of this converter is presented in Figure 1.12

![Figure 1.13: Digital Control Scheme for ZVS-PSM-FB Converter](image-url)
The LUT produces an optimal large signal duty cycle \( (D_{\text{op}}) \) which is adjusted by a small signal compensation network \( (\hat{d}) \) produced by the feedback network and in doing so improves dynamic response, decreases complexity and increases flexibility. This LUT based process of control forms one of the foundations of the proposed digital controller in this thesis.

Design of a digital controller for the ZVS-PS-FB converter is also presented in [36] using a FPGA microprocessor. Figure 1.13 shows the block diagram of the controller.

![Figure 1.14: FPGA based digital controller for ZVS-PSM-FB Converter](image)

This technique improves upon [34] by utilizing the benefits of FPGA vs DSP controllers and was shown to increase the speed of the controller significantly so that more advanced control algorithms may be implemented. The specific advantages and disadvantages between FPGA and DSP microprocessors are discussed in further detail in the Chapter 2.

When reviewing the benefits of digital control versus analog control, it is clear that many reasons exist as to why the switch mode power converter control industry is heading in the digital control direction. From a research and design standpoint, the ability to implement effective new design iterations in a cost effective, flexible manner is
a clear benefit for digital control over analog control. The case for digital control is especially clear when dealing with converters that have non-linear dynamics where the ability to implement intelligent and adaptive control theory significantly reduces the complexity of the controller design process.

1.11 Thesis Objective

This thesis aims to present a simple, cost-effective LUT-based digital controller for the AE-ZVS-PSM-FB converter in a SOFC application. By achieving ZVS and voltage regulation under any load or line condition, this controller will be able to reduce the complexity drawback common to the analog controller, while ensuring the enhanced benefits of the AE-ZVS-PSM-FB converter and overall gain of the SOFC. The position of the AE-ZVS-PSM-FB converter as the first stage of the two stage power conversion for SOFC makes it the key motivation for research given the drawbacks under light load operating conditions. The digital controller presented in this paper is the first digital design for this particular converter.

An in-depth analysis of the proposed controller will be presented in this work. Verification will be given by Matlab simulations and Matlab/PSIM interface simulations, along with experimental switching sequence results using a Xilinx FPGA chip for demonstration-of-concept.

1.12 Thesis Organization

The goal of Chapter 1 was to provide background on the general trend of the power industry towards the creation of cost effective, highly efficient power generation technologies and to identify the Solid-Oxide Fuel Cell as one such application. The
Chapter focused on the benefits of improving the power conversion aspect of the SOFC and identified AE-ZVS-PS-FB converter as the latest step forward thus far. The key limitation of the Adaptive Energy ZVS-PS-FC converter was presented as the need for a complex non-linear control and was used to identify the purpose of evaluating the key benefits of digital control. The research discussed Section 1.10 was then used to establish the purpose and motivation for the proposed digital controller presented in Chapter 3.

Chapter 2 reviews the steady state operation of the AE-ZVS-PS-FB converter and ensured that equations established properly apply to the converter. The look-up table concept of control is presented and applied in static simulation of the circuit using the calculated phase shift values from the steady state equations. The simulations were used to validate the base model of the proposed digital controller and the results were discussed.

In Chapter 3, the proposed LUT-based digital controller was presented as a solution to the high complexity of the control circuit required for the AE-ZVS-PS-FB converter. The three main components of the digital control design were presented and discussed in detail. Simulations and experimental results are used to demonstrate proof of concept and to show that proper switching sequence was achieved under different operating conditions.

Chapter 4 implements the proposed controller for a variety of different operating conditions under dynamic conditions. An interfaced simulation setup between Matlab and PSIM was constructed for the proposed digital controller and AE-ZVS-PS-FB converter to perform the dynamic tests. Simulation results for different step changes in the load and line, along with “worst case” step changes, were demonstrated to provide
analysis for the performance of the controller. Experimental results utilizing a Xilinx test board was presented with analysis of these results reviewed and verified for output voltage regulation and ZVS.

The final chapter will conclude this thesis. A summary of the results will be presented, along with a review of the contributions and possible suggestions for future work.
Chapter 2: Adaptive-Energy Zero-Voltage-Switching Phase-Shift Full-Bridge Converter and the Look-Up Table Concept

2.1 Introduction

The benefits of the AE-ZVS-PS-FB converter, such as: higher efficiency than traditional ZVS-PS-FB converters, ZVS over all line-load conditions, no frequency-limitations and cost effectiveness at sufficient power levels make the converter an excellent choice for low power transfer systems. The key drawback is that the analog control implementation that ensures ZVS is complex and time-consuming to implement. The proposed digital control uses a Look-Up Table (LUT) approach to simplify the controller design, minimize the design time along with providing the other added benefits of digital control as discussed in Chapter 1. Before implementing the LUT digital control, the equations governing the AE-ZVS-PS-FB converter must be verified to ensure ZVS is achieved under pre-determined operating values. This chapter will review the steady state equations of this converter as well as outline, justify and verify the LUT concept.

2.2 AE-ZVS-PS-FB Converter Steady State Analysis

The AE-ZVS-PS-FB converter is comprised of two single bridge ZVS-PSM-FB converters connected at the midpoint of each leg by auxiliary inductors (L_{auxA} and L_{auxB}). Depending on the amount of phase shift between the bridges, the auxiliary inductors are able to store energy that can be used to ensure that ZVS is achievable for the entire load.
spectrum. The steady state analysis of this converter is split into two different parts, each concentrating on the different phase shifts present during operation. The first part of this chapter reviews the analysis that governs the leg-to-leg phase shift ($\Theta$), which regulates the output voltage in each bridge and ZVS under heavy load conditions. The second part of this chapter investigates the bridge-to-bridge phase shift ($\phi$), which ensures that the required energy is stored in the auxiliary inductor for ZVS to be achieved under light load conditions.

2.2.1 The Leg-to-Leg Phase Shift ($\Theta$)

In the AE-ZVS-PS-FB converter, both transformer voltage and current equations are the same as for the conventional single bridge ZVS-PSM-FB converter. This is true since the auxiliary inductors are passive elements and have no effect on the steady state operation of the overall converter [15]. The input-to-output voltage ($V_{OUT}/V_{IN}$) characteristics and steady state analysis are also identical to those derived for the ZVS-PSM-FB converter and therefore, the well documented, steady state analysis of the conventional ZVS-PSM-FB was used [20]. The ideal transformer waveforms for voltage and current are presented in Figure 2.1, where $V_P$ and $V_S$ are the primary and secondary voltage, while $I_P$ and $I_S'$ are the primary and secondary current respectively ($I_S'$ is the primary representation of the secondary current). The equations from [20] that describe the steady state operation are based on the terms defined in Figure 2.2
The following equations were derived in [20] and will be used in further steady state analysis for this circuit.
Effective Duty Cycle: \( \theta_{\text{eff}} = \frac{N_p}{N_S} \frac{V_{\text{OUT}}}{V_{\text{IN}}} \)  
\( \text{(2.1)} \)

Delta Duty Cycle: \( \Delta \theta = \frac{2V_{\text{OUT}}}{R_O} \frac{V_{\text{OUT}}}{L_O} \left( \frac{T_S}{2} - \frac{\theta_{\text{eff}} T_S}{2} \right) \)  
\( \text{(2.2)} \)

Duty Cycle (Leg-to-Leg Phase Shift): \( \theta = \theta_{\text{eff}} + \Delta \theta \)  
\( \text{(2.3)} \)

Peak Primary Current: \( I_{\text{PK}} = \frac{N_S}{N_P} \frac{V_{\text{OUT}}}{R_O} + \frac{V_{\text{IN}} - \frac{N_P}{N_S} V_{\text{OUT}}}{\left( \frac{N_P}{N_S} \right)^2 L_O} \left( \frac{\theta_{\text{eff}} T_S}{2} \right) \left( \frac{1}{2} \right) \)  
\( \text{(2.4)} \)

Initial Slope Peak: \( I_1 = I_{\text{PK}} - \frac{V_{\text{IN}} - \frac{N_P}{N_S} V_{\text{OUT}}}{\left( \frac{N_P}{N_S} \right)^2 L_O} D_{\text{eff}} \frac{T_S}{2} \)  
\( \text{(2.5)} \)

Final Slope Peak: \( I_2 = I_{\text{PK}} - \frac{N_S}{N_P} \frac{V_{\text{OUT}}}{L_O} \left( (1 - \theta) \frac{T_S}{2} \right) \)  
\( \text{(2.6)} \)

From these equations it can be seen that \( \Theta \) is governed by the inductor and capacitor values of the circuit along with the output current (\( I_O \)), input voltage (\( V_{\text{IN}} \)) and output voltage (\( V_{\text{OUT}} \)).

### 2.2.2 The Bridge-to-Bridge phase shift (\( \Phi \))

The steady state analysis of the AE-ZVS-PS-FB converter has been previously described in [15]. As discussed previously in section 1.8.3, the AE-ZVS-PS-FB converter utilizes a pair of auxiliary inductors connected across the midpoint of each bridge. The
bridge-to-bridge phase shift ($\phi$) between each single bridge operations in this converter was examined to so as to confirm that the required energy was stored in the auxiliary inductors for ZVS to be achieved under all line-and-load conditions. By adjusting $\phi$, the auxiliary inductors are able to compensate for the shortfall of stored energy in the leakage inductance of the transformers and are utilized most often under light load conditions. Figure 2.3 shows the ideal auxiliary circuit waveforms.

![Figure 2.3: Ideal Auxiliary Circuit Waveforms](image)

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The ideal AE-ZVS-PS-FB converter waveforms were presented in [15] and are shown in Figure 2.4 and Figure 2.5.

Figure 2.4: Ideal Waveforms of the AE-ZVS-PS-FB Converter
The equation for \( \phi \) was developed using interval-by-interval steady state analysis of these waveforms \([15]\) and is presented in (2.7).
Bridge-to-Bridge Phase Shift:

\[
\phi = \left[ \frac{V_{in}}{\sqrt{\frac{L_{aux}L_{lk}}{2C_{sb}(L_{aux} + L_{lk})}}} \sin \left( \frac{1}{\sqrt{\frac{L_{aux} + L_{lk}}{2C_{sb}L_{aux}L_{lk}}}} t_d \right) - I_2 \right] \frac{360 f_s 2L_{aux}}{V_{in}} \tag{2.7}
\]

It can be seen from this equation that \(\phi\) is dependant on many different variables; however, if it is assumed that the converter is designed for a desired operating point, the inductor and capacitor values can be considered constant since they would be physical values in the circuit. Also, this circuit operates with a constant switching frequency and therefore it can be assumed that \(f_s\) are a constant value as well. Due to this, \(\phi\) is only dependant on the variable values of \(V_{in}, I_O\) and \(V_O\). These dependants are similar to that of \(\Phi\) for the leg-to-leg phase shift.

### 2.3 Analog Control Method and Operation for \(\phi\)

Operation of an analog controller for \(\phi\) has previously been presented in [15]. The method described utilizes the ability to determine the rate at which the drain-source voltage of the MOSFET is decreasing to zero. By ensuring that an appropriate amount of dead time is present for the drain-source voltage to reach zero, the controller was able to achieve ZVS operation. This method required that the MOSFET drain-source voltage was monitored using a sample-and-hold chip and compared to a reference signal. The resulting control signal from this comparison would be converted through two stages to
create a phase-shifted clocking pulse. This clocking pulse would be used in the analog voltage regulator operating the phase shifted bridge. The key drawback of this method is that an extremely fast sample-and-hold chip is needed to acquire the rate of decline of the MOSFET drain-source voltage. At the time of publication of [15], a marketed sample-and-hold chip able to achieve the speed needed to operate under the experimental 250 kHz design was not available. Although this converter provides a new technological approach, it is limited by a design process which is complex to implement and time-consuming to achieve satisfactory results for different operating conditions of the converter.

2.4 ZVS and Output Voltage Regulation

The steady state equations governing the \( \Theta \) phase shift and \( \Phi \) phase shift have been presented. Both equations are dependent on the AE-ZVS-PS-FB converter design specifications for the inductors and capacitors along with the output voltage, output current and input voltage. Implementation of the AE-ZVS-PS-FB converter requires that be chosen that match the desired operating point. The operating point refers to expected line and load conditions, power level, switching frequency and any abnormalities that the circuit must be able to handle (step changes, transient changes, etc.). Many of these conditions are interconnected and based on a specific power conditioning goal. After the converter is designed based on its desired operating point, the inductor and capacitor values can be considered constant since they are physical values in the circuit. This leaves the relationships dependant on \( V_{\text{OUT}} \), \( I_0 \), and \( V_{\text{IN}} \).

The proposed digital control makes the primary assumption based on the aforementioned relationships. If one of the values is to remain constant during operation,
then that value can be entered as a constant into the relationship while the other two values are used as varying inputs. Depending on the varying input values, the produced $\Theta$ and $\phi$ results will reflect a constant expected output value. Since output voltage regulation is a desired outcome, this assumption is applied to the output voltage value. Therefore, depending on the value of load current and input voltage, $\Theta$ and $\phi$ will need to be adjusted to ensure that $V_{\text{OUT}}$ remains constant within an acceptable limit. The proposed controller in these thesis is controlling the first of 2 stages in a power conversion scheme. This means that the final output voltage regulation can have a slight ripple within an acceptable limit for the second stage to produce the proper AC output voltage. In many cases, this is roughly 5% - 10% of the expected $V_{\text{OUT}}$, for this thesis 5% was chosen as an acceptable limit. ZVS is achieved in the circuit since both equations describe the steady state analysis for ZVS operation. Implementing this with an analog control would be complex and may be unobtainable; however, a digital controller has the ability to solve the equations using logic thus simplifying the converter control implementation. The following section will discuss the general differences in digital control and the advantages and disadvantages with regard to this application.

2.5 General Differences in Digital Control Design

So far, the benefits of the ZVS-PSM-FB converter have been presented along with the different adaptations made to increase ZVS across the line and load range. The topology used for this thesis, which utilizes adaptive energy storage behaviour, was selected for its ability to achieve ZVS with lower auxiliary component count and higher efficiency. The differences discussed in Chapter 1 between analog control and digital control outlined the benefits of digital control technology in power converter design. The
previous sections have presented the steady state analysis developed in previous works, and how it would apply to digital control technology. The leg-to-leg duty cycle and bridge-to-bridge phase shift equations that govern the converter during operation were presented.

This section proposes using a FPGA controller over a DSP for the digital control hardware since a FPGA controller can operate faster then a DSP controller for a switch mode power system due to its concurrent operation. As well, this section proposes using a look-up table (LUT) versus online equation solving as the main control method, again for faster operation effectiveness.

2.5.1 FPGA and DSP controller comparison

Initial digital controller systems were Digital Signal Processing (DSP) based designs [43]. These controllers were used because their math orientated resources can be utilized for complex controller algorithms with many arithmetic operations. DSP is based on a sequential operation, where instructions are executed one after another and in the case of power system control this may prove to be a large disadvantage when working with high switching frequency systems. As the computational time eventually grows with the complexity of the control, the performance of the converter rapidly decreases as computational time comes closer to the switching period of the converter [44].

Field Programmable Gate Arrays (FPGAs) are able to avoid the pitfall of DSP controllers. The internal logic, and therefore the control procedures, of the FPGA controller are executed simultaneously and continuously, or under concurrent operation, which is opposite to the sequential operation utilized by DSP control [43]. A FPGA controller uses a fixed-point, parallel computational structure that provides computational
speeds upwards of 100 times greater than that realized with DSP controllers. FPGA based systems are also able to use separate fixed-point format for each individual signal in a system, which is unachievable in DSP based systems. [45] The use of the separate fixed-point format allows specific critical points to maintain higher computational precision while lower precision can be utilized for non-critical points, along with mitigating the numerical difficulties caused by finite-word-length effects. FPGA controls are able to achieve all of these advantages while still offering the ability to reprogram, which is a primary benefit of digital control over analog control [1, 37]. In [9], the timing of iterations between the DSP-based implementation and FPGA-based implementation were compared (see Figure 2.6 and 2.7) and it is apparent that the FPGA allowed extensively more overlap from iteration to iteration then the DSP.

As discussed earlier, the AE-ZVS-PS-FB converter utilizes the benefits of operating with a high switching frequency, and has a primary drawback of a complex control implementation. The FPGA-based control is able to utilize these attributes, and
this is the main reason why an FPGA control is used in the proposed digital control presented in Chapter 3.

2.5.2 Online solving versus Look Up Tables (LUT)

In digital control, there are two methods for solving equations required in the control process. One method uses logic to solve the control equations in real time as the varying inputs are fed in pulses using a sample-and-hold process. This real time solver method, when applied to the AE-ZVS-PS-FB converter, would provide output parameter values for each phase shift value. However, there is a drawback with this method as the switching period of the converter would be limited by the speed at which the controller could work through the equation under worst case conditions. Given the chosen topography, this limitation becomes increasingly difficult as the controller would have to solve two separate equations that are to be applied at varying times in the switching period which complicates the ability to adjust either phase shift value quickly. The second method of the use of Look-Up-Tables (LUT) for solving, as described in [34], can be used to replace real time calculations when a finite range and precision of input and output value is known or satisfactory. The amount of time needed to search a LUT depends on the resolution of the table, or amount of data stored which is based on the specific application range. In the case of the chosen converter topology, a finite range is known from its line and load spectrum. The minimum resolution of the LUT in the proposed digital controller will be discussed in Section 3.4. The proposed overall design presented in Chapter 3 is efficient, flexible and has the ability to be broadly used in other power system applications.
2.6 LUT Table Concept Applied to the AE-ZVS-PS-FB Converter

To this point, the steady state equations governing the AE-ZVS-PS-FB converter have been reviewed with a focus on the interdependence of ZVS and Output Voltage regulation to $\Theta$ and $\varphi$, and their inputs $I_0$ and $V_{in}$. The benefits of FPGA vs DSP digital controls along with a comparison of LUTs vs online calculations were presented in the previous section and the proposed digital controller discussed in Chapter 3 draws from these benefits and interdependences. The LUT concept must first be discussed with respect to the selected converter and the concept must be verified before moving forward with the proposed digital control design.

The LUT concept that will be applied to the AE-ZVS-PS-FB converter utilizes the equations for $\Theta$ and $\varphi$ to maintain ZVS and Output Voltage Regulation. The foundation of the LUT concept, in order for the ZVS and Output voltage regulation to be achieved, requires the phase shift between the switches in the circuit to be operated at specific $\Theta$ and $\varphi$ values for given values of $V_{out}$, $V_{in}$ and $I_0$. The relationship between these values was presented in the steady state analysis of the AE-ZVS-PS-FB converter in Section 2.2. The primary assumption of this thesis states that, if $V_{out}$ is entered as a constant value into the equation while $I_0$ and $V_{in}$ are left as varying inputs, then the resulting $\Theta$ and $\varphi$ will adjust the switching operation to produce ZVS and Output Voltage Regulation. Any changes in $V_{out}$ will be reflected in $I_0$, which is expected to be much smaller in magnitude than $V_{out}$ (roughly 100 times in the design applications) and is therefore more sensitive to output load adjustments. There is no feedback for this topology since final output voltage regulation is handled by the second stage inverter of the fuel cell power transfer scheme (Figure 1.2). This controller must produce output voltage with an
acceptable variance. This variance is described in the minimum precision and resolution section, Section 3.4. The LUT concept pre-determines all of the expected results of the $\Theta$ and $\phi$ equations within a reasonable resolution prior to implementation of the control theory. Therefore, the LUT would provide the required $\Theta$ and $\phi$ values based on $I_O$ and $V_{IN}$ input values to maintain ZVS and a regulated $V_{OUT}$.

To illustrate this concept, a simple graphical representation of a LUT is presented in Figure 2.8 and a block diagram of the AE-ZVS-PS-FB converter and LUT controller is presented in Figure 2.9.

![Figure 2.8: Graphical Representation of a LUT stored values](image-url)
The AE-ZVS-PS-FB block has two inputs ($V_{IN}$ and the switching values based on the LUT stored $\Theta$ and $\phi$) and two outputs ($V_{OUT}$, $I_O$). The LUT controller reads the $I_O$ and $V_{IN}$ values from the converter and outputs the required $\Theta$ and $\phi$ (as switching triggers) to the converter. How the proposed digital controller converts the $\Theta$ and $\phi$ values to switching triggers will be discussed in Chapter 3 while this section will assume that there is a direct relation. If the $V_{IN}$, $I_O$ or both values were to change, the LUT would adjust immediately to the new input values and produce proper $\Theta$ and $\phi$ trigger switching values using the pre-determined values it has stored that would ensure ZVS and output voltage regulation. Again, there is no feedback in this topology since final output voltage regulation is handled by the second stage inverter of the fuel cell power transfer. The following section will verify this concept through a PSIM design example simulation.

2.7 PSIM Design Example of LUT Concept applied to AE-ZVS-PS-FB Circuit

To verify the LUT concept and for the AE-ZVS-PS-FB circuit, a design example has been created using the PSIM power electronics simulation software. The goal of
these simulations was to prove the simulation model performed as expected and, for a
given constant load current ($I_O$) and line voltage ($V_{IN}$), that ZVS and output voltage
regulation were maintained. The simulation process is divided into two steps; the first
step is to solve the steady state equations of $\Theta$ and $\phi$ for the testing line and load
condition, the second step is to simulate the AE-ZVS-PS-FB converter under the
previously used line and load condition using the $\Theta$ and $\phi$ values from step 1 and observe
the simulation results for ZVS and output voltage regulation. This process separates the
operation of the control and circuit to verify that using $I_O$ and $V_{IN}$ will produce the proper
$\Theta$ and $\phi$ values to achieve ZVS and Output Voltage Regulation. The design example
specifications were similar to the ones developed in [15] so that it could be used as a
comparison circuit for analysis. Successful simulation results using the pre-determined
values form the basis for the proposed digital control presented in Chapter 3.

2.7.1 Determining $\Theta$ and $\phi$ Values for Line and Load Conditions

To generate the LUT contents, a Matlab m-code program was created that utilized
the steady-state equations, (2.3) and (2.7). The physical circuit component values and the
switching frequency presented in the design example were considered constants when
solving the steady-state equations. Following the primary assumption of the LUT
concept, $V_{OUT}$ was considered a constant value leaving the only variable inputs into the
equation as $V_{IN}$ and $I_O$, as expected. There were two outputs from the Matlab
calculations, one for the leg-to-leg phase shift $\Theta$ and another for the bridge-to-bridge
phase shift $\phi$. Depending on the line and load condition used for each design example
test, different $\Theta$ and $\phi$ values were calculated and used in the test setting for that
simulation. The Matlab code used to determine $\Theta$ and $\phi$ can be found in Appendix A.
2.7.2 PSIM Design Example of LUT Concept under Steady State Operation

Table 2.2 contains the design specifications for the AE-ZVS-PS-FB converter that was created in the PSIM:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Load Output Power, P_\text{OUT}</td>
<td>300 W/Bridge</td>
</tr>
<tr>
<td>Output Voltage, V_\text{OUT}</td>
<td>300 V</td>
</tr>
<tr>
<td>Input Voltage Range, V_\text{IN}</td>
<td>20 V – 32 V</td>
</tr>
<tr>
<td>Output Filter Inductance, L_\text{O}</td>
<td>1000 uH</td>
</tr>
<tr>
<td>Output Filter Capacitance, C_\text{O}</td>
<td>0.47 uF</td>
</tr>
<tr>
<td>Snubber Capacitor, C_{\text{sb}}</td>
<td>54 nF</td>
</tr>
<tr>
<td>Leakage Inductance, L_{\text{lk}}</td>
<td>317 nH</td>
</tr>
<tr>
<td>Transformer Turns Ratio, N = N_p/N_s</td>
<td>25</td>
</tr>
</tbody>
</table>

Table 2.1: LUT-Concept Design Example Values

In each simulation, the input voltage, output load and switching sequence for the converter switches was held constant for 0.5ms (125 switching cycles). The switching sequence applied was from the pre-determined Θ and φ values calculated in MatLab for the specific V_{\text{IN}} and I_{\text{O}} applied values. To demonstrate that ZVS was achieved in both of the bridges, a sample gate and switch voltage for a switch are presented.

Figures 2.10, 2.11 and 2.12 illustrate the achievement of ZVS for switch S_7 with 100%, 60% and 1% load respectively, with an input voltage of 24V. Although only ZVS results for switch S_7 are shown, simulation results proved ZVS was achieved for all 8 switches along with output voltage staying within the 5% allowable voltage error.

Figure 2.13 and 2.14 depict the achievement of ZVS for switch S_3, S_7, S_1, S_5 under worst case scenario of 0% load and an input voltage of 32V. Again, simulation results showed ZVS was achieved for all switches not shown in Figure 2.13 and 2.14 along with acceptable output voltage results.
Figure 2.10: Simulated Waveform S7: 100% load, VIN = 24V

Figure 2.11: Simulated Waveform S7: 60% load, VIN = 24V
Figure 2.12: Simulated Waveform S7: 1% load, VIN = 24V

Figure 2.13: Simulated Waveforms (S1 & S3): 0% load, VIN = 32V
These results show that a working AE-ZVS-PS-FB converter PSIM model has been created that can achieve ZVS using pre-determined $\Theta$ and $\varphi$ values over a wide range of operating conditions. This model was used in latter simulations when testing the proposed digital controller described in the next chapter.

2.8 Summary

In this chapter, the steady state analysis of the AE-ZVS-PS-FB converter was presented with attention focused on the leg-to-leg phase shift $\Theta$, and bridge-to-bridge phase shift $\varphi$. Using this analysis, the primary drawback of control complexity of the AE-ZVS-PS-FB converter for analog control implementation was discussed, along with the ability of the digital control to reduce this complexity. A general comparison of FPGA-based and DSP-based digital controls was presented outlining the benefits of FPGA-based control. The weakness of a real time calculation system when compared to
a LUT system was used as a basis for the development of the LUT concept for the AE-ZVS-PS-FB converter. Simulation results with PSIM were used to test the validity of the steady-state analysis and the application of the LUT concept. This chapter was able to demonstrate that the LUT concept could be applied to the AE-ZVS-PS-FB converter with successful simulation results, and therefore form the basis for the proposed digital control presented.
Chapter 3: Proposed LUT-based Digital Controller

In Chapter 1, the AE-ZVS-PS-FB converter was presented as a circuit that achieved both the benefits of higher switching frequency and ZVS with minimal drawbacks. A comparison of digital control to analog control was also presented with emphasis on the benefits of dealing with the drawback of control complexity in the AE-ZVS-PS-FB converter. Chapter 2 discussed the AE-ZVS-PS-FB converter in depth, with focus on the steady state analysis that governs the operation of the circuit with primary equations for the leg-to-leg phase shift $\Theta$ and bridge-to-bridge phase shift $\varphi$ being presented. The advantages of using a FPGA-based control over a DSP-based control and a LUT over online calculations were also discussed as a prelude to the presentation of the LUT concept applied to the AE-ZVS-PS-FB converter. Simulation results from PSIM were presented to confirm the equations developed in the steady state analysis and the application of the LUT concept to the AE-ZVS-PS-FB Converter.

The previous chapters have laid the basis for the proposed FPGA-based LUT digital controller that will be presented in this chapter. Chapter 3 will provide a discussion of the three primary components of the proposed controller, along with the design theory behind each component. An interval by interval timing analysis is also presented for steady state conditions and again with step change to an input. The minimum precision analysis stored values in the LUT is discussed in depth for ensuring that ZVS is achieved and output voltage regulation is within acceptable limits.
Simulation results using SimuLink are presented to verify the design for proper switching sequence dependent on a given input.

### 3.1 Digital Control Description

![Digital Control Diagram](image)

*Figure 3.1: Proposed Digital Controller Layout in SimuLink*

The proposed digital control is displayed in Figure 3.1, which is based on SimuLink block representation. The layout of the proposed digital control is broken
down into three main operation areas, or components. The first component is the switch trigger component composed of counters, comparators, and logic gates used to drive the switches of the converter. The second component includes the LUTs used for the storage of pre-determined Θ and φ values. The third component is the sampling component based on flip-flop gates used to control the frequency of input values from the power converter (I₀ and V.IN). These three major components are designed to ensure that the converter operates properly while maintaining the benefits of ZVS.

3.2 Principle of Operation

The proposed controller is based on an applied component based design theory which utilizes discrete components and timing. Each component operates in parallel with the other while information from the converter and its conversation is computed in a series orientation. A simple block diagram of this process is presented in Figure 3.2.
In brief, the process begins at the sampling component, which periodically monitors the digital controller’s inputs \(V_{IN}\) and \(I_O\) at a frequency faster than the switching frequency of the converter. This information is relayed to the LUT component to match the outputs of the converter to the appropriate \(\Theta\) and \(\phi\) stored within each LUT. The \(\Theta\) and \(\phi\) value are then passed directly to the switch trigger component, which modifies them into a switching sequence that is relayed to the switch drivers of the converter. This process is designed to ensure adjustments in the control pattern for the converter will react within one switching cycle if a change in the operating point of the converter occurs. The following sections provide analysis of the internal structure of each component and their specific objectives.

### 3.3 Switch Trigger Component

The purpose of the switch trigger component was to ensure that the proper switching sequence is promptly delivered to each of the eight switch drivers of the converter, based on the received phase shift values from the LUT component. The switch trigger component was based on a combination of three sub-components, the reference leg design, the \(\Theta\) leg design and the \(\phi\) leg design. The latter two sub-components are variations of the reference leg design.

There are three primary objectives that must be met by the switch trigger component. The objectives are based around the principal goal of delivering a switching sequence to the circuit so that proper operation of the converter may be maintained for static and dynamic conditions. The first objective of the reference leg is to ensure that all switches are operated at the same constant switching frequency, as designated by the specific design of the converter. This is an important objective since the steady-state
equations governing the $\Theta$ and $\phi$ LUT values are determined using this switching frequency and inability to achieve this objective would jeopardize ZVS and output voltage regulation. The second objective is to ensure that each switch operates at a relative 50% duty cycle under static circuit conditions. Under ideal conditions, each switch would operate at a 50% duty cycle, however, energy transfer between passive components in the circuit is not instantaneous and therefore each switch must operate at less than 50% to ensure that energy transfer for ZVS is achieved. The third primary objective is to guarantee that neither switch is active at the same time so as to avoid shorting the input source to the converter.

The three primary objectives of the switch trigger were resolved in the design of the reference leg sub-component which forms the basis for the $\Theta$ leg and the $\phi$ leg sub-components. The variations made to the reference leg design to develop the $\Theta$ leg and the $\phi$ leg sub-components were made to resolve the specific objective of the $\Theta$ leg and the $\phi$ leg sub-components. Both the $\Theta$ and the $\phi$ leg must achieve proper switching sequence modification when new $\Theta$ and $\phi$ values are delivered from the LUT component, while ensuring that the modifications are completed quickly and without compromising the achievements of the reference leg design.

3.3.1 Reference Leg Sub-component

During the design process, the reference leg had two defined goals; first to resolve the three primary objectives of the switch trigger component, and second to form the basis for the $\Theta$ leg design and the $\phi$ leg design. Figure 3.3 shows the Simulink layout of the reference leg sub-component, which is an independent process whose switching
sequence forms the basis for each of the proceeding sub-components of the switch trigger component.

Figure 3.3: Reference Leg Sub-Component Layout

The process begins with the high frequency digital clock feeding the counter Clk input to produce the incremental Cnt signal that increases with each period of the digital clock. The counter Clk input is the input for the clocking signal used to generate the incremental count signal, in this case Cnt. The counter component is reset when a comparator finds that the Cnt present value is equal to a constant input value, Period (the switching period of the converter based on the frequency of the digital clock). This achieves the first primary objective of the switch trigger in maintaining constant switching frequency; the latter aspects of the reference leg design are fed from the Cnt signal. The switching sequence for the first switch of the reference leg (switch Q₁) is generated by a less-than comparator that produces an active high signal as long as Cnt is below the constant input Switch A turn-off (the pre-determined duty cycle value for the switch). This produces a duty cycle that is less then 50% by the required dead time, t₅₆, to
ensure proper energy transfer for ZVS. The same concept of using incremental changes to a predefined turn off time is applied to the second switch of the reference leg (switch Q4). Two logic gates are used to generate a switching sequence that is active high when the Cnt signal is between the half switching period value and the switch B turn-off time, which is the proper turn off time to ensure that the required dead time is present for ZVS. The logic gates compare the Cnt value to pre-defined input values for half period (Half Period) and the switch B turn-off (Switch B turn-off). The output signal of the logic gates are relayed to an equality comparator that produces an active high signal for Q4 when both inputs are active high. The first logic gates uses a greater-than comparator to ensure that the Cnt value must be above a constant input Half Period (the half period of the switching cycle of the converter) and the second logic gate uses a less then comparator to deactivate the Q4 signal when the Cnt value is above the constant input Switch B turn-off. Since Switch A turn-off and Switch B turn-off values produce the proper dead time for ZVS, the second primary objective would be achieved. Using the same Cnt input as the driver for both switching sequences would achieve the third primary objective as both switches are activated at different value ranges of the Cnt signal.

### 3.3.2 Θ Leg Sub-component

As mentioned earlier, the Θ leg sub-component is based on a variation of the reference leg sub-component adapted to produce a switching sequence in the opposite leg of the bridge for the proper Θ phase shift. The objective of this leg is to achieve quick response to changes in the Θ input while maintaining the three primary objectives of the switch trigger component. Figure 3.4 shows the SimuLink layout of the Θ leg design.
The action of the $\Theta$ leg sub-component is driven by the same high frequency digital clock as the one used in the reference leg which is used as a Clk input for the $\Theta$ counter and $Q_2$ counter. The $\Theta$ counter increments in the same fashion as the counter from the reference leg design. However, it is reset when the Cnt signal from the reference leg design is equal to the $\Theta$ input value from the LUT component. As result of the Cnt signal driving the $\Theta$ leg sub-component the same switching period is maintained for both sub-components. This offsets the timing of the $\Theta$ leg sub-component by the proper $\Theta$ phase delay from the reference leg and therefore enables the rest of the sub-component to follow the reference leg design. However, slight changes are made to ensure that perturbations in the $\Theta$ value adjust the switching sequence while maintaining the three primary objectives of the switch trigger component. Switch A ($Q_3$ in this case) is still active high when the Cnt $\Theta$ value is less then Switch A Turn-Off, but now a new count signal Cnt $\Theta_B$ must be above the half period value for that signal to be passed on to the converter. This is done to ensure that the $Q_3$ signal is not activated while the $Q_2$ signal is still active high, and also ensures that the proper dead time for ZVS power transfer is
maintained. The $Q_2$ signal is generated by the Cnt $\Theta_B$ counter which is reset when the Cnt $\Theta$ value reaches the half period mark. When the Cnt $\Theta_B$ signal is reset at the Cnt $\Theta$ half period mark, $Q_2$ becomes active high until the Cnt $\Theta_B$ signal is less than the Switch A turn-off value. Changes in the $\Theta$ input value would either prolong the $Q_2$ signal and shorten $Q_3$ or result in the opposite response, dependent on whether the $\Theta$ input value is increased or decreased. Within one switching cycle, the switching sequence for $Q_2$ and $Q_3$ are adjusted for the new $\Theta$ input value.

### 3.3.3 $\phi$ Leg Sub-component

The $\phi$ leg sub-component is in actuality a combination of two $\Theta$ leg sub-components with addition counters and resets to properly offset the overall sub-component timing for the $\phi$ and $\Theta$ input values. Figure 3.5 illustrates the layout of the $\phi$ leg sub-component with block representation for the two $\Theta$ leg sub-component embedded within the layout. It is assumed that each of the $\Theta$ leg sub-components operate in a similar manner with the $\Theta$ counter in each $\Theta$ leg sub-component replaced by the $\phi$ counter and $\phi/\Theta$ counter respectively. The counter driving the $\Theta$ leg sub-component that produces the $Q_5$ and $Q_8$ signals (which are related to the $Q_3$ and $Q_2$ signals respectively) are reset when the Cnt signal from the reference leg reaches the $\phi$ input value, while the $\Theta$ leg sub-component that produces the $Q_7$ and $Q_6$ signals (which are also related to the $Q_3$ and $Q_2$ signals respectively) are reset when the Cnt $\phi$ (from the $\phi$ counter) reaches the $\Theta$ input value. These reset values create the proper timing off-set for the $Q_5$-$Q_8$ switching sequences.
3.4 LUT Component

As discussed in Section 2.6, the LUT component stores pre-determined $\Theta$ and $\phi$ values that are based upon the steady-state analysis of the AE-ZVS-PS-FB converter and relays these values to the switch trigger component depending on the inputs from the sampling component outputs ($V_{IN}$ and $I_O$). There are three primary objectives for the LUT component that determine the precision, resolution and data storage type for the LUT component. The first objective is to guarantee that the proper forms of the $\Theta$ and $\phi$ values are stored within the LUTs, thus removing the need for a conversation technique between the switch trigger component and the LUT component. The second objective is to ensure that the minimum precision of the data values is met; however, it will be shown that the precision will be based on the switching frequency utilized in the converter in comparison to the switching frequency of the base digital clock within the controller. The final primary objective of the LUT component is to determine the minimum resolution of the LUTs that will ensure that the output voltage is within the allowable error limits while ZVS is maintained.
To accomplish the first objective of the LUT component, the application of the $\Theta$ and $\phi$ values was required. As described in section 3.3, the switch trigger component uses the LUT outputs in comparison with a Cnt value to produce the proper time offset for the leg-to-leg phase shift and bridge-to-bridge phase shift. The Cnt value is based on a counter that is incremented by a high frequency digital clock and is reset periodically when the Cnt value reaches a constant period value (the switching period of the converter). Depending on the period of the high frequency digital clock, the Cnt value will have a different maximum value and therefore the timing offset value will be larger or smaller. The $\Theta$ and $\phi$ values stored in the LUT must be stored as a possible Cnt value that represents the proper timing offset of the Cnt period to achieve the first objective.

### 3.4.1 Minimum Precision of LUT stored values, $\Theta$ and $\phi$

The precision of the data values stored in the LUT must be accurate enough to ensure that the output values will result in ZVS conditions within the circuit, and that output voltage errors will be within the acceptable 5% threshold. This precision is dependent on the period of the high frequency digital clock utilized in the switch trigger component, because it determines the max Cnt value, which represents the required switching period for the converter. A higher switching frequency for the digital clock results in a larger max Cnt value and range, since the switching frequency is considered constant during controller design. A higher max Cnt value and range allows for more precise data, since the $\Theta$ and $\phi$ are used in a comparison to the incrementing Cnt value. Stored data must be represented as a whole number since the $\Theta$ and $\phi$ are used in direct comparison with the incrementing Cnt value. As a result, the frequency of the digital clock must be high enough to allow the stored data values to achieve the precision.
necessary to allow the converter to operate effectively. The possible error calculation was used to determine the minimum error allowance that would maintain output voltage regulation within the 5% threshold. This was done by solving the steady state equation, (2.3), under ideal "worst case" conditions. Next, an error value was assigned to the calculated ideal $\Theta$ phase shift and solved for the error value at the boundary condition for an output voltage of 5% error.

$$\theta_{\text{ideal}} = \frac{N_P V_{OUT\text{Ideal}}}{N_S V_{IN}} + \frac{2V_{OUT\text{Ideal}}}{R_O} - \frac{V_{OUT\text{Ideal}}}{L_O} \left( \frac{T_S}{2} - \frac{N_P V_{OUT\text{Ideal}}}{N_S V_{IN}} \right)$$

(3.1)

$$\theta_{\text{ideal}} + X_\theta = \frac{N_P V_{OUT\pm5\%}}{N_S V_{IN}} + \frac{2V_{OUT\pm5\%}}{R_O} - \frac{V_{OUT\pm5\%}}{L_O} \left( \frac{T_S}{2} - \frac{N_P V_{OUT\pm5\%}}{N_S V_{IN}} \right)$$

(3.2)

Where,

$X_\Theta = \Theta$ error value

$\Theta_{\text{ideal}} = \text{ideal } \Theta \text{ value}$

$V_{OUT\text{Ideal}} = \text{ideal output voltage}$

$V_{OUT\pm5\%} = \text{ideal output voltage } +/- 5\%$

A similar error analysis may be performed on the $\varphi$ phase shift steady state analysis. The error analysis requires a calculated $\varphi$ under ideal conditions and again under error conditions using the ideal $\varphi$ and $V_{OUT}$ error boundary to solve the $\varphi$ error value. This analysis uses equation 2.7 and further sub-equations presented in Chapter 2.
to determine the minimum precision for $\varphi$. The minimum precision analysis may be viewed as a minimum order of magnitude needed for all stored values, since the error value may be used to determine the minimum range of Cnt values required and therefore the minimum frequency of the digital clock.

### 3.4.2 Minimum Resolution of LUT Inputs, $V_{IN}$ and $I_O$

The minimum resolution of the LUT component may be determined in an analogous fashion to that of the minimum precision calculations. As mentioned previously, the resolution is defined as the spacing between stored values over a set range (as seen in graphical representation of a LUT in Figure 2.8). In the case of the proposed controller, the set range would be the line and load spectrum of the converter. To determine the minimum resolution, the steady state equations of the converter are used to determine the ideal “worst case” phase shift values. The calculated ideal “worst case” phase shift solutions are used within a reverse calculation (3.2), with the output voltage adjusted to the boundary error condition (+/− 5%) and error value included with the requested resolution’s input value (either $V_{IN}$ or $I_O$). The error calculation for the minimum resolution of $V_{IN}$ is shown in (3.3) and (3.4).

$$\theta_{ideal,V_{IN}} = \frac{N_p}{N_s} \frac{V_{OUT\,ideal}}{V_{IN\,ideal}} + \frac{2V_{OUT\,ideal}}{R_O} \frac{V_{OUT\,ideal}}{L_O} \left( \frac{T_S}{2} - \frac{N_p}{N_s} \frac{V_{OUT\,ideal}}{2} \right)$$

$$\left(V_{IN} + X_{V_{IN}}\right)^2 \left[ \left(-\theta_{ideal,V_{IN}}\right) \frac{N_p}{N_s} \frac{T_S}{2L_{ik}} \right] +$$
\[
(V_{IN} + X_{V_{IN}}) \left[ \frac{N_p}{N_s} V_{OUT \pm 5\%} \left( \frac{N_p}{N_s} \frac{T_s}{2L_p} \right) - \frac{2V_{OUT \pm 5\%} T_s}{R_o} - \frac{V_{OUT \pm 5\%}}{2L_o} \right] + (-\theta_{ideal, V_{IN}}) \left( \frac{V_{OUT \pm 5\%} T_s}{2L_o} \right) = 0
\]  (3.4)

Where,

\( X_{VIN} = V_{IN} \) error value

\( V_{IN_{ideal}} = \) ideal \( V_{IN} \) value

\( V_{OUT_{ideal}} = \) ideal output voltage

\( V_{OUT\pm5\%} = \) ideal output voltage +/- 5%

The calculated minimum resolution represents the allowable mid-point between two input references within the LUT component, in other words, values are only needed for twice the \( X_{VIN} \) result. The minimum resolution analysis for Io is completed in a similar fashion and is shown in (3.5) and (3.6).

\[
\theta_{ideal, I_O} = \frac{N_p}{N_s} V_{OUT_{ideal}} \frac{V_{OUT_{ideal}} L_o}{I_o} - \frac{2I_{O_{ideal}}}{L_o} \left( \frac{T_s}{2} - \frac{N_p}{N_s} \frac{V_{OUT_{ideal}}}{2} \right) \left( \frac{T_s}{2} \left( \frac{V_{IN}}{L_p} - \frac{V_{OUT_{ideal}}}{L_o} \right) \right)
\]  (3.5)

\[
I_{O_{ideal}} + X_{IO} = \left( \theta_{ideal, I_O} - \frac{N_p}{N_s} \frac{V_{OUT \pm 5\%}}{V_{IN}} \right) \frac{T_s}{2} \left( \frac{V_{IN}}{L_p} - \frac{V_{OUT \pm 5\%}}{L_o} \right) + \frac{V_{OUT \pm 5\%}}{L_o} \left( \frac{T_s}{2} - \frac{N_p}{N_s} \frac{V_{OUT \pm 5\%}}{2} \right)
\]  (3.6)

Where,

\( X_{IO} = I_{O} \) error value

\( I_{O_{ideal}} = \) ideal \( I_{O} \) value

\( V_{OUT_{ideal}} = \) ideal output voltage
\[ V_{OUT+/-5\%} = \text{ideal output voltage +/‐ 5\%} \]

It should also be noted that the precision and resolution of the LUT component is dependent on the selection of the FPGA chip as the capacity of the memory must sufficiently contain the required amount of raw data. However, for the purpose of this thesis, the memory storage capabilities of the FPGA chip are assumed to be much greater than the required data storage.

### 3.5 Sampling Component

The sampling component has two primary objectives; the first being to deliver the outputs from converter to the LUT component in a quick and concise manner. The values collected from the converter \((V_{IN} \text{ and } I_0)\) are passed through at a rate that allows the LUT component to calculate the associated \(\Theta\) and \(\varphi\) values before receiving new input information. This rate should be fast enough to allow changes in the operating point of the converter to be relayed through the controller for sufficient reaction time, since the switching frequency of the converter is a constant value and the rate should be based on a ratio to this frequency. A sampling ratio of 100 times the switching frequency was considered an acceptable minimum for this study. The second primary objective of the sampling component is to round the input data from the converter to the requirements based on the LUT minimum resolution, which allows smaller amounts of data to be transferred to the LUT component, thus leading to fewer obstacles in providing a higher transfer rate. In designing transfer frequency of the sampling component, ample dead time should be allocated for the rounding process and data transfer.
3.6 Operational Timing

Figures 3.6 and 3.7 show the ideal timing operation for the switch trigger component based on inputs from the LUT component for steady state operation. The entire process involves 18 unique switching intervals from time $t_0$ to $t_0 + T_S$. However, to limit repetition, only the repeating interval of $t_0$ to $t_6$ is discussed in terms of illustrating the operating philosophy. This interval describes the effects of the $\Theta$ phase shift timing delays effect on switch Q3 and Q2, which is comparable to Q5 and Q8 for $\varphi$ and Q7 and Q6 for $\Theta$ and $\varphi$. Figures 3.8 and 3.9 show the ideal timing operation of the switch trigger component during step change operation to further illustrate the switch trigger component philosophy. Again, only the interval $t_0$ to $t_6$ will be explained to avoid repetition.
Figure 3.6: Ideal Timing Sequence for Steady State Operation
Figure 3. 7: Ideal Timing Sequence for Steady State Operation
Logic levels are activated or deactivated based on the comparison of input values, which in many cases involves the comparison of a constant input to incrementing count values. During this interval-by-interval explanation, it is assumed that the proper comparison is made to drive the logic levels in the proper direction.

The process starts at $t_0$ with the Cnt value being reset to 0, which in turns activates $Q_1$ and pushes the signal SB high. At $t_1$, Cnt value has incremented to the $\Theta$ value received from the LUT component, which resets the Cnt$\Theta$ value to 0 and pushes $S\Theta_A$ high. Under steady state conditions Cnt$\Theta_B$ reaches the half period value and Cnt $\Theta_{BHP}$ is pushed high, which in turn activates $Q_3$. At time $t_2$ Cnt has reached the $\varphi$ value and resets Cnt$\varphi$ to 0. At this time $S\varphi_A$ becomes high, as well, Cnt$\varphi_{BHP}$ is driven high under steady state operation, which activates $Q_5$. At time $t_3$, Cnt$\varphi$ reaches the $\Theta$ threshold and resets Cnt$\varphi-\Theta$ to 0, driving $S\varphi-\Theta_A$ and Cnt$\varphi-\Theta_{HP}$ high while activating $Q_7$. At this point, the proper phase shift timing delay has been implemented within the switching sequence based on the input $\Theta$ and $\varphi$ value from the LUT component. The remaining goal of the switch trigger component is to ensure that the opposing switches on each leg are activated at the half period mark of each respective counter while deactivate the first group of switches early enough for the proper dead period.

At $t_4$ Cnt reaches the Switch A Off value and deactivates $Q_1$ while at $t_5$ Cnt reaches the Half Period value and activates $Q_4$ while driving Cnt$_{HP}$ high. The difference between Half Period and Switch A Off (along with the difference between Period and Switch B Off) is the required dead time to ensure proper energy transfer. At $t_6$, Cnt$\Theta$ reaches Switch A Off which drives $S\Theta_A$ low and deactivates $Q_3$, while at $t_7$ Cnt$\Theta$ equals
the Half Period value, which resets CntΩB, driving CntΩ_BHP low and activating Q2. This process is repeated in the same manner for the Q5/Q8 and Q7/Q6 switch pairings.

Figures 3.8 and 3.9 show a similar ideal switching sequence for the switch trigger component during step change operation. A step change in Ω was applied over interval t_0 to t_6 in order to examine the effects on Q_1/Q_2/Q_3/Q_4, however, it may be assumed that a similar process is applied to the other switch pairings for φ and Ω changes.
Figure 3.8: Ideal Timing Sequence for $\Theta$ Step Change Conditions
Figure 3.9: Ideal Timing Sequence for θ Step Change Conditions
The step change analysis begins under steady state conditions after \( t_0 \) when Cnt initially reaches the \( \Theta_1 \) value thus resetting Cnt\( \Theta \) and activating Q. At \( t_1 \), the \( \Theta \) value from the LUT component changes from \( \Theta_1 \) to \( \Theta_2 \), which is associated with a change in operating conditions in the converter. At \( t_2 \), Cnt reaches the \( \Theta_2 \) and resets Cnt\( \Theta \) which drives SO\( A \) high but Q is not activated since Cnt\( \Theta_{BHP} \) is still low as Cnt\( \Theta \) has not passed the Half Period value (Q is still active at this point). As Q and Q\( A \) were not activated simultaneously the objective of the switch trigger component, which states that no switch on a single leg is active at the same time, is satisfied. At \( t_3 \), Cnt\( \Theta \) reaches the Switch A Off value and drives SO\( A \) low, at \( t_4 \) Cnt\( \Theta_B \) reaches the Half Period value and drives Cnt\( \Theta_{BHP} \) high, but since SO\( A \) is low, Q is not activated. At \( t_5 \) Cnt\( \Theta_B \) reaches the Switch A Off value and de-activates Q leaving the required dead time for energy transfer before \( t_6 \). At \( t_6 \), Cnt reaches \( \Theta_2 \) and Cnt\( \Theta_B \) reaches the Half Period value which simultaneously drives SO\( A \) and Cnt\( \Theta_{BHP} \) high which together activate Q. At this point the process enters steady state operation.

A step change in the opposite direction (Figures 3-10 and 3-11) would result in a similar corrective process with Q (and the opposite switch in the other switching pairs) being active higher for longer the usual instead of Q, as was shown in the previous example. During a step change, the reference legs (Q\( \) and Q\( \)) are unaffected given that their timing is the basis of all switching sequences. It was observed, from these interval examinations, that the switch trigger component is able to adjust effectively to changes in input \( \Theta \) and \( \phi \) values while still achieving the required objectives.
Figure 3.10: Ideal Timing Sequence for Θ Step Change Conditions
Figure 3.11: Ideal Timing Sequence for $\Theta$ Step Change Conditions
3.7 SimuLink Simulation Results

The performance of the proposed digital controller was simulated using the SimuLink sub-program in Matlab, as shown in Figure 3-1. The goal of the simulations was to demonstrate the ability of the system to operate successfully under steady state and step change conditions. It was expected that the simulations would demonstrate the proper phase shift time delay for switch drive signals, Q₁-Q₈ based on given input values (I₀ and V_IN) into the sampling component.

The design presented in Chapter 2 was used with the following constant variables presented in Table 3.1

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Load Output Power, P_OUT</td>
<td>300W/Bridge</td>
</tr>
<tr>
<td>Output Voltage, V_OUT</td>
<td>300V</td>
</tr>
<tr>
<td>Input Voltage Range, V_IN</td>
<td>20V-32V</td>
</tr>
<tr>
<td>Output Filter Inductance, L_O</td>
<td>1000uH</td>
</tr>
<tr>
<td>Output Filter Capacitance, C_O</td>
<td>0.47uF</td>
</tr>
<tr>
<td>Snubber Capacitance, C_sb</td>
<td>54nF</td>
</tr>
<tr>
<td>Leakage Inductance, L_lik</td>
<td>317nH</td>
</tr>
<tr>
<td>Transformer Turns Ratio, N=Nₕ/Nₛ</td>
<td>25</td>
</tr>
<tr>
<td>Switch Frequency, fₛ</td>
<td>250kHz</td>
</tr>
<tr>
<td>Switch Period, Tₛ = 1/fₛ</td>
<td>4000ns</td>
</tr>
</tbody>
</table>

Table 3. 1: AE-ZVS-PS-FB Converter Design Example Values
Based on the design conditions of the AE-ZVS-PS-FB converter from Table 3.1, the following values were used in the proposed digital converters simulation set up, Table 3.2).

<table>
<thead>
<tr>
<th>Digital Clock Frequency, $f_{s,dc}$</th>
<th>100MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Clock Period, $T_{s,dc} = 1$ Cnt Increment</td>
<td>10ns</td>
</tr>
<tr>
<td>Period</td>
<td>400</td>
</tr>
<tr>
<td>Half Period</td>
<td>200</td>
</tr>
<tr>
<td>Switch A Off</td>
<td>178</td>
</tr>
<tr>
<td>Switch B Off</td>
<td>378</td>
</tr>
<tr>
<td>Sampling Frequency, $f_{s,s}$</td>
<td>50MHz</td>
</tr>
<tr>
<td>Sampling Period, $T_{s,s}$</td>
<td>20ns</td>
</tr>
</tbody>
</table>

Table 3.2: LUT-Based Digital Controller Design Example Values

It should be noted that in Simulink the counter components have an automatic reset function that was utilized for these simulations and set at the Period value.

### 3.7.1 Steady State Operation Simulation Results

The steady state operation simulations demonstrate the primary objectives of the Switching Trigger, LUT and Sampling Components by achieving the expected switching sequence of the output switch trigger signals based on simulated converter inputs.

Given a constant $V_{IN} = 24V$ and $I_O = 90\%$, Figure 3.12 illustrates the respective timing delay between $Q_1/Q_3$ and $Q_1/Q_5$ to demonstrate expected delay based on the inputs from the LUT component ($\Theta = 0.44us$, $\varphi = 1.38us$). It is assumed that all switches achieve this type of proper timing delay. Figure 3.13 shows $Q_1$, $Q_3$ and $Q_5$ (for $V_{IN} = 32V$ and $I_O = 10\%$) with expected timing delays of $\Theta = 1.28us$, $\varphi = 1.86us$ while Figure 3-
14 shows the respective timing delay between Q\textsubscript{1}, Q\textsubscript{3} and Q\textsubscript{5} (for V\textsubscript{IN}=20V, I\textsubscript{O}=50\%) with timing delays of $\Theta = 0.45\text{us}$, $\varphi = 0.23\text{us}$.

**Figure 3.12**: Q\textsubscript{1}, Q\textsubscript{3} & Q\textsubscript{5} switching sequence for V\textsubscript{IN} = 24V and I\textsubscript{O} = 90\%
Figure 3.13: Q1, Q3 & Q5 switching sequence for $V_{IN} = 32V$ and $I_O = 10\%$

Figure 3.14: Q1, Q3 & Q5 switching sequence for $V_{IN} = 20V$ and $I_O = 50\%$
The results of these simulations showed that the proposed controller was able to demonstrate proper switching sequence for simulated inputs under steady state operating conditions.

### 3.7.2 Step Change Operation Simulation results

The step change operation simulations demonstrate the primary objectives of the Switching Trigger, LUT and Sampling Components by achieving the expected switching sequence of the output switch trigger signals based on simulated converter inputs before and after the step change has occurred.

The results of a simulation switching sequence are shown in Figure 3.15. For a given $V_{IN}$ step change of 20V to 32V ($I_O = 10\%$) at the 30us mark for $Q_1$, $Q_3$ and $Q_5$, $\Theta$ is expected to increase from 0.74us to 1.39us and $\phi$ from 1.76us to 1.86us. In Figure 3.16, the switching sequence for $Q_1$, $Q_3$ and $Q_5$ is shown for a $I_O$ step change from 100$\%$ to 10$\%$ ($V_{IN} = 24V$) at the 30us mark and $\Theta$ is expected to increase from 0.37us to 1.03us with $\phi$ increasing from 1.08us to 1.82us. Figure 3.17 illustrates the switching sequence for $Q_1$, $Q_3$ and $Q_5$ for a $V_{IN}$ (32V to 24V) and $I_O$ (10$\%$ to 100$\%$) step change at the 30us mark. Over this period $\Theta$ is expected to decrease from 1.28us to 0.37us and $\phi$ from 1.85us to 1.08us.
Figure 3.15: Q1, Q3 & Q5 switching sequence for step change $V_{IN}$: 20V to 24V, Load: 10%

Figure 3.16: Q1, Q3 & Q5 switching sequence for step change $I_O$: 100% to 10%, $V_{IN}$: 24V
The proposed controller successfully demonstrated proper timing delay adjustments within the expected period of time for all step change simulations. The proposed digital controller has been verified for further implementation through the above simulation results.

3.8 Xilinx Experimental Results

The results produced by the Simulink simulations provided proof of concept for the FPGA based LUT-digital controller presented in this thesis. To solidify proof of concept, experimental results were produced using an FPGA chip and consistent input values. The simulation conditions of the Simulink tests were used for the experimental set-up and can be seen in Tables 3.1 and 3.2. The goal of these tests is to produce similar
results to those seen in the simulation results under steady state operating conditions for different operating points.

### 3.8.1 ML310 Xilinx Experimental Test Board

The experimental results were produced using a Xilinx FPGA chip on the ML310 development platform. The specifications for the ML310 board and the FPGA chip are presented in Table 3.3. The development platform had an internal clocking signal produced by a 100 MHz oscillator (period of 10 ns), which matched the value used in the simulation results for the Digital Clock Period. More information is discussed in Appendix A.

<table>
<thead>
<tr>
<th>Xilinx FPGA Device Family</th>
<th>Virtex-II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>XC2VP30</td>
</tr>
<tr>
<td>Package</td>
<td>FF896</td>
</tr>
<tr>
<td>User Clock Signal</td>
<td>100 MHz system clock oscillator (3.3V)</td>
</tr>
</tbody>
</table>

*Table 3.3: Xilinx ML310 Demonstration Board Specifications*

### 3.8.2 Experimental Results

The FPGA Xilinx chip was fed a consistent input signal for all results based on the testing situation. Figures 3.19, 3.20, 3.21, 3.22 and 3.23 show the experimental results for \( V_{IN} = 20V \) and 10% loading as the input values respectfully. In Figure 3.19, it can be seen that the reference signal \( Q_1 \), has the expected switching period of 4000ns, while in Figures 3.20 and 3.21 it can be seen that the other switch on the reference leg operates in an inverse fashion to \( Q_1 \) with the required dead time of roughly 220ns that was required. Figure 3.22 shows a time delay of 742ns between switch signal \( Q_5 \) and \( Q_7 \), which represents the expected \( \Theta \) phase delay of 74ns, while Figure 3.23 shows a time
delay of 1388ns between switch signal $Q_1$ and $Q_5$, which represents the expected $\phi$ phase of 1390ns.

Figure 3. 18: Experimental $Q_1$ Waveform: $V_{IN} = 20V$, Load = 10%

Figure 3. 19: Experimental $Q_1$ & $Q_4$ Waveforms: $V_{IN} = 20V$, Load = 10%
Figure 3.20: Experimental $Q_1$ & $Q_4$ Waveforms: $V_{IN} = 20V$, Load = 10%

Figure 3.21: Experimental $Q_1$, $Q_5$ & $Q_7$ Waveforms: $V_{IN} = 20V$, Load = 10%

Figure 3.22: Experimental $Q_1$, $Q_5$ & $Q_7$ Waveforms: $V_{IN} = 20V$, Load = 10%
Figures 3.24 to 3.28 shows similar experimental results with input voltage $V_{IN} = 20V$ and loading of 100%. Figure 3.24 shows the expected reference signal for $Q_1$ switching period, while Figures 3.25 and 3.26 show the expected dead time between $Q_1$ and $Q_4$. Figure 3.27 shows a time delay between $Q_5$ and $Q_7$ of 470ns, which was the expected $\Theta$ phase delay. Figure 3.28 shows the $\varphi$ phase delay between $Q_1$ and $Q_5$, with the expected result 240ns phase shift result produced.

![Figure 3.23: Experimental $Q_1$, Waveform: $V_{IN} = 20V$, Load = 100%](image1)

![Figure 3.24: Experimental $Q_1$ & $Q_4$, Waveforms: $V_{IN} = 20V$, Load = 100%](image2)
Figure 3.25: Experimental $Q_1$ & $Q_4$ Waveforms: $V_{IN} = 20V$, Load = 100%

Figure 3.26: Experimental $Q_1$, $Q_5$ & $Q_7$ Waveforms: $V_{IN} = 20V$, Load = 100%

Figure 3.27: Experimental $Q_1$, $Q_5$ & $Q_7$ Waveforms: $V_{IN} = 20V$, Load = 100%
3.9 **Chapter Summary**

In this chapter the proposed digital controller for the AE-ZVS-PS-FB converter was presented with a description of the three primary components; the switch trigger component, LUT component and sampling component. The description of the switch trigger component was comprised of three smaller sub-components; reference leg, $\Theta$-leg and $\varphi$-leg subcomponents used to achieve the outlined objectives for that component. The presentation of LUT component discussed the minimum precision and resolution of the input and output values needed to ensure proper error thresholds are met, while the explanation of the sampling component outlined that component’s objective as a buffer between the outputs of the converter and inputs to the LUT component.

The ideal operational timing of the proposed digital controller was discussed for steady state operation along with the operation under input step change conditions. Finally, Simulink simulation results were presented to verify the final design and demonstrate proper switching sequence was achieved for steady state and step change operations.
Chapter 4: Dynamic Response of Proposed Digital Controller and Experimental Results

In the previous chapter, the proposed LUT-base digital controller was presented. A design example was presented based on the values used in the confirmation of the LUT concept applied to the converter in section 2.7. The controller was able to demonstrate proper switch sequence waveforms for given inputs, either steady state or step change, using the Simulink simulation tool. These values were static functions fed to the controller and therefore could not demonstrate any dynamic response to adjustments in the converter. The focus of this chapter is on the presentation of a dynamic simulation model for use with the LUT digital controller using a PSIM/Simulink interface. The first simulations were run under open connection conditions to demonstrate that the interface model produced the expected results. These results were expected to closely match the LUT concept PSIM simulation results presented in Section 2.7. After confirmation of the open connection simulation results, the next set of simulations was run under integrated interface conditions. These simulations were performed in order to demonstrate that the proper dynamic response in the system occurred for steady state and step change conditions.

4.1 PSIM and Simulink Interface Model

An interactive simulation model was required to produce a dynamic response design example for both the proposed controller and the AE-ZVS-PS-FB converter. The
model needed to provide a feedback loop for dynamic values of input voltage and output current of the converter, to be provided to the digital controller model. These dynamic values are used by the digital model to provide switching sequence drivers of the switches within the converter model.

As presented in Section 2.7 the AE-ZVS-PS-FB converter was modeled to verify the LUT concept using PSIM 7.0.5 while the proposed digital controller was simulated using Simulink. The interactions between these two programs were made possible by a Simulink module created by PSIM 7.0.5 referred to as SimCoupler. SimCoupler dynamically links the PSIM model and Simulink model by operating the PSIM model from within the Simulink simulation using the generated netlist from the PSIM model. The netlist generated by the PSIM model represents the operating conditions of the model that could be used in the interaction between the two simulation programs. Results for both models were produced during the simulation to allow confirmation of operating values and timing, with both models operating for the same simulation time length and similar simulation time steps. The PSIM program uses an application called SLINK in and out nodes in the PSIM model to relay data from the Simulink model during simulation. The design examples use in-link nodes placed at the drivers of the switches while out link nodes were placed at sensors for the input voltage and output current.

4.2 Design Example for Dynamic Value Simulation Tests

The design example values for the converter used in the dynamic response simulations are identical to the ones used in section 2.7 and 3.7, while the digital controller values used in section 3.7 are shown in Table 4.2 and 4.3 respectively.
## Table 4.1: Design Example AE-ZVS-PS-FB Converter Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Load Output Power, $P_{OUT}$</td>
<td>300W/Bridge</td>
</tr>
<tr>
<td>Output Voltage, $V_{OUT}$</td>
<td>300V</td>
</tr>
<tr>
<td>Input Voltage Range, $V_{IN}$</td>
<td>20V-32V</td>
</tr>
<tr>
<td>Output Filter Inductance, $L_O$</td>
<td>1000uH</td>
</tr>
<tr>
<td>Output Filter Capacitance, $C_O$</td>
<td>0.47uF</td>
</tr>
<tr>
<td>Snubber Capacitance, $C_{sb}$</td>
<td>54nF</td>
</tr>
<tr>
<td>Leakage Inductance, $L_{lk}$</td>
<td>317nH</td>
</tr>
<tr>
<td>Transformer Turns Ratio, $N=N_p/N_s$</td>
<td>25</td>
</tr>
<tr>
<td>Switch Frequency, $f_s$</td>
<td>250kHz</td>
</tr>
<tr>
<td>Switch Period, $T_s = 1/f_s$</td>
<td>4000ns</td>
</tr>
</tbody>
</table>

## Table 4.2: Design Example LUT-based Digital Controller Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Clock Frequency, $f_{s,dc}$</td>
<td>100MHz</td>
</tr>
<tr>
<td>Digital Clock Period, $T_{s,dc} = 1$ Cnt Increment</td>
<td>10ns</td>
</tr>
<tr>
<td>Period</td>
<td>400</td>
</tr>
<tr>
<td>Half Period</td>
<td>200</td>
</tr>
<tr>
<td>Switch A Off</td>
<td>178</td>
</tr>
<tr>
<td>Switch B Off</td>
<td>378</td>
</tr>
<tr>
<td>Sampling Frequency, $f_{s,s}$</td>
<td>50MHz</td>
</tr>
<tr>
<td>Sampling Period, $T_{s,s}$</td>
<td>20ns</td>
</tr>
</tbody>
</table>

As discussed in Section 3.4, the stored values within the LUT component require a minimum resolution and precision value in order to guarantee that the converter stays within the expected error boundaries. The following sections will discuss the minimum resolution and precision boundaries.

### 4.2.1 Minimum Precision

The minimum precision analysis is performed to determine the least allowable values for $\Theta$ and $\varphi$ stored within the LUT table that would not result in the output voltage
exceeding the error boundary of 5% of $V_{OUT}$. In Section 3.4, equations 3-1 and 3-2 were used to determine the minimum precision separation for $\Theta$. The equations were used under a worst case scenario in which the input voltage was at its peak rated value and output loads were light (approximately 1%). These settings allowed for the determination of the minimum precision required for the controller. All component values for 3.3 were taken directly from the design example for worst case scenario of the $\Theta$ precision calculation along with the following values.

<table>
<thead>
<tr>
<th>$\Theta_{ideal}$</th>
<th>0.3275</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUTideal}$</td>
<td>300V</td>
</tr>
<tr>
<td>$V_{OUT\pm 5%}$</td>
<td>300V $\pm$ 5% (15V)</td>
</tr>
</tbody>
</table>

Table 4.3: Calculated Minimum Precision

Solving equation 3-1 for the $\Theta$ error, $X_\Theta$ yields 0.139 for $V_{OUT} = 315V$ and 0.077 for $V_{OUT} = 285V$. Using these results, the worst case scenario would occur when $V_{IN} = V_{IN,max} = 32V$ and load is 1% while the output voltage $V_{OUT}$ would not be expected to drop below 285V. As $\Theta$ is represented as a time value proportional to the switching period (4000ns), the stored values would have a minimum precision of 154ns. The minimum precision used during simulations was 10ns, which simplified computation and provided a buffer against the error boundary.

The same analysis was used for determining the minimum $\varphi$ precision needed based on the design example. Equation 2-7, was used to solve for the ideal and worst case scenario conditions. The minimum $\varphi$ precision was determined to be 0.010 or 20.29ns. For the reasons described above, a precision value of 10ns was used for all stored $\varphi$ values within the LUT component.
4.2.2 Minimum Resolution

The minimum resolution analysis for the design example was performed to determine the minimum separation of stored LUT values for the given inputs, $V_{IN}$ and $I_O$. As with the minimum precision calculations, minimum resolution analysis was accomplished by solving for the input value under both ideal and worst case scenario conditions. The opposing input was held constant at worst case scenario conditions during analysis of the other input. Eq 3.3 was used to solve for the minimum $V_{IN}$ ($V_{IN_{min}}$) with the opposing input held constant (for worst case conditions). All component values for Eq 3.3 were taken directly from the design example.

Eq 3.3 is a quadratic equation and therefore the solution of this equation yielded two values for $V_{IN_{min}}$, 18.512 and 1.00028. The lower value was used as the minimum resolution for the result of the example. To check the validity of the calculated value, the minimum resolution analysis was performed on only the effective $\Theta$ ($\Theta_{eff}$) Eq (2.1) since it forms part of the total $\Theta$ Eq 2-3. This analysis produced a minimum $V_{IN}$ resolution of 1, which was close to the calculated value using the full $\Theta$ equation. As discussed in section 3.4, the minimum resolution analysis delivers the minimum mid-point required between input references for calculated stored values and therefore the minimum separation based on a given input between stored values should be twice the error value $X_{VIN}$, or in this case, greater than 2. To further protect against design error a separation of 1 was used between all $V_{IN}$ input values.

The minimum resolution analysis for the input value $I_O$ was presented in Eqs. 3-4 and 3-5 and was performed under a worst case scenario of maximum rated input voltage.
and light load conditions (circa 1%). All component values from the design example were used in the analysis.

The minimum resolution analysis for $I_O$ determined a midpoint of 6.5% (0.065A) for all input load values, or a minimum separation of 13% (0.13A). To prevent possible design error, a separation of 5% (0.05A) was used between all input load values for calculating stored $\Theta$ and $\varphi$ values.

<table>
<thead>
<tr>
<th>$V_{IN,ideal}$</th>
<th>20V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT,ideal}$</td>
<td>300V</td>
</tr>
<tr>
<td>$V_{OUT+/-5%}$</td>
<td>300V +/− 5% = 285V</td>
</tr>
<tr>
<td>$I_{O,ideal}$</td>
<td>0.01A</td>
</tr>
<tr>
<td>$V_{OUT,ideal}$</td>
<td>300V</td>
</tr>
<tr>
<td>$V_{OUT+/-5%}$</td>
<td>300V +/− 5% = 285V</td>
</tr>
</tbody>
</table>

Table 4.4: Calculated Minimum Resolution Values

The minimum resolution analysis also had an impact on the rounding required for the sampling component. Since the chosen minimum resolution for $V_{IN}$ had was 1V, all $V_{IN}$ values sampled from the converter were rounded to the nearest volt, with the minimum resolution of $I_O$ set to 0.05A, all sampled $I_O$ values were rounded to the nearest 50mA.

4.3 Open Connection Interface Simulation

To verify the operation of the Simcoupler interface an open connection simulation was performed under steady state conditions with an output load of 60% and input voltage of 28V. For the open connection simulation, no feedback from the output values
of the converter were relayed to the LUT controller. Figure 4.1 shows the ZVS waveforms for switch Q7 under open connection simulation.

![Figure 4.1: ZVS for Simulated Voltage Waveforms Q7: V\textsubscript{IN} = 28V, Load = 60%](image)

### 4.4 Dynamic Response Interface Simulation Results

After verifying the operation of the Simcoupler interface, the next step involved conducting dynamic response simulations with a completed feedback loop between the AE-ZVS-PS-FB converter and the LUT controller. The interconnected simulations operated under steady state and step change conditions while switch S7 was observed for ZVS. As Q7 is the lagging leg it required the longest dead time to properly achieve ZVS. Figure 4.2 shows ZVS for switch Q7 under steady state operation between the converter and controller with an input voltage of 24V and output load of 80%. Figure 4.3 shows the full simulation results for an input voltage step change from a minimum rating of 20V...
to a maximum rating of 32V while operating under full load conditions (100%). Figures 4.4 and 4.5 show ZVS for switch Q₇ before and after the step change occurs respectively, while Figure 4.6 shows the output voltage over the simulation range. It can be seen that the output voltage does not leave the defined error boundary of +/- 5% of nominal voltage (300V) during the step change operation. The final dynamic response simulation varied the load step change between 10% and 100% while operating under the minimum rated input voltage (20V). Figures 4.7 and 4.8 show the achievement of ZVS for switch Q₇ before and after the step function application respectively.

Figure 4. 2: ZVS for Simulated Voltage Waveforms Q₇: \( V_{IN} = 24V \), Load = 80%
Figure 4. 3: ZVS for Simulated Voltage Waveforms Q5: $V_{IN} = 20V-32V$, Load = 100%

Figure 4. 4: ZVS for Simulated Voltage Waveforms Q5: $V_{IN} = 20V$, Load = 100%
Figure 4. 5: ZVS for Simulated Voltage Waveforms Q7: \( V_{IN} = 32V, \) Load = 100%
Figure 4. 6: Simulated Output Voltage Waveforms $V_{O1}$ & $V_{O2}$: $V_{IN} = 20V-32V$, Load = 100%

Figure 4. 7: ZVS for Simulated Voltage Waveforms $Q_7$: $V_{IN} = 20V$, Load = 10%
Figure 4.8: ZVS for Simulated Voltage Waveforms $Q$: $V_{\text{IN}} = 20\text{V}$, Load = 100%

4.5 Chapter Summary

The dynamic response of the combined AE-ZVS-PS-FB converter and LUT-based digital controller were presented. The interconnection of the Simulink program for the digital controller and the PSIM program for the AE-ZVS-PS-FB converter allowed the operation of the converter to be examined in steady state and step change conditions. A design example was used to demonstrate the validity of the interconnection model. Minimum precision and resolution were calculated for the design example and used in the open connection and dynamic connection simulations. Both sets of results were examined for ZVS operating conditions to ensure that the proper switching signal was
being relayed to the converter during the simulation. Successful simulation results allowed for verification of the LUT-based digital controller concept.
Chapter 5: Summary and Contributions

5.1 Summary

The advantages and disadvantages of fuel-cell power generation were discussed along with the evolution towards the ZVS-PS-FB converter for use in the first stage of a multi-stage power conversion scheme. This research focused on the benefits of the AE-ZVS-PS-FB converter when applied to fuel-cell power generation. The advantage of digital control versus analog control in power controllers was also examined with attention focused on their simplicity and low-cost implementation.

Steady state analysis of the AE-ZVS-PS-FB converter identified control complexity as a main drawback of the converter and required the development of control equations for use with the proposed digital controller. Use of the FPGA based digital controller, which utilizes the Look-Up Table concept, was outlined and the LUT concept was applied to the AE-ZVS-PS-FB converter. The system was verified through simulations in Matlab.

The LUT based digital controller and its three major components were discussed in terms of their prime objectives. Ideal operation for each major component was also discussed on an interval by interval basis. Simulations using the controller were performed under steady state and step change conditions, thus providing proof of concept. Experimental results for the LUT based digital controller were further demonstrated using the Xilinx FPGA XC2VP30 chip.
Finally, a dynamic response interface model, which was used to determine the effectiveness of the proposed design, was presented. The interface model simulated the inter-connected converter and controller under steady state and step change conditions to ensure that ZVS was maintained throughout the operation.

5.2 Contributions

The development of a simple, robust, flexible and cost effective LUT-based digital controller represents the key contribution of this dissertation. Through both simulated and experimental analyses, the capability of the LUT-based digital controller to achieve a zero voltage switching sequence for the novel AE-ZVS-PS-FB converter over all operating conditions was described. Even during a worst case scenario involving light load conditions, the converter achieved a zero voltage switching sequence. The controller was able to overcome the primary drawback of the converter in terms of the control complexity in a simple, efficient manner, while maintaining the advantages of the converter. Due to the relative simplicity of the design process, it is reasonable to consider this controller to be a substitute for the currently utilised, more complex, analog controllers.

An additional major contribution of this work is the establishment of the LUT-based digital controller as a cost-effective controller implementation. Applied to a novel converter design for fuel-cell based power generation, the proposed controller was observed as cost effective due to its simplicity of design and undemanding hardware requirements. The LUT-based digital controller allowed the benefits of fuel-cell power generation and the AE-ZVS-PS-FB converter to be fully realized without a costly controller implementation.
5.3 Future Work

The research discussed above has presented the possibility of research in three major areas of focus.

i. Hardware Design Optimization:

One of the key benefits of the controller is that it builds upon existing digital technological advantages that are present in different applications. The drawback is that these technologies are not optimized for this power converter control and adjustments at the onset of the initial control chip design could yield significant advantages. It is therefore suggested that an optimized hardware design be developed specifically for this LUT-based digital power controller that can fully utilize the advantages of the latest digital technology and the simplicity of the proposed controller.

ii. Improve Dynamic Performance:

In this thesis, the establishment of the LUT-concept for the novel converter was the primary goal. However, to improve upon dynamic performance of the converter, further research is needed to determine the full effects of proposed LUT-based digital controller. These effects should be evaluated with respect to controller efficiency, effectiveness and the other advantages that have been discussed for the LUT-based digital controller.

iii. Expand Flexibility:

A major advantage of the design discussed above is the flexibility of the digital control design process. This advantage was established with the application of the controller to a novel (less then 1 year old) converter design.
The added flexibility achieved through this design could be expanded to allow new converter restraints to be incorporated into the digital controller design or to decrease the time needed for design verification. Therefore, research into the flexibility limitations of the LUT-based digital controller design process, in terms of reduced development cost and time for novel converter designs across different power converter families should be performed.
References


Appendix A: Xilinx ML310 Development Platform

All experimental results produced were demonstrated using the Xilinx built ML310 development platform. The development board offers a Virtex-II Pro XC2VP30-based embedded platform, with over 30,000 logic cells available within the FPGA. The development board utilizes an internal oscillator operating at 100MHz, with multiple I/O ports for upload and control applications. Figure A.1 below shows the block diagram for the entire development board below.

![Block Diagram of Xilinx ML310 Development Platform](image)

This research makes use of the LED and GPIO I/O ports for monitoring the results from the uploaded proposed controller design. The sixteen available pins allowed for all eight switching signals, include ground signals, to be output from the board during
experimental testing. The output pins and the associated microcontrollers are outlined in a block diagram presented in Figure A.2.

![Block Diagram for LCD Connectivity](image)

**Figure A. 2: Block Diagram for LCD Connectivity**

The parallel cable IV interface was used to program the Xilinx board with the proposed controller, along with uploading input variables for testing. The Wavepro 7000, 1 GHz oscillator manufactured by Lecroy, captured the switching sequence experimental results produced by the ML310 development platform.