A Novel Variable Inductor-Based VCO Design with 17% Frequency Tuning Range for IEEE 802.11ad Applications

by

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Abstract

This thesis focuses on the design and analysis of a novel variable inductor (VID) based VCO solution to the frequency tuning range (TR) limitation of the IEEE 802.11ad compliant radio systems. The IEEE 802.11ad standard has drawn strong attention from the industry as the next generation affordable multi-gigabit speed wireless communication standard. Prepared for the global market, IEEE 802.11ad compliant systems are required to cover a broad 8 GHz TR centered on 60 GHz. This wide TR at V band imposes significant challenge to the VCO design in radio transceivers, and makes the TR of the integrated VCO a major bottleneck to the successful commercialization of many IEEE 802.11ad compliant radio systems today.

As an effort to solve the current TR problem for the IEEE 802.11ad compliant radio systems, 2 VCOs designs based on this novel VID-based solution and a conventional Colpitts-Clapp VCO design are presented in this thesis report. The novel VCOs integrate a VID into the differential Colpitts configuration to create a feasible solution to the aforementioned TR problem. The VID in the VCO tank eliminates the base node varactors and their fixed parasitic capacitance that degrades TR in conventional VCO designs, while the differential Colpitts configuration provides advantageous performance at mm-wave frequencies and high output power for real-world applications. Also, a fundamental 30 GHz Colpitts-Clapp VCO was developed in conjunction with
the other 2 VCOs for comparison purposes.

One of the 2 VID-based VCO designs is a fundamental 30 GHz VID-based Colpitts VCO that covers 17% TR for proof of concept to the novel topology. Another is an IEEE 802.11ad compliant 60 GHz VCO chain consists of the 30 GHz VID-based Colpitts VCO and a frequency doubler covering 17% TR with 3 dBm output power and -115.7 dBc/Hz phase noise at 10 MHz offset. The conventional Colpitts-Clapp VCO is used to compare with the other 2 VID-based VCOs. As the measurement results indicate, this VID-based VCO topology provides a viable solution to overcome the TR bottleneck in the current IEEE 802.11ad compliant VCO development. All 3 VCOs are fabricated using a 130 nm SiGe BiCMOS process.
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# Contents

Abstract \hspace{1cm} i

Acknowledgments \hspace{1cm} iii

Contents \hspace{1cm} v

List of Tables \hspace{1cm} vii

List of Figures \hspace{1cm} viii

Glossary \hspace{1cm} xiii

Chapter 1: Introduction \hspace{1cm} 1

1.1 The Demand for High Speed yet Economical VCO with Wide Frequency Tuning Range \hspace{1cm} 1

1.2 The Solution Provided by This Work \hspace{1cm} 2

1.3 Organization of Thesis \hspace{1cm} 3

Chapter 2: Background \hspace{1cm} 4

2.1 A Brief Description of IEEE 802.11ad Standard and the Design Goals \hspace{1cm} 4

2.2 Review of Selective Feedback VCO Topologies \hspace{1cm} 6

2.3 Differential Colpitts VCO Operation Details and Performance Optimizations \hspace{1cm} 9

2.4 Varactor Bank Operations and Q-Factor Optimizations \hspace{1cm} 17

2.5 Variable Inductor Operation and Integration on VCO \hspace{1cm} 22

2.6 Frequency Doubler Operation \hspace{1cm} 29

2.7 Definitions of Figure of Merit for VCOs \hspace{1cm} 32

2.8 Selected Literature Review of VCO Design Topologies \hspace{1cm} 34

Chapter 3: The Design of 30 GHz VID-Based Differential Colpitts VCO \hspace{1cm} 42

3.1 VCO Design Details \hspace{1cm} 43
List of Tables

2.1 Simplified varactor bank operation demonstration . . . . . . . . . . . . 20
2.2 Comparison of the state-of-the-art VCOs reviewed in this section . . 41

3.1 Inductor Specifications . . . . . . . . . . . . . . . . . . . . . . . . . . 59
3.2 30 GHz VID-based Colpitts VCO component list . . . . . . . . . . . . 61
3.3 Three bits varactor analysis . . . . . . . . . . . . . . . . . . . . . . . . . 64
3.4 30 GHz VID-based differential Colpitts VCO performance summary . 72

4.1 60 GHz VID-based differential Colpitts VCO component list . . . . 79
4.2 30 GHz VID-based differential Colpitts VCO performance summary . 89

5.1 30 GHz Colpitts-Clapp VCO component list . . . . . . . . . . . . . . 96
5.2 30 GHz VCO gain comparison . . . . . . . . . . . . . . . . . . . . . . . . 102
5.3 30 GHz VID-based differential Colpitts VCO performance summary . 104

6.1 Comparison of 30 GHz VCOs . . . . . . . . . . . . . . . . . . . . . . . 107
6.2 Comparison of 60 GHz VCOs . . . . . . . . . . . . . . . . . . . . . . . 108
List of Figures

2.1 Simplified oscillator circuits of (a) Colpitts type oscillator, (b) Clapp type oscillator, and (c) Hartley type oscillator . . . . . . . . . . . . . 7
2.2 Simplified single-ended Colpitts VCO . . . . . . . . . . . . . . . . . . 10
2.3 Simplified differential Colpitts VCO . . . . . . . . . . . . . . . . . . 16
2.4 Simplified differential Colpitts-Clapp VCO . . . . . . . . . . . . . . 18
2.5 Simplified single-sided varactor bank . . . . . . . . . . . . . . . . . . 20
2.6 VID equivalent circuit . . . . . . . . . . . . . . . . . . . . . . . . . . 22
2.7 Simplified VID equivalent circuit . . . . . . . . . . . . . . . . . . . . 22
2.8 Sample $L_{eq}$ vs $R_v$ simulated at 30 GHz . . . . . . . . . . . . . . 24
2.9 Sample $Q$ vs $R_v$ simulated at 30 GHz . . . . . . . . . . . . . . . . . 26
2.10 Simplified frequency doubler circuit . . . . . . . . . . . . . . . . . . . 30
2.11 The cross-coupled VCO with the output buffer stage . . . . . . . . 35
2.12 Frequency vs. VC (voltage control) of the cross-coupled VCO . . . 35
2.13 The first fully integrated differential Colpitts VCO presented in 1997 36
2.14 A differential Colpitts VCO operates at 74 GHz implemented using 0.13 $\mu$m SiGe BiCMOS technology . . . . . . . . . . . . . . . . . . . . 38
2.15 The die photograph of the 74 GHz VCO . . . . . . . . . . . . . . . . . 39
2.16 The schematic of the VID-based cross-coupled VCO proposed by T. Y. Lu, et al. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 40
2.17 The measured phase noise performance of the VID-based cross-coupled VCO proposed by T. Y. Lu, et al. .................................................. 41

3.1 30 GHz VID-based VCO schematic, shows the VID in (1), the varactor bank in (2), the switching HBT in (3), the current mirror bias in (4), and the CC output buffer in (5) .................................................. 44

3.2 Transformer windings radii and its impact of $L_{eq}$ of the VID. Different curves in different colors represent VID characteristics with transformers of different winding radii. .................................................. 46

3.3 Transformer performance in terms of (a) the transformer winding inductances, (b) the transformer winding Q factors, and (c) the transformer coupling coefficient $k$ .................................................. 47

3.4 Demonstration of the NMOS transistor in terms of (a) the terminal resistance $R_{eq}$ and (b) the terminal capacitance $C_v$ with different device widths (slight ripples in the simulation results were due to the limitations by the simulator used and can be ignored) .......................... 48

3.5 Isolated VID schematic .................................................. 48

3.6 Isolated VID layout .................................................. 49

3.7 Inductive tuning performance of the VID .................................. 50

3.8 The 50 fF varactor layout .................................................. 51

3.9 The 50 fF, 100 fF, and 200 fF varactor layouts from bottom to top 52

3.10 The 50 fF, 100 fF, and 200 fF varactors tuning curves .......... 52

3.11 The layout of the 10 μm switching HBT .................................. 54

3.12 10 μm HBT frequency dependent characteristics .......................... 55
3.13 Simulated differential waveforms captured from the VCO using buffer HBT pair with (a) 6 µm and (b) 3 µm emitter size for the CC output buffer. Marker M0 points to the waveform at the collector nodes of $Q_1$ and its twin, M1 points to the waveform at the base node of $Q_1$ and its twin, and M2 points to the waveform at this final output nodes of $Q_2$ and its twin.

3.14 The layout of $L_3$.

3.15 30 GHz VID-based VCO layout.

3.16 Simulated frequency tuning characteristics of the 30 GHz VID-based VCO.

3.17 Adjacent bands overlap.

3.18 Simulated phase noise at 1 MHz offset from the 30 GHz VID-based differential Colpitts VCO.

3.19 Photo of the 30 GHz VID-based differential Colpitts VCO.

3.20 Measurement setup for the 30 GHz VID-based differential Colpitts VCO.

3.21 Measured frequency tuning curves of the 30 GHz VID-based differential Colpitts VCO.

3.22 Measured vs. simulated phase noise values of the 30 GHz VID-based differential Colpitts VCO.

3.23 Measured differential output power from the 30 GHz VID-based differential Colpitts VCO.

4.1 60 GHz VID & frequency doubler based VCO schematic.
4.2 The 60 GHz VID-based differential Colpitts VCO waveforms captured at the collector node of the VCO and the output of the frequency doubler, clearly demonstrating the frequency doubling behavior by the frequency doubler .......................................................... 76
4.3 Frequency doubler module layout .................................................. 77
4.4 The layout of the 60 GHz VID-based VCO chain .............................. 78
4.5 Simulated frequency tuning characteristics of the 60 GHz VID-based VCO chain ................................................................. 80
4.6 Simulated phase noise variations of the 60 GHz VID-based Colpitts VCO chain ................................................................. 81
4.7 Photo of the 60 GHz VID-based VCO chain ....................................... 82
4.8 Measurement setup for the 60 GHz VID-based differential Colpitts VCO ................................................................. 84
4.9 Measured frequency tuning curves of the 60 GHz VID-based differential Colpitts VCO ................................................................. 85
4.10 Measured vs. simulated phase noise values of the 60 GHz VID-based differential Colpitts VCO ................................................................. 87
4.11 Demonstration of the strong interferences coupled onto the phase noise measurement of the 60 GHz VID-based Colpitts VCO chain ............. 88
4.12 Measured output power of the 60 GHz VID-based differential Colpitts VCO ................................................................. 88

5.1 30 GHz Colpitts-Clapp VCO schematic ............................................ 92
5.2 The base inductor used in the 30 GHz differential Colpitts-Clapp VCO ................................................................. 93
5.3 The base inductor characteristics .......................................................... 94
5.4 30 GHz differential Colpitts-Clapp VCO layout ..................................... 95
Glossary

AMOS
Acronym for accumulation-mode MOSFET. One type of varactor. It is constructed by using n+ source-drain diffusion in a n-well.

BiCMOS
A type silicon-based process that both bipolar junction transistor and field-effect transistor can be fabricated on the same die.

CMOS
Acronym for complementary metal-oxide-semiconductor. A standard silicon based process that contains both n-type and p-type transistors.

CC
Acronym for common-collector, a configuration of transistors. Often used to describe amplifiers.

CE
Acronym for common-emitter, a configuration of transistors. Often used to describe amplifiers.

DC-to-RF efficiency
The ability of a transistor in a certain bias condition to convert DC power into radio-frequency power.

\( f_{\text{max}} \)

The maximum frequency of oscillation of a transistor. When reach \( f_{\text{max}} \) the transistor has power gain of 1 (0 dB).

\( f_T \)

The unity-gain frequency (or cutoff frequency) of a transistor. When reach \( f_T \) the transistor has current gain of 1 (0 dB).

**HBT**

Acronym for heterojunction bipolar transistor. A type of bipolar junction transistor.

**IEEE 802.11ad**

Also known as WiGig. A next generation multi-gigabit wireless communication standard designed to have maximum data rate up to 6.75 Gbit/s. It operates on 60 GHz bands.

\( k_{VCO} \)

VCO gain, or sometimes referred to as VCO sensitivity. It shows the rate of change of oscillation frequency as a function of input control voltage, hence with unit Hz/V. Higher \( k_{VCO} \) can result in higher phase noise.

**LNA**

Acronym for low noise amplifier. It is used to amplify a weak signal with minimum added noise.
LSB
Acronym for least significant bit. It refers to the right-most bit in a binary number string.

MOSFET
Acronym for metal-oxide-semiconductor field-effect transistor. Another transistor type beside bipolar junction transistor. It conducts current by pinching channel in the channel region according its gate voltage.

MSB
Acronym for most significant bit. It refers to the left-most bit in a binary number string.

$NF_{\text{min}}$
The minimum noise figure from a component. It is minimum ratio of the signal to noise ratio at input vs at output, expressed in decibel.

off-capacitance
The equivalent capacitance of a varactor when its terminal voltage is at low state.

on-capacitance
The equivalent capacitance of a varactor when its terminal voltage is at high state.

PA
Acronym for power amplifier. It is used to boost signal power. Normally can be found at the output stage of a multi-stage integrated circuit.
**PDK**

Acronym for process design kit. Foundries across the world release PDKs tailored for specific technologies to ease and regulate the design process.

**PLL**

Acronym for phase-locked loop. It is a frequency synthesizer in radio systems. It creates an open or closed-loop control to a VCO to stabilize its phase of the output signal. An integrated VCO is not very useful to a radio system without integrated into a phase-locked loop.

**PVT**

Acronym for process voltage temperature variation. It is often used to describe the unpredictable performance difference between simulation and measurement results due to variations in fabrication process, voltage conditions, and operating temperature.

**RF**

Acronym for radio frequency, which covers frequencies from 3 kHz to 300 GHz.

**SiGe**

Acronym for silicon germanium. A controlled amount of germanium is doped into silicon to reduce its band gap, hence creating superior high frequency performance.

**TR**

Acronym for tuning range of the oscillation frequency of a VCO.

**VCO**
Acronym for voltage controlled oscillator. It is a device that converts control voltage into output frequency signals.

**VID**

Acronym for variable inductor. It changes its equivalent inductance according to control voltage.

**Vtune**

In this thesis, it represents the tuning voltage to the VCO tank. It can be regarded as the control voltage of either the variable inductor, or varactors, depending on the VCO topology.

**WiGig**

Another name for the IEEE 802.11ad standard, which is introduced in more details in 2.1.
Chapter 1

Introduction

1.1 The Demand for High Speed yet Economical VCO with Wide Frequency Tuning Range

In recent years, backed by the high demand from the original equipment, backhaul, and consumer markets, the drive for affordable multi-gigabit speed wireless communication systems has became increasingly strong. The IEEE 802.11ad (WiGig) standard was developed under this high demand as the answer to the future of high speed wireless communications.

An IEEE 802.11ad compliant radio system is required to operate from 57.24 to 65.88 GHz in order to cover the 4 bands specified by the standard [1]. This wide frequency span (14.4%) in V band imposes challenges for the industry to realize a suitable signal source with low cost, low power consumption, low phase noise, high stability, high output power (Pout), and wide frequency tuning range (TR).

The recent works targeted on the 60 GHz band have shown promising performances [2] [3] [4] [5] [6], and they have proven the feasibility of commercializing high-frequency CMOS-based VCOs in various applications to reduce cost. Those VCO
designs are implemented in either selective feedback or cross-coupled VCO topolo-
gies, but the TR adjustment are all done through changing the VCO tank varactor
and inductor characteristics. Because of the limitations of the tank varactors and
inductors, or the VCO topology, none of those designs provide a suitable solution for
IEEE 802.11ad applications due to their limited TR and/or low Pout.

The industrial partner of this project, Peraso Technologies Inc. has encountered
the same performance bottleneck of insufficient VCO TR on their current generation
IEEE 802.11ad radio system. The performance of their current integrated VCO is
beyond the IEEE 802.11ad standard requirement except the TR. Therefore, as an
effort to widen VCO TR and contribute to the commercial deployment of IEEE
802.11ad radio systems, this collaborated research project was formed.

1.2 The Solution Provided by This Work

By combining emitter node varactor coarse frequency tuning and base node variable
inductor (VID) frequency fine tuning onto a Colpitts based VCO unit, a novel solu-
tion to the aforementioned signal source TR issue is created for IEEE 802.11ad radio
systems and presented in this thesis. This VCO topology is implemented in 2 VCOs.
One VCO operates on 30 GHz center frequency as the fundamental VCO, the other is
connected to a frequency doubler to output around 60 GHz signals for the implemen-
tation to IEEE 802.11ad compliant radio systems. Both of the 2 VCOs achieve 17%
TR, which fully covers the IEEE 802.11ad standard requirement. To the author’s
knowledge, this is the first time that such VCO topology has been implemented in
silicon technologies for millimeter-wave applications.
1.3 Organization of Thesis

The thesis report is organized in the following manner. Chapter 2 introduces the background information on the operation of generic Colpitts and Colpitts-Clapp VCOs, VID, frequency doubler, the concept of figures of merit, as well as the IEEE 802.11ad standard. Chapter 3 discusses the design, measurement, and evaluation for the proposed 30 GHz VID-based VCO in detail. Chapter 4 describes the design, measurement, and evaluation of the proposed 60 GHz VID-based VCO chain, with the detailed information on the design and implementation of the frequency doubler. Chapter 5 shows the design, measurement, and evaluation of a conventional 30 GHz Colpitts-Clapp VCO, which was designed to provide a point of reference for the novel design of the VID-based VCOs, as well as an alternative to the VID-based VCOs to be implemented in the 60 GHz VCO chain presented in this thesis report.
Chapter 2

Background

This chapter starts with the review of several different VCO design topologies, then it explains the operation of typical Colpitts and Colpitts-Clapp VCOs, VID, and other preliminary information of such a system before focusing on the more detailed discussion in the later chapters.

2.1 A Brief Description of IEEE 802.11ad Standard and the Design Goals

On April 1st 2009, the Wireless Gigabit Alliance was established to develop specifications for audio, video, and data transmission in the mm-wave frequency band, operating in both line-of-sight or non-line-of-sight environments. The result was the creation of the WiGig standard, which was adopted by IEEE as IEEE 802.11ad draft 0.1 on May 20th 2010.

IEEE 802.11ad standard avoids the now congested 2.4 / 5 GHz frequency bands and utilizes the globally available 60 GHz band to achieve a maximum data rate of 6.75 Gbps (IEEE 802.11n has a maximum data rate of 0.6 Gbps in comparison). This high date rate makes IEEE 802.11ad an ideal topology for short range wireless
transmission of uncompressed audio, video, and other data streams that require multi-gigabit links. As the latest standardization issued for the 60 GHz specifications, IEEE 802.11ad standard features wide range use cases using both single carrier and OFDM, with multiple vendor support. The use of 60 GHz frequency also utilizes the unique absorption characteristics. In the atmosphere, 60 GHz is the absorption resonance of oxygen, this feature limits propagation in secured applications, and reduces co-channel interference.

The benefits of the 60 GHz IEEE 802.11ad standard imposed several challenges for the designers. Firstly, there are 4 channels specified in the IEEE 802.11ad standard, which are from 57.24 to 59.4 GHz, 59.4 to 61.56 GHz, 61.56 to 63.72 GHz, and 63.72 to 65.66 GHz. This means that to design a IEEE 802.11ad complaint radio system for the global market, the VCO in the system has to have at least 14.4% TR, which is not trivial for any CMOS-based 60 GHz VCO. Secondly, the topologies implemented in lower frequencies are not as easily achievable at 60 GHz. Things such as mismatch and cable length play very crucial role in the design and implementation of any 60 GHz wireless systems. Thirdly, IEEE 802.11ad standard has 2 GHz modulation bandwidth, which is 100 times wider than the modulation bandwidth for IEEE802.11n. This requires major redesign of the radio system as well as the antennas. Third, path losses are significant at 60 GHz. Most existing IEEE 802.11ad compliant systems employ on-die antenna, which makes chip performance evaluation difficult.

Despite those challenges, many world-leading organizations in the telecommunications and semiconductors industries have joined the Wireless Gigabit Alliance and are contributing to the development of IEEE 802.11ad standard. The first IEEE 802.11ad commercial silicon was announced in the 2nd half of 2012. It is anticipated that the
first IEEE 802.11ad compliant product will be commercially available in early 2014.

The goal of the project was to design a VCO that has more than 15% TR around 60 GHz to cover all 4 channels; phase noise lower than 100 dBc/Hz at 10 MHz offset, which is equivalent to the current VCO designed by the industrial partner; and more than 0 dBm output power to drive the following stages in a radio system.

2.2 Review of Selective Feedback VCO Topologies

The VCOs designed in this work are in Colpitts configuration. But before focus on this configuration directly, it is beneficial and important to understand other configurations.

The most frequently used VCO configurations in the selective feedback oscillator class are Colpitts, Clapp, and Hartley types. To help readers distinguish between those closely related configurations, this section compares the pros and cons among those oscillator designs under the selective feedback oscillator class.

Figure 2.1 shows 3 types of oscillator configurations under selective feedback class. Shown in Figure 2.1a is the simplified Colpitts type oscillator. The tank of the Colpitts type oscillator consists of 2 capacitors and an inductor. These 3 elements form a RLC network and select the oscillating frequency of the oscillator. The resistive loss of the 3 elements is countered by the negative resistance generated by the transistor $Q$, forming a feedback loop which maintains the oscillation in the tank. That is the reason why Colpitts oscillators are categorized under selective feedback class. The oscillation in this oscillator circuit is started by noise, and further amplified and sustained by the transistor $Q$, thereby forming an electronic oscillator. To convert a Colpitts oscillator into a VCO, normally the capacitor $C_2$ is replaced by a varactor.
2.2. REVIEW OF SELECTIVE FEEDBACK VCO TOPOLOGIES

Ideally, the other capacitor $C_1$ can be converted into a varactor instead. But in reality this is rarely done, because capacitor $C_1$ is also used to reduce the process variation of the transistor $Q$. This is briefly how Colpitts oscillators operate. The detailed operation and optimization of Colpitts VCOs is explained in 2.3.

Figure 2.1b demonstrates a simplified Clapp type oscillator. Different from a Colpitts oscillator, the single inductor in the tank has been replaced by a series (can be parallel as well) combination of a capacitor and an inductor in the tank of a Clapp oscillator, as also described in 2.3 [7] [8]. To modify it into a VCO, the frequency tuning is done through varying $C_3$ while keep $C_1$ and $C_2$ constant. Clapp configured VCOs offer 2 main advantages. The first is that it can provide more consistent

![Figure 2.1: Simplified oscillator circuits of (a) Colpitts type oscillator, (b) Clapp type oscillator, and (c) Hartley type oscillator](image-url)
2.2. REVIEW OF SELECTIVE FEEDBACK VCO TOPOLOGIES

output power level than Colpitts configuration. Because in a Colpitts oscillator, $C_2$ is often varied for frequency tuning, but doing so will change the voltage division ratio between $C_1$ and $C_2$, and negative resistance, hence varying the oscillation condition across the frequency TR, resulting in fluctuation of output power levels. This problem is avoided in Clapp VCOs since both $C_1$ and $C_2$ are kept constant and only $C_3$ is varied throughout the tuning process, resulting a more consistent output power level. Another advantage is obtained by placing $C_3$ in parallel with $L$, which will reduce the size of $C_3$ to achieve the same oscillating frequency, hence reducing the negative impact of the fixed parasitic capacitance in $C_3$. However, Clapp VCOs have a drawback that their TR is reduced compared to Colpitts VCOs because of the introduction of $C_3$ [9]. This TR reduction is resolved by combining Colpitts and Clapp configurations into one VCO, which is the Colpitts-Clapp VCO configuration that is explained in detail in 2.3.

Figure 2.1c shows a simplified Hartley type oscillator. Different from a Colpitts oscillator, all the L and C components are swapped on Hartley oscillators. Similar to the Clapp configuration, Hartley VCOs offer an attractive benefit that the frequency tuning is done by varying $C$ by employing a varactor, which does not alter the oscillation condition in contrast to varying $C_2$ in a Colpitts VCO. However, the Harley configuration requires to use double the amount of inductors in the tank compared to the Colpitts configuration, and inductors occupy much larger die area than varactors do, hence the Hartley configuration is rarely implemented on ICs.

So far the discussion has been focused on the selective feedback class VCOs, there is another popular oscillator class, the cross-coupled class. Today, cross-coupled VCOs represent by far the most popular VCO topology implemented in CMOS technologies.
2.3. DIFFERENTIAL COLPITTS VCO OPERATION DETAILS AND PERFORMANCE OPTIMIZATIONS

for general applications. Compared to Colpitts VCO designs, cross-coupled VCOs require a lower transconductance to obtain stable oscillations [10] [9]. This translates to a lower DC power consumption required by a typical cross-coupled VCO when compared to a typical Colpitts VCO that oscillates at the identical frequency and is fabricated using the same process. Due to less inductors are needed in a typical cross-coupled VCO design, it often occupies less chip area than a typical Colpitts VCO design. However, in terms of oscillation performance, cross-coupled VCOs suffer from lower output power, higher phase noise, and narrower frequency TR when compared to Colpitts VCOs for a given bias current, which are the main reasons why there is a large amount of Colpitts VCOs in high precision mm-wave applications today [11]. This thesis will focus primarily on the discussion of Colpitts VCOs under the selective feedback oscillator class.

\section*{2.3 Differential Colpitts VCO Operation Details and Performance Optimizations}

This section establishes the detailed understandings of the Colpitts VCO topology used in this VCO design.

In order to understand how a differential Colpitts VCO operates, a good starting point is to look at the single-ended version Colpitts oscillator. The simplified version of a single-ended Colpitts oscillator is shown in Figure 2.2 (bias structures omitted). Starting from the top, \( L_1 \) is an inductive load that has 2 main functions. One is that it separates \( V_{CC} \) from the ac signal at the collector node while not causing significant DC voltage drop (an RF choke). The other is that it is a part of the output network of the Colpitts oscillator (since the output is taken from the collector node), hence \( L_1 \).
is often designed to resonate with the transistor’s intrinsic capacitance $C_{CE}$ ($C_{CS}$) as operating frequency to maximize output power [12]. Below $L_1$ is the collector node of the switching HBT $Q_1$, which is also the output port of the oscillator.

The structure located at the base and emitter nodes of $Q_1$ is the tank of this oscillator. The node $V_B$ is inserted with $Q_1$ bias and it is an AC ground. The inductive portion of the tank is provided by the base inductor $L_B$. The capacitive portion of the tank is obtained by the imaginary part of the input impedance $Z_{in}$ of $Q_1$’s base node. $Z_{in}$ is given by

$$Z_{in} = R_{in} (\omega) + \frac{1}{j\omega C_{in} (\omega)}, \tag{2.1}$$

where $C_{in}$ is the capacitive portion that forms the tank, and $R_{in}$ is the negative resistance generated through the HBT. The value of $L_B$ can be assumed independent of frequency due to its relatively small physical size. Knowing both the inductive and the capacitive components of the tank, the oscillation frequency of this single-ended
Colpitts oscillator can then be formulated the same way as a regular LC resonator

\[
 f_{osc} = \frac{1}{2\pi\sqrt{L_B C_{in}}} .
\]  

(2.2)

\(C_{in}\) consists of all the actual capacitance at \(Q_1\)'s emitter node, plus various intrinsic capacitance of \(Q_1\). It can be formulated as

\[
 C_{in} = \frac{(C_1 + C_{BE}) C_2}{C_1 + C_{BE} + C_2} + (1 + A) C_{BC} ,
\]  

(2.3)

where \(C_{BE}\) is the intrinsic capacitance measured between the base and the emitter nodes of \(Q_1\). \(C_{BC}\) is the intrinsic capacitance measured between the base and collector nodes of \(Q_1\). \(A\) is the inverting gain from the collector to the base node of \(Q_1\) that causes \(C_{BC}\) to be amplified by Miller effect. Because \(C_{BE}\) is sensitive to the process voltage temperature (PVT) variation, a much larger capacitor \(C_1\) is inserted between \(Q_1\)'s base and emitter nodes, so that the capacitance between these 2 nodes can be dominated by the constant \(C_1\). Also, \(C_1\) and the ratio of \(C_1/C_2\) need to be made large to reduce oscillation phase noise, the reason will be discussed later in this section.

In an ideal environment, either \(C_1\) or \(C_2\) can be turned into a varactor to convert the Colpitts oscillator into a VCO. However, in actual implementations, \(C_1\) is placed in parallel with the base-emitter capacitance of \(Q_1\), which can significantly reduce the capacitance variation between the base and the emitter node. Hence, instead of \(C_1\), \(C_2\) is most often implemented as a varactor \(C_{var}\) in Colpitts VCOs. Capacitor \(C_2\) in Figure 2.2 is to imitate the emitter varactor \(C_{var}\) in an actual Colpitts VCO.

Because in (2.3), the term \((C_1 + C_{BE})\) is much larger than \(C_{var}\) (or \(C_2\) in Figure
2.3. DIFFERENTIAL COLPITTS VCO OPERATION DETAILS AND PERFORMANCE OPTIMIZATIONS

2.2), also $C_{var}$ is much larger than $(1 + A) C_{BC}$, (2.3) can be approximated as

$$C_{in} \approx C_{var},$$

(2.4)

and hence if given that $C_{var}$ is a function of its varactor control voltage $V_{tune,C}$, (2.2) can be recast to

$$f_{osc}(V_{tune,C}) = \frac{1}{2\pi \sqrt{L_B C_{var}(V_{tune,C})}}$$

(2.5)

and this how a single-ended Colpitts oscillation can behave as a VCO. The last but not least thing to notice in the simplified circuit is that in (2.5), $f_{osc}(V_{tune,C})$ is controlled via only variable $V_{tune,C}$, which gives the VCO 1 degree of freedom and limits the frequency tuning performance of such a VCO. The VID-based VCOs presented in this work exploited this idea and make $L_B$ in (2.5) also tunable, enabling the VID-based VCOs’ $f_{osc}(V_{tune,C})$ 2 degrees of freedom and hence improved frequency coverage of the VCOs. This can be expressed as

$$f_{osc}(V_{tune,L}, V_{tune,C}) = \frac{1}{2\pi \sqrt{L_B(V_{tune,L}) C_{var}(V_{tune,C})}}.$$  
(2.6)

The operation of VID will be introduced in 2.5, and demonstrated via Colpitts VCO integrations in Chapter 3 and 4.

Also, revealed by (2.5), in order to widen the frequency TR while maintain the same center frequency, $L_B$ should be minimized so that $C_{var}$ can be maximized, hence widen the frequency TR. This is practically desirable, to an extent. This point will become more apparent once the phase noise considerations are introduced later in this section.

The designer must also make sure that the switching transistor $Q_1$ is able to
generate larger negative resistance $R_{in}$ than the total loss of the tank, so that the loop gain of the oscillator remains positive, and the oscillation can be started and maintained throughout the operation period. This is done by setting the appropriate dimensions in conjunction with emitter bias current ($I_E$) for the switching transistor, so that the transistor’s cutoff frequency ($f_t$), maximum oscillation frequency ($f_{max}$), and minimum noise figure ($NF_{min}$) can be optimized according to the application and condition. Once the transistor’s dimensions are set, the term $f_t$ refers to the upper frequency limit for the transistor to produce current gain, the term $f_{max}$ refers to the upper frequency limit for the transistor to produce power gain. Together these 2 parameters provide gain to maintain oscillation in the tank. In general, both $f_t$ and $f_{max}$ are positively proportional to $I_E$ up to a point (the peak), then they become negatively proportional, which should be avoided in VCO design. The term $NF_{min}$ refers to that at one particular frequency (can be the center frequency of the VCO), the minimum noise figure can be theoretically reached with respect to an appropriate $I_E$ level. In general, $NF_{min}$ reduces as $I_E$ increases (desirable) up to a point then this relation is inverted (undesirable). Therefore, these 3 parameters must be optimized according to the specific requirement and much attention must be paid when designing the appropriate switching transistor for a VCO.

Modified on Leeson’s formula [13], the phase noise of an oscillator can be approximated as

$$S_{\Delta out} = 2 \frac{|I_n|^2}{|V_{tank,pp}|^2} \frac{1}{(C_1 + C_{BE})^2 \left(\frac{C_1 + C_{BE}}{C_{var}} + 1 \right)} \frac{1}{\Delta \omega^2},$$

(2.7)

where $V_{tank,pp}$ is the peak-to-peak voltage swing in the tank of the VCO, $I_n$ is the sum of all noise current originated from the switching HBTs, and $\Delta \omega$ is the offset frequency.
Equation (2.7) reveals that, in order to reduce phase noise, both $C_1$ itself and the ratio of $C_1/C_{var}$ need to be as large as possible. Now recall as aforementioned, in order to widen TR, $C_{var}$ should be maximized, which is contradictory the high $C_1/C_{var}$ ratio required to obtain better phase noise performance. This is clearly a trade-off between phase noise performance and TR of all LC-based VCOs.

Also, (2.7) says that a high tank voltage swing represented by $V_{tank}$ is required as well to obtain low phase noise performance. However, having large tank voltage swing at the base node will increase power consumption of a Colpitts oscillator. This trade-off between phase noise performance and power consumption can be understood in the following ways. Firstly, larger transistor size must be used to allow high base voltage swing, while the larger the transistors are, the higher collector (drain) current they need to draw, hence directly increase the oscillator’s DC power consumption. Secondly, higher tank voltage swing also requires higher $V_{CC}$. This requirement can be understood through this equation (for one time instance):

$$\left(V_{CC} - v_{C,peak}\right) - \left(V_B - V_{BE} - v_{B,peak}\right) > V_{CE,sat} \tag{2.8}$$

for which a Colpitts oscillator has to satisfy this voltage requirement at the collector (drain) and the emitter (source) nodes of the switching transistor to produce desired oscillation. In this equation, $v_{b,peak}$ is the peak amplitude of the base voltage swing, $v_{c,peak}$ is the peak amplitude of the collector voltage swing, $V_{CE}$ is the collector-emitter saturation voltage of $Q_1$. $v_{b,peak}$ and $v_{c,peak}$ carry opposite signs because there is a 180° phase difference between the collector and the emitter nodes. Equation (2.8)
can be rearranged as the following

\[ V_{CC} - V_B + V_{BE} - V_{CE,\text{sat}} > v_{B,\text{max}} + v_{C,\text{max}} \]

which clearly states that \( V_{CC} \) is positively proportional to \( v_{b,\text{peak}} \). Hence a high \( V_{CC} \) is needed given a high tank voltage oscillation, which lead to increasing DC power consumption.

With a solid understanding on the single-ended version, the operation of a differential Colpitts VCO is straightforward to analyze. Figure 2.3 demonstrates a typical differentially configured Colpitts VCO. The differential varactor pair \( C_{\text{var}} \) is connected between the emitter nodes of the transistor pair. Their capacitances change simultaneously as the control voltage \( V_{\text{tune}} \) changes. The emitter inductor pair \( L_2 \) is new in the differential configuration. There are 2 main functions they perform in a Colpitts VCO. Firstly, they decoupled the signals at the emitter nodes of the 2 transistors, hence allowing the implementation of the common tail current source at the bottom of the circuit. Secondly, they are designed reduce noise of the 2nd order harmonic content at the common-node by satisfying this condition:

\[ f_{osc} > \frac{1}{2\pi \sqrt{L_2 C_{\text{var}}}} \]

The differential structure rejects common-mode noise originating from the voltage biases (supply pushing), the control line \( (V_{\text{tune}}) \), and tail current source. It can produce larger base voltage swing (reduces phase noise as mentioned earlier). Also,
implementing differential structure enables the designer to obtain second order harmonic signals from the VCO (traditionally called push-push signal), making silicon-base VCOs generate oscillations well beyond 300 GHz [11]. Those are very beneficial factors to VCO performance. Therefore, most VCOs today are implemented in differential configuration.

Based on Colpitts VCOs, the Colpitts-Clapp topology was proposed in recent years as a hybrid structure between Colpitts and Clapp VCO configurations [14]. A typical differential Colpitts-Clapp VCO is demonstrated in Figure 2.4. There are 2 frequency tuning elements in this VCO, which can be identified by the extra tuning elements ($C_{var}$) located at the base node of the switching transistor in addition to
the varactors ($C_{\text{tune}}$) at the emitter node in Colpitts VCOs. Controlled via $V_{\text{tune1}}$, those extra varactors $C_{\text{var}}$ at the base node provide an extra degree of freedom for frequency tuning in addition to $C_{\text{tune}}$, hence Colpitts-Clapp VCOs are capable of precise operations at a wider frequency TR compared to Colpitts VCOs. One popular frequency tuning design for Colpitts-Clapp VCOs is that, the varactors at the emitter node of the switching transistor are fed with digital signals and are in charge of coarse frequency tuning (i.e. band switching), and the varactors at the base node is fed with analog signals and are in charge of fine frequency tuning (i.e. in-band adjustment). In this way a Colpitts-Clapp VCO can cover a wide frequency TR without increasing the VCO gain, $k_{\text{VCO}}$, which reduces phase noise and improves the locking performance of the PLL where the Colpitts-Clapp VCO is going to be embedded. Also, because the base varactors are connected to the base node of the switching transistors that is biased close to $V_{\text{CC}}/2$ for maximum base voltage swing, the control voltage across the varactors are maximized to from $-V_{\text{CC}}/2$ to $+V_{\text{CC}}/2$, which is very beneficial for integrating into charge pump equipped PLLs [9].

2.4 Varactor Bank Operations and Q-Factor Optimizations

The operation of the varactor bank in the emitter node and the ways to optimize the varactor Q-factor will be introduced in this section.

As implemented in Figure 2.3 and 2.4, varactors play very important roles to determine performance of a VCO. In a modern wireless communication system, Colpitts-Clapp topology is often employed for it is capable of both fine and course frequency tunings. Normally, the fine tuning part is to continuously vary the oscillation frequency by controlling base varactors through analog control voltages, while the coarse
tuning is finished by digitally send high or low voltages to different varactors in the bank in the emitter node to switch oscillation frequency in finite steps (a.k.a band switching).

For demonstration purpose, there is only 1 pair of differential varactors connected to the emitter node of the switching HBT in the above VCO schematics. In an actual VCO, there could be numerous of them. For simplicity, a single-sided varactor bank will be used to demonstrate how it operates. Shown in Figure 2.5 is a typical varactor bank implemented in the emitter node of a Colpitts (or Colpitts-Clapp) VCO. Assuming the varactors are all accumulation-mode MOSFET (AMOS) based,
for the 3 varactors in the bank, \( C_{\text{bit0}} \) has the largest capacitance so it weights as the most significant bit (MSB), \( C_{\text{bit1}} \) has medium capacitance, and \( C_{\text{bit2}} \) has the smallest capacitance so it weights as the least significant bit (LSB). The 3 DC voltage sources right to the varactors are digital control lines which control the terminal voltages of the varactors. For example, when \( V_{\text{bit0}} \) is at 0 V (low), \( C_{\text{bit0}} \) is in accumulation mode, the input capacitance is high and this is referred to as on-state, when \( V_{\text{bit0}} \) is at 1.5 V (high), \( C_{\text{bit0}} \) is in depletion mode, the input capacitance is low and this is referred to as off-state. In an attempt to evenly distribute the frequency bands, \( C_{\text{bit0}}, C_{\text{bit1}}, \) and \( C_{\text{bit2}} \) are often binary weighted, forming \( 2^3 = 8 \) equally spaced frequency bands. For example, if \( C_{\text{bit0}} \)'s on-capacitance is \( a=200 \) fF, then \( C_{\text{bit1}} \) and \( C_{\text{bit2}} \)'s on-capacitances will be \( b=100 \) fF and \( c=50 \) fF respectively. Varactors are normally biased to have a least half of their on-capacitance when they are at off state, so ideally \( C_{\text{bit0}}, C_{\text{bit0}}, \) and \( C_{\text{bit0}} \)'s off-capacitances are \( A=100 \) fF, \( B=50 \) fF, and \( C=25 \) fF. As demonstrated by Table 2.1, when the digital control counts from state 000 to 111, each of the 3 varactors switches between accumulation and depletion modes and enables the total input capacitance \( C_{\text{var}} \) to gradually vary from 350 fF to 175 fF at a step of 25 fF. Therefore the output frequency of the VCO is changed accordingly. This is how a varactor bank switches between different frequency bands in a VCO. Also keep in mind that, although \( C_{\text{var}} \) changes with a constant step size, the spacing between different frequency bands that the VCO operates on will not necessarily be equal. This is due to the inverted square root relationship between \( f_{\text{osc}} \) and \( C_{\text{var}} \) as shown in (2.5). This point will become clearer in later chapters.

In order to achieve minimal phase noise, the quality factor \( Q \) of the oscillation tank on a VCO must be maximized. The varactor is an important component in the
tank of a VCO, hence optimizing its Q-factor is crucial to reduce the phase noise of a VCO.

Because varactors implemented on VCOs are usually based on AMOS, a varactor’s Q-factor is determined by the gate, channel, source-access, and drain-access resistances [12]. According to [15], the gate resistances of multi-finger MOSFETs with single or double-sided contacts are given respectively by

$$R_G = \frac{R_{cont}}{N_f} + \frac{R_{G-SQ}}{L_{phys}} \left[ W_{ext} + \frac{W_f}{3} \right]$$  \hspace{1cm} (2.11)
In these 2 equations, $R_{cont}$ is the contact resistance, $N_{cont}$ is the number of the contacts per gate finger, $R_{G-SQ}$ is the gate poly sheet resistance per square, $L_{phys}$ is the physical channel length, $W_{ext}$ is the gate extension beyond the active region, $W_f$ is the finger width, and $N_f$ is the number of parallel connected gate fingers. By comparing these two equations, it is clear that varactors with double-sided gate contacts have lower gate resistance. Furthermore, in order to obtain lower $R_G$, $W_f$ should be minimized and $N_f$ should be maximized within the technology allowance. However, because the product of $W_f$ and $N_f$ represents the total gate width, which determines the off-capacitance of a varactor (i.e. when gate voltage is 0 V), reducing $W_f$ and increasing $N_f$ should be kept in a constant ratio so that their product remains constant. This point is more obvious in reducing the channel resistance of a varactor, which is given as

$$R_{ch} = \frac{R_{CH-SQ}}{12} \frac{L_{phys}}{W_f N_f},$$

where $R_{CH-SQ}$ is the sheet resistance of the channel material. From this equation, the practical way of reducing channel resistance is by choosing the minimum channel (gate) length ($L_{phys}$) provided by the certain technology, rather than increasing $N_f$ and $W_f$ together during the design process, otherwise the characteristics of the varactor will change. The source-access and drain-access resistances can be minimized by implementing parallel gate fingers.
2.5 Variable Inductor Operation and Integration on VCO

Similar to varactors, which have the ability to vary its capacitance with respect to control voltage, variable inductor (VID) can be treated as a dual to varactor that it changes its inductance with respect to given control voltages. Recent works have reported VID-based VCOs with high TR up to 16.07% [2] [16]. Figure 2.6 illustrates the VID topology used in this design. The circuit contains a transformer, a variable resistor $R_v$, and the parasitic capacitance $C_v$ from $R_v$. $L_p$ and $L_s$ are the primary and secondary winding inductances of the transformer respectively, and the transformer has coupling coefficient $k$. As derived in [16], looking into the VID from the primary winding, the VID can be modeled as a variable inductor $L_{eq}$ in parallel with a variable
resistor $R_{eq}$ as

$$L_{eq}(R_v, \omega) = \frac{R_v^2 L_p [1 - \omega^2 C_v L_s (1 - k^2)]^2 + \omega^2 L_p L_s^2 (1 - k^2)^2}{R_v^2 (1 - \omega^2 C_v L_s) [1 - \omega^2 C_v L_s (1 - k^2)] + \omega^2 L_s^2 (1 - k^2)}$$  \hspace{1cm} (2.14)$$

and

$$R_{eq}(R_v, \omega) = \frac{R_v^2 L_p [1 - \omega^2 C_v L_s (1 - k^2)]^2 + \omega^2 L_p L_s^2 (1 - k^2)^2}{R_v k^2 L_s}.$$  \hspace{1cm} (2.15)$$

For the equivalent inductance $L_{eq}$, when variable $R_v$ is small, (2.14) can be approximated as

$$L_{eq}(0, \omega) = L_p \left(1 - k^2\right).$$  \hspace{1cm} (2.16)$$

Similarly, when variable $R_v$ is large, (2.14) can be approximated as

$$L_{eq}(\infty, \omega) = L_p \left(1 + \frac{\omega^2 L_s C_v}{1 - \omega^2 L_s C_v} k^2\right).$$  \hspace{1cm} (2.17)$$

Interestingly, by comparing (2.16) with (2.17), it is obvious that $L_{eq}(\infty, \omega)$ depends on the parasitic capacitance $C_v$ while $L_{eq}(0, \omega)$ does not. This is the major advantage of implementing a VID in a VCO: the ability to vary $L_{eq}$ without being affected by the parasitic capacitance ($C_v$) of the tuning element as long as $R_v$ is kept low. Knowing the maximum and minimum values of $L_{eq}$, the inductance tuning ratio can then be formulated as

$$\alpha \equiv \frac{[L_{eq}(\infty, \omega) - L_{eq}(L_0, \omega)]}{L_{eq}(\infty, \omega)} = \frac{k^2}{1 - \omega^2 C_v L_s (1 - k^2)} > k^2.$$  \hspace{1cm} (2.18)$$

It is important to note that, (2.16) to (2.18) will only be valid if the self-resonant frequency formed by parallel $L_s$ and $C_v$ is higher than the operating frequency $\omega$ in those equations. In this case the condition $\omega^2 C_v L_s < 1$ holds and hence $L_{eq}$
monotonically increases with $R_v$. On the other hand, if the self-resonant frequency given by $L_s$ and $C_v$ is lower than the operating frequency $\omega$, the monotonicity between $L_{eq}$ and $R_v$ may be lost, $\omega^2C_vL_s > 1$ holds, which can lead to false lock of a PLL [16]. Therefore, in order to integrate VID topology in VCO design, it is important to design the VID with self-resonance frequency beyond the operating frequency of the VCO. Using Figure 2.6 as an example, setting $L_p = L_s = 500 \, \text{pH}$, $k = 0.4$, varying $R_v$ from 0 to 800 $\, \Omega$ and $C_v$ from 0 fF to 30 fF, (2.14) will produce Figure 2.8. This figure clearly shows that while $L_{eq}$ monotonically increases with variable $R_v$, $L_{eq}$ is independent to $C_v$ when $R_v$ is small, and dependent to $C_v$ when $R_v$ is large. Also notice that the inductance tuning ratio is always no less than $k^2 = 0.16$ entirely in this plot as predicted by (2.18).

Figure 2.8: Sample $L_{eq}$ vs $R_v$ simulated at 30 GHz

From Figure 2.8, it can be observed that there exists a linear range where $L_{eq}$
2.5. VARIABLE INDUCTOR OPERATION AND INTEGRATION ON VCO

increases almost linearly with $R_v$ regardless of $C_v$ values. In this case the linear range is from $R_v = 0 \, \Omega$ to about 110 $\Omega$ in the figure. The $R_v$ linear range representation $R_{lin}$ can be derived from (2.15) as

$$R_{lin} = \sqrt{\omega^2 L_s^2 (1 - k^2) (6k^2 - 1)},$$  \hspace{1cm} (2.19)$$

which can further produce the linear range of the tunable inductance, $L_{eq,lin}$, from (2.14)

$$L_{eq,lin} (R_v, \omega) = L_1 \left[ R_v \frac{\sqrt{6k^2 - 1}}{6\sqrt{\omega^2 L_s^2 (1 - k^2)}} + (1 - k^2) \right],$$  \hspace{1cm} (2.20)$$

which is also independent of $C_v$.

Another important parameter of VIDs is Q-factor. Its detailed derivation is shown in Appendix A, the final Q-factor representation can be written as the following:

$$Q_{eq} = \frac{R_v^2 R_p (1 - \omega^2 C_v L_s) + \omega^2 L_p L_s^2 (1 - k^2) + \omega^2 k^2 R_v^2 C_v L_p L_s (1 - \omega^2 L_2 C_v)}{R_p R_v (1 - \omega^2 C_v L_s)^2 + \omega^2 L_s (k^2 L_p R_v - R_1 L_s)},$$  \hspace{1cm} (2.21)$$

where $R_p$ is the parasitic resistance found on the primary winding of the transformer. Using the same example setup as in Figure 2.8 with this equation to plot the Q-factors given by different $C_v$ values, the results are shown in Figure 2.9. Notice that in general the Q-factor plot shows a kind of “U” shape. This is reasonable because when $R_v$ is either nearly short or open, the total resistive loss of the transformer is minimized, hence the Q value will be high, which happens at the two ends of the TR.

At this point it will be beneficial to summarize the pros and cons of this VID design. For the benefits, the most important aspect is that this VID is capable of operating independently of the parasitic capacitance as long as the variable $R_v$ is
2.5. VARIABLE INDUCTOR OPERATION AND INTEGRATION ON VCO

controlled within the $R_{lin}$ range as shown in (2.14) - (2.20). This is a very significant attribute of the VID because it can potentially widen the TR of a VCO without taking the damage from increased parasitic capacitance in the tank. Another benefit is that by employing a VID in the base node, it replaces the differential varactors in parallel with the differential inductors in the base node, which can reduce the complexity of the VCO (especially on reducing the amount of active components), hence making the simulation more straight forward and accurate. For the drawbacks, on the other hand, as shown in Figure 2.9, the Q of the VID can be lower than a state-of-the-art inductor or varactor, which in turn may impact the phase noise level of the VCO. For instance, the varactors used in this design has minimum Q of around 10, but the VID has minimum Q of 4. This low Q causes performance degradation to the VCO with VID. This point will be elaborated in detail in the following chapters. Another
drawback is although 1 VID will replace numerous inductors and varactors in the
 tank making the simulation more straight forward, a VID can still occupy larger die
 area. As discussed above, in order to desensitize the VCO, the rate of change of \( L_{eq} \)
 with respect to \( V_{tune} \) ought to be low. This is achieved by designing the transformer
 with a low coupling coefficient \( k \), which requires the primary windings to be more
 apart from the secondary windings, and ultimately increases the footprint of the VID.

In a typical IC integrated VID circuit, the transformer is implemented using an
 integrated spiral stack-up transformer, and the variable resistor is implemented with
 operating 1 or more MOSFETs in triode region. There are many parameters from this
 transformer and MOSFET combination that can be changed to significantly alter the
 characteristics of the VID. Dealing with this amount of parameters simultaneously can
 be daunting at first, however up till the moment this thesis was written (late 2013), the
 concept of VID still quite new, and there is no written design methodology available
 for designer to review. Here the thesis author presents his method, contributing as
 a starting point and reference for the future investment and improvement on VID
 designs:

1. Using (2.6) to roughly estimate the required tank inductance variation in order
   to achieve desired in-band TR. The approximate nominal value for the varactor
   bank can be used for quick hand calculations.

2. Once obtained the desired tank inductance TR, use electronic design automation
   (EDA) tools to perform EM simulations to obtain the desired dimensions and
   geometries of the primary and secondary windings, so that the inductances of
   the 2 windings are close to the mid-point of the inductive TR. Also ensure that
   the Q-factor for each winding is maximized.
3. As described by (2.18), a lower coupling coefficient \((k)\) between the 2 windings of the transformer can reduce the rate of change of the equivalent inductance of the VID, hence reducing the VCO gain \((k_{VCO})\) and helping to reduce the phase noise level of the VCO. Therefore the transformer should be adjusted by changing the gap between the 2 windings.

4. Extract and simulate the transformer model with an ideal capacitor and resistor to obtain the required linear resistance variation range \((R_{lin}\) in (2.19)) and the capacitance levels.

5. Determining the MOSFET dimensions to fill the desired \(R_{lin}\) range within a certain gate voltage range, which is equivalent to \(V_{tune}\) and can be provided by the charge pump of the PLL. Note that as the gate voltage of the MOSFET changes, the resistance and capacitance between the source and the drain change significantly. On-resistance and off-capacitance are hardly defined in this case. Hence the MOSFET in a VID cannot be treated simply as a switch. Rather, the goal here is to find a set of MOSFET dimensions that provide the desire \(R_{lin}\) variation within a specified \(V_{tune}\) range. On the other hand, as long as the MOSFET is operated within the \(R_{lin}\) range, its terminal capacitance \(C_{ds}\) is not a primary concern.

6. Iterate until the desire VID characteristics are achieved.
2.6 Frequency Doubler Operation

Just like every other circuit in mm-wave regime, tradeoffs have to be managed throughout the design of VCOs. Oscillation frequency is arguably the most counteractive one among all those tradeoffs. It counteracts almost all other parameters of a VCO and degrades them as the frequency goes up. Hence reducing the VCO’s burden by reducing its oscillation frequency, and then multiplying the output signal by a relatively simpler circuit may provide attractive advantages [3] [11]. For the case of frequency doublers, the incorporation of frequency doubler with VCO provides the following benefits to the entire system:

1. It relaxes the VCO specification to allow it operate at half of the required frequency, which in turn avoids the performance degradation of components in the VCO, varactors in particular.

2. It reduces the PLL power consumption by eliminating or reducing the number of current mode logic (CML) frequency dividers.

3. It reduces the load pulling effect on the VCO. The frequency multiplier stage will convert the loading effects into at most changes in amplitude for the VCO.

4. Because the VCO operates at lower frequencies, the active components are further away from their $f_T$’s and $f_{max}$’s, hence the gain is higher, which translate to higher VCO efficiency.

The simplified version of the frequency doubler topology employed in this design is shown in Figure 2.10. Assuming the differential signals to the input of the frequency doubler are perfect single-tone sinusoidal waves, in short the operation principle of
this frequency doubler is based on the following steps. First, the transistor pair \( Q_1 \) and \( Q_2 \) are driven into non-linear region, meaning that they only conduct current at certain times (conduction angle \(< 360^\circ\) ). Second, the input differential signals at the base (gate) nodes of \( Q_1 \) and \( Q_2 \) are translated to differential current swings at the collector (drain) nodes. Due to the nonlinearity of the transistor pair, harmonics are introduced to the differential current at the collector nodes. The differential currents with harmonic contents from the two half-circuits of this circuit are combined at the common node of the collector nodes of \( Q_1 \) and \( Q_2 \). All odd harmonics cancel out and all even harmonics add up. Third, the inductor placed at the common collector node has a specific resonant frequency, which will present maximum impedance to the common collector node. This resonant frequency is selected to be the second harmonic frequency of the input differential signals. Therefore, the second harmonic voltage swing at the common collector node (the output node of this frequency doubler) dominants other even harmonics because of the maximum impedance it sees.
In order to understand in detail and optimize the design of a frequency doubler, the collector current is a good starting point. The collector current expression can be expanded using Fourier series as

\[ I_c(t) = I_0 + I_1 \cos(\omega t) + I_2 \cos(2\omega t) + \cdots + I_n \cos(n\omega t). \] (2.22)

In this series, as derived in [17], the \( n \)th harmonic current amplitude \( I_n \) can be written as

\[ I_n = I_{MAX} \frac{4t_0}{\pi T} \left| \frac{\cos \left( n\frac{t_0}{T} \right)}{1 - \left( 2n \frac{t_0}{T} \right)^2} \right|, \] (2.23)

where \( I_{MAX} \) is the peak current at the collector node, the term \( \frac{t_0}{T} \) represents the conduction angle of the transistors, and \( T \) is the period of the fundamental signal. In order to preserve conversion gain and efficiency in transistor multiplication, \( I_{MAX} \) should be set with respect to the transistor size so that the current density at the collector node is less than the peak \( f_T \) current density of the transistor, \( J_{PfT} \). The conduction angle also needs to be chosen carefully, as it affects the DC-to-RF efficiency.

From (2.22), the DC current amplitude \( I_0 \) (the 0th harmonic content) at the collector node (the common node) can be expressed as

\[ I_0 = 2I_{MAX} \frac{2t_0}{\pi T}, \] (2.24)

and the second harmonic current amplitude \( I_2 \) is

\[ I_2 = 2I_{MAX} \frac{4t_0}{\pi T} \left| \frac{\cos \left( 2\frac{t_0}{T} \right)}{1 - \left( 4 \frac{t_0}{T} \right)^2} \right|. \] (2.25)
2.7. DEFINITIONS OF FIGURE OF MERIT FOR VCOS

Notice that both (2.24) and (2.25) are obtained by summing up the currents from the 2 half circuits, therefore they are multiplied by a factor of 2.

After understanding the current perspective of the frequency doubler, the frequency doubler can be further refined to produce maximum DC-to-RF efficiency. The output power of the frequency multiplier is determined by

\[ P_L = \frac{V_2 I_2}{2}, \]  

(2.26)

where \( V_2 \) is the output voltage amplitude at the collector node as in Figure 2.10.

The optimum large signal load resistance can then be determined as

\[ R_{L, opt} = \frac{V_2}{I_2} \]  

(2.27)

Finally, the DC-to-RF efficiency of this frequency doubler is expressed as

\[ \eta_{DC} = \frac{P_L}{P_{DC}} \leq \frac{I_n}{2I_0} = \frac{\cos (\pi n t_0 T)}{1 - (2n t_0 T)^2}. \]  

(2.28)

2.7 Definitions of Figure of Merit for VCOs

Every VCO has a handful of important parameters, such \( f_{osc}, \) TR, phase noise, \( P_{DC}, \) \( P_{out}, k_{VCO}, \) etc. There should be a way to cross-compare different VCOs with different VCO parameters and designs topologies. Different VCO figures of merit (FOMs) are defined for this purpose just like for LNAs and PAs.

One popular basic FOM used in academia and industry is defined as the following [18].

\[ FOM = L(\Delta f) - 20 \log(\frac{f_{osc}}{\Delta f}) + 10 \log(\frac{P_{DC}}{1 \text{mW}}). \]  

(2.29)
Inside this formula, $\Delta f$ is the offset frequency with respect to the carrier frequency, and $L(\Delta f)$ is the phase noise obtained at a specific offset frequency. Also notice that $P_{DC}$ in this FOM equation is in linear unit (mW) not logarithmic. This FOM serves only as a general judgment of the level of performance of a VCO, as it does not include the consideration of TR nor output power.

A more comprehensive FOM formula is given below, in which the consideration of TR is included into the calculation of FOM. It is named $FOM_T$ [18].

$$FOM_T = L(\Delta f) - 20 \log\left(\frac{f_{osc}}{\Delta f}\right) + 10 \log\left(\frac{P_{DC}}{1 \text{mW}}\right) - 20 \log\left(\frac{TR}{10\%}\right).$$ \hspace{1cm} (2.30)

$FOM_T$ is used in comparisons where the TRs of the VCOs are prioritized.

A more comprehensive FOM formula that considers both TR and output power of a VCO is given below. It is called $FOM_{TP}$ [19].

$$FOM_{TP} = L(\Delta f) - 20 \log\left(\frac{f_{osc}}{\Delta f}\right) + 10 \log\left(\frac{P_{DC}}{1 \text{mW}}\right) - 20 \log\left(\frac{TR}{10\%}\right) - 10 \log\left(\frac{P_{out}}{1 \text{mW}}\right),$$ \hspace{1cm} (2.31)

where the output power $P_{out}$ is in unit of mW. $FOM_{TP}$ is used in comparisons where TRs and output powers of the VCOs are prioritized more over other parameters.

In all cases, the smaller the FOM value is, the higher level of performance the VCO has. Typical FOM values for CMOS-based VCOs are from -160 to -190 dBc/Hz. These FOMs will be used to compare VCO performance in the following chapters in this thesis.
2.8 Selected Literature Review of VCO Design Topologies

A state-of-the-art cross-coupled 64 GHz VCO was presented by Lianming Li, et al. [5]. This VCO was designed to reduce DC power consumption and phase noise in a typical cross-coupled VCO by introducing capacitance splitting and gate-drain impedance balance techniques. Both techniques were accomplished by inserting decoupling inductors between the base and drain nodes of the transistor pair. The schematic of this VCO is shown in Figure 2.11. In short, capacitance splitting requires to insert an inductive component between the gate of one transistor and the drain of the other transistor, so that the parasitic capacitances of the transistor pair are split and the $g_m$ generation efficiency of the transistors can be improved. With this higher $g_m$ efficiency, the size of the transistors can be scaled down, which leads to lower DC power consumption. On the other hand, this gate-drain impedance balance technique specifies the value of the inserted inductor. The inserted inductor was treated as an impedance transforming block between the gate node (the input) and the drain node (the output). By changing the impedance transforming coefficient (i.e. the inductance), one has obtained the freedom to set the transistor total parallel resistance (also reduced from being able to scale down the transistor size) and the parallel resistance of the transistor terminal impedance to optimize the tank Q-factor, hence returning a better phase noise performance as well. As the result, this cross-coupled VCO managed to obtain 8.75% TR and a phase noise of -95 dBc/Hz at 1 MHz offset. This VCO consumes a remarkably low 3.16 mW DC power with 0.6 V DC supply, and its output power is -14 dBm.

However, there is one important thing to notice in the design of this VCO. As shown in Figure 2.11, this VCO has 8.75% TR yet it features a single frequency
tuning component, the varactor pair at the drain node. This means that all its frequency variation is covered in 1 single tuning band, which can lead to a high $k_{VCO}$. A high $k_{VCO}$ will increase phase noise of the VCO and imposes difficulties to the corresponding phase-lock loop (PLL) design, hence expanding a single tuning band across a wide frequency range is usually avoided. Instead, multiple tuning bands can be used to remedy this situation.

Figure 2.13 shows the first fully integrated differential Colpitts VCO reported
by Leonard Dauphinee, et al. in 1997 [20]. This VCO was fabricated using 0.8µm BiCMOS technology. It operates at 1.5 GHz and features a differential Colpitts structure with integrated LC resonators. Compared to conventional cross-coupled VCOs of the same era, the advantages of this differential Colpitts VCO are listed as following:

1. The impact of the base-emitter capacitance to the oscillation frequency is minimized by placing the varactors in series with the base-emitter capacitance of the transistor.

2. The load capacitance effect on the oscillation frequency (which alters it) is isolated by placing the inductor-varactor tank at the base and emitter nodes of the transistors, while the output is tapped at the collector node.

3. The TR is enlarged because the ac ground at the varactor common node is located at the emitter node of the transistors, which does not appear in parallel to any transistor intrinsic capacitance.

Figure 2.13: The first fully integrated differential Colpitts VCO presented in [20]
2.8. SELECTED LITERATURE REVIEW OF VCO DESIGN TOPOLOGIES

Dauphinee’s VCO reported to have 10% TR, a phase noise of -105 dBc/Hz at 100 kHz offset, which was the lowest phase noise for fully integrated VCOs that operate in the 1 to 2 GHz range at that time. The VCO operates on 3.6 V DC supply, consumes 40 mW DC power, and its output power was reported at 6.6 dBm into a 100 Ω differential load.

As a much more recent example (published in January 2013), Giuseppina Sapone, et al. reported a differential Colpitts VCO design for W-band (75 – 110 GHz) [21]. This VCO shares the same configuration of traditional differential Colpitts VCOs with its novelty that its RF output is magnetically coupled to the output buffer through an integrated transformer. This VCO operates at 74 GHz center frequency and it was implemented using 130 nm SiGe BiCMOS technology. The schematic of this VCO is shown in Figure 2.14. The primary winding of the transformer behaves as the base node inductors in the LC tank as seen in Figure 2.13. The oscillation signal is then magnetically coupled onto the secondary winding of the transformer, which is the output node of the VCO, contrasts to the traditional differential Colpitts VCO where the output is taken at the collector node of the switching transistors (as seen in Figure 2.13). A very high output decoupling was also achieved with the implementation of the transformer at the base node. Moreover, the transformer is capable of increasing the output voltage swing as well as eliminating the effect of $C_{bc}$ by Miller Effect. In terms of the performance, this VCO has 4.86% TR and phase noise of -99.3 dBc/Hz at 1 MHz offset. This VCO operates on 2.5 V DC supply, consumes 65 mW DC power, and its output is measured at 2 dBm with the buffer.

The actual die photograph of the VCO is shown in Figure 2.15. One last thing to notice from this VCO, just like the cross-coupled VCO in Figure 2.11, this Colpitts
2.8. SELECTED LITERATURE REVIEW OF VCO DESIGN TOPOLOGIES

Figure 2.14: A differential Colpitts VCO operates at 74 GHz implemented using 0.13 µm SiGe BiCMOS technology [21].

VCO also has only one frequency tuning component, namely the varactor pair at the emitter node.

A 60 GHz VID-based cross-coupled VCO was demonstrated by T. Y. Lu, et al. [16] recently. This VCO is fabricated using 90 nm CMOS process and the schematic of this VCO is shown in Figure 2.16. Located in the drain node, the VID in this cross-coupled VCO contains 7 nMOSFETs connected in parallel, in which $M_f$ fine tunes the oscillating frequency with analog control signals $V_{fine}$, and $M_{c1}$ to $M_{c6}$ are binary weighted nMOSFETs that coarse tune the oscillating frequency with digital control signals $V_{b1}$ to $V_{b6}$ correspondingly. The reason to connect multiple transistors to the secondary winding of the transformer in the VID is to exploit the greatest benefit of this VID design. As stated by (2.16) in 2.5, that as long as the equivalent resistance created by the transistor(s) is kept small enough, the inductive variation generated...
by the VID is independent of the parasitic capacitance of the transistor(S). Overall, this VID-based cross-coupled VCO can be tuned from 52.2 to 61.3 GHz, which is 16% TR, it recorded lowest phase noise of -118.75 dBc/Hz at 10 MHz offset and 8.8 mW of power consumption. However, this VID-based cross-coupled VCO design has a major drawback. As shown in Figure 2.17, in the most part of tuning range, the phase noise (at 10 MHz) of this VCO increases rapidly beyond -100 dBc/Hz for the multi-band operation and above -75 dBc/Hz for the single-band operation, which devastates its applications. This high phase noise level can be attributed to 2 main reasons. One is that because the VID is the only frequency tuning element of this cross-coupled VCO, the Q variation of the VID dominants the phase noise performance of this VCO. As shown in Figure 2.9 that the Q factor of this VID design will drop around the middle of its $L_{eq}$ variation range. Therefore the phase noise level of this VCO
Figure 2.16: The schematic of the VID-based cross-coupled VCO proposed in [16] is significantly risen by the Q drop of the VID. Another reason is that unlike in a Colpitts VCO design, where the frequency tuning elements are placed in the gate (base) or source (emitter) nodes, the VID of this VCO is placed in the drain node of the switching transistors, there is no isolation between this only frequency tuning element and the external load. This lack of isolation will couple external noise onto the gate node voltage swing, and alter the input impedance of the VID looking from the drain node of the switching transistors. This phase noise degradation can be mitigated by adopting the VID structure in the gate (base) node of a Colpitts VCO, which is demonstrated in the following chapters.

As a summary, Table 2.2 lists and compares the performance of the state-of-the-art VCOs reviewed in this section.
2.8. SELECTED LITERATURE REVIEW OF VCO DESIGN TOPOLOGIES

Figure 2.17: The measured phase noise performance of the VID-based cross-coupled VCO proposed in [16]

Table 2.2: Comparison of the state-of-the-art VCOs reviewed in this section

<table>
<thead>
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<th>Reference</th>
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<th>[16]</th>
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<td>90 nm CMOS</td>
<td>130 nm SiGe BiCMOS</td>
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<td>VID-based cross-coupled</td>
<td>Diff. Colpitts</td>
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<td>-174.3</td>
</tr>
</tbody>
</table>

*aExclude output buffer if presented*
Chapter 3

The Design of 30 GHz VID-Based Differential Colpitts VCO

Although the focus of this work is on the IEEE 802.11ad applications at around 60 GHz, as discussed in 2.6 it can be beneficial to operate the VCO at fundamental frequencies slower than 60 GHz. In this case, the combination of a 30 GHz VCO with a frequency doubler was designed and evaluated. This chapter explains the design details of the 30 GHz VID-based differential Colpitts VCO. The simulation and measurement results were used to verify and evaluate this 30 GHz VCO design are also included in this chapter.
3.1 VCO Design Details

Due to Colpitts topology’s abilities to provide more stable oscillation, wider TR, and higher output power in mm-wave applications as discussed in 2.8, it was chosen as the VCO design topology for this work over the cross-coupled topology. Also, this 30 GHz VID equipped VCO was implemented in differential configuration to suppress the common-mode noise, reduce the effect of control line pushing, and enables the extraction of higher order harmonics (the push-push signal) from its common nodes. The complete 30 GHz VID-based differential Colpitts VCO is shown in Figure 3.1. Its varactor bank in the emitter node coarse-tunes to switch the frequency band according to the input digital input, the VID in the base node fine-tunes the oscillation frequency on top of the selected frequency band, thereby unlike traditional Colpitts VCOs, this VID-based Colpitts VCO obtains 2 degrees of freedom on frequency tuning (similar to Colpitts-Clapp VCOs) and is optimized to widen the TR for the IEEE 802.11ad applications.

The design of this 30 GHz VID-based VCO is broken down into different sub-sections to ease reading. The design of the VID, the varactor bank, the switching HBT, the current mirror, and the output buffer are discussed in 3.1.1 to 3.1.5 respectively. The design of the inductors will be shown afterward. This chapter is finished with summaries.

3.1.1 The VID Design

The VID designed in this work consists a transformer and an NMOS transistor. The geometry of the transformer windings has a profound impact on the VID characteristics. Generally, as discussed in 2.5, the target is to obtain high Q, low coupling
Figure 3.1: 30 GHz VID-based VCO schematic, shows the VID in (1), the varactor bank in (2), the switching HBT in (3), the current mirror bias in (4), and the CC output buffer in (5).

Coefficient \((k)\), and accordingly low inductances for both the primary and the secondary transformer windings. As a part to reduce the trace series resistance and hence increase the Q of the primary and the secondary windings, both the primary and secondary windings of the transformer in the VID have trace width = 8 \(\mu\text{m}\).
They were laid out parallelly in metal layers 4, 5, 6, and they are connected back to back through vias on the windings. The Q factor for the transformer itself is around 25.5. The combination of trace width and spacing between the primary and the secondary windings determines the $k$ of the transformer, which in turn contributes to the rate of change of $L_{eq}$ and $L_{eq,lin}$ in (2.20) from 2.5. To balance these 2 contradictory factors, as well as the general area occupied by the VID, the trace spacing for both the primary and secondary windings of the transformer was set to 8 $\mu$m to cooperate with the set trace width. This trace spacing and width combination yields a coupling coefficient $k = 0.41$. The equivalent inductance ($L_{eq}$) of the VID is positively proportional to the radii of the primary and secondary windings (spiral). As demonstrated by Figure 3.2, at a given trace spacing and trace width (so that $k$ is nearly held constant), by reducing the radii of the windings from the top to the bottom curves, the range of $L_{eq}$ variation is nearly constant while the minimum and maximum $L_{eq}$ values of the VID were shifted downwards. After iterations, the desired values of the inner radius of the primary and the secondary windings to achieve the correct $f_{osc}$ are 52 $\mu$m and 36 $\mu$m, and as a result the inductance for the primary and the secondary windings themselves are $L_p = 188.5$ pH and $L_s = 154.8$ pH respectively. Figure 3.3 demonstrates these specifications of the transformer used in the VID. The Q factors for the 2 windings are high and the coupling coefficient of the transformer is low, these are very beneficial to the VCO performance.

The variable resistor $R_v$ and its parasitic capacitance $C_v$ in Figure 2.6 were implemented by an NMOS transistor. This NMOS transistor plays an equally important role as the transformer in determining the characteristics of the VID. As shown in Figure 3.4a and 3.4b, as the width of an NMOS transistor increases from the bottom
3.1. VCO DESIGN DETAILS

Figure 3.2: Transformer windings radii and its impact of $L_{eq}$ of the VID. Different curves in different colors represent VID characteristics with transformers of different winding radii.

to the top curves (all other parameters remains constant), the terminal equivalent resistance $R_{eq}$ variation from $V_{tune} = 0$ V to 1 V reduces, while the terminal capacitance $C_{v}$ increases in this $V_{tune}$ range. Since $R_{eq}$ variation is positively proportional to the $L_{eq}$ variation of the VID, narrower FET provides large $R_{eq}$ variation, which leads to the TR increment of the VCO as a whole. However, employing a narrow FET leads to 2 drawbacks. One is that the rate of change of $L_{eq}$ is increased, which will increase the VCO gain ($k_{VCO}$) and worsen the phase noise performance of the VCO. Another drawback can be understood with the assistance of Figure 2.8, because narrower FET has smaller $C_{v}$, the linear range of the tunable inductance of the VID, $L_{eq,lin}$ is reduced. This is counteractive and should be avoid. According to different applications, this trade-off has to be addressed correspondingly. The NMOS
3.1. VCO DESIGN DETAILS

transistor implemented in this design has gate length 45 \( \mu m \), gate width 130 nm, and 5 fingers. This set of dimensions enables the MOSFET to provide a suitable \( R_{DS} \) variation to the transformer within the specified control voltage range of 0.3 V to 1.5 V from the charge pump in the targeted PLL.

All together, the VID schematic setup is shown in Figure 3.5 and its layout arrangement is shown in Figure 3.6. As demonstrated by Figure 3.7, with the tuning voltage \( (V_{tune}) \) ranging from 0.3 V to 1.5 V (the realistic tuning voltage that the charge pump in the targeted PLL will supply), the VID is able to vary its input inductance from 114 pH to 93 pH and the Q value changes from approximately 8 to 4 during the entire process.
3.1. VCO DESIGN DETAILS

Figure 3.4: Demonstration of the NMOS transistor in terms of (a) the terminal resistance $R_{eq}$ and (b) the terminal capacitance $C_v$ with different device widths (slight ripples in the simulation results were due to the limitations by the simulator used and can be ignored)

Figure 3.5: Isolated VID schematic
3.1. VCO DESIGN DETAILS

Figure 3.6: Isolated VID layout
3.1. VCO DESIGN DETAILS

3.1.2 The Varactor Bank Design

As shown in Figure 3.1, there are 3 differential varactor pairs in the emitter node forming VCO coarse frequency control bit2, bit1, and bit0 respectively. More differential varactor pairs could be included to further widen the TR, but for proof of concept purpose, only 3 varactor pairs were implemented in this design to ease the measurement. In order to evenly cover the designed tuning band, the off-capacitances of bit2, bit1, and bit0 varactor pairs are binary weighted as 50 fF, 100 fF, and 200 fF respectively. As discussed in 2.4, the finger width $W_f$ of all varactors should be minimized to obtain lower gate resistance. Hence the 50 fF varactor consists of 2 MOSFET sub-cells. Each cell has 10 gate fingers ($N_f = 10$), 1.5 $\mu$m gate finger width ($W_f = 1.5 \mu$m, which is the minimum value allowed by the design kit), and 134 nm channel length ($L_{phys} = 134$ nm). The 100 fF varactor consists of 2 MOSFET
3.1. VCO DESIGN DETAILS

Figure 3.8: The 50 fF varactor layout

Each cell has $N_f = 20$, $W_f = 1.5 \mu m$, and $L_{phys} = 134$ nm. Finally the 100 fF varactor also consists of 2 MOSFET sub-cells. Each cell has $N_f = 40$, $W_f = 1.5 \mu m$, and $L_{phys} = 134$ nm. Figure 3.8 shows the close-up view of the layout of the 50 fF varactor, and Figure 3.9 shows the layout of the 50 fF, 100 fF, and 200 fF varactors together. Finally, Figure 3.10 shows the simulated tuning curve of the 3 varactors with respect to the tuning voltage. This figure shows that those varactors have 2:1 capacitance ratio when their terminal voltage $V_{var}$ varies from 0 V to 1.5 V. A capacitance ratio of nearly 4:1 can be achieved if both terminals of each varactor can be biased separately through DC-blocking capacitors (similar to the base node varactors in a Clapp VCO), so that $V_{var}$ varies from -1.5 V to 1.5 V, but this was not implemented in this VCO design because it is not supported by the digital control subcircuit in the current radio system that this VCO was designed for.

3.1.3 The Switching HBT Design

As mentioned in 2.3, the switching transistor $Q_1$ and its twin in Figure 3.1 provide loop gain to start and sustain the oscillation in the tank, hence the transistor is
3.1. VCO DESIGN DETAILS

Figure 3.9: The 50 fF, 100 fF, and 200 fF varactor layouts from bottom to top

Figure 3.10: The 50 fF, 100 fF, and 200 fF varactors tuning curves
3.1. VCO DESIGN DETAILS

Crucial to an oscillator design. The fact that the oscillation frequency in a VCO varies according to the control signals stresses more demand for the switching transistors, because instead of operating at a single frequency, they must be low noise and able to provide sufficient gain throughout this entire frequency TR to maintain a stable oscillation. In this differential Colpitts VCO design, HBT $Q_1$ and its twin share 3C4B2E dimensions: 3 collectors, 4 bases, and 2 emitters with length measured at 5 $\mu$m each, as shown in Figure 3.11. Each HBT is biased to have 10 mA of emitter current ($I_E$). Those HBT dimensions and bias condition were chosen with respect to the HBT’s high frequency characteristics. The 3 curves in Figure 3.12 represent the $f_t$, $f_{max}$, and $N_F_{min}$ characteristics of the HBT of aforementioned dimensions (refer to 2.3 for detailed explanations on the 3 important parameters). Notice that in this figure the 2 vertical axises (frequency and $N_F_{min}$) are linear and the horizontal axis ($I_E$) is logarithmic. Approximately, both $f_t$ and $f_{max}$ peak at around $I_E = 19$ mA, which means that given the bias current flowing through this HBT is 19 mA, this HBT is capable to provide current and power gains, and maintain oscillation up to about 280 GHz (refered to the vertical axis). If such a HBT based oscillator operates beyond 280 GHz, no matter how much bias current is being fitted through the HBT, this HBT will no longer produce any current and power gain, and the oscillation will cease eventually. Also, the lowest $N_F_{min} = 2.1$ dB of this HBT configuration can be found at $I_E = 2.5$ mA. This means that this HBT will have its lowest noise figure of 2.1 dB if it is biased at $I_E = 2.5$ mA. A low noise figure of the switching transistor is very beneficial to a VCO, because it can reduce the phase noise of the VCO. However, when considering $N_F_{min}$ together with $f_t$ and $f_{max}$ in this case, using 2.5 mA emitter current may not leave enough buffer zone for the VCO to counter PVT variations.
3.1. VCO DESIGN DETAILS

Figure 3.11: The layout of the 10 $\mu$m switching HBT

and other unpredictable factors to guarantee performance. As a balance point to maintain the HBT’s low noise figure, to fight PVT variations and to utilize the high frequency potential of this HBT, the emitter bias current of 10 mA was chosen and implemented in the design of this 30 GHz VID-based VCO. This bias current can be further reduced in the future design revisions of this VCO after this 10 mA scheme is fully evaluated.
3.1. VCO DESIGN DETAILS

3.1.4 Biasing of the VCO

As shown in Figure 3.1, the switching HBTs in the VCO are biased using current mirror topology. Compared to direct voltage bias of the base of the HBTs through a resistive voltage divider, the current mirror method is a more robust method for bias. If PVT variation is significant, then both the switching HBT pair and the current mirror HBT will be affected simultaneously, hence maintain a constant mirroring ratio. This current mirror includes a 7.5 ohms tail resistor $R_{tail}$, a CBE configured HBT $Q_3$ with 2 $\mu$m emitter width, and a 75 $\Omega$ bias resistor $R_2$. The collector of the bias HBT is connected to an external current source (the integrated DC central of the WiGig radio) through a 570 $\Omega$ resistor for isolation. Linking this 2 $\mu$m HBT to the 10 $\mu$m switching HBT pair (in total 20 $\mu$m) produces a mirroring ratio of 1:10, the ratio between $R_2$ and $R_{tail}$ is also controlled at 1:10, hence the bias currents between the
bias HBT and the summation of the switching HBT pair is 1:10, which is 2 mA for
the bias HBT and 10 mA for each switching HBT as mentioned before. Also notice
that the traditional tail transistor is replaced by $R_{\text{tail}}$ in this bias scheme. This was
done to prevent noise leakage from the tail transistor into the switching HBTs.

3.1.5 The Output Buffer Design

The common-collector (CC) configuration was chosen for the output buffer for the 30
GHz VID-based VCO. As shown in Figure 3.1, the output buffer consists of a pair
of 3C4B2E HBTs ($Q_2$ and its twin) with 3 $\mu$m per emitter. The buffer HBTs are
biased using a pair of 50 $\Omega$ emitter resistors $R_{\text{buf}}$. Theoretically, Colpitts configured
VCOs are well suited with common-base (CB) output buffers, which presents a very
low impedance to the VCO, hence allowing the VCO current to be transferred to
the load without loading the tank [22] [9]. However, CB configuration will reduce
headroom of the switching HBTs, hence reduce the voltage swing in the tank. Also,
employing CB output buffers will make the integration with the following stage more
complex, the inductive load $L_1$ has to be redesigned to accommodate the CB buffer.
Also, the choice of employing a CC output buffer stage instead of a common-emitter
(CE) configuration was simply because the level of the voltage oscillations at the
collector nodes of the switching HBTs are quite high at more than 1.8 V peak-to-
peak. Voltage gain is not a priority in this case. Since this VCO will be measured with
50 $\Omega$ apparatus, which is considered low impedance when compared to the collector
node of the switching HBT, it is important to have a voltage buffer to maintain the
current level in such a high-low impedance transition. Nevertheless, this CC buffer
was included for the sake of the 30 GHz Colpitts VCO breakout alone. It is not
needed when the VCO is connected to the frequency doubler for its real intended function (as will be shown in Chapter 4). Hence it made sense to choose an output buffer topology that can be easily deleted without requiring modification to the main circuit. That is why the CC configuration was favored over the more traditional CE and CB configurations. The dimensions of the buffer HBTs have a profound effect on the final current output and its own power consumption. The dimension of 3C4B2E with 6 \( \mu \text{m} \) emitter length (2 emitters with 3 \( \mu \text{m} \) per emitter) for each HBT was chosen to maintain output power on the external 50 \( \Omega \) load, while not consuming too much power. Figure 3.13 compares the different output differential voltage level on a 50 \( \Omega \) load. By reducing the HBT size from 6 \( \mu \text{m} \) to 3 \( \mu \text{m} \), the output differential voltage level drops from 1 V peak-to-peak to less than 0.5 V peak-to peak, which is not desirable for measuring this prototype VCO.

### 3.1.6 The Inductors Design and Summary

Being a LC-tank type VCO, there are many inductors distributed in the circuit. Spiral inductors are placed at the collector nodes (\( L_1 \) pair), between the base node and the current mirror (\( L_2 \)), the emitter nodes (\( L_3 \) pair), and the common mode tail (\( L_4 \)) in this VCO. In order to achieve the desired \( f_{\text{osc}} \) and TR, the designed inductances are, \( L_1 = 100 \text{ pH} \), \( L_2 = 600 \text{ pH} \), \( L_3 = 500 \text{ pH} \), and \( L_4 = 250 \text{ pH} \). Table 3.1 contains their detailed specifications obtained from EM simulations (using Integrand EMX) for each inductor above. Aside from accurately achieving designed inductances, these spiral inductors are also tailored to have high Q-factors, which help reducing phase noise of such a sensitive system. All inductors implemented in this 30 GHz VID-based VCO are octagonal as this shape can have moderately better RF performance compared to
3.1. VCO DESIGN DETAILS

Figure 3.13: Simulated differential waveforms captured from the VCO using buffer HBT pair with (a) 6 $\mu$m and (b) 3 $\mu$m emitter size for the CC output buffer. Marker M0 points to the waveform at the collector nodes of $Q_1$ and its twin, M1 points to the waveform at the base node of $Q_1$ and its twin, and M2 points to the waveform at this final output nodes of $Q_2$ and its twin.
3.2. SIMULATION RESULTS AND ANALYSIS

<table>
<thead>
<tr>
<th>Item</th>
<th>Sides</th>
<th># of Turns</th>
<th>Inner Radius (um)</th>
<th>Trace Width (um)</th>
<th>Spacing (um)</th>
<th>L @ 30 GHz (pH)</th>
<th>Peak SRF (GHz)</th>
<th>Q @ 30 GHz</th>
<th>Guard Ring</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>8</td>
<td>1.5</td>
<td>8</td>
<td>3</td>
<td>3</td>
<td>103.2</td>
<td>207.5</td>
<td>19.3</td>
<td>No</td>
</tr>
<tr>
<td>L2</td>
<td>8</td>
<td>3</td>
<td>18.6</td>
<td>2.2</td>
<td>10</td>
<td>648.9</td>
<td>51</td>
<td>20.38</td>
<td>Yes</td>
</tr>
<tr>
<td>L3</td>
<td>8</td>
<td>2.75</td>
<td>13</td>
<td>2.2</td>
<td>2.5</td>
<td>496.5</td>
<td>77.9</td>
<td>16.37</td>
<td>Yes</td>
</tr>
<tr>
<td>L4</td>
<td>8</td>
<td>2.5</td>
<td>10.2</td>
<td>2.2</td>
<td>1.4</td>
<td>243.5</td>
<td>95.8</td>
<td>15.01</td>
<td>No</td>
</tr>
</tbody>
</table>

Table 3.1: Inductor Specifications

square inductors [23]. Except $L_2$ and $L_3$ that was laid in only metal layer 6, all other inductors were drawn in metal layer 5 and 6 in parallel. Both $L_2$ and $L_3$ feature broken guard rings around the inductor trace. Figure 3.14 shows that the $L_3$’s spiral traces are partially enclosed by the broken guard ring. This is another effort to improve passive component Q-factors, because guard rings isolate the inductor from substrate noise current generated by other components nearby, reduce energy loss due to the Eddy current (hence less resistive, higher Q values), and a broken configuration will not reduce component inductance (hence will not reduce Q value) as a close guard ring does [24]. Due to area limitations, $L_1$ and $L_4$ do not have guard rings.

In summary, the components and their parameters are listed in Table 3.2. The overall layout for the 30 GHz VID-based VCO together with its pad frame is shown in Figure 3.15. The total circuit area is 350 µm (h) x 405 µm (w), the area including pads is 575 µm (h) x 650 µm (w) circuit limited.

3.2 Simulation Results and Analysis

According to Cadence Spectre simulations based on the extracted circuit components, this 30 GHz VID-based differential Colpitts VCO behaves as shown in Figure 3.16.
Determined by the 3 binary-weighted differential varactors, there are 8 bands selectable from this VCO, and the continuous frequency coverage provided by this VCO is from 27.39 GHz to 34.93 GHz, a total of 7.54 GHz, or 24.2% TR.

There are a few things to observe from Figure 3.16. The first thing is about the amount of overlaps between different adjacent frequency bands. This can also be viewed from Figure 3.17, which the adjacent bands overlap regularly changes from around 70% to 60%. However, between band 100 and band 011 where the MSB varactor ($C_{bit0}$, the 200 pH varactor) switches from off to on-state, the corresponding frequency bands shifts up significantly, causing a lower overlap at 31%. This sudden frequency overlap drop is due to the parasitic capacitances of $C_{bit0}$. The varactors used in this VCO design are based on MOSFET (A-MOS), hence some of the varactors’ properties are naturally inherited from MOSFETs, including the tendency of the larger the device size, the larger the parasitic capacitance that the device has. As a
### 3.2. SIMULATION RESULTS AND ANALYSIS

Table 3.2: 30 GHz VID-based Colpitts VCO component list

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Component Name</th>
<th>Description</th>
<th>Specs. @ 30 GHz</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor</td>
<td>$C_1$</td>
<td>Tank</td>
<td>500 fF</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$C_2$</td>
<td>De-decouple</td>
<td>10 pF</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$C_3$</td>
<td>De-decouple</td>
<td>1.2 pF</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$C_{tail}$</td>
<td>De-decouple</td>
<td>3 pF</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$C_{blk}$</td>
<td>De-decouple</td>
<td>1 pF</td>
<td>2</td>
</tr>
<tr>
<td>Inductor</td>
<td>$L_1$</td>
<td>Inductive load</td>
<td>100 pH</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$L_2$</td>
<td>Current bias isolation</td>
<td>600 pH</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$L_3$</td>
<td>Common mode isolation</td>
<td>500 pH</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$L_4$</td>
<td>Ac-decouple</td>
<td>250 pH</td>
<td>1</td>
</tr>
<tr>
<td>Transformer</td>
<td>$L_p$</td>
<td>Primary winding</td>
<td>188.5 pH</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$L_s$</td>
<td>Secondary winding</td>
<td>154.8 pH</td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td>$R_1$</td>
<td>Off-chip isolation</td>
<td>570 Ω</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$R_2$</td>
<td>Bias current setup</td>
<td>75 Ω</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$R_{tail}$</td>
<td>Switching HBT bias</td>
<td>7.5 Ω</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$R_{buf}$</td>
<td>Output buffer HBT bias</td>
<td>50 Ω</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$R_{DC}$</td>
<td>Control noise isolation</td>
<td>500 Ω</td>
<td>4</td>
</tr>
<tr>
<td>Varactor</td>
<td>$C_{bit0}$</td>
<td>Digital tuner bit0</td>
<td>50 fF</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$C_{bit1}$</td>
<td>Digital tuner bit1</td>
<td>100 fF</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$C_{bit2}$</td>
<td>Digital tuner bit2</td>
<td>200 fF</td>
<td>2</td>
</tr>
<tr>
<td>Transistor</td>
<td>$Q_1$</td>
<td>VCO switching HBT</td>
<td>3C4B2E, 5 μm / E</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$Q_2$</td>
<td>Output buffer HBT</td>
<td>3C4B2E, 3 μm / E</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>$Q_3$</td>
<td>Current mirror reference</td>
<td>CBE, 2 μm / E</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$M_1$</td>
<td>VID control</td>
<td>L = 0.13 μm, W = 45 μm, 5 fingers</td>
<td>1</td>
</tr>
</tbody>
</table>

result, although the varactors in the varactor bank are scaled to have off-capacitance of 50 fF, 100 fF, and 200 fF (as introduced in 2.4 that their off-capacitance is approximately half of their on capacitance), revealed by simulation in Figure 3.10 that they actually differ from those intended capacitances. By referring to the readings from Figure 3.10, other than the intended on and off-capacitance, each varactor has been assigned with their simulated on and off capacitances: bit0 varactor has simulated
As summarized in Table 3.3 (an extended version of table 2.1 in 2.4), the 3 bits (3 pairs of varactors) switch on and off to create capacitance variation from 377 fF to 197 fF. While the capacitances of the smaller varactors bit1 and bit2 are not very far off from the intended values, the largest varactor bit0 has 29 fF and 17 fF more...
3.2. SIMULATION RESULTS AND ANALYSIS

Figure 3.16: Simulated frequency tuning characteristics of the 30 GHz VID-based VCO

capacitance at on and off-states compared to the ideal values. When the varactor bank switches state from 000 to 011 or from 100 to 111 the capacitance reduces in steps of 22 to 25 fF, but when switching state 011 to 100 (bit0 state changes) the capacitance changes rapidly by 44 fF, which causes a significant capacitance jump when switching from band 011 to band 100, hence lead to the frequency jump observed in Figure 3.16. The solution to this problem is that, instead of use varactors with different dimensions that can lead to different parasitic capacitances, it is better to use varactor module in a unit of 50 fF, so in order to achieve the intended capacitances, $C_{bit2}$ contains 1 module, $C_{bit1}$ contains 2 modules, and $C_{bit3}$ contains 4 modules.

Another observation is that the overall shape of those frequency tuning curves on Figure 3.16 is reminiscent to the VID inductance tuning characteristics shown on Figure 3.7. Since the capacitance of the varactors are fixed by the control signal within
3.2. SIMULATION RESULTS AND ANALYSIS

Figure 3.17: Adjacent bands overlap

Table 3.3: Three bits varactor analysis

<table>
<thead>
<tr>
<th>bit0</th>
<th>bit1</th>
<th>bit2</th>
<th>Name</th>
<th>Total Capacitance Composition</th>
<th>Ideal Capacitance (fF)</th>
<th>Simulated Capacitance (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(C_0)</td>
<td>(a+b+c)</td>
<td>350</td>
<td>377</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(C_1)</td>
<td>(a+b+C)</td>
<td>325</td>
<td>355</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(C_2)</td>
<td>(a+B+c)</td>
<td>300</td>
<td>331</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(C_3)</td>
<td>(a+B+C)</td>
<td>275</td>
<td>309</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(C_4)</td>
<td>(A+b+c)</td>
<td>250</td>
<td>265</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(C_5)</td>
<td>(A+b+C)</td>
<td>225</td>
<td>243</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>(C_6)</td>
<td>(A+B+c)</td>
<td>200</td>
<td>219</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>(C_7)</td>
<td>(A+B+C)</td>
<td>175</td>
<td>197</td>
</tr>
</tbody>
</table>

each single frequency band, the VID control signal \(V_{\text{tune,L}}\) solely controls the in-band frequency tuning of the VCO. Therefore, due to the inversely proportional relationship between \(f_{\text{osc}}\) and \(V_{\text{tune,L}}\) as shown in (2.6), the final VCO output frequency versus the tuning voltage curves are closely related to the inverted version of the frequency tuning curve of the VID.

The simulated phase noise characteristics of the 30 GHz VID-based differential Colpitts VCO is shown in Figure 3.18. The plot includes the phase noise variations in band 000 and band 111, which also represent the lowest and highest phase noises.
obtained from this VCO. There are 2 important things to notice in this plot. One important thing is that, the phase noise of this VCO peaks at around 0.6 V. This is because the rate of change of $L_{eq}$ is the largest in the VCO, causing largest VCO gain in this range, hence producing higher phase noise. This verifies the positively proportioned relationship between VCO gain and phase noise. Another thing is the observation that the phase noise level of the higher band is higher than the one from the lower band. This may look unreasonable at first. Similar to capacitors, the Q-factor of the varactor can be approximated as

$$Q = \frac{1}{\omega_0 C R_C},$$  \hspace{1cm} (3.1) \tag{3.1}

where $\omega_0$ is the resonance frequency of the varactor, $C$ is the equivalent capacitance, and $R_C$ is the series resistance of the varactor. One can see that the Q of a varactor should increase as the tuning voltage increases, since the equivalent capacitance is negatively proportional to the tuning voltage. So the phase noise level should drop as the VCO operate at higher bands. However, this is not true. First, as pointed out by Thomas Lee in [23], the phase noise of a VCO is a function of many factors, not solely depends on the Q-factor of the tank. Second, as the operating frequency of the VCO is being tuned higher, all components in the circuit respond to it, their Q-factors will quickly roll off, the negative resistances of the active components will reduce, and the entire circuit will become more prone to extrinsic noises, etc. All those factors combine and outweigh the Q increase of the emitter node varactors, hence raise the overall phase noise level as the VCO operates at higher bands.
3.3. MEASURED RESULTS AND ANALYSIS

The fabricated die of the 30 GHz VID-based differential Colpitts VCO is shown in Figure 3.19. The turnaround time for the fabrication at STMicroelectronics took 3 months, which is longer than in general 2 months turnaround time for the more common 45 nm CMOS designs. This can be considered a minor drawback of the 130 nm BiCMOS process.

The measurement setup for this 30 GHz VID-based differential Colpitts VCO is shown in Figure 3.20. The 6 DC inputs on the VCO are $I_{bias}$, $V_{tune}$, $V_{CC}$, $V_{bit0}$, $V_{bit1}$, and $V_{bit2}$. They were controlled by the 6 DC outputs from the 3 Agilent E3646A DC power supplies. The DC bias current of the VCO through the $I_{bias}$ port was further verified through the multimeter during each measurement. Because the output of this VCO is differential but the spectrum analyzer has 1 input port, 1 port from the VCO
The measured frequency tuning performance of the 30 GHz VID-based differential Colpitts VCO is shown in Figure 3.21. Under the designed bias conditions, this fabricated VCO operated from 28.28 GHz to 33.47 GHz in the 8 bands, translating
Figure 3.20: Measurement setup for the 30 GHz VID-based differential Colpitts VCO
to 17% TR. Compared to the simulated frequency performance of the VCO in Figure 3.16, which returned 24% TR. This 7% TR reduction is due to 3 main reasons. The first reason is due to the limited accuracy of the EDA tools used, the mutual couplings between different component in the layout, especially inductors, were not fully captured during the simulation. This was due to the limitation of the EDA tools used. The second reason is that there were extra dummy metals inserted into the layout after the final simulation but before the final sign-off of the design, which was due to a communication delay with the foundry before the tapeout. For instance, the square metal piece inserted in the center of the transformer in Figure 3.19 was made without simulation right before the sign-off of the design. The third reason is the PVT variation between the simulation and the measurement environment. As the result of those factors, the usable $V_{tune}$ range of this VID-based Colpitts VCO is from 0.1 to 0.9 V.

Figure 3.22 shows the phase noise performance of the 30 GHz VID-based differential Colpitts VCO. In this figure, the 2 different dashed lines are the simulated phase noises for the lowest band 000 and the highest band 111, and the solid lines are the measured phase noises. Although as described in Appendix C that today’s phase noise simulation accuracy is still quite low, it serves the purpose of providing insights to the actual measurement results, hence both the measured and the simulated (identical to Figure 3.18) phase noise results are overlaid together. There are 2 important observations in this plot. The first phenomenon is that the high band (i.e. band 111) experiences higher phase noise compared to the low band (i.e. band 000). This observation matches to the simulated results and the description in 3.2. The second is that the measured phase noise results of the 2 bands are more apart from
3.3. MEASURED RESULTS AND ANALYSIS

![Measured frequency tuning curves of the 30 GHz VID-based differential Colpitts VCO](image)

Figure 3.21: Measured frequency tuning curves of the 30 GHz VID-based differential Colpitts VCO

each other than in the simulation while generally centered on the simulated results, which is partly ascribed to the EDA tools' inability to include all parasitic effects during simulation. Also, this can be related to the impact from the noisy measurement environment to the sensitive circuit. The fine-tune control line ($V_{\text{tune}}$) of this VCO was designed as single-ended to ease the measurement setup, which lacks the ability to reject common-mode noise and noise coupled from DC lines of the VCO. This 30 GHz VID-based Colpitts VCO was measured at Queen’s University in Kingston, so the measured signals were contaminated by the campus radio and AM radio signals in the ambient environment. Those are the reasons that caused the fluctuations between the simulated results and the measured results on the phase noise measurement of this 30 GHz VID-based Colpitts VCO.

The output power of this 30 GHz VID-based differential Colpitts VCO is shown
3.3. MEASURED RESULTS AND ANALYSIS

Figure 3.22: Measured vs. simulated phase noise values of the 30 GHz VID-based differential Colpitts VCO

in Figure 3.23. The apparatus loss and the 3 dB loss single-ended loss have been de-embedded from the results. The measurement results are very consistent and are close to the simulated results, which were in terms of the output voltage swings at more than 1 V peak-to-peak onto 50 Ω off-chip load.

Finally, the performance of this 30 GHz VID-based differential Colpitts VCO is listed in Table 3.4 below. The meanings and calculations of the different FOMs used in this section is discussed in 2.7.
3.3. MEASURED RESULTS AND ANALYSIS

Figure 3.23: Measured differential output power from the 30 GHz VID-based differential Colpitts VCO

Table 3.4: 30 GHz VID-based differential Colpitts VCO performance summary

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>130 nm BiCMOS</td>
</tr>
<tr>
<td>$f_{osc}$ range (GHz)</td>
<td>28.3 - 33.5</td>
</tr>
<tr>
<td>TR (%)</td>
<td>16.8</td>
</tr>
<tr>
<td>SSB PN (dBc/Hz)</td>
<td>-101.4</td>
</tr>
<tr>
<td>$P_{out}$ (dBm)</td>
<td>4</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td>40.3</td>
</tr>
<tr>
<td>$V_{CC}$ (V)</td>
<td>1.4</td>
</tr>
<tr>
<td>$FOM$ (dB)</td>
<td>-175.1</td>
</tr>
<tr>
<td>$FOM_T$ (dB)</td>
<td>-179.6</td>
</tr>
<tr>
<td>$FOM_{TP}$ (dB)</td>
<td>-183.4</td>
</tr>
</tbody>
</table>
Chapter 4

The Design of 60 GHz VID-Based Differential Colpitts VCO

Built on the foundation of the 30 GHz VID-based Colpitts VCO in Chapter 3, this chapter explains the design details of the 60 GHz differential VID-based VCO. The simulation and measured results are analyzed in this chapter.
4.1 VCO Design Details

This 60 GHz VID-based differential Colpitts VCO was constructed on the foundation of the 30 GHz VID-based differential Colpitts VCO introduced in Chapter 3. This 60 GHz VCO was fabricated in 130 nm SiGe BiCMOS technology. The 60 GHz output frequency is achieved by connecting the slightly modified 30 GHz VID-based differential Colpitts VCO to a frequency doubler. Hence the 30 GHz VID-based VCO functions as a fundamental tone generator in this 60 GHz VCO chain design. The schematic of the 60 GHz VCO chain can be viewed at Figure 4.1.

Since this 60 GHz VCO is based on the 30 GHz VID-based VCO, most of the design details of this 60 GHz VCO are similar to those of the 30 GHz VID-based VCO except the inclusion of the frequency doubler. The general operation and the principles to design for the components of a frequency doubler are introduced in 2.6. In this frequency doubler design, the HBT \( Q_4 \) and its twin share CBEBC configuration with 3 \( \mu \)m emitter length, the common-mode inductive load \( L_5 = 252 \) pH, the DC bypass capacitor \( C_{bk} \) and its twin are 1 pH each, the tail resistor \( R_3 \) is 25 \( \Omega \). On the current biasing circuit of the frequency doubler, \( Q_5 \) has CEB configuration with emitter length 1 \( \mu \)m, the tail resistor is 150 \( \Omega \), the isolation resistor \( R_6 \) is 570 \( \Omega \), the frequency doubler tail resistor \( R_3 \) is 25 \( \Omega \), the 2 DC bypass capacitors \( C_4 \) and \( C_5 \) are 2.4 pH and 1.2 pH respectively. The resistors \( R_5 \) is 5 \( k\Omega \), \( R_4 \) and its twin are 2 \( k\Omega \), they are used to match the base input impedances between the 1 \( \mu \)m \( Q_5 \) and the 3 \( \mu \)m \( Q_4 \) pair to allow accurate base voltage control. The mirroring ratio between the bias HBT \( Q_5 \) and the \( Q_4 \) pair is 1:6, hence there is approximately 1 mA current flow through \( Q_5 \) and 6 mA current through the \( Q_4 \) pair (3 mA each).

Also, the implementation of the frequency doubler eliminates the need for the CC
4.1. VCO DESIGN DETAILS

buffer implemented in the 30 GHz Colpitts VCO. As mentioned in 3.1 that a CC buffer
does not have voltage gain, and because the connection is made right into the base
node of the switching HBTs in the frequency doubler, the frequency doubler is able to
present a large input impedance to the output of the 30 GHz VID-based VCO. So the
CC output buffer used in the 30 GHz VCO was left out in this 60 GHz VCO chain.
The final output is directly obtained from the collector common-node of the frequency
4.1. VCO DESIGN DETAILS

Figure 4.2: The 60 GHz VID-based differential Colpitts VCO waveforms captured at the collector node of the VCO and the output of the frequency doubler, clearly demonstrating the frequency doubling behavior by the frequency doubler.

doubler (net “fx2_out” in Figure 4.1). The simulated waveforms obtained when the 60 GHz VCO chain is connected to a 50 Ω load is demonstrated by Figure 4.2, where marker M0 indicates the peak-to-peak voltage of oscillation at the collector node of the VCO, and marker M2 indicates the peak-to-peak voltage of oscillation at the output of the frequency doubler (fx2_out node in Figure 4.1). The VCC of this frequency doubler is set to 1.8 V to increase its headroom for voltage swing and it consumes around 10 mW of DC power. Hence according to (2.28), the DC-to-RF efficiency of this frequency doubler is around 10%. The frequency doubling behavior of this frequency doubler is demonstrated in this figure. The frequency doubler layout is shown in Figure 4.3 and the layout for the entire 60 GHz differential Colpitts VCO...
4.2 Simulation Results and Analysis

According to Cadence Spectre simulations based on the extracted circuit components, this 60 GHz VID-based Colpitts VCO chain behaves as shown in Figure 4.5. The behavior is similar to that of the 30 GHz base VCO shown in Figure 3.16, plus the doubled frequencies. With the help from the frequency doubler, its TR remains at 25% as the 30 GHz base VCO, but now this VCO chain is able to oscillate from 54.35 GHz to 69.95 GHz, which fulfills the stringent TR requirement from the IEEE.
Figure 4.4: The layout of the 60 GHz VID-based VCO chain
### 4.2. SIMULATION RESULTS AND ANALYSIS

Table 4.1: 60 GHz VID-based differential Colpitts VCO component list

<table>
<thead>
<tr>
<th>Component Type</th>
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4.2. SIMULATION RESULTS AND ANALYSIS

Figure 4.5: Simulated frequency tuning characteristics of the 60 GHz VID-based VCO chain

802.11ad standard for the global market. Also, the parasitic capacitance on $C_{bit0}$ affects this 60 GHz VCO chain in the same way to the 30 GHz Colpitts VCO, which leads to a larger frequency jump between band 011 and band 111. The solution to this issue is discussed in 3.2.

The phase noise characteristics of the 60 GHz VID-based Colpitts VCO chain is shown in Figure 4.6. The plot includes the phase noise variations in band 000 and band 111, which also represent the lowest and highest phase noises obtained from this VCO. The phase noise performance of the 60 GHz VCO chain was simulated at 10 MHz offset frequency instead of 1 MHz to match to the measurement setting. This point will become clearer in the next section. One important thing to observe is that, while the overall shapes of the phase noise plots for band 000 and 111 are fairly similar between the 30 GHz VID-based VCO and the 60 GHz VID-based VCO chain, the levels have been shifted lower by about 10 dBc/Hz in the 60 GHz case. This is
4.3. MEASURED RESULTS AND ANALYSIS

Due to the combination of the 10 MHz offset and the frequency doubling behavior. According to [13], phase noise roll-off from 1 MHz to 10 MHz offset can be assumed to be 20 dB/decade, but frequency doubling will unavoidably increase by 6 dB, both of those assumptions are made in an ideal environment. Hence ideally, the 60 GHz VCO phase noise taken at 10 MHz offset should be 14 dBc/Hz lower than the phase noise taken at 1 MHz offset of the 30 GHz VCO. Through the phase noise simulations, the difference between the two scenarios are around 10 dBc/Hz, which can be reasonable in more realistic environment provided by the simulation tools.
Figure 4.7: Photo of the 60 GHz VID-based VCO chain
4.3 Measured Results and Analysis

The die of the 60 GHz VID-based differential Colpitts VCO is shown in Figure 4.7, and the measurement setup is shown in Figure 4.8. There were 2 major difference on the measurement setup between the 60 GHz VID-based VCO and the two 30 GHz VCOs. The first one was that 1 more DC power supply and multimeter were used for the 60 GHz VCO chain, as it requires 2 more DC inputs by the frequency doubler, which were port \( V_{CC18,FREQx2} \) and \( I_{bias,FREQx2} \). The second difference was that in order to measure the 60 GHz output from the VCO with the Rohde & Schwarz FSUP spectrum analyzer that tops out at 26.5 GHz, frequency down-convert mixing was performed between the VCO output and the spectrum analyzer input. As shown in Figure 4.8, the direct output signal from the frequency doubler was fed to a Millitech 15-03090 low-noise amplifier (LNA) and then to a mixer, yet another input to the mixer came from the Agilent E8257D signal generator through a QiunStar QPW-50662018-P2 power amplifier (PA). Both of the 2 amplifiers were inserted to overcome to loss of the passive mixer. The LNA was chosen to amplify the frequency doubler output to minimize added noise, and the PA was inserted to the signal generator output since its output signal has over 20 dB lower phase noise level at 1 MHz and 10 MHz offsets compared to the proposed 60 GHz VCO chain across the entire TR, so that the measured results would still be dominated by the performance of the VCO. The signal generator was setup to output at around 1.5 GHz lower frequency than the output signal from the frequency doubler, so that the down-converted signal at around 1.5 GHz can be easily read off of the spectrum analyzer. The final frequency tuning characteristics can be obtained by summing the 1.5 GHz mixed result with the corresponding signal generator output.
Figure 4.8: Measurement setup for the 60 GHz VID-based differential Colpitts VCO
4.3. MEASURED RESULTS AND ANALYSIS

Figure 4.9: Measured frequency tuning curves of the 60 GHz VID-based differential Colpitts VCO

Figure 4.9 shows the frequency tuning characteristics of the 60 GHz VCO chain. This VCO chain operates from 56.3 GHz to 67.2 GHz, which is doubled the frequency from its fundamental 30 GHz VCO in Figure 3.21. The TR for this 60 GHz VCO chain is as expectedly 17% TR, identical to its fundamental 30 GHz VCO. The frequency doubler precisely doubles the fundamental frequency from the 30 GHz VCO and this 60 GHz VCO chain covers from 56.3 GHz to 67.2 GHz. On the target, the IEEE 802.11ad standard requires frequency coverage from 57.24 GHz to 65.88 GHz [1], which is fully included the in TR of this 60 GHz VID-based differential Colpitts VCO chain. Therefore, this VCO is applicable to IEEE 802.11ad applications.

The phase noise measurement results of the 60 GHz VCO chain are shown in Figure 4.11. Immediately to be noticed is that the phase noise measurement of the 60 GHz VCO chain was done at 10 MHz offset, rather than 1 MHz offset used for the 30
4.3. MEASURED RESULTS AND ANALYSIS

GHz VCO. Due to lack of 60 GHz capable equipment, the measurement could not be conducted at Queen’s University in Kingston, which has relatively less ambient interference due to its low population density compared to Toronto downtown. Instead, the measurement for the 60 GHz VCO chain was done at the industrial partner’s lab, which has minimal EM shielding and it is located very close to the CN tower in Toronto downtown. Toronto downtown can be considered as one of the noisiest areas across Canada due to its dense population. There is a great amount of 24 hours active radio devices, including many powerful AM radio stations that occupy the spectrum from 840 KHz to 1.69 MHz, and FM radio stations occupy from 88.1 to 108 MHz. Figure ?? demonstrates the various interferences that coupled onto the phase noise measurement of the 60 GHz VID-based Colpitts VCO chain. In this figure, the vertical axis is the amount of spectrum phase noise measured in dBc/Hz, the horizontal axis is the offset frequency in GHz. In the left hand side of this figure, there are strong interferences surrounding the 1 MHz spectrum, which are mostly coupled from the AM radio signals. In the right hand side of this figure, there are also strong interferences surrounding the 100 MHz spectrum, which are mainly coupled from the FM radio signals. In contrast, the region around the 10 MHz spectrum is the cleanest. These interferences rendered the inability to measure phase noise of the 60 GHz VCO chain at 1 MHz or 100 MHz offset, hence 10 MHz offset was chosen under such circumstance to most accurately reflect the intrinsic properties of the measured VCO.

Back on to Figure 4.11, it can be observed that the simulated and measured results have good agreement. The overall discrepancy between the simulated and the measured phase noise results are within 5 dB, except for when $V_{tune} = 0.2$ V at band 000. To explain this difference, other than the aforementioned inaccurate varactor models
4.3. MEASURED RESULTS AND ANALYSIS

Figure 4.10: Measured vs. simulated phase noise values of the 60 GHz VID-based differential Colpitts VCO

provided by the process design kit (PDK), this difference can also be attributed to the fact that although the 60 GHz VCO chain was measured at 10 MHz offset, the results were still affected by the strong ambient interference, because the fine-tune control line ($V_{\text{tune}}$) and the VCO output were designed as single-ended to ease measurement, and the shielding at the industrial partner’s lab was not as tight as expected, hence the phase noise measurement was intruded by the ambient interference.

The output power of this 60 GHz VID-based Colpitts VCO chain is shown in Figure 4.12. As expected, as $V_{\text{tune}}$ increases to about 0.6 to 0.9 V, the output power dropped lower as the Q of the VID, hence the Q of VCO tank dropped overall. Nevertheless, this VCO chain produces output power constantly higher than 1.5 dBm throughout its operation range, which is very beneficial when driving stages after the VCO chain.

Finally, the performance of this 60 GHz VID-based differential Colpitts VCO chain is summarized in Table 4.2 below. The meanings and calculations of different FOMs
4.3. MEASURED RESULTS AND ANALYSIS

Figure 4.11: Demonstration of the strong interferences coupled onto the phase noise measurement of the 60 GHz VID-based Colpitts VCO chain

Figure 4.12: Measured output power of the 60 GHz VID-based differential Colpitts VCO
used in this section is discussed in 2.7.

Table 4.2: 30 GHz VID-based differential Colpitts VCO performance summary

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Performance</th>
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<tr>
<td>TR (%)</td>
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Chapter 5

The Design of 30 GHz Colpitts-Clapp VCO

The design details, simulated and measured results of the 30 GHz differential Colpitts-Clapp VCO are demonstrated in this chapter. This Colpitts-Clapp VCO is designed in companion with the 30 GHz VID-based Colpitts VCOs as another candidate of the fundamental VCO in the 60 GHz VCO chain. They were both fabricated using the same 130 nm SiGe BiCMOS process on the same wafer, so that the performance of the novel VID-based Colpitts topology and the conventional Colpitts-Clapp VCO topology can be meaningfully compared.
5.1 VCO Design Details

As first introduced in 2.3, the differential Colpitts-Clapp configuration is a popular VCO design to achieve wider TR at mm-wave frequencies. The performance of the Colpitts-Clapp configuration has been analyzed in detail in [14] [9] and [11]. This 30 GHz differential Colpitts-Clapp VCO was constructed based on the Colpitts configuration of the 30 GHz VID-based differential VCO introduced in Chapter 3, the major change is that the VID is replaced by the differential varactors and inductors in the VCO tank, meaning that the fine frequency tuning in this Colpitts-Clapp VCO is accomplished by the tank varactors instead of the VID.

As shown in Figure 5.1, the VID core seen in Figure 3.1 has been replaced by the inductor pair $L_{\text{base}}$ and the varactor pair $C_{\text{tune}}$. The fundamental operation of Colpitts-Clapp VCOs is introduced in 2.3 along with Colpitts VCOs. In this particular Colpitts-Clapp VCO, in order to obtain a better frequency band overlap and reduce $k_{\text{VCO}}$, $L_{\text{base}}$ is set to 83 pH and $C_{\text{tune}}$ is set to 60 fF. There are 2 reasons that limited the attempt to further increase the size of the tank varactors to increase the TR of the VCO. The first is due to the process limitation of the inductor. At 30 GHz, reducing the tank inductance much below the chosen value will create inductors with very low Q-factor. Using low Q tank inductors should be avoid as it will restrict the oscillation condition, increase DC power consumption, and increase phase noise.

The second limit is from the varactor itself. The larger the varactor, the larger parasitic capacitance it carries. Unlike the varactor, the parasitic capacitance is fixed, and larger parasitic capacitance can significantly jeopardize the TR. The rest of the components on this Colpitts-Clapp VCO are identical to the 30 GHz VID-based VCO. This components swap also shows the flexibility that this Colpitts VCO core
can be modified to suit different configurations.

Figure 5.1: 30 GHz Colpitts-Clapp VCO schematic

Figure 5.2 shows the layout of $L_{\text{base}}$. It has 1.25 turns to achieve the desired inductance and to ease the connection between the differential layout. In order to minimize phase noise, the base inductor $L_{\text{base}}$ was optimized on its Q-factor, this leads to a trace width of 4.5 $\mu$m, inner radius of 11.65 $\mu$m, and trace spacing of 0.6 $\mu$m. The EM simulation results of $L_{\text{base}}$ in Figure 5.3 reveal that this spiral inductor
sports 81.5 pH inductance, 18.3 Q-factor at 30 GHz, and self-resonant frequency at 185.4 GHz.

Figure 5.2: The base inductor used in the 30 GHz differential Colpitts-Clapp VCO
Figure 5.4 shows the overall layout of this 30 GHz differential Colpitts-Clapp VCO. It is very similar to the layout of the 30 GHz VID-based differential Colpitts VCO, except the VID is replaced by the base inductor and varactor pairs. Approximately the VID has total width 120 µm and total length 130 µm, yet the total width and length for the base inductor pair are 120 µm and 50 µm, which is significantly smaller than the VID. Hence the absence of the VID on this Colpitts-Clapp VCO helps to reduce the size of the VCO core to 304 (w) x 245 (l) µm (without the current bias subcircuit). This is an important benefit of the Colpitts-Clapp VCOs over the VID-based Colpitts VCOs, which can potentially improve system integration and reduce...
5.1. VCO DESIGN DETAILS

fabrication cost. The components and their parameters are presented in Table 5.1.

Figure 5.4: 30 GHz differential Colpitts-Clapp VCO layout
5.2 Simulation Results and Analysis

The frequency tuning curves produced by the 30 GHz differential Colpitts-Clapp VCO are shown in Figure 5.5. Due to the replacement of the VID with the base inductors and varactors, the general shape of those curves is very different from the curves for the VID-based VCOs in Figure 3.16 and 4.5. With these 8 bands, this VCO is...
5.3. MEASURED RESULTS AND ANALYSIS

able to be tuned from 27.63 GHz to 34.38 GHz, which translates to a TR of 21.7%. This simulated TR fulfills the requirement from the IEEE 802.11ad standard, but is lower than the 30 GHz VID-based VCO’s 24.2% TR. Notice that, however, this VCO requires $V_{tune}$ up to 2.5 V to achieve this 21.7% TR. As aforementioned, all the VCO designs presented in this thesis are tailored to operate with the industrial partner’s PLL, which can generate its $V_{tune}$ for up to 1.5 V. When factoring in this requirement, the frequency variation is dropped to from 27.63 GHz to 33.86 GHz, a TR of 20.3%. This TR is limited by the $V_{tune}$, and can be solved by implementing differential control lines to the tank varactors. The frequency band overlap ranges from 61% between band 001 and band 000 to 44% between band 110 to band 101. Notice that the existence of the frequency gap between band 100 and band 101, this is expected since the 3 pairs of varactors at the emitter node are unchanged between the 30 VID-based and the Colpitts-Clapp VCO designs.

5.3 Measured Results and Analysis

The fabricated die of the 30 GHz Colpitts-Clapp VCO is shown in Figure 5.6. The turnaround time for the fabrication at STMicroelectronics took 3 months, which is longer than in general 2 months turnaround time for the more common 45 nm CMOS designs. This can be considered a minor drawback of using the less common 130 nm SiGe BiCMOS process.

Figure 5.7 shows the measurement setup of the 30 GHz Colpitts-Clapp VCO. It shared the same setup as the 30 GHz VID-based Colpitts VCO in 3.3 and it was similarly measured at Queen’s University.

The measured frequency tuning curves are shown in Figure 5.8. Notice that all
5.3. MEASURED RESULTS AND ANALYSIS

Figure 5.5: Simulated 30 GHz Colpitts-Clapp VCO frequency tuning curves

Oscillation frequencies are shifted downward in the measured results. In the simulation this VCO covers from 27.63 GHz to 34.38 GHz with 21.7% TR. However, in the measurement results, the same VCO covers from 25.02 GHz to 29.44 GHz with 16.2% TR. When considering that $V_{\text{tune}}$ varies only from 0 to 1.5 V, the VCO covers from 25.02 GHz to 29.15 GHz with 15.2% TR. This frequency shift can be attributed to 2 main reasons. The first is the parasitic extraction accuracy of the tank inductors with the bias network that connects to them. Another reason is again the model accuracy of the base varactors. We can conclude from the fact that the oscillation frequencies shifted lower, that both the actual inductance from the inductors and capacitance from the varactors are larger than the extracted results. These discrepancies can be factored into the next design iteration to create a Colpitts-Clapp VCO that is more accurately centered around 30 GHz.

In terms of phase noise performance, this 30 GHz Colpitts-Clapp VCO performs
better than the 30 GHz VID-based Colpitts VCO. As shown in Figure 5.9, on average, band 000 phase noise of the VID-based VCO is 3.34 dBC higher than the Colpitts-Clapp VCO, and band 111 phase noise is 11.45 dBC higher. This can be mainly caused by 2 contributors. The first contributor is the tank Q factor of the Colpitts-Clapp VCO, which is higher than the one in the VID-based Colpitts VCO. As Figure 3.7
5.3. MEASURED RESULTS AND ANALYSIS

Figure 5.7: Measurement setup for the 30 GHz differential Colpitts-Clapp VCO
5.3. MEASURED RESULTS AND ANALYSIS

indicates, at 30 GHz, once $V_{\text{tune}}$ is increased beyond 0.3 V, the Q factor of the VID will drop below 8.5 with a minimum of approximately 4.2. On the other hand, for the tank of the Colpitts-Clapp VCO, as Figure 5.3 shows, the major series resistance provider, the tank inductor, has Q around 18 at 30 GHz, which is much more than the VID in the VID-based VCO. As the result, the tank Q of the Colpitts-Clapp VCO is higher than that of the VID-based VCO. Another contributor is the VCO gain. When $V_{\text{tune}}$ is from 0 to 1.5 V, the VCO gains (represented by frequencies) of each band of both the Colpitts-Clapp VCO and the VID-based Colpitts VCO are listed in Table 5.2. This table clearly indicates that the VCO gains of the VID-based Colpitts are higher than that of the Colpitts-Clapp VCO. As discussed in 2.5, the phase noise level is positively proportional to VCO gain. These 2 factors mean that the Colpitts-Clapp VCO has lower phase noise than the VID-based Colpitts VCO.
Table 5.2: 30 GHz VCO gain comparison

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<tr>
<td>000</td>
<td>1.33</td>
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Therefore, further adjustment to the 30 GHz VID-based Colpitts VCO is required in the future in order to excel in terms of phase noise performance.

Another interesting observation from Figure 5.9 is that, opposite to the VID-based VCOs presented in this thesis, for which the phase noise curves have a tendency to rise in the middle of the $V_{tune}$ range, this Colpitts-Clapp VCO’s phase noise is the lowest in the middle. This can be explained by realizing the difference in the fine frequency tuning element in the tank between the 2 configurations. In the 2 VID-based VCOs, frequency fine tuning is done using the VID. As shown in Figure 3.7, the Q-factor of the VID drops when $V_{tune}$ increases. On the other hand, the Colpitts-Clapp employs varactors for frequency fine tuning. As discussed in 3.2, that the Q-factor for varactors increases with $V_{tune}$, which is opposite to how the VID behaves in terms of Q-factor vs. $V_{tune}$. These Q-factor variations will in turn cause the overall tank Q to change, leading to the different phase noise curves. This is the main cause for the different phase noise shapes observed from the VID-based Colpitts VCO and the Colpitts-Clapp VCO in this thesis.

The measured output power is shown in Figure 5.10. Because of higher tank Q and lower phase noise, the 30 GHz Colpitts-Clapp VCO produces stronger tank
5.3. MEASURED RESULTS AND ANALYSIS

Figure 5.9: Measured phase noise values of the 30 GHz differential Colpitts-Clapp VCO voltage swing, hence the output power level of this 30 GHz Colpitts-Clapp VCO is higher than the 30 GHz VID-based Colpitts VCO as shown in Figure 3.23.

Finally, the performance of this 30 GHz differential Colpitts-Clapp VCO is listed in Table 5.3 below. The meanings and calculations of different FOMs used in this section is discussed in 2.7.
5.3. MEASURED RESULTS AND ANALYSIS

Figure 5.10: Measured output power of the 30 GHz differential Colpitts-Clapp VCO

Table 5.3: 30 GHz VID-based differential Colpitts VCO performance summary

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<th>Characteristics</th>
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<tr>
<td>TR (%)</td>
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<tr>
<td>SSB PN (dBc/Hz)</td>
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<td>$P_{out}$ (dBm)</td>
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<td>$FOM_{TP}$ (dB)</td>
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Chapter 6

Conclusions and Future Work

6.1 Summary and Performance Cross Comparisons

Three VCO designs were presented and evaluated in this thesis report. The 30GHz version of this VID-based Colpitts VCO topology was also compared with the conventional Colpitts-Clapp type VCO. The measured results confirmed that the novel VCO topology functioned as intended, and did so consistently. Their individual performance can be viewed from Tables 3.4, 4.2, and 5.3.

Table 6.1 and Table 6.2 summarize the cross-comparisons between the VCOs presented in this thesis with other published state-of-the-art VCOs at 30 GHz and 60 GHz correspondingly. The FOM formulas used in these comparisons are discussed in 2.7. In both comparisons, unlike many of the other designs that their FOM dropped when TR and output power are considered, the FOM of the VID-based Colpitts VCOs presented in this thesis become more superior as these factors are added in to the calculation. This FOM increase matches the objectives of this project, which are to improve VCO TR while maintaining output power and other key parameters to enable implementations into IEEE 802.11ad compliant radio systems. Another
important thing to notice is that, the FOMs reported in these 2 tables were calculated based on the best measurement readings from the VCOs presented. Hence the performance variations are not reflected in those scores. For instance, the $FOM_T$ and the $FOM_{TP}$ reported from [16] are -188.54 and -181.94 dBc/Hz, which are exceptionally high scores. However, the VCO presented in that work has phase noise variation as much as 47 dB within its $V_{tune}$ range, which will significantly hinder its application into real-world radio systems, despite its high FOM scores. On the other hand, as comparison, the 60 GHz VID-based Colpitts VCO presented in this thesis has maximum phase noise variation of less than 20 dB between the 2 extreme frequency bands, making this VCO a much more stable and consistent building block in a radio system. Nevertheless, one major obstacle must be overcome before taking this VID-based Colpitts VCO design to the next level, commercialization, is that the phase noise level would need to be improved by about 5 to 10 dBc/Hz.

6.2 Conclusion

With the supervision of Dr. Brian Frank at Queen’s University and the generous support from the industrial partner, a novel VID-based Colpitts VCO topology was designed, simulated, fabricated, and measured through the 3 VCO prototypes. Although the phase noise performance of the VID-based Colpitts VCOs requires further improvements, this novel VCO topology was capable of widening the TR to suit the IEEE 802.11ad compliant applications, which is the main accomplishment of this work. The VID in the base node of the VCO eliminated the negative effects of the fixed parasitic capacitance, the emitter node varactors provided frequency coarse tuning through digital input signals, the frequency doubler upconverted the 30 GHz
6.2. CONCLUSION

Table 6.1: Comparison of 30 GHz VCOs

<table>
<thead>
<tr>
<th>Reference</th>
<th>[25]</th>
<th>[26]</th>
<th>[27]</th>
<th>This work</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18 µm CMOS</td>
<td>0.35 µm SiGe BiCMOS</td>
<td>0.18 µm SiGe BiCMOS</td>
<td>130 nm SiGe BiCMOS</td>
<td>130 nm SiGe BiCMOS</td>
</tr>
<tr>
<td>( f_{osc} ) (GHz)</td>
<td>30</td>
<td>30.4</td>
<td>37</td>
<td>30.9</td>
<td>27.2</td>
</tr>
<tr>
<td>TR (%)</td>
<td>1.3</td>
<td>2.6</td>
<td>6.2</td>
<td>16.8</td>
<td>15.2</td>
</tr>
<tr>
<td>PN (dBc/Hz) @ 1MHz</td>
<td>-104.1</td>
<td>-97.5</td>
<td>-102</td>
<td>-101.4</td>
<td>-105.5</td>
</tr>
<tr>
<td>( P_{DC} ) (mW)</td>
<td>2.3</td>
<td>16.8</td>
<td>2.7</td>
<td>40.2</td>
<td>40.2</td>
</tr>
<tr>
<td>( P_{out} ) (dBm)</td>
<td>-14</td>
<td>-3.8</td>
<td>N/A</td>
<td>4</td>
<td>4.4</td>
</tr>
<tr>
<td>( FOM ) (dBc/Hz)</td>
<td>-190.3</td>
<td>-174.9</td>
<td>-185.8</td>
<td>-175.1</td>
<td>-178.2</td>
</tr>
<tr>
<td>( FOM_T ) (dBc/Hz)</td>
<td>-172.6</td>
<td>-163.2</td>
<td>-181.7</td>
<td>-179.6</td>
<td>-181.8</td>
</tr>
<tr>
<td>( FOM_{TP} ) (dBc/Hz)</td>
<td>-158.6</td>
<td>-159.4</td>
<td>N/A</td>
<td>-183.6</td>
<td>-186.2</td>
</tr>
</tbody>
</table>

*aExclude output buffer if presented*

fundamental VCO output to 60 GHz signals and provided desirable output buffering, and the Colpitts VCO topology provided top tier high frequency performance and high output power. Built on the previous research in the area, this novel VID-based Colpitts VCO design was successfully designed and implemented as an alternative VCO topology for the IEEE 802.11ad applications.

Much experience has been gained throughout the project, and insight has been gained into many ways this VCO design could be improved. For a successful commercialization ready VCO into IEEE 802.11ad compliant radio systems, many of the future works suggested in 6.3 of this VCO topology need to be completed first.

The fundamental goal that need to be reached for this project to be considered
6.2. CONCLUSION

Table 6.2: Comparison of 60 GHz VCOs

<table>
<thead>
<tr>
<th>Reference</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
<th>[6]</th>
<th>[16]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>65 nm CMOS</td>
<td>130 nm SiGe BiCMOS</td>
<td>90 nm CMOS</td>
<td>90 nm CMOS</td>
<td>0.35 µm SiGe</td>
<td>90 nm CMOS</td>
<td>130 nm SiGe BiCMOS</td>
</tr>
<tr>
<td>Topology</td>
<td>VID-based cross-coupled</td>
<td>Diff. Colpitts</td>
<td>Cross-coupled</td>
<td>Cross-coupled</td>
<td>VID-based cross-coupled</td>
<td>VID-based diff. Colpitts</td>
<td></td>
</tr>
<tr>
<td>$f_{osc}$ (GHz)</td>
<td>63.2</td>
<td>62.3</td>
<td>58.8</td>
<td>64</td>
<td>60</td>
<td>56.8</td>
<td>61.7</td>
</tr>
<tr>
<td>$TR$ (%)</td>
<td>8.8</td>
<td>4.5</td>
<td>4.3</td>
<td>8.8</td>
<td>20</td>
<td>16</td>
<td>17.7</td>
</tr>
<tr>
<td>$PN$ (dBc/Hz)</td>
<td>-107 @ 10 MHz</td>
<td>-106 @ 1 MHz</td>
<td>-100 @ 1 MHz</td>
<td>-95 @ 1 MHz</td>
<td>-89.5 @ 1 MHz</td>
<td>-118.8 @ 10 MHz</td>
<td>-115.7 @ 10 MHz</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)$^a$</td>
<td>15.5</td>
<td>78.6</td>
<td>20</td>
<td>3.2</td>
<td>217</td>
<td>8.7</td>
<td>45.5</td>
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<tr>
<td>$P_{out}$ (dBm)</td>
<td>4</td>
<td>11.2</td>
<td>-15</td>
<td>-14</td>
<td>-35</td>
<td>-6.6</td>
<td>3</td>
</tr>
<tr>
<td>$FOM$ (dBc/Hz)</td>
<td>-171.11</td>
<td>-182.9</td>
<td>-182.4</td>
<td>-186.1</td>
<td>-152.2</td>
<td>-184.4</td>
<td>-174.9</td>
</tr>
<tr>
<td>$FOM_T$ (dBc/Hz)</td>
<td>-170</td>
<td>-176</td>
<td>-175.1</td>
<td>-185</td>
<td>-158.2</td>
<td>-188.5</td>
<td>-179.9</td>
</tr>
<tr>
<td>$FOM_{TP}$ (dBc/Hz)</td>
<td>-174</td>
<td>-187.2</td>
<td>-160.1</td>
<td>-171</td>
<td>-123.2</td>
<td>-181.9</td>
<td>-182.8</td>
</tr>
</tbody>
</table>

$^a$Exclude output buffer if presented

successful was to provide an alternative VCO design to address the current VCO TR limitation in IEEE 802.11ad applications. This goal has been achieved firmly. The ultimate hope for this project was to create a refined and robust VCO topology suitable to the successful commercialization of the IEEE 802.11ad radio systems. This goal is a continuous work in progress as the industrial partner became interested and invested more financial support into the measurement and improvement of this novel VCO topology. All in all, this was a successful project.
6.3 Future Work

This section discusses possible additions and improvement to the novel VCO topology presented in this thesis report. Opportunities for expanding the functionality certainly exist. A few foreseeable extensions of this VID-based Colpitts topology beyond the scope of this thesis are also discussed.

An improvement to the phase noise performance must be implemented before this VID-based Colpitts topology can be used to replace the conventional Colpitts-Clapp topology. Although has superior TR coverage, the measurements in section 5.3 had revealed that the current VID-based VCO design has inferior phase noise performance compared to the conventional Colpitts-Clapp VCO design. Possible remedies for this include implementing differential control for frequency fine tune, modifying the MOSFET geometry to reduce the rate of change of $R_{eq}$, changing the transformer geometry to obtain higher Q and lower coupling coefficient, and optimizing the HBT dimensions to increase tank voltage swing.

A single-ended controlled line (for $V_{tune}$) was implemented in this project in order to ease the measurement. However, the insufficient amount of EM shielding in the microwave labs at Queen’s University and the industrial partner make it difficult to make accurate measurements (especially on phase noise). The single-ended control line lacks the ability to reject common-mode noise coupled from the ambient noise, hence causes control line pushing. Instead of single-ended control line, differential control lines should be implemented in the future, the phase noise measurement results are expected to be improved because of its common-mode rejection ability.

The MOSFET in the VID plays a vital rule in that it determines the variation of $R_{eq}$ in Figure 2.7, and it can significantly changes the rate of change of $L_{eq}$ and $Z_{in}$ of
6.3. FUTURE WORK

the VID, hence change the VCO gain. By modifying the MOSFET in the following way, the phase noise level of the VID-based VCO can be reduced.

In the triode region of n-type FETs, the $I_{DS}$-$v_{DS}$ characteristic can be described by

$$i_D = k'_n \frac{W}{L} \left[ (V_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right], \quad (6.1)$$

where $k'_n$ is the process transconductance parameter, $V_t$ is the cutoff voltage of the MOSFET, and $V_{GS}$ is the gate voltage that we control (which is equivalent to $V_{tune}$). Assuming $v_{DS}$ is small, the terminal resistance between the drain and the source, $R_{DS}$, can be expressed by

$$R_{DS} = \frac{v_{DS}}{i_D} = \frac{v_{DS}}{k'_n \frac{W}{L} (V_{GS} - V_t) v_{DS}} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_t)}, \quad (6.2)$$

which tells that $R_{eq}$ is a function of $V_{GS}$, or $V_{tune}$. Now, since the length of the channel ($L$) and the process transconductance parameter ($k'_n$) are fixed by the process, one can reduce the rate of change of $R_{eq}$ by enlarging the channel width, $W$. This is how changing the geometry of the MOSFET can change the characteristics of the VID as an entity, and this change may be very beneficial to reduce phase noise.

The transformer in the current VID design employs metal layer 5 and 6. In the future the Q of the transformer can be further increased by stacking more layers in parallel, and connecting each layer by more vias, hence to enlarge the conductor cross-section and reduce the number of squares for easier electron migration. Also, the gap between the primary and the secondary windings can be further enlarged to reduce the transformer coupling coefficient ($k$), hence to reduce the rate of change of $L_{eq}$, and further reduce the VCO gain.
6.3. FUTURE WORK

The geometry and bias condition for the switching HBTs in the VCO core can be refined to produce higher gain, hence larger tank swing in the base node. This possibility is already hinted by Figure 3.12. Also, right now this VCO draws 20 mA current through these 2 HBTs, which is slightly overkill for a VCO application. By refining the HBT geometry, the bias current can be reduced.

Last but not least, more measurements should be done to the existing VCOs in the near future. Not only repeating the frequency tuning, phase noise, and output power measurement in a better shielded environment, but also the die to die performance variation can also be tested throughout the entire wafer, so that the reliability of this VID-based VCO design can be verified.

Also, there are 2 variants of the VID implementation that can be investigated in the future. One is that instead of operating the VID as fine tune element in the base node, it can also be implemented in the emitter to replace those varactors for frequency coarse tuning. This requires an opposite design direction as if using the VID in the base node for fine tuning, which the $k$ of the transformer should be increased as much as possible and the width of the MOSFET in the VID should be reduced. Both of those adjustments are simpler to complete than the opposite, proving that VID may be better suited for coarse frequency tuning. Another benefit by placing the VID in the emitter to perform coarse tuning is that since the size of the VID will be greatly reduced due to the allowance of higher $k$, hence closer winding separations and narrower trace widths can be employed, the size of the circuit can potentially be reduced, hence increase the integration and reduce the fabrication cost. Another variant is to investigate instead of varying the equivalent resistance of the VID, how will the VCO behave if its capacitance $C_v$ in the VID is varied. The capacitance
is shown as $C_v$ in Figure 2.6. This may also create an attractive alternative to the current VID design. Because the resistance in the VID does not need to change, it can be designed low to improve the Q factor of the VID, which can contribute to reducing the phase noise of the VCO as a whole.
Bibliography


Appendix A

Detailed Q-Factor Derivation for VID

The detailed Q-factor derivation is presented in this section, as a complement to 2.5.

A.1 Description

Based on Figure 2.6, a general lumped-element model for the VID is shown in Figure A.1, where $R_P$ and $R_S$ are primary and secondary winding parasitic resistances respectively. The impedance looking into the equivalent circuit connects to the secondary winding, $Z_S$ can be formulated as

$$Z_S = \frac{R_S + R_v + jC_v\omega R_S R_v}{1 + j\omega C_v R_v}. \quad (A.1)$$

Figure A.1: The idealized tank oscillation waveforms
A.1. DESCRIPTION

Under the assumption that $R_S$ is much smaller than the variable $R_v$, A.1 can be simplified to

$$Z_S = \frac{R_v}{1 + j\omega C_v R_v}.$$  \hspace{1cm} (A.2)

Knowing $Z_S$, the input impedance of this VID, $Z_{in}$ can be formulated as

$$Z_{in} = R_P + j\omega L_P + \frac{\omega k^2 L_P L_S}{j\omega L_S + Z_S}.$$  \hspace{1cm} (A.3)

The Q-factor of the VID can be calculated as the ratio of the imaginary part of $Z_{in}$ (stored energy) versus the real part of $Z_{in}$ (energy loss),

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} = \frac{\omega R_v^2 L_P (1 - \omega^2 C_v L_s) + \omega^2 L_P L_s^2 (1 - k^2) + \omega^2 k^2 R_v^2 C_v L_P L_s (1 - \omega^2 L_2 C_v)}{R_P R_v (1 - \omega^2 C_v L_s)^2 + \omega^2 L_s (k^2 L_P R_v - R_1 L_s)}.$$  \hspace{1cm} (A.4)

which matches to (2.21).
Appendix B

Detailed Layout Component Views

The closed-up views of the key components on the 3 VCOs are shown in this section. The colors on all layout screen shots were inverted to ease printing. For the naming conventions used in this section, please refer to Figure 3.1, 4.1, and 5.1 for the 3 VCOs correspondingly.

B.1 Detailed Component Layouts for the 30 GHz VID-based Colpitts VCO

Figure B.1: Closed-up view for L1
B.1. DETAILED COMPONENT LAYOUTS FOR THE 30 GHZ VID-BASED COLPITTS VCO

Figure B.2: Closed-up view for C1

Figure B.3: Closed-up view for the resistor bank for $R_{tail}$
B.1. DETAILED COMPONENT LAYOUTS FOR THE 30 GHZ VID-BASED COLPITTS VCO

Figure B.4: Closed-up view for the MOSFET $M_1$ in the VID

Figure B.5: Closed-up view for the output CC buffer $Q2$
B.2 Detailed Component Layouts for the 60 GHz VID-based Colpitts VCO Chain

Figure B.6: Closed-up view for the FD frequency select inductor $L_5$
B.2. DETAILED COMPONENT LAYOUTS FOR THE 60 GHZ VID-BASED COLPITTS VCO CHAIN

Figure B.7: Closed-up view for the HBT pair $Q_4$ in the frequency doubler

Figure B.8: Closed-up view for the resistor bank for $R_3$ in the frequency doubler
B.3 Detailed Component Layouts for the 30 GHz Colpitts-Clapp VCO

Figure B.9: Closed-up view for the base varactor $C_{\text{tune}}$

Figure B.10: Closed-up view for the base inductor $L_{\text{base}}$
Figure B.11: Closed-up view for the core of the 30 GHz Colpitts-Clapp VCO
Appendix C

Limitations in Current VCO Phase Noise Simulation

The poor accuracy and its reasons are discussed briefly in this section.

C.1 Description

Phase noise is a very important performance parameter of any VCO. Together with other parameters such as the oscillation frequency, the TR, and the output power, the applications for a particular VCO is determined. However, using EDA tools to accurately simulating phase noise of VCOs has been quite a challenge even today. The reasons are briefly discussed in this section.

Regardless of the VCO topology, the voltage swing in the tank is always designed to be large. This enables us to accurately apply large signal models to the switching transistors in a VCO. In such condition, the tail current $I_{tail}$ of the VCO flows in and out of the tank developing the tank voltage swing $V_{tank}$ with the tank parallel resistance $R_p$ at resonance. Due to the selectivity of the LC structure in the tank, only the fundamental component will be preserved in the tank, the current fundamental
component under the large signal condition can be written as $\frac{\pi I_{\text{tail}}}{4}$, hence producing tank voltage swing $\frac{\pi I_{\text{tail}} R_p}{4}$. The waveforms can be visualized in Figure C.1, where $i_N$ is the noise current in the tank.

The tank is affected by noise whenever the tank voltage makes a zero-crossing [9]. In other words, the noise from various sources will be apparent to and amplified by the transistors when they are in quiescent bias point. This is concluded by the Leeson noise model in [13] and it’s employed by most of the phase noise simulations. However, this model does not include the effects of spectrum folding in the VCO tank, which can fold in the noise occurring at higher harmonics and DC into the oscillation, all these are made worse by the limited accuracy of the nonlinearity of transistor models, eventually let the simulator underestimate the effect of phase noise on the VCO performance. Therefore, up until today, phase noise simulations in various EDA tools mostly provide as a general guideline to the VCO designers, rather than some thing to be fully relied on.