A NEW DC UPS FOR DC POWER DISTRIBUTION SYSTEM IN DATA CENTER

by

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Abstract

In recent years, the 380V DC and 48V DC distribution systems have been extensively studied for the latest data centers. It is widely believed that the 380V DC system is a very promising candidate because of its lower cable cost compared to the 48V DC system. However, previous studies have not adequately addressed the low reliability issue with the 380V DC systems due to large amount of series connected batteries. In this thesis, a quantitative comparison for the two systems has been presented in terms of efficiency, reliability and cost. A new multi-port DC UPS with both high voltage output and low voltage output is proposed. When utility ac is available, it delivers power to the load through its high voltage output and charges the battery through its low voltage output. When utility ac is off, it boosts the low battery voltage and delivers power to the load form the battery. Thus, the advantages of both systems are combined and the disadvantages of them are avoided. High efficiency is also achieved as only one converter is working in either situation. Details about the design and analysis of the new UPS are presented.

For the main AC-DC part of the new UPS, a novel bridgeless three-level single-stage AC-DC converter is proposed. It eliminates the auxiliary circuit for balancing the capacitor voltages and the two bridge rectifier diodes in previous topology. Zero voltage switching, high power factor, and low component stresses are achieved with this topology. Compared to previous topologies, the proposed converter has a lower cost, higher reliability, and higher efficiency. The steady state operation of the converter is analyzed and a decoupled model is proposed for the converter.

For the battery side converter as a part of the new UPS, a ZVS bidirectional DC-DC converter based on self-sustained oscillation control is proposed. Frequency control is used to ensure the ZVS operation of all four switches and phase shift control is employed to regulate the converter output power. Detailed analysis of the steady state operation and design of the converter are presented.

Theoretical, simulation, and experimental results are presented to verify the effectiveness of the proposed concepts.
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Table of Contents

Abstract ................................................................................................................................. ii
Acknowledgements ............................................................................................................... iii
List of Tables ....................................................................................................................... ix
List of Abbreviations ........................................................................................................... x
Chapter 1 Introduction ........................................................................................................ 1
  1.1 Power Distribution Systems for Data Centers ............................................................. 1
    1.1.1 AC Distribution System ...................................................................................... 2
    1.1.2 DC Distribution System .................................................................................... 3
  1.2 Comparison of the 48V DC and 380V DC Distribution System ....................................... 5
    1.2.1 Efficiency Comparison ...................................................................................... 5
      1.2.1.1 DC UPS Efficiency .................................................................................... 5
      1.2.1.2 PSU Efficiency ......................................................................................... 6
      1.2.1.3 Cable Loss .................................................................................................. 8
      1.2.1.4 Overall Efficiency ..................................................................................... 12
    1.2.2 Reliability Comparison ....................................................................................... 13
    1.2.3 Cost Comparison ............................................................................................... 16
      1.2.3.1 Power Converter Cost ............................................................................... 16
      1.2.3.2 Cable Cost ................................................................................................. 16
      1.2.3.3 Battery Cost .............................................................................................. 17
      1.2.3.4 Overall Cost ............................................................................................. 17
    1.2.4 Proposed DC UPS ............................................................................................ 18
  1.3 Thesis Objective ......................................................................................................... 20
  1.4 Thesis Outline ............................................................................................................ 22
Chapter 2 Single-Stage AC-DC Converter ........................................................................ 23
  2.1 AC-DC Converter in DC distribution system ............................................................ 23
  2.2 Power Factor Correction ............................................................................................ 23
    2.2.1 Passive PFC ..................................................................................................... 24
    2.2.2 Active PFC ...................................................................................................... 25
      2.2.2.1 Two-Stage AC-DC Converter .................................................................. 27
      2.2.2.2 Single Stage AC-DC Converter ............................................................... 27
  2.3 Review of Single Stage AC-DC Converter .................................................................... 28
    2.3.1 Based on flyback/forward converter .................................................................. 28
2.3.2 Based on Half Bridge................................................................. 29
2.3.3 Based on Full Bridge Converter.................................................. 30
2.3.4 Based on Resonant Converter....................................................... 33
2.3.5 Based on Three level converter....................................................... 34
2.4 Summary of Literature Review on Single-Stage AC-DC converter............. 36
Chapter 3 Bridgeless Three-Level Resonant Single-Stage AC-DC Converter without Auxiliary Circuit .................................... 38
3.1 Introduction...................................................................................... 38
3.2 Bridgeless AC-DC Converters.......................................................... 38
3.3 Principle Operation and Control Method of Proposed Converter............. 41
  3.3.1 Principle Operation.................................................................... 41
  3.3.2 Discharge Patterns of the Boost Inductor...................................... 46
  3.3.3 Controller for the Proposed Converter........................................... 47
3.4 Steady State Analysis...................................................................... 48
  3.4.1 Rectifying Stage........................................................................ 48
  3.4.2 DC Bus Capacitor Selection......................................................... 53
  3.4.3 DC-DC Resonant Converter Stage................................................ 58
  3.4.4 Decoupled Model of the Proposed Converter............................... 61
3.5 Simulation Results........................................................................ 66
3.6 Experimental Results..................................................................... 72
Chapter 4 ZVS Bidirectional DC-DC converter ...................................... 76
  4.1 Introduction...................................................................................... 76
  4.2 Proposed Battery Side Converter.................................................... 76
    4.2.1 Battery Charging Mode............................................................... 77
    4.2.2 Battery Discharging Mode.......................................................... 83
  4.3 Simulation Results........................................................................ 87
    4.3.1 Battery Charging Mode............................................................... 88
    4.3.2 Battery Discharging Mode.......................................................... 90
Chapter 5 Summary and Conclusion ...................................................... 93
  5.1 Summary of Contributions............................................................... 93
  5.2 Conclusion....................................................................................... 94
  5.3 Suggested Future work ................................................................. 95
References............................................................................................. 96
Appendix A PSIM Simulation Schematics............................................... 107
Appendix B PCB Schematic and Layout for the Proposed Single-Stage AC-DC Converter.................................................. 109
List of Figures

Figure 1.1. Traditional AC Distribution System .............................................................. 3
Figure 1.2. Delta Conversion Online UPS ........................................................................... 3
Figure 1.3. 48V DC Distribution System ........................................................................... 4
Figure 1.4. 380V DC Distribution System ........................................................................ 4
Figure 1.5. Efficiency curve for an isolated 6 kW 48V DC rectifier (Emersion Network Power) ............... 6
Figure 1.6. Efficiency curve for an isolated 15 kW 380V DC rectifier (Emersion Network Power) .......... 6
Figure 1.7. A Sine Amplitude Converter™ ...................................................................... 7
Figure 1.8. The efficiency curve of a 300W PSU in 48V DC system (Vicor) ......................... 7
Figure 1.9. The efficiency curve of a 300W PSU in 380V DC system (Vicor) ....................... 8
Figure 1.10. Server rack cabinet diagram ...................................................................... 9
Figure 1.11. Power density per rack from 2006 to 2014[17]................................................... 9
Figure 1.12. A typical floor layout for a 300 kW datacenter ............................................. 10
Figure 1.13. Block diagram of the proposed multi-port DC UPS ....................................... 19
Figure 1.14. Proposed DC UPS based on single-stage AC-DC converter and series-parallel resonant circuit .................................................................................................................................................. 20
Figure 2.1. Passive PFC circuit ...................................................................................... 25
Figure 2.2. CCM PFC average current control circuit ...................................................... 26
Figure 2.3. DCM PFC control circuit .............................................................................. 27
Figure 2.4. Two-Stage AC-DC converter ....................................................................... 28
Figure 2.5. Single-Stage AC-DC converter proposed by M.T.Madigan [47] ......................... 29
Figure 2.6. A ZVZCS single-stage half-bridge PFC converter [54] ..................................... 30
Figure 2.7. Asymmetrical PWM full-bridge AC-DC converter with reduced dc bus voltage [61] .... 31
Figure 2.8. Magnetic switch phase shift full-bridge AC-DC converter with reduced dc bus voltage [63] 32
Figure 2.9. A Simple current-fed AC-DC converter [65-66] ............................................. 33
Figure 2.10. Parallel resonant AC-DC converter [69] .................................................... 33
Figure 2.11. Three-level AC-DC converter with magnetic switch [82] ............................... 35
Figure 2.12. Three-level resonant AC-DC converter [86] .............................................. 36
Figure 3.1. Traditional bridgeless AC-DC converter ....................................................... 39
Figure 3.2. Totem-pole bridgeless AC-DC converter ...................................................... 40
Figure 3.3. Proposed bridgeless three-level resonant AC-DC converter ......................... 40
Figure 3.4. Switching sequence of one switching cycle for the proposed converter in Figure 3.3 .... 41
Figure 3.5 Equivalent circuit of each mode for the proposed converter ........................... 44
Figure 3.6. Three discharge patterns for the boost inductor ................................................................. 46
Figure 3.7. Controller of the proposed converter .................................................................................. 47
Figure 3.8. Critical value of $L_{ab}$ with 400V dc bus voltage and full load (1kW) .................................. 50
Figure 3.9. Critical value of $L_{ab}$ with 800V dc bus voltage and full load (1kW) ................................. 50
Figure 3.10. The input current during one half cycle of the input ac voltage ........................................ 52
Figure 3.11. DC bus capacitor voltages and the input ac voltage .......................................................... 54
Figure 3.12. Peak to peak voltage difference between two dc bus capacitors ($V_{bus_{avg}} = 400$V and $f_s = 200$ kHz) ........................................................................................................................................... 57
Figure 3.13. Peak to peak voltage difference between two dc bus capacitors ($V_{bus_{avg}} = 800$V and $f_s = 200$ kHz) ........................................................................................................................................... 57
Figure 3.14 Model of Resonant Converter with $V_{ab}$ and $i_s$ ................................................................ 57
Figure 3.15. Output voltage for different $Q$ and $K$ ($V_{bus} = 400$V, $D = 0.5$, $P_{out} = 1$kW). .............. 60
Figure 3.16. Decoupled model of the proposed converter ......................................................................... 62
Figure 3.17. Power delivered by the Rectifier ($P(R_{eq})$) at $V_{in} = 110$Vrms, $V_{bus} = 400$V ................. 63
Figure 3.18. Power delivered by the Rectifier ($P(R_{eq})$) at $V_{in} = 220$Vrms, $V_{bus} = 800$V ................. 63
Figure 3.19. Operating area of the proposed converter when $D = 0.48$, $V_{bus} = 400$V ......................... 64
Figure 3.20. Operating area of the proposed converter when $D = 0.17$, $V_{bus} = 800$V ................. 65
Figure 3.21. Operating points for the proposed converter with the chosen parameters at $V_{in} = 110$Vrms. 65
Figure 3.22 Power factor with $V_{in} = 110$Vrms and $V_{in} = 220$Vrms under different load conditions (simulation) .................................................................................................................................... 67
Figure 3.23. 110Vrms input voltage ($v_{in}$), filtered input current ($I_{emc}$) and its harmonics with 50% load... 68
Figure 3.24. 220Vrms input voltage ($v_{in}$) and filtered input current ($I_{emc}$) and its harmonics with 50% load ................................................................................................................................................. 68
Figure 3.25. $V_{cb1}$, $V_{cb2}$ and their difference under different load condition at $V_{bus} = 400$V ............. 69
Figure 3.26. $V_{cb1}$, $V_{cb2}$ and their difference under different load condition at $V_{bus} = 800$V ............. 69
Figure 3.27. ZVS operation illustration of upper switches ($S_2$) and bottom switch ($S_3$) with $V_{bus} = 400$V .70
Figure 3.28. ZVS operation illustration of upper switches ($S_2$) and bottom switch ($S_3$) with $V_{bus} = 400$V .71
Figure 3.29. Resonant current $i_s$ and resonant circuit voltage $v_{ab}$ when $V_{bus} = 400$V ...................... 71
Figure 3.30. Resonant current $i_s$ and resonant circuit voltage $v_{ab}$ when $V_{bus} = 800$V .................. 72
Figure 3.31. (a) input voltage ($v_{in}$) and filtered input current ($i_{emc}$), (b) $V_{CB1}$ and $V_{CB2}$ (DC coupling).... 74
Figure 3.32. $V_{CB1}$ and $V_{CB2}$ (AC coupling) and filtered input current when $V_{bus} = 140$V at (a) $D = 0.3$, (b) $D = 0.18$ ........................................................................................................................................................... 74
Figure 3.33. Resonant voltage ($V_{ab}$) and resonant current ($i_s$) at (a) high duty cycle, (b) low duty cycle... 75
Figure 3.34. gate voltage ($v_{gs}$) and switch voltage ($v_{ds}$) to illustrate ZVS for (a) $S_2$, (b) $S_1$ .................................................. 75
Figure 4.1. Proposed battery side converter ................................................................................................................................. 77
Figure 4.2 Battery side converter in battery charging mode ........................................................................................................ 78
Figure 4.3. Equivalent circuit of the battery side converter in battery charging mode ................................................................. 78
Figure 4.4. Operations of the battery side converter in charging mode .......................................................................................... 79
Figure 4.5. resonant current ($I_s$) with different $\theta_a$ at $f_s = 220$kHz for (a) $V'_{cp} = 150$V (b) $V''_{cp} = 200$V ........... 82
Figure 4.6. battery charge current ($I_b$) with different $\theta_a$ at $f_s = 220$kHz for (a) $V'_{cp} = 150$V (b) $V''_{cp} = 200$V ....................................................................................................................................................... 82
Figure 4.7. Controller of the battery side converter in battery charging mode .............................................................. 83
Figure 4.8. Battery side converter in discharging mode .................................................................................................................. 84
Figure 4.9. Operations of the battery side converter in the battery discharge mode ................................................................. 85
Figure 4.10. Equivalent circuit of the battery side converter in battery discharging mode .................................................. 85
Figure 4.11. Controller of the battery side converter in battery discharging mode ................................................................. 87
Figure 4.12. battery current $I_b$ and $\theta_a$ when $I_b$ is regulated at 9A. ................................................................. 89
Figure 4.13. battery current $I_b$ and $\theta_a$ when $I_b$ is regulated at 5A. ................................................................. 89
Figure 4.14. resonant current $I_{s2}$ and voltage $v_{ab2}$ when $I_b$ is at (a) 9A, (b) 5A ................................................................. 90
Figure 4.15. Output voltage of battery side converter and the control variable $\theta_b$ at full load .................................................. 91
Figure 4.16. Output voltage of battery side converter and the control variable $\theta_b$ at 20% load ................................................. 91
Figure 4.17. resonant current $-I_{s2}$ and voltage $v_{ab2}$ when the output power is at (a) 20% load, (b) full load ......................................................................................................................................................... 92
List of Tables

Table 1.1. Cable selection for a 300kW 48V DC and 380V DC power distribution system.......................... 11
Table 1.2. Overall efficiency of 48V DC and 380V DC distribution systems............................................. 12
Table 1.3. Failure Modes for different types of lead-acid battery [].......................................................... 14
Table 1.4. System reliability for 48V DC and 380V DC distribution systems with different $k$ and $n$........ 15
Table 1.5. Overall cost of 48V DC and 380V DC power distribution system.................................................. 18
Table 1.6. Comparison between 48V DC distribution system, 380V DC distribution system and the distribution system with the proposed UPS. .................................................................................................................. 19
Table 2.1 Comparison of voltage-fed and current-fed single-stage AC-DC converter................................. 36
Table 3.1. Circuit component selection for the proposed converter. ................................................................. 66
Table 4.1. Component selected for the simulation of battery side converter............................................... 88
List of Abbreviations

**Acronyms:**

AC: Alternating Current
CCM: Continuous Conduction Mode
CM: Common Mode
CRM: Critical Conduction Mode
DC: Direct Current
DCM: Discontinuous Conduction Mode
EMC: Electromagnetic compatibility
EMI: Electromagnetic interference
IT: Information Technology
MOSFET: Metal-oxide-semiconductor field-effect transistor
PDU: Power Distribution Unit
PF: Power Factor
PFC: Power Factor Correction
PSU: Power Supply Unit
PV: photovoltaic
PVC: Polyvinyl Chloride
PWM: Pulse Width Modulation
SPEIC: single-ended primary-inductor converter
THD: Total Harmonic Current
UPS: Uninterrupted Power Supply
VR: Voltage Regulator
VRLA: valve-regulated lead-acid battery
ZVS: Zero Voltage Switching
ZCS: Zero Current Switching

Symbols:

1. Circuit Parameters

\( C_{b1} \): DC bus capacitor 1

\( C_{b2} \): DC bus capacitor 2

\( C_{ds} \): Drain source capacitor

\( C_{s1} \): Series resonant capacitor of main AC-DC converter

\( C_{s2} \): Series resonant capacitor of battery side converter

\( C_{p1} \): Parallel resonant capacitor of main AC-DC converter

\( C_{p2} \): Parallel resonant capacitor of battery side converter

\( C_f \): Output filter capacitor at output side

\( C_{bf} \): Output filter capacitor at battery side

\( D_1 \): Rectifier diode 1

\( D_2 \): Rectifier diode 2

\( D_{c1} \): Clamping diode 1

\( D_{c2} \): Clamping diode 2

\( L_{in} \): Boost inductor

\( L_{f1} \): Output filter inductor at output side

\( L_{f2} \): Output filter inductor at battery side

\( L_{s1} \): Series resonant inductor of main AC-DC converter

\( L_{s2} \): Series resonant inductor of battery side converter

\( N_1 \): Number of turns of the primary winding of the isolation transformer

\( N_2 \): Number of turns of the secondary winding of the isolation transformer

\( N_3 \): Number of turns of the tertiary winding of the isolation transformer
2. Variable Used in Analysis

a. For the analysis of data center power distribution system:

- $C_{\text{converter, 48}}$: Power converter cost of the 380V DC system
- $C_{\text{cable, 48}}$: Cable cost (the 380V DC system)
- $C_{\text{battery, 48}}$: Battery cost (the 380V DC system)
- $C_{\text{converter, 380}}$: Power converter (the 380V DC system)
- $C_{\text{cable, 380}}$: Cable cost (the 380V DC system)
- $C_{\text{battery, 380}}$: Battery cost (the 380V DC system)
- $I_{\text{rated, total}}$: Rated current of the data center
- $I_{\text{rack, 380}}$: Current form PDU to racks of (the 380V DC system)
- $I_{\text{PDU, 380}}$: Current form UPS to PDU (the 380V DC system)
- $I_{\text{rack, 48}}$: Current form PDU to racks (the 48V DC system)
- $I_{\text{PDU, 48}}$: Current form UPS to PDU (the 48V DC system)
- $R_{\text{PDU, 48}}$: Cable resistance form UPS to PDU (the 48V DC system)
- $R_{\text{rack, 48}}$: Cable resistance form PDU to racks (the 48V DC system)
- $R_{\text{PDU, 380}}$: Cable resistance form UPS to PDU (the 380V DC system)
- $R_{\text{rack, 380}}$: Cable resistance form PDU to racks (the 380V DC system)
- $P_{L, total, 380}$: Total cable loss (the 380V DC system)
- $P_{L, PDU, 380}$: Cable loss form UPS to PDU (the 380V DC system)
- $P_{L, rack, 380}$: Cable loss form PDU to racks (the 380V DC system)
- $P_{L, PDU, 48}$: Cable loss form UPS to PDU (the 48V DC system)
- $P_{L, rack, 48}$: Cable loss form PDU to racks (the 48V DC system)
- $P_{L, total, 48}$: Total cable loss (the 48V DC system)
- $P_{\text{rated}}$: Rated power of the data center
- $r$: statistic reliability of a single VRLA battery cell
Efficiency of the cables

b. For the analysis of the proposed converters:

\( C_{\text{eff, bus}} \): Effective dc bus capacitance

\( D \): Duty Cycle

\( \Delta E_{cb1} \): Change of the stored energy in \( C_{b1} \)

\( \Delta E_{cb2} \): Change of the stored energy in \( C_{b2} \)

\( K \): ratio of \( C_p \) and \( C_s \)

\( K_2 \): ratio of \( C_{p2} \) and \( C_{s2} \)

\( f_{\text{line}} \): line frequency of the input ac voltage

\( f_s \): Switching frequency of the main AC-DC converter

\( f_{r} \): Resonant frequency of the main AC-DC converter

\( f_{s2} \): Switching frequency of battery side converter in battery charging mode

\( f_{r2} \): Resonant frequency of the main AC-DC converter

\( f_{s3} \): Switching frequency of battery side converter in battery discharging mode

\( I_{\text{rms}} \): RMS value of the current

\( I_{\text{rms}, 1} \): fundamental RMS value of the current

\( I_{\text{rms}, n} \): Harmonic RMS value of the current

\( i_b \): Battery charge current

\( I_b \): Peak value of \( i_b \)

\( i_{\text{Lin}} \): The boost inductor current

\( I_{\text{Lin, peak}} \): Peak value of \( i_{\text{Lin}} \)

\( d_1 \): fraction of the switching period during which \( i_{\text{Lin}} \) decreases through one of \( C_{b1} \) and \( C_{b2} \)

\( d_2 \): fraction of the switching period during which \( i_{\text{Lin}} \) decreases through \( C_{b1} \) and \( C_{b2} \)

\( i_{\text{Lin(ave)}} \): The average value of the boost inductor current
$i_{Dc2,avg}$: Average value of the current go through $D_{c2}$

$i_i$: Resonant current of the main AC-DC converter

$I_i$: Peak value of $i_i$

$i_{s2}$: Resonant current of the battery side converter

$I_{s2}$: Peak value of $i_{s2}$

$K_d$: Ration of the fundamental RMS current and total RMS current

$\phi$: Phase difference between voltage and current

$Q_{cb1}$: Charges stored in $C_{b1}$

$Q_{cb1}$: Charges stored in $C_{b1}$

$\Delta Q_1$: Changes of the charge stored in $C_{b1}$

$\Delta Q_2$: Changes of the charge stored in $C_{b2}$

$T_s$: switching period

$L_{eq}$: equivalent inductance of the resonant tank in the battery side converter

$P_{in}$: Input power of the main AC-DC converter

$P_{out}$: Output power of the main AC-DC converter

$P_b$: power transferred by the battery side converter

$Q_r$: Quality factor of the main AC-DC converter

$Q_{r2}$: Quality factor of the battery side converter

$R_L$: Load resistance

$R_{ac}$: Equivalent ac $R_L$ of the main AC-DC converter

$R_{ac2}$: Equivalent ac $R_L$ of the battery side converter

$R_{eq}$: equivalent resistance of in the decouple model of the main AC-DC converter

$v_{in}$: The input ac voltage

$V_{in,rms}$: RMS value of the input ac voltage

$V_{bus}$: Dc bus voltage
$V_{bus\_ripple}$: Voltage ripple of the dc bus voltage 

$v_{cb1}$: voltage across $C_{b1}$ 

$v_{cb2}$: voltage across $C_{b2}$ 

$V_{cb1}$: The average value of $v_{cb1}$ 

$V_{cb2}$: The average value of $v_{cb2}$ 

$\Delta v$: Peak value of the voltage difference of $C_{b1}$ and $C_{b2}$ 

$V_{diff\_pp}$: Peak-to-peak value of the voltage difference of $C_{b1}$ and $C_{b2}$ 

$v_{cp}$: voltage across the parallel capacitor $C_{p}$ 

$V_{cp}$: Peak value of $v_{cp}$ 

$V_{out}$: Output voltage of the main AC-DC converter 

$V_{out2}$: Output voltage of the battery side converter 

$v_{ab}$: Input voltage to the resonant tank of the main AC-DC converter 

$V_{bat}$: Battery voltage 

$v_a$: Voltage of the leg A in the battery side converter 

$v_b$: Voltage of the leg B in the battery side converter 

$V_{c1}$: Carrier voltage 1 for the battery side converter 

$V_{c2}$: Carrier voltage 2 for the battery side converter 

$v_{ab2}$: Input voltage to the resonant tank of the battery side converter 

$v_{ab2\_f}$: fundamental component of $v_{ab2}$ 

$V_{ab2\_f}$: Peak value of $v_{ab2\_f}$ 

$v'_{cp}$: Input voltage to the battery side converter in battery charging mode 

$V'_{cp}$: Peak value of $v'_{cp}$ 

$v_{ds}$: Drain source voltage 

$v_{gs}$: Gate source voltage 

$\theta$: The phase difference between $i_{s2}$ and $v_a$
$\theta_1$: The phase difference between $i_{s2}$ and $v_b$. 

$\theta_{cr}$: Boundary angle between two different discharge pattern of $i_{Lin}$. 

$\theta_x$: The phase difference between $v_{ad2}$ and $v'_{cp}$. 

$\theta_y$: The phase difference between $i_{s2}$ and $v'_{cp}$. 

Chapter 1

Introduction

Due to the shifting from traditional paper-based systems to digital data information system and the development of online storage and cloud computing. Data centers are becoming the essential to almost every sector of the global economy and the major energy consumers in the world [1-2]. High efficiency and high reliability are the two main requirements for the power distribution systems for these data centers. However, plenty researches and surveys have shown that the traditional AC distribution system for date center has low efficiency and low reliability because of its multiple conversion stages. In recent years, DC distribution systems become promising because of its fewer conversion stages and high compatibility with renewable energy such as photovoltaic system (PV) or wind energy. There are two basic DC distribution systems and they have been discussed for over a decade. The first one is 48V DC distribution system, which has been implemented in the telecommunication industry for a long time. The another one is 380V DC distribution system, which is newer and has been proposed recently.

1.1 Power Distribution Systems for Data Centers

Normally the power distribution system is composed of four major parts:

Part1. Uninterrupted Power Supply (UPS): This part converts the incoming utility AC power to the desired voltage level (either AC or DC). The energy storage system (battery pack, flywheel or fuel cell) included in the UPS starts delivering power to the distribution system when the power outage happens and the utility power is off.

Part2. Power Distribution Unit (PDU): The PDU contains circuit protection devices, wiring, terminal and connectors to deliver power from UPS to different load server racks. Normally an isolation transformer is required in AC Distribution Systems.
Part 3: Power Supply Unit (PSU): The function of PSU is converting the distribution bus voltage level to a lower DC voltage (normally 12V) for the motherboard. In an AC power distribution system, the PSU converter the input AC voltage to 12V DC. While for DC distribution system, the input of PSU is DC instead of AC, the input voltage level is either 48V or 380V depending on the system requirements.

Part 4. Voltage Regulator (VR): The VR converts is on the motherboard. It converts 12V DC to different lower DC voltage such as 5V, 3.3V and 1.1V for the different electrical load on the motherboard such as CPU, cooling fans and memory.

The existing and proposed power distribution systems could be divided into two main categories: AC distribution system and DC distribution system.

1.1.1 AC Distribution System

The architecture of the traditional AC Distribution System is shown in Figure 1.1. This system suffers from double conversion UPS. In this UPS, the AC input is converted to DC voltage which could charge the battery pack in the energy storage system. On the other hand, when the power outage happens, The DC voltage from the battery pack is converted back to the corresponding AC voltage in order to deliver power through the distribution system. Since the entire power flow goes through both the battery charger and the inverter, large amount of power loss happens during these two conversion stages and the overall system efficiency is low [3-4]. A new AC UPS architecture called delta conversion online UPS is proposed and studied in [5-6] as Figure 1.2 shows. This architecture could save power loss by delivering majority power of input to output directly, only the difference power (delta power) between input and output go through the AC/DC and DC/AC converter like double conversion UPS. However, it needs more components and the control method is very complex [5], which makes this architecture costly and less reliable.
1.1.2 DC Distribution System

In order to complete eliminate the losses in the UPS of the AC distribution system, the concept of DC distribution system is proposed for data centers. In this system, no extra rectifier and inverter are required for charging and discharging the battery as the bus voltage is dc. The DC distribution system could be divide into two main categories: high voltage (380V DC) and low voltage (48V DC). Figure 1.3 and Figure 1.4 present the architecture of these two DC distribution system. It could be notice that the dc bus voltage is the only difference between them and the rest of the system is almost same. Both systems have a higher efficiency compare to legacy AC distribution system by eliminating the DC-AC stages in UPS, the AC-DC stage in the PSU and the PDU transformer.
The 48V DC distribution system has been used in telecommunication industry for several decades. However, different from telecommunication facilities, the rack power density in data centers is increasing rapidly in recent years, therefore many data centers have to place energy storage system and power system in separate rooms with long distance to the server racks [7]. Since the cable copper required to transfer same amount of power with 48V DC system is several tens of times when compared with the 380V DC system. The cable copper cost and lost for the 48V DC system significantly increases for data centers [8-9]. In addition, the global trend of copper price is also increasing. The above reasons make the 380V DC system a very promising future choice for data center power distribution systems.

Although the 380V DC system is proven to have a higher efficiency and lower cost for the copper cables, reliability of the power distribution system is also one of the key factors in the design of a data center. The reliability of a tire 4 data center should be higher than 99.99% [10]. However, in the 380V DC system, a large number of battery cells are connected in series to achieve a high voltage. If the battery cells have a high risk of open circuit failure. This will dramatically decrease the reliability of the 380V DC system compared to the 48V DC system.
1.2 Comparison of the 48V DC and 380V DC Distribution System

In the next section, a detail quantitative comparison between the 48V DC system and 380V DC system will be presented by expanding upon previously researches [11]. Three key factors of data center power distribution system: overall efficiency, overall cost and system reliability, will be discussed with a 300 kW data center example. A new DC UPS will also be proposed to combine the advantage of both systems.

1.2.1 Efficiency Comparison

Since the VR and PDU are almost same for both 48V DC and 380V DC distribution systems, the power losses of those parts will not be discussed here. The following comparison is concentrated on the efficiency of the voltage conversion stages in DC UPS and PSU, as well as the power losses in the distribution cables.

1.2.1.1 DC UPS Efficiency

The basic function and architecture of DC UPS in both systems are very similar, it is consisting of a one phase or three phase rectifier, an energy storage system (usually battery cells or fuel cells) and some performance monitoring devices. The DC UPS converts input ac voltage to a regulated 48V DC or 380V DC output voltage. Commercial products for 48V DC UPS are very common in the market since 48V DC system has been used for a long time. Many vendors like Emerson Network Power, ELTELIK, ABB, EATON and Delta Electronics have also developed 380V DC UPS based in the previous 48V DC UPS products.

Most UPS products are designed to be modularized and extendable for easy maintenance and high flexibility. Generally, the rated power for a single module rectifier is from 2 kW to 5 kW. Multiple rectifier modules could be connected in parallel to achieve a higher power capability. Similarly, the energy storage capability could also be increase by connecting more battery strings in parallel.

The rectifier topology in most products contain a power factor corrected AC-DC converter and an isolated DC-DC converter. The highest efficiency among the 48V DC UPS is around 95% to 96% [12], while for 380V DC UPS is around 96% to 97% [13]. Figure 1.5 and Figure 1.6 shows the typical efficiency curves
for most 48V DC UPS and 380V DC UPS. 380V DC UPS has a slightly higher efficiency due to the lower load current when compared to 48V DC UPS.

Figure 1.5. Efficiency curve for an isolated 6 kW 48V DC rectifier (Emersion Network Power)

Figure 1.6. Efficiency curve for an isolated 15 kW 380V DC rectifier (Emersion Network Power)

1.2.1.2 PSU Efficiency

The input DC voltage is stepped down to 12V with an isolated DC-DC converter. Due to the rapid growth of cloud computing, back-end servers and internet. The power requirements of these datacenters have increased a lot. This put tremendous pressure on PSU vendors to design higher efficiency and higher power density converters.
There are various PSU vendors for both 48V DC system and 380V DC system such as Emerson, Delta electronics, Powerone, Eaton and Vicor. The highest efficiency PSU in the market is provide from Vicor for both systems. This PSU is based on a ZVS/ZCS Sine Amplitude Converter (SAC™) as Figure 1.7 shows. The efficiency for 48V PSU is around 95% to 96% [14] while the efficiency for 380V PSU is around 94% to 95% [15]. Figure 1.8 and Figure 1.9 show the typical efficiency curves.

![Figure 1.7. A Sine Amplitude Converter™](image)

![Figure 1.8. The efficiency curve of a 300W PSU in 48V DC system (Vicor)](image)
1.2.1.3 Cable Loss

The copper loss of the power cable is also a critical factor to be considered in the design of a data center power distribution system. Since the current going through the cable is inversely proportional to the distribution voltage for a fixed amount of transferred power and the power loss is the square of the current times the cable resistor. The cable loss of the 48V DC system is about 62 times of the cable loss of the 380V DC system. However, the cable used in the 48V DC system has a much larger diameter than the 380V DC system for a much higher current capability. This makes the cable used have a lower resistance. Therefore, the practical cable loss of the 48V DC system will be lower than the theoretical value.

The server machines in most modern data centers are mounted in rack cabinets, which contain multiple servers stacked one above the other, as Figure 1.10 shows. These rack cabinets are usually placed in a row which is called aisles. Hence the length of distribution cables is depending on the rack power density, higher rack power density means less distribution cable and less cable copper loss. Figure 1.11 shows the average rack power density in recent years. Although it is possible to fill a rack with blade servers and achieve a rack density of 20 kW or more, but the average power density is not as high as expected when mixed IT loads with much lower power density such as server racks, storage racks, and networking racks are considered. On the other hand, the performance per watt of IT devices is improving fast recently so there is no significant cost saving with higher densities [16]. The optimal rack power density is about 5kW.
according to numerous report and analysis [16,17,18]. For an example of medium size 300 kW data center, 60 racks are required to distribution the total power.

![Server rack cabinet diagram](image1.png)

**Figure 1.10. Server rack cabinet diagram**

![Power density per rack from 2006 to 2014](image2.png)

**Figure 1.11. Power density per rack from 2006 to 2014[17]**

The floorplan or layout of a data center server room determines how the racks are distributed and the optimal distance between two racks rows. It also have a critical impact on the complexity and efficiency of power distribution system, especially for cable losses [19]. Figure 1.12 shows the preferred size for server room [20] and power room. The server room is 28’ by 46’ (8.5m x 14m) with 10 racks in a row and each row is
powered up by a PDU. The room size is optimized so that each rack row has a wide enough hot-aisle/cold-aisle pair to reduce the amount of hot air taken by the IT equipment. Therefore, the cable length from each PDU to each rack row could be estimated as 10m, which is slightly higher than the width (8.5m) of the server room. In the power room, the distance form UPS to PDU is 20m according to the similar calculation in [21].

Figure 1.12. A typical floor layout for a 300 kW datacenter

The cable selection from UPS to PDU and from PDU to racks for both distribution system are shown in Table 1.1 according to the floorplan of the datacenter and Havells Power & Control cables catalogue 2016 [22]. All the cables used here are single core armored, PVC insulated copper cable for the ease of calculation. The cable resistance and the rated current for each cable are also in Table 1.1. With the cable length, the cable resistances and the cable loss for each distribution system could be calculated as the following:

The cable loss for 48V system is:

\[ P_{L_{PDU_{48}}} = \left( \frac{I_{PDU_{48}}}{8} \right)^2 \times R_{PDU_{48}} \times 48 = \left( \frac{1041.7}{8} \right)^2 \times \frac{0.387}{1000} \times 20 \times 48 = 6299.2W \]  \hspace{1cm} (0.1)

\[ P_{L_{rack_{48}}} = \frac{I_{rack_{48}}^2}{1000} \times R_{rack_{48}} \times 60 = 104^2 \times \frac{0.524}{1000} \times 10 \times 60 = 3400W \]  \hspace{1cm} (0.2)
\[ P_{L_{\text{total}}_{48}} = P_{L_{\text{rack}}_{48}} + P_{L_{\text{PDU}}_{48}} = 9699.2W \] 

(0.3)

where: \( P_{L_{\text{PDU}}_{48}} \) is the power losses from UPS to PDU.

\( P_{L_{\text{rack}}_{48}} \) is the power losses from PDU to racks.

\( P_{L_{\text{total}}_{48}} \) is the total cable losses for 48V DC distribution system.

<table>
<thead>
<tr>
<th></th>
<th>48V DC system</th>
<th>380V DC system</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Rated Current</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{rated, total}} )</td>
<td>6250A</td>
<td>789.4A</td>
</tr>
<tr>
<td><strong>From UPS to PDU</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rated Current for each PDU ( (I_{PDU}) )</td>
<td>1041.7A</td>
<td>131.57A</td>
</tr>
<tr>
<td>Cable chosen</td>
<td>8x50sq.mm</td>
<td>1x50sq.mm</td>
</tr>
<tr>
<td>(rating current 165A each cable)</td>
<td>(rating current 165A each cable)</td>
<td></td>
</tr>
<tr>
<td>Cable resistance</td>
<td>0.387Ω/km</td>
<td>0.387Ω/km</td>
</tr>
<tr>
<td><strong>From PDU to racks</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rated current for each rack ( (I_{\text{rack}}) )</td>
<td>104A</td>
<td>13A</td>
</tr>
<tr>
<td>Cable chosen for each rack</td>
<td>1x35sq.mm</td>
<td>1x4sq.mm</td>
</tr>
<tr>
<td>(rating current 130A)</td>
<td>(rating current 35A)</td>
<td></td>
</tr>
<tr>
<td>Cable resistance</td>
<td>0.524Ω/km</td>
<td>4.61Ω/km</td>
</tr>
</tbody>
</table>

Table 1.1. Cable selection for a 300kW 48V DC and 380V DC power distribution system

Similarly, the cable loss for 380V system could also be calculated as:

\[ P_{L_{\text{PDU}}_{380}} = (I_{PDU_{380}})^2 \times R_{PDU_{380}} \times 6 = (131.57)^2 \times \frac{0.387}{1000} \times 20 \times 6 = 803.9W \] 

(0.4)
\[ P_{L\_rack\_380} = (I_{rack\_380})^2 \times R_{rack\_380} \times 60 = (13)^2 \times \frac{4.61}{1000} \times 10 \times 60 = 467.454W \]  
(0.5)

\[ P_{L\_total\_380} = P_{L\_rack\_380} + P_{L\_PDU\_380} = 1271.35W \]  
(0.6)

The cable loss for the 48V DC system is almost eight times of the 380V DC system. It is obvious that the 380V DC system saves a lot of power on the cables compared to the 48V DC system. If the power rating of the data center is higher (more than 1MW or even higher), the cable loss advantages of 380V system is more significant.

If the cable loss in this section is redefined as cable efficiency \( \eta_{cable} \) as the following

\[ \eta_{cable} = \left(1 - \frac{P_{total}}{P_{rated}}\right) \times 100\% \]  
(0.7)

and \( P_{rated} \) is 300 kW.

Therefore, for a 300kW medium size data center, the cable efficiency is 96.767% and 99.576% for 48V DC system and 380V DC system respectively.

<table>
<thead>
<tr>
<th></th>
<th>48V DC system</th>
<th>380V DC system</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC UPS Efficiency</strong></td>
<td>Peak: 96%</td>
<td>Peak: 97%</td>
</tr>
<tr>
<td></td>
<td>40% to 100% load!&gt;95.5%:</td>
<td>40% to 100% load!&gt;96%:</td>
</tr>
<tr>
<td><strong>Cable efficiency</strong></td>
<td>96.767% (cable loss is 9699.2W)</td>
<td>99.576% (cable loss is 1271.35W)</td>
</tr>
<tr>
<td><strong>PSU Efficiency</strong></td>
<td>Peak: 96%</td>
<td>Peak: 95.5%</td>
</tr>
<tr>
<td></td>
<td>40% to 100% load!&gt;95%:</td>
<td>40% to 100% load!&gt;94.5%:</td>
</tr>
<tr>
<td><strong>Overall Efficiency</strong></td>
<td>Peak: 89.2%</td>
<td>Peak: 92.24%</td>
</tr>
<tr>
<td></td>
<td>40% to 100% load!&gt;87.79%:</td>
<td>40% to 100% load!&gt;90.33%:</td>
</tr>
</tbody>
</table>

Table 1.2. Overall efficiency of 48V DC and 380V DC distribution systems

1.2.1.4 Overall Efficiency
Based on the data from previous sections, the overall efficiency for 48V DC system and 380V DC system is calculated in Table 1.2. The converter efficiency for both systems are very close. But the 380V DC system has much lower losses on the cables compared to the 48V DC system. As a result, the overall efficiency of the 380V DC system is almost 3% higher than the overall efficiency of the 48V DC system.

1.2.2 Reliability Comparison

The energy storage system in the DC UPS also plays a critical role in keeping a high reliability for data center. When the utility power is interrupted, the energy stored in the UPS continues to deliver power to the whole data center for several minutes. During that time the standby power source (normally diesel or natural gas generator) could be switched on and begin delivering power to the data center. Although the on time of the UPS is relatively short, it is long enough for the starting up of the standby power.

Among various energy storage technologies such as super-capacitors, fuel cells and different kinds of batteries, lead-acid battery is the most common energy storage component used in data centers due to its low cost, high energy capacity and high safety. Lithium battery has a much better energy density compared to lead-acid battery, but it is not commonly implemented in high power energy storage application since it is expensive and explosive.

Lead-acid is divided into two categories: flooded cell (known as vented cell or wet cell) and valve-regulated (VRLA) cell. The acid tank of flooded cell is not sealed, when the battery is charging or discharging, it will continuously vent oxygen and hydrogen vapour. Periodic water replenishment and maintenance are required for this type of battery. While VRLA battery is a sealed battery therefore does not require special maintenance compared to flooded cell, VRLA battery also offers a higher power density and lower capital cost, which makes it a common choice for UPS systems under 500 kW.

Similar to flooded cells, VRLA battery also vents oxygen and hydrogen vapour over time and the battery dries out and fails, Table 1.3 shows different failure modes for VRLA batteries. Among those failure mode, dry-out is the major one. High ambient temperature, overcharge of the battery, poor ventilation and many other factors will accelerate this process. In the end open circuit failure will happen for the battery cells. If
the fail cell is part of a series connected battery string, the whole string will stop delivering power to the system, which leads to very poor system reliability. Therefore, VRLA battery packs are always implemented with redundant parallel strings. Compared to the 48V DC system, the 380V DC system has more battery cells connected in series, which dramatically decrease the system reliability.

<table>
<thead>
<tr>
<th></th>
<th>Flooded</th>
<th>VRLA</th>
<th>MBC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid corrosion</td>
<td>86%</td>
<td>59%</td>
<td>59%</td>
</tr>
<tr>
<td>Cell Short</td>
<td>10%</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Leakage</td>
<td>1%</td>
<td>2%</td>
<td>1%</td>
</tr>
<tr>
<td>Block interconnect open</td>
<td>3%</td>
<td>3%</td>
<td>1%</td>
</tr>
<tr>
<td>Cell interconnect open</td>
<td>&lt;1%</td>
<td>1%</td>
<td>2%</td>
</tr>
<tr>
<td>Dry out</td>
<td>&lt;1%</td>
<td>33%</td>
<td>36%</td>
</tr>
<tr>
<td>Thermal runaway</td>
<td>&lt;1%</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td>Cell reversal</td>
<td>&lt;1%</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td><strong>Failure mode (primary)</strong></td>
<td><strong>Shorted</strong></td>
<td><strong>Open</strong></td>
<td><strong>Open</strong></td>
</tr>
</tbody>
</table>

Table 1.3. Failure Modes for different types of lead-acid battery [23]

In order to quantitatively calculate the reliability for 48V DC system and 380V DC system, \( r \), the reliability of a single 2V VRLA battery cell could be statistically defined. It is the probability that a randomly selected sample battery cell still functioning after a time period passed. In practical this reliability will decrease with the increasing running time, but a constant \( r \) of 0.995 is assumed here to simplify the calculation. Therefore, the reliability for a single series connected battery string is 0.8867 (0.995\(^2\)) for the 48V DC system and 0.3858 (0.995\(^{190}\)) for the 380V DC system. The reliabilities of both systems are far below the reliability standard of datacenters. A \( k\)-out-of-\( n \) parallel configuration could be deployed to increase the reliability. The number \( k \) is the minimum required number of operating battery strings and \( n \) is the total number of battery strings. The reliability for a \( k\)-out-of-\( n \) configuration is calculated by summing a series of binomial
distribution for different operation cases [24], when $k$ is equal to 1, this configuration becomes a fully redundant system.

<table>
<thead>
<tr>
<th>Configurations</th>
<th>$k$ and $n$</th>
<th>Battery reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>48V DC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>380V DC</td>
</tr>
<tr>
<td>1 string,1 operating</td>
<td>N/A</td>
<td>0.8867</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.3858</td>
</tr>
<tr>
<td>2 strings,1 operating</td>
<td>2,1</td>
<td>0.98716</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.62276</td>
</tr>
<tr>
<td>4 strings,2 operating</td>
<td>4,2</td>
<td>0.99468</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.63309</td>
</tr>
<tr>
<td>4 strings,1 operating</td>
<td>4,1</td>
<td>0.99983</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.85769</td>
</tr>
<tr>
<td>5 strings,1 operating</td>
<td>5,1</td>
<td><strong>0.99998</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.9126</td>
</tr>
<tr>
<td>6 strings,3 operating</td>
<td>6,3</td>
<td>0.997955</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.42625</td>
</tr>
<tr>
<td>6 strings,2 operating</td>
<td>6,2</td>
<td>0.999899</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.74398</td>
</tr>
<tr>
<td>6 strings,1 operating</td>
<td>6,1</td>
<td>0.999998</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.94631</td>
</tr>
<tr>
<td>8 strings,1 operating</td>
<td>8,1</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.97975</td>
</tr>
<tr>
<td>10 strings,1 operating</td>
<td>10,1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.99236</td>
</tr>
<tr>
<td>12 strings,1 operating</td>
<td>12,1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.99712</td>
</tr>
<tr>
<td>16 strings,1 operating</td>
<td>16,1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.99959</td>
</tr>
<tr>
<td>20 strings,1 operating</td>
<td>20,1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>0.99994</strong></td>
</tr>
</tbody>
</table>

Table 1.4. System reliability for 48V DC and 380V DC distribution systems with different $k$ and $n$

Table 1.4 shows the reliabilities of the 48V DC system and 380V DC system under different $k$-out-of-$n$ configurations. Only 5 fully redundant strings are required to achieve a tier 4 (99.995%) reliability standard for the 48V DC system. The reliability of the same configuration for the 380V DC system is only 91.26%, which is much less than 48V DC system. Additional 16 battery strings are required for 380V DC system to achieve the tier 4 standard reliability. This result shows 48V DC system has a huge advantage in system reliability when compared to 380V DC system.
1.2.3 Cost Comparison

Besides efficiency and reliability, the cost of a datacenter is also an important factor. The cost of a datacenter has already been mentioned several times in the analysis of cable and reliability. In this section, a detailed and quantitatively cost analysis for a 400 kW datacenter is presented. Again, the PDU and VR of the system are not discussed here since they are very similar for both systems.

1.2.3.1 Power Converter Cost

With the development of power electronics technology, most of today’s DC UPS and PSU could achieve very high efficiency and they have very similar architectures and topologies. Therefore, the power converters costs of the 48V DC system and 380V DC system are also be very similar. In terms of DC UPS, a 15 kW module will cost about $5500 for the 48V DC system and $4000 for the 380V DC system. While for the PSU, the price of a typical 300W Vicor 48V PSU is $147.17 [25], while the price of a typical 300W Vicor 380V PSU is $211.74 [26]. The power converter cost for both systems could be calculated as following:

\[
C_{\text{converter}, 48} = \frac{300}{15} \times 5500 + \frac{300}{0.3} \times 147.17 = 257169 \text{ Rs}
\]

\[
C_{\text{converter}, 380} = \frac{300}{15} \times 4000 + \frac{300}{0.3} \times 211.7 = 291699 \text{ Rs}
\]

1.2.3.2 Cable Cost

As shown in Table 1.1, eight 50 mm\(^2\) cables in parallel are required to share the current for each PDU in the 48V DC system while only one is required in 380V DC system. The amount of cable copper cost for the 48V DC system is huge, especially in large size datacenters. Moreover, the cost of copper is increasing rapidly in the recent years. Combining the cable details of Table 1.1 and a typical power cables price list of 2014 [27], the cable cost for each system could be calculated as following (\(C_{\text{cable}, 48}\) is the cable cost for the 48V DC system and \(C_{\text{cable}, 380}\) is the cable cost for the 380V DC system):

\[
C_{\text{cable}, 48} = 8 \times 6 \times 1073 \times 20 + 60 \times 767 \times 5 = 1260180 \text{ Rs} = 19007 \text{ Rs}
\]

\[
C_{\text{cable}, 380} = 1 \times 6 \times 1073 \times 20 + 60 \times 245 \times 5 = 202260 \text{ Rs} = 3050.6 \text{ Rs}
\]
The result shows cable cost of 380V system is only 16.42% of the 48V DC system. Furthermore, because multiple cables are connected in parallel to share the large current in the 48V DC system. Much more area is required to place and route these cables. Moreover, much more installation fee is also required for the whole power distribution system is also higher. These additional cost further increases the overall cost of the 48V DC system.

1.2.3.3 Battery Cost
According to the datasheet of Emersion 48V DC UPS [12], 3 strings of 4 x 12V 200Ah Enersys NP200-12BFR battery blocks are suggested for a 50 kW 48V DC UPS module with 13 minutes battery-up time. Therefore a 300 kW datacenter needs about 72 battery blocks and the price of the single battery block is $400 [28], Based on Table 1.1, 5 fully redundancy strings are required to meet the reliability requirement of tier 4 datacenter, Therefore, the total cost for the battery of the 48V DC system $C_{\text{battery,48}}$ could be calculated as the following:

$$C_{\text{battery,48}} = 400 \times 3 \times 4 \times 300 / 50 \times 5 = $144000$$

(0.12)

Similarly, based on the datasheet in [13], 5 battery trays with 28x12V 8Ah Enersys NPX-35TFR battery blocks per tray could support a 30 kW Emersion 380V DC UPS module for 13 minutes. 1867 battery blocks are needed for 400 kW rated power and the price of a single battery block is $16 [29]. In order to have a tire 4 reliability, 20 redundant battery strings are required according to, the total cost $C_{\text{battery,380}}$ could be calculated as following:

$$C_{\text{battery,380}} = 16 \times 28 \times 5 \times 300 / 30 \times 20 = $448000$$

(0.13)

According to equation (1.12) and (1.13), the battery cost of the 380V DC system is about 3.1 times of the cost of the 48V battery system for the same tier4 reliability requirement.

1.2.3.4 Overall Cost
The overall cost for the 48V DC system and the 380V DC system are presented in Table 1.5. Although the cable cost for the 380V DC system is much less than the 48V DC system, the overall cost for the 380V DC
system is much higher than the 48V DC system. This is because the battery cost for the 380V DC system is $304000 higher than the 48V DC systems under same reliability requirement, which is much higher than the saving of cable cost. Moreover, the power converter cost for the 380V DC system is also slightly higher than the 48V DC system. These above reasons result in a higher overall cost for the 380V DC system compare to the 48V DC system.

<table>
<thead>
<tr>
<th></th>
<th>48V DC system</th>
<th>380V DC system</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power converter cost</strong></td>
<td>$257169</td>
<td>$291699</td>
</tr>
<tr>
<td><strong>Cable cost</strong></td>
<td>$19007</td>
<td>$3050.6</td>
</tr>
<tr>
<td><strong>Battery cost(with tier 4 reliability requirement)</strong></td>
<td>$144000</td>
<td>$448000</td>
</tr>
<tr>
<td><strong>Overall cost</strong></td>
<td>$420176</td>
<td>$742750</td>
</tr>
</tbody>
</table>

Table 1.5. Overall cost of 48V DC and 380V DC power distribution system

1.2.4 Proposed DC UPS

From the previous analysis, it is obvious that the 48V DC system has advantages in system reliability while the 380V DC system has advantages in overall efficiency. In order to combine the advantage of both systems, a new three-port DC UPS architecture is proposed in Figure 1.13.

This DC UPS is composed of a main isolated AC-DC converter with a high frequency transformer and a bidirectional DC-DC battery side converter to charge/discharge the VRLA battery pack. The input is standard 110V<sub>rms</sub> AC or 220V<sub>rms</sub> AC utility power used in Canada and U.S. The output voltage for the load side is 380V DC and the output voltage for the battery side is 48V DC. The two output ports share one high frequency transformer to increase efficiency and power density. Therefore, by delivering power at high voltage (380V DC) and charging/discharging battery pack at low voltage (48V DC), this new DC UPS could achieve both high overall efficiency and high system reliability. The power converter cost in the new DC UPS is marginally higher than 380V DC system as it involves one more bi-directional DC-DC converter and one more transformer winding for 48V DC battery pack.
The detailed comparison between the 48V DC system, the 380V DC system and the new DC UPS system is presented in Table 1.6 (for the calculation in overall cost, it is assumed that the power converter cost of the new UPS is 1.5 times of the 380V DC system). Compared to the conventional 380V DC system, the new system with the proposed DC UPS has a 21.3% lower overall cost and 9.57% higher reliability. However, the overall cost of the new system is still higher than the 48V DC system. This is because the high input voltage PSU used in the proposed UPS is very similar as the one in the 380V DC system. This PSU is much more expensive than the PSU in the 48V DC system. However, with the increasing popularity of high voltage distribution, the price for high input voltage will keep decreasing in the future.

![Block diagram of the proposed multi-port DC UPS]

**Figure 1.13. Block diagram of the proposed multi-port DC UPS**

<table>
<thead>
<tr>
<th></th>
<th>48V DC system</th>
<th>380V DC system</th>
<th>DC system with proposed DC UPS</th>
<th>Improvement compared to 380V DC system</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall Efficiency</td>
<td>89.2%</td>
<td>92.24%</td>
<td>92.24%</td>
<td>Same</td>
</tr>
<tr>
<td>Reliability (with 5 fully redundant strings)</td>
<td>0.99998</td>
<td>0.9126</td>
<td>0.99998</td>
<td>9.57% higher</td>
</tr>
<tr>
<td>Overall cost (with tier 4 reliability requirement)</td>
<td>$420119</td>
<td>$7428 11</td>
<td>$584600</td>
<td>21.3% lower</td>
</tr>
</tbody>
</table>

Table 1.6. Comparison between 48V DC distribution system, 380V DC distribution system and the distribution system with the proposed UPS.
Figure 1.14. Proposed DC UPS based on single-stage AC-DC converter and series-parallel resonant circuit

Figure 1.14 shows the detailed implementation of the UPS in Figure 1.13. The proposed UPS is composed of two parts: a main AC-DC converter and a battery side converter. When input ac is on, the UPS is in standard mode. The main AC-DC converter is delivering power to the load and the battery side converter is charging the battery. When input ac is off, the UPS is in backup mode. The main AC-DC converter stop working and the battery side converter is delivering power to the load from the battery. In order to increase the efficiency and optimize cost, a single-stage PFC converter is selected for the main AC-DC converter. Zero voltage switching can also be achieved with the use of a series-parallel resonant circuit for both main AC-DC converter and battery side converter.

The focus of this thesis is the analysis, design and implementation of the proposed DC UPS. The following sections describe the main objectives and detailed outline of the thesis.

1.3 Thesis Objective

The following are the objectives of this thesis:
1. Develop a new DC UPS architecture for power distribution system used in data centers. This new architecture should combine the advantage of both 48V and 380V DC power distribution systems. Only one converter should be operating in either standard mode or back up mode.

2. Develop a single-stage AC-DC converter as the main AC-DC converter part of the new DC UPS with the following features:

   - Tightly regulated the output voltage and dc bus voltage with a wide range of input voltage (110-220Vrms)
   - The ac line current should comply with IEC1000-3-2 and IEC1000-3-4 standards. High power factor should be achieved with a wide load range.
   - The dc bus voltage should be well balanced over the two dc bus capacitors.
   - ZVS operations of all switches should be achieved with a wide load range.
   - Minimum circuit components should be used for the converter to achieve the aforementioned features.

3. Develop a bidirectional DC-DC converter as the battery side converter part of the new DC UPS with the following features:

   - When the converter is in battery charging mode (standard mode), it should tightly regulate the battery charging current.
   - When the converter is in battery discharging mode (back up mode), it should boost the low battery voltage and tightly regulate the output voltage.
   - ZVS operations of all switches should be achieved with a wide load range.
   - Reduce the number of components. This could be achieved by utilizing the parallel resonant capacitor from the main AC-DC converter as part of the resonant circuit in back up mode.
4. Model and analyze the proposed converter topologies to study their steady state operation.

5. Generate simulation and experimental results to prove the effectiveness of the proposed concept, validate converter performance and verify the accuracy of proposed modeling and calculation.

1.4 Thesis Outline

The thesis consists of five chapters:

Chapter 2 presents a literature review of single-stage AC-DC converters. The advantages and disadvantages of the different topologies of single stage AC-DC converters are compared and discussed.

In Chapter 3, a new single stage three-level resonant AC-DC converter is proposed for the main AC-DC part of the new DC UPS. The proposed converter can achieve high power factor and ZVS for all switches. No auxiliary circuit is required to balance the voltages of the two dc bus capacitors. The steady state operation of the proposed converter is analyzed. A decoupled average power model is built for the design of proposed converter. The simulation and experimental waveforms of a prototype converter are also presented to verify the effectiveness of the proposed converter.

Chapter 4 presents a new ZVS bidirectional DC-DC converter based on self-sustained oscillation control for the battery side converter part of the proposed DC UPS. All four switches have ZVS in a wide load range. The steady operation of both battery charging and discharging mode of the converter are analyzed.

The thesis is summarized in Chapter 5. Thesis contributions are summarized. Conclusions are drawn based on the obtained simulation and experiment results. Suggestions for future work are also presented.
Chapter 2

Single-Stage AC-DC Converter

2.1 AC-DC Converter in DC distribution system

In chapter 1, a new DC UPS is proposed to combined the advantages of both the 48V DC and 380V DC distribution systems. Similar as conventional DC UPS, the main AC-DC converters in the proposed DC UPS is the most important part. It is the beginning of the entire DC power distribution which converts the input AC voltage to a desired DC voltage. When the converter draws power from the AC main, it should keep the input current purely sinusoidal and in phase with the input ac voltage to achieve a close to unity power factor. Several international standards such as IEC 1000-3-2 [30], IEC 1000-3-4 [31] and IEEE-519-1992 [32] provide the input power quality requirements of the AC-DC converter for different applications. On the other hand, the output DC voltage of the converter should be well regulated regardless of the change of input ac voltage or load. In the following sections, a literature review of AC-DC converter focusing on single-stage converter is presented.

2.2 Power Factor Correction

The power factor (PF) is defined as the ratio of real power (P) to the apparent power (S), It is a factor to measure the power utilization efficiency of the converter. For pure sinusoidal voltage and current waveform, the PF could be defined as

\[ PF = \frac{P}{S} = \cos \phi \]  

(1.1)

\( \phi \) is the phase shift between voltage and current.

But when the voltage is sinusoidal and current is not sinusoidal. The PF is defined as:

\[ PF = \frac{I_{\text{rms}}}{I_{\text{rms}}} \cos \phi = K_d \cos \phi \]  

(1.2)

\( K_d \) is the ratio of the fundamental RMS current and the total RMS current.
\[ K_d = \frac{I_{\text{rms},1}}{I_{\text{rms}}} = \frac{I_{\text{rms},1}}{\sqrt{I_{\text{rms},1}^2 + I_{\text{rms},2}^2 + \ldots + I_{\text{rms},n}^2}} \]  \hspace{1cm} (1.3)

\[ \text{THD} = \frac{\sqrt{I_{\text{rms},1}^2 + I_{\text{rms},2}^2 + \ldots + I_{\text{rms},n}^2}}{I_{\text{rms},1}} \]  \hspace{1cm} (1.4)

Thus, the PF could be represented as:

\[ \text{PF} = \frac{\cos \varphi}{\sqrt{1 + \text{THD}^2}} \]  \hspace{1cm} (1.5)

According to the equation (1.18), both displacement between current and voltage (\( \cos \varphi \)) and the distortion current (THD) will result in a poor PF. A good AC-DC converter should keep the current in phase with the voltage and minimize the current harmonics at the same time.

To deliver the same amount of power, an AC-DC converter with poor PF draws much higher current from input than the converter with unity power factor. This extra current increases the copper losses in the converter and therefore the converter efficiency is reduced. It also increases the economic cost of the converter and makes the voltage regulation difficult. Therefore, a close to unity power factor is a key requirement of the AC-DC converter. The methods to achieve this are called power factor correction (PFC).

In the rest of this section, two basic PFC methods are presented.

### 2.2.1 Passive PFC

The simplest and most straightforward way to reduce input current harmonics is using passive components circuit such as capacitor or LC filter. As Figure 2.1 shows. This passive circuit could be located either before or after the rectifier bridge of the AC-DC converter. Several passive PFC techniques have been researched in the past such as using LC series resonant circuit to filter out high order harmonics current [33]. This PFC method has several advantages and drawbacks: the advantages are simple implementation, low EMI and high efficiency. However, since the corner frequency of the filter is very low (less than
300Hz), the filter is always bulky and heavy, especially for high power application. This limits the implementation of passive PFC method in high power applications [34-35].

![Passive PFC circuit diagram]

Figure 2.1. Passive PFC circuit

### 2.2.2 Active PFC

Switching converters with active switch devices and passive component are used in this method to shape the input current from the AC utility and regulate the output voltage. With proper control method, close to unity power factor can be achieved. Since the switches in the active PFC converter are operating in high frequency, this PFC method has a lot of advantages compared to the passive PFC such as lower harmonic current, smaller component size and higher power factor. However, the control method and design of the converter is more challenging compared to passive PFC [36].

The operation mode of active PFC operation could be classified as continuous conduction mode (CCM), discontinuous conduction mode (DCM) and critical conduction mode (CRM). CCM usually has two control loops: the slow outer loop is used to regulate the output DC voltage and generates a current reference for the inner loop; the fast inner loop is used to shape the input current as a pure sinusoid waveform with the current reference from the outer loop. Many control methods have been studied for the inner control loop such as peak current control, average current control and hysteresis current control [37-40]. Average current control, as Figure 2.2 shows, is the most popular one among them. Figure 2.3 shows the DCM PFC. This control method only has the slow voltage loop since the discontinuous input current is naturally following
the input voltage waveform to have a sinusoid shape [41]. Hence, the design and cost of the DCM PFC is much simpler and lower than CCM. But since the input current is always switching between zero and peak current, the current harmonics and component current rating for DCM converter is much higher compared to CCM. Large size EMI filter is also required to reduce excessive harmonic current. This drawback makes DCM converter not suitable for high power application. CRM is a control method operating at the boundary of CCM and DCM. The input current start rising right after it drops to zero [42].

Since the output voltage of the AC-DC converter is not suitable for many applications, another DC-DC converter is normally required to further step down the voltage. The active PFC AC-DC converters could also be categorized into two-stage AC-DC and single-stage AC-DC converters. They are discussed in the rest of this section.

![CCM PFC average current control circuit](image)

Figure 2.2. CCM PFC average current control circuit
2.2.2.1 Two-Stage AC-DC Converter

Figure 2.4 shows the blocking diagram of a two-stage AC-DC converter, the first rectifying stage makes the input current sinusoidal shape and keeps it in phase with the input ac voltage. Boost converters are most commonly applied in this stage and the inductor current could be continuous or discontinuous as discussed above [43]. Other topologies such as buck, buck-boost and SPEIC could also be adopted in the rectifying stage, but the performance is not good due to the degraded efficiency and high component stresses [44-46]. The second DC-DC stage is normally an isolated step down converter to further adjust the dc voltage depending on the requirements of various applications. Topologies like forward, flyback, full bridge converter or resonant converter could be adopted here. A high volume DC bus capacitor is located between the rectifying stage and the DC-DC stage to reduce the low frequency ripple.

2.2.2.2 Single Stage AC-DC Converter

Although two-stage AC-DC converter could achieve high power factor, low harmonic current and well-regulated output DC voltage, they are expensive, inefficiency and bulky because the topology contains two converters. Due to the increasing demand of high power density and high efficiency for power converters,
many efforts have been made to design smaller and more cost effective converter with less components and smaller size that can still comply with regulatory agency requirement. This makes single-stage AC-DC converters become a promising choice in recent years.

Single-stage AC-DC converter could be considered as an integration of the rectifying stage and DC-DC stage of the traditional two-stage AC-DC converter. By sharing the switching operation of the two stages, both input current shaping and output dc voltage regulating could be achieved with limited number of switches. The converter could have a better performance of efficiency, cost and size.

2.3 Review of Single Stage AC-DC Converter

Numerous researches have been done about single stage AC-DC converter. Different topology combinations of rectifier stage and DC-DC stage generates different single stage AC-DC converter topologies [47-86]. The most common choice for the rectifier stage is boost converter. Depending on different application and power level, the topology variations always happens at the DC-DC stage. In the following parts the major topology of single stage AC-DC converter are categorized and reviewed.

2.3.1 Based on flyback/forward converter

The first and simplest single stage AC-DC converter was proposed in 1992 by M.T.Madigan, which is a combination of boost converter and flyback/forward converter [47] as Figure 2.5 shows. The rectifying stage is in DCM and DC-DC stage is in CCM with duty cycle control. This topology is very cost effective
since it is implemented with only one switch. However, If the duty cycle is used to regulate output voltage, the line current is left un-regulated and PFC is not achieved. Therefore, DCM with inherent PFC must be used for the rectifying stage [48], which limits the power range of this converter. Moreover, the dc bus voltage of the converter is strongly depending on the load current. When the output is regulated, the dc bus voltage is very high under high input ac and light load condition [49]. This makes the design and component selection impractical since capacitor and switch with high voltage rating always have a higher cost and loss. Operating both stages in DCM solves this problem but the current distortion is high and the output voltage is oscillating [50].

![Diagram of AC-DC Converter](image)

Figure 2.5. Single-Stage AC-DC converter proposed by M.T.Madigan [47]

Voltage feedback loop with a coupled winding structures are proposed in [51-53] to reduce the high voltage stress on the storage capacitor. But addition components and cost makes the converter bulky and expensive. Efficiency degrade always happens on those proposed converters because of the circuiting current and additional diodes [53].

2.3.2 Based on Half Bridge

Half bridge circuit is also a promising choice for the single-stage AC-DC converter. Majority of this topology category could be consider as a combination of boost converter and some resonant circuit [50]. Because of the use of resonant circuit, the converter normally has ZVS or ZCS for all the switches. In [54], a ZVZCS converter is proposed as Figure 2.6 shows. ZVS is achieved with the lagging inductor current and ZCS is achieved with the resonance between the leakage inductance and snubber capacitor. A lot of
variation based on this topology are proposed [55-59]. In order to decrease the size of input EMI filter and increase the efficiency, some topologies with interleaving-inductor are proposed [55-56]. Topologies with different resonant circuits such as LCC or LLC are also proposed in [56-59] in order to optimize and circuiting current and increase the efficiency.

![Diagram](image)

Figure 2.6. A ZVZCS single-stage half-bridge PFC converter [54]

These converters have advantages in size, efficiency and cost. However, almost all the proposed converters are operating in DCM mode, this mode has a lot of current ripple and on the switches so high current rating switches are required. A lot conduction losses are also generated which complemented the advantages of ZVS or ZCS. Moreover, this type of converter is controlled either by duty cycle or frequency. When the output is well-regulated, the dc bus is still unregulated which is similar as the aforementioned problem[59]. High voltage rating capacitor and switches are required for the converter, which increases the loss and cost. The above problems limit the usage of this topology to low power application such as LED driver and electrical ballast driver.

### 2.3.3 Based on Full Bridge Converter

Full bridge circuit is also widely used in single stage AC-DC converters for higher power level applications. In [60], standard phase-shift PWM control is implemented with auxiliary windings and the converter have soft switching for all the switches. the auxiliary winding acts like a switch to counteract DC bus voltage so the charge or discharge of the boost inductor could be done simultaneously with the phase shift operation.
But the excessive dc bus voltage also appears when the rectifying stage is in CCM. Many efforts have been done to solve the high dc bus voltage problem [61-64]. In [61-62] a new PWM controlled full-bridge converter is proposed as Figure 2.7 shows, the DC bus voltage is limited at 450V by directly connect the boost inductor with the isolation transformer. But the converter is operating with asymmetrical PWM where the top switches conduct current longer. A phase-shift PWM control full-bridge converter is proposed and studied in [63-64] as Figure 2.8 shows. This converter is a improvement of [60] which also contains an auxiliary circuit. This circuit acts as a magnet switch to cancel out the dc bus just like [60]. In one switching cycle, the dc bus capacitor gets discharged twice while only get charged once. Secondly, since the dc bus voltage is not fully canceled when boost inductor gets charged, less energy is transferred from the ac input compare to [60]. Therefore, this converter has a much lower dc bus voltage compare to [60]. However, the auxiliary circuit and diodes always conduction during the full switching cycle, which generate a lot conduction loss in high power applications.

Figure 2.7. Asymmetrical PWM full-bridge AC-DC converter with reduced dc bus voltage [61]
Figure 2.8. Magnetic switch phase shift full-bridge AC-DC converter with reduced dc bus voltage [63].

The converter with the dc bus capacitor discussed before could be considered as “voltage-fed” converter since the energy is transferred between load and converter components when the dc capacitor voltage increase or decrease. In order to avoid the excessive and unregulated dc bus voltage problem. Another category called “current-fed” converters are proposed in [65-68]. Figure 2.9 shows the circuit diagram of a typical current-fed AC-DC converter. Those converters normally do not require a bulky dc bus capacitor and the boost inductor is connected directly to the input of full-bridge converter. But the absence of dc bus capacitor causes the high voltage ringing and overshoot when the switch is turning on and off. A very high low frequency ripple also appears at the output.
2.3.4 Based on Resonant Converter

Resonant converters are also being considered as a promising choice for AC-DC converters [69-75]. They have advantages such as ZVS, high efficiency, high power density and cost effective. Among different resonant converters, parallel (LC) and series-parallel (LCC) resonant converters are qualified for power factor correction since they have the feature of voltage boost. Figure 2.10 shows an example of LCC resonant converter as AC-DC converter.

However, this type of converter could also be categorized as current-fed converter as they are also lack of dc bus capacitor. Hence, they still suffer from the high double line frequency ripple problem mentioned.
before, Furthermore, since the input ac voltage has a large variation range. A wide frequency variation is required to regulate the output. The design of EMI filter and selection of passive component become difficult. To solve this problem, self-sustained oscillating control was first published in [72]. This control method uses both frequency control and phase shift control to regulate the output voltage. The lagging angle between resonant voltage and resonant current is fix to a small value and the phase shift is used to regulate the output voltage. This method significantly decreases the frequency variation range. Based on this method, a number of control optimizations and new converter topologies are demonstrated in [73-75]. But the double line frequency ripple problem is still found in these converters.

2.3.5 Based on Three level converter

Based on previous discussion, the high dc bus voltage problem is limiting the development of high power single-stage AC-DC converter. New topologies and new techniques are required to overcome this problem. Three-level converter is widely used in high voltage DC-DC converter [76-80]. With four switches connected in series, the voltage stress on each switch is reduced to half of the dc bus voltage. Therefore, the dc bus voltage could easily go as high as 800V or more. This feature makes it a good candidate to solve the high dc bus voltage problem for single stage AC-DC converters. The first single stage AC-DC converter based on three-level converter is proposed in [81]. In [82-83], A three-level AC-DC converter similar to [60] is proposed as Figure 2.11 shows, the auxiliary windings is used to counteract the DC bus voltage when charging the boost inductor. The rectifying stage is in DCM and DC-DC stage is in CCM. However, similar as before, the auxiliary circuit and diode consume a lot of power with high power application. Furthermore, since there is only one control variable, which is already used to regulate the output voltage. Although the voltage stress of the component is reduced, the dc bus voltage is still left unregulated.
Some new three-level AC-DC converter with two separate control variable are proposed in [84-85]. However, the converter in [84] has two addition diode and one of them is conducting when the output inductor is charging. Therefore, the conduction loss is high and converter efficiency get degraded. While for the converter in [85], the sum of charging time of boost inductor and output inductor is less than half of one switching period. This significantly limits the yield power of this converter.

A promising three-level converter with two control variable is proposed in [86] as Figure 2.12 shows. Two control loop is used in this converter: the duty cycle loop is used to regulate the dc bus voltage while the frequency loop is used to regulate the output voltage. ZVS is also achieved for all four switches within a wide operating range. With reduced switch voltage stress and independent control loop, the dc bus voltage could be more than 600V with standard MOSFET. However, because of the unbalance charging of the two dc bus capacitors. An auxiliary circuit consist of a transformer winding and two diodes is required to balance the two dc capacitor voltages cycle by cycle, which increase the cost, loss and size of the converter.
2.4 Summary of Literature Review on Single-Stage AC-DC converter

The aforementioned single-stage AC-DC converters can be divided into two categories: voltage-fed converters (with dc bus capacitors) and current-fed converters (no dc bus capacitors). A comparison of these two approaches is shown in Table 2.1.

<table>
<thead>
<tr>
<th></th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage-fed</td>
<td>• Low double line frequency ripple</td>
<td>• Both the rectifying stage and DC-DC stage are in DCM mode</td>
</tr>
<tr>
<td></td>
<td>• Fixed frequency</td>
<td>• Auxiliary winding circuit normally required</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Unregulated DC bus voltage</td>
</tr>
<tr>
<td>Current-fed</td>
<td>• CCM mode could be easily achieved in the rectifying stage</td>
<td>• Large double line frequency ripple</td>
</tr>
<tr>
<td></td>
<td>• No auxiliary circuit</td>
<td>• Large frequency variation range</td>
</tr>
</tbody>
</table>

Table 2.1 Comparison of voltage-fed and current-fed single-stage AC-DC converter

For data center application, the voltage-fed topology is a more promising choice because it provides a very long hold up time. The hold-up time is a term describe how long the converter could maintain output within specified voltage range when input power is shut down. During this time the power supply is transferred
form ac utility to batteries or from battery to utility. Usually the hold-up time should be significantly longer than the transfer time. When input ac is off, the voltage on the capacitor decrease slowly since the dc bus capacitor stores normally stores large amount of energy. Therefore, the time to maintain a desirable output voltage is much longer than current-fed converters. Secondly, since IT load and equipment are very sensitive to voltage variation. Very tight voltage regulation is a key requirement for the power supply. As mentioned before, the output of current-fed converter is difficult to tightly regulated since it contains a very higher second order ripple.

However, the major problem of voltage-fed converters is the unregulated and high DC bus voltage. This problem results in the use of high voltage rating switches which has a very high turn-on resistance. Furthermore, the highest voltage rating for MOSFET in the market is about 600V to 650V while the dc bus voltage for voltage-fed converter could easily higher than that [60].

Based on the discussion of section 2.3.5, three-level converter is a good candidate to solve the problem and the converter proposed in [86] is the most promising one. However, this converter suffers from the additional transformer and diode in the auxiliary circuit which required to balancing the voltage of the two dc bus capacitor.

In chapter 3, A new three level resonant AC-DC converter is proposed to solve the voltage imbalance problem in [86] without auxiliary circuit. Furthermore, the proposed converter also have a higher efficiency and simpler control compared to [86]. Furthermore, detail analysis about the steady state and design of the proposed converter is also presented in chapter3. This new converter is well suited for the main AC-DC converter part of the new DC UPS proposed in chapter 1.
Chapter 3

Bridgeless Three-Level Resonant Single-Stage AC-DC Converter without Auxiliary Circuit

3.1 Introduction

In chapter 2, it was concluded that the voltage-fed AC-DC converter is a better choice for data center applications. However, high voltage component stress is the major problem of voltage-fed AC-DC converter. Although this could be solved with a three-level converter, the previous converters described in the literature review still have the unregulated DC bus voltage problem, which decrease converter reliability. A novel three-level resonant AC-DC converter operating with two control variables is presented in [86]. This converter regulates DC bus voltage with PWM control and regulates output voltage with frequency control. However, the voltage imbalance between the two DC bus capacitors is the major drawback of this converter.

In this chapter, a new bridgeless three-level single-stage AC-DC converter will be proposed to solve the voltage imbalance problem found in previous topologies. The outline of this chapter is as follows: Section 3.2 gives an introduction and review about the family of bridgeless AC-DC converters. Section 3.3 describes the principle operation and control method of the proposed converter. Section 3.4 presents the detailed analysis of the steady state operation of the propose converter. Simulation results and experimental results are provided in Section 3.5 and 3.6 to prove the validity of the proposed concept.

3.2 Bridgeless AC-DC Converters

Although the conventional boost converter is a very popular choice for the rectifying stage of single-stage AC-DC converter, the conduction loss of the diode rectifier is critical, which limits the converter efficiency in high power applications. Bridgeless AC-DC converters were presented to solve this problem. It significantly increases converter efficiency by reducing the conduction loss of the diode rectifier bridge,
especially for high power application. Various topologies of bridgeless AC-DC converter have been proposed [87-91]. The traditional bridgeless AC-DC converter is shown in Figure 3.1. One of the MOSFET body diode conducts during the discharge of boost inductor. However, in the negative half-cycle of input ac, the output ground is connected to a high frequency pulsating voltage source when the switch is on and off. This generates a much higher common-mode (CM) electromagnetic noise compared to conventional boost AC-DC converter [87]. Significantly large CM chokes are required for this converter to meet the EMC standards. The power density is reduced and cost is increased as a result. Some modifications have been made to solve this problem, such as adding one more inductor and diode in [89], but these modifications have a low component utilization and high cost.

Figure 3.1. Traditional bridgeless AC-DC converter

The totem-pole bridgeless AC-DC converter [87] shown in Figure 3.2 is an attractive choice to reduce the large common-mode noise found in traditional bridgeless AC-DC converter. During the positive half-line cycle of input ac, $D_1$ is always conducting. $Q_1$ conducts when the boost inductor ($L_{in}$ in Figure 3.2) is charging and $Q_2$ freewheels the current of $L_{in}$ and transfers the energy stored in $L_{in}$ to the output. $Q_2$ conducts complementary when $L_{in}$ is discharging to reduce conduction loss. During the negative half-line cycle of input ac, $D_2$ is always conducting. $Q_2$ conducts when $L_{in}$ is charging and $Q_1$ freewheels the current of $L_{in}$. $Q_1$ also conducts complementarily as $Q_2$ during the positive half-cycle of input ac voltage. Because of the symmetrical operation properties during one full line cycle of input ac, this topology can be of the method to solve the voltage imbalance problem in [86].
Figure 3.3 shows the proposed converter. It is an integration of totem-pole bridgeless AC-DC converter and three-level converter, although one of the dc bus capacitor get overcharged in one half-cycle of input ac, the opposite operation happens in the next half-cycle of input ac so that the other capacitor also get exact same amount of overcharged. In this way, the voltages of two dc bus capacitors are naturally balanced without any additional auxiliary circuit. Furthermore, due to the elimination of the two rectifier diodes, the proposed converter also has a lower cost and higher efficiency compare to [86].

Figure 3.2. Totem-pole bridgeless AC-DC converter

Figure 3.3. Proposed bridgeless three-level resonant AC-DC converter.
3.3 Principle Operation and Control Method of Proposed Converter

3.3.1 Principle Operation

The operation modes of the proposed converter are shown in Figure 3.4. Because of the symmetrical operation of the converter, only the operations modes in the positive half-line cycle of the input ac voltage are described.

Figure 3.4. Switching sequence of one switching cycle for the proposed converter in Figure 3.3
Mode 1 (t₀ to t₁): S₁ and S₂ are turned on at t₀. The energy of \( C_{bl} \) is transferred to the load. Meanwhile the boost inductor (\( L_{m} \)) gets charged by \( V_m \) and the current flows through it increases. The voltage across the resonant tank (\( V_{ab} \)) is positive and equal to the voltage of \( C_{bl} \) (half of the dc bus voltage) while \( C_{bl} \) is delivering energy to the load through the resonant circuit. The resonant current flows through \( S₁, S₂ \) and the resonant circuit. This mode ends at \( t₁ = DT_s \), \( D \) is the duty ratio of the boost stage and it ranges from 0 to 0.5\( T_s \), where \( T_s \) is the period of one switching cycle.

Mode 2 (t₁ to t₂): S₁ is turned off at t₁. The boost inductor starts to discharge and the stored energy is transferred to \( C_{bl} \). The drain source capacitor (\( C_{ds} \)) of \( S₁ \) get charged. When the switch voltage of \( S₁ \) reaches the voltage of \( C_{bl} \). Diode \( D_{c₁} \) conducts and clamps the voltage of \( S₁ \) to the voltage of \( C_{bl} \) (half of the dc bus voltage). At the same time, the sum of switch voltages of \( S₃ \) and \( S₄ \) decrease from the dc bus voltage to the voltage of \( C_{b₂} \). Since the \( C_{ds} \) of \( S₃ \) and \( S₄ \) are identical, each of them has a switch voltage equals to half of the voltage of \( C_{b₂} \). \( V_{ab} \) is zero and the resonant current circulates through \( D_{c₁}, S₂ \) and the resonant circuit. At the end of this mode (\( t₂ = 0.5T_s \)), the voltage of \( C_{bl} \) is slightly higher than the voltage of \( C_{b₂} \) since only \( C_{bl} \) get charged during this mode, but this voltage increment is very smaller compared to the total voltage of \( C_{bl} \). Furthermore, in the next half-cycle of input ac voltage, exact same amount of overcharge happens to \( C_{b₂} \) so the dc bus voltage is distributed equally on \( C_{bl} \) and \( C_{b₂} \) during one full cycle of input ac voltage. The voltage difference of \( C_{bl} \) and \( C_{b₂} \) has a periodic fluctuation, which could be neglected with proper selection of \( C_{bl} \) and \( C_{b₂} \). Detailed discussion about this fluctuation will be presented later.

Mode 3 (t₂ to t₃): S₂ is turned off at t₂. Because the resonant current \( i_r \) is lagging, the sum of the boost inductor and resonant current goes through \( S₁ \) and \( S₄ \). \( C_{ds} \) of \( S₃ \) and \( S₄ \) get discharged and \( C_{ds} \) of \( S₂ \) get charged. When \( C_{ds} \) of \( S₃ \) and \( S₄ \) is fully discharged, the body diodes of \( S₃ \) and \( S₄ \) conduct before their gating signal and the sum of the switch voltages over \( S₁ \) and \( S₂ \) is equal to the dc bus voltage.
**Mode 4** (t₃ to t₄): Since $C_{ds}$ of $S_3$ and $S_4$ are fully discharged, $S_3$ and $S_4$ are turned on with zero voltage switching at $t₃$. The boost inductor continues to discharge through $C_{b1}$ and $C_{b2}$ so the two dc bus capacitors get the same charge. $V_{ab}$ is negative and its amplitude is equal to the voltage of $C_{b2}$, which is the half of the dc bus voltage. $C_{b2}$ starts delivering energy to the resonant circuit and load. The resonant current flows through $S_3$, $S_4$ and the resonant circuit.

This mode ends when all the energy stored in the boost inductor are transferred to $C_{b1}$ and $C_{b2}$ and the current of the boost inductor decrease to zero.

**Mode 5** (t₄ to t₅): The boost inductor current decreases to zero at $t₄$. Depending on the instantaneous input ac voltages and dc bus voltages, the boost inductor has three different discharge patterns, which will be discussed in details in later section. The discharge process may end before or after half of the switching cycle. The resonant current still circulates through $S_3$, $S_4$ and the resonant circuit.

**Mode 6** (t₅ to t₆): Similar to **Mode 2**, $S_4$ is turned off at $t₅$ and $C_{ds}$ of $S_4$ get charged. When $C_{ds}$ of $S_4$ reaches the voltage of $C_{b2}$. Diode $D_{c2}$ conducts and clamps the switch voltage of $S_4$ to the voltage of $C_{b2}$. $V_{ab}$ drops to zero and the resonant circuit flows through $S_3$, $D_{c2}$ and the resonant circuit.

**Mode 7** (t₆ to t₇): $S_3$ is turned off at $t₆$. Similar to **Mode 3**, $C_{ds}$ of $S_3$ and $S_2$ get discharged by the lagging resonant current. When $C_{ds}$ of $S_3$ and $S_2$ are fully discharged, the body diodes of $S_3$ and $S_2$ conduct before their gate signals. The sum of the switch voltages over $S_3$ and $S_4$ is equal to the dc bus voltage. After that $S_3$ and $S_2$ are turned on with ZVS and the next switching cycle repeats from **Mode 1**.

In the negative-half-cycle of input ac voltage, opposite switching operations are implemented on the converter: $S_3$ and $S_4$ are turned on when the boost inductor is charging, while $S_1$ and $S_2$ are turned on when the boost inductor is discharging. Thus, ZVS operations are achieved for all four switches.
Figure 3.5 Equivalent circuit of each mode for the proposed converter
The operation of the proposed converter has the following remarks:

- When the charging of the boost inductor ends, the sum of the boost inductor current and resonant current discharges $C_{ds}$ of the switches which will be turned on ($S_3$ and $S_4$ in the positive half-cycle of input ac voltage; $S_1$ and $S_2$ in the negative half-cycle of the input ac voltage). Therefore, ZVS operations for these two switches are guaranteed. However, for the other two switches, which are turned on when the inductor starts charging, the difference between the resonant current ($i_r$) and the boost inductor current ($i_{Lin}$) discharges their $C_{ds}$ instead of the sum. Since the converter is operated in DCM, the boost inductor current is always zero when the inductor starts charging at the end of every cycle, the difference between $i_r$ and $i_{Lin}$ is always positive and ZVS operations of the other two switches are also guaranteed. However, if the converter is operating in CCM, ZVS will lost when $i_{Lin}$ is larger than $i_r$. This happens most probably at the peak of the input ac voltage where $i_{Lin}$ is also at its peak.

- In [86], since the two bottom switches ($S_3$ and $S_4$) always carry the sum of $i_r$ and $i_{Lin}$ while the other two switches ($S_1$ and $S_2$) always carry the difference of $i_r$ and $i_{Lin}$. As a result, the current stresses of $S_3$ and $S_4$ are much higher than the current stresses of $S_1$ and $S_2$. But in proposed converter, the two bottom switches and the two top switches carry the sum of the boost inductor and the resonant current alternatively every half-cycle of input ac voltage. Hence, current stress is equally distributed over four switches during a full cycle of the input ac voltage. When the load is light and the duty cycle ($D$) is small, the current stresses of the two middle switches ($S_2$ and $S_3$) are higher than the other two switches ($S_1$ and $S_4$). When the load is heavy and $D$ is close to 0.5, the current stresses for all four switches are very close. This makes the switch selection and heat sink design simpler for the proposed converter.

- Since two rectifier diodes are eliminated in the proposed converter, it has a higher efficiency compared to [86]. This improvement is obvious at low input voltage and heavy load.
3.3.2 Discharge Patterns of the Boost Inductor

After the boost inductor current reaches the highest value ($I_{\text{Lin,peak}}$), the discharge pattern of the boost inductor is different depending on both input voltage and dc bus voltage. Figure 3.6 shows three different discharge patterns:

![Figure 3.6. Three discharge patterns for the boost inductor](image)

**Pattern 1**: The boost inductor current decrease to zero during Mode 2 and all the discharge current goes through one switch ($S_2$ or $S_3$) and one dc bus capacitor ($C_{b1}$ or $C_{b2}$) depending on the polarity of the input ac voltage. All the energy stored in the boost inductor is transferred to either $C_{b1}$ or $C_{b2}$.

**Pattern 2**: In this pattern, the boost inductor current does not decrease to zero at the end of Mode 2, it drops to an intermediate value ($I_{\text{Lin,peak2}}$). Only part of the energy stored in the boost inductor is transferred to one dc bus capacitor ($C_{b1}$ or $C_{b2}$) depending on the polarity of the input ac voltage. Then the remaining energy is transferred to the two dc bus capacitors $C_{b1}$ and $C_{b2}$, the boost inductor current decay to zero at the end of Mode 4.

**Pattern 3**: All the discharge current goes through the two dc bus capacitors $C_{b1}$ and $C_{b2}$. All the energy stored in the boost inductor is equally shared by $C_{b1}$ and $C_{b2}$.

Because of **Pattern 1** and **Pattern 2**, the voltage of one dc bus capacitor is slightly higher than the other at the end of current half-cycle of the input ac voltage. However, in the next half-cycle, the other dc bus
capacitor gets same amount of overcharge. Therefore, the dc bus voltage is well balanced over the two dc bus capacitors in one full cycle of input ac voltage.

3.3.3 Controller for the Proposed Converter

The controller for the proposed converter is shown in Figure 3.7. There are two independent control loops in the proposed converter: PFC control loop and output control loop. The output loop is used to regulate the output voltage with variable switching frequency ($f_s$) control. The output voltage is sensed to determine the switching frequency for the next switching cycle and the saw tooth carrier signal is generated for the PWM generator. The PFC loop is used to regulate dc bus voltage with duty cycle ($D$) control, $D$ is determined by the conduction time of either $S_1$ (when the input is positive) or $S_4$ (when the input is negative).

![Controller of the proposed converter](image)

Figure 3.7. Controller of the proposed converter
and it is ranged from 0 to 0.5. Since the rectifying stage of proposed converter is always in DCM mode, the outside envelope of boost inductor current is sinusoid and automatically follows the input ac voltage. High power factor is achieved without the control loop of the boost inductor current. This makes the controller for the proposed converter easy to design and implement. But DCM operation generates large high frequency current ripples, the EMI filter of the proposed converter should be carefully designed to filter out those noise.

3.4 Steady State Analysis

3.4.1 Rectifying Stage

Since the converter is operating in DCM, the input current starts from zero at the beginning of every switching cycle. At the end of the charging stage. The boost inductor current is determined by:

\[
L_{in} \frac{di_{Lin,k}}{dt} = v_{in,k}
\]  

(2.1)

\[
I_{Lin_{,peak}} = \frac{D_k v_{in,k}}{L_{in}} T_{s,k}
\]  

(2.2)

where \(L_{in}\) is the input inductance, \(i_{Lin}\) is the boost inductor current, \(v_{in}\) is the input ac voltage, \(D\) is the duty cycle, \(T_s\) is the switching period.

The subscript \(k\) means the current switching cycle of the calculation is made. Since the frequency of the input ac is much lower than the switching frequency. The input ac voltage could be considered as a constant value during one switching cycle.

In order to ensure the converter is operating in DCM under all operating points, the boost inductor current should decay to zero when the \(D\) is maximum, the following equation should be satisfied:
\[
\frac{D_k V_{in,k}^2}{L_{in}} \leq \frac{(1-D_k)(V_{bus} - V_{in,k})^2}{L_{in}}\ T_{s,k}
\]  

(2.3)

Assume the input power is equal to the output power (converter efficiency is 100%)

\[
P_o = P_{in} = \frac{D_k V_{in,k}^2}{2L_{in}}\ T_{s,k}
\]  

(2.4)

Combine equation (3.3) and equation (3.4), the following condition should be satisfied to ensure DCM:

\[
L_{in} \leq \frac{D(1-D_k)2V_{bus}^2}{2P_o} \ T_{s,k}
\]  

(2.5)

If the boost inductor discharges as Pattern 2 or Pattern 3, In order to meet the current harmonic standard [30-31], the dc bus voltage range is selected from 400V to 800V for the input voltage range from 110Vrms to 220Vrms based on the calculation of [86]. Therefore, the dc bus voltage is determined by:

\[
V_{bus} = 2.4V_{in,\text{rms}} + 164
\]  

(2.6)

Figure 3.8 and Figure 3.9 show the relationship between the critical value of \( L_{in} \) and duty cycle with 400V and 800V dc bus voltage under full load (1 kW). The inductance selected for the boost inductor should be less than the critical value. Normally, lower dc bus voltage and higher switching frequency correspond to a lower critical value curve. For each curve, higher inductance gives a smaller allowable range of duty cycle selection. For example, in Figure 3.8, with a 20\( \mu \)H boost inductor, the switching frequency should below 300kHz when duty cycle is ranged from 0.1 to 0.5. As the proposed converter is designed to operating over 200kHz, 10\( \mu \)H is selected for the boost inductor in order to have a wide range of switching frequency.

Based on the aforementioned analysis, the input current discharges in three patterns. The average value of input current during one switching cycle of each pattern is discussed as following:

**Pattern 1:** the input current decrease to zero before half of the switching cycle, all the energy in the boost inductor is transferred to one dc bus capacitor. Therefore:
Figure 3.8. Critical value of $L_{in}$ with 400V dc bus voltage and full load (1kW)

Figure 3.9. Critical value of $L_{in}$ with 800V dc bus voltage and full load (1kW)
\[ 0 = I_{Lin_{-peak}} - \left( \frac{V_{bus}}{2} - v_{in,k} \right) \frac{d_{1,k}}{L_{in}} T_s \]  \hspace{1cm} (2.7) \]

where \( d_{1,k} T_s \) is the time for the current decay to zero and it is determined by:

\[ d_{1,k} = \frac{D_k v_{in,k}}{V_{bus} - v_{in,k}} \]  \hspace{1cm} (2.8) \]

The average value of input current during one switching cycle is given by:

\[ i_{Lin(ave)_{-1}}(\omega t) = D_k^2 \frac{v_{bus} \sin(\omega t)}{2L_{in} f_s \left( V_{bus} / V_m - 2 \sin(\omega t) \right)} \]  \hspace{1cm} (2.9) \]

**Pattern 2**: the discharge starts through one switch (\( S_2 \) or \( S_3 \)) and one of the dc bus capacitors (\( C_{b1} \) or \( C_{b2} \)) depending on the polarity of the input ac voltage. The input current doesn’t decay to zero at the end of Mode 3. It drops to a new value \( I_{Lin_{-peak2}} \). This discharge time is:

\[ d_{1,k} = 0.5 - D_k \]  \hspace{1cm} (2.10) \]

At \( 0.5T_s \), the input current is:

\[ I_{Lin_{-peak2}} = I_{Lin_{-peak}} - \left( \frac{V_{bus}}{2} - v_{in,k} \right) \frac{1 - D_k}{L_{in} f_s} \]  \hspace{1cm} (2.11) \]

Then the input current discharges through the two dc bus capacitors \( C_{b1} \) and \( C_{b2} \), this discharge time \( d_{2,k} T_s \) is given by:

\[ d_{2,k} = \frac{v_{in,k}}{2} - \frac{D_k}{V_{bus}} \]  \hspace{1cm} (2.12) \]

The average value of the input current over one switching cycle is determined by:

\[ i_{Lin(ave)_{-2}} = \frac{1}{4L_{in} f_s \left( V_{bus} - v_{in,k} \right)} \left[ D_k v_{in,k} \left( V_{bus} - v_{in,k} \right) + \frac{1}{2} \left( v_{in,k} - V_{bus} \left( 0.5 - D_k \right) \right) \left( V_{bus} \left( 0.5 - D_k \right) + v_{in,k} \left( 2D_k - 0.5 \right) \right) \right] \]  \hspace{1cm} (2.13) \]
**Pattern 3:** all the energy of the boost inductor is transferred to the two dc bus capacitors. \(d_{1,k}\) is zero in this pattern and the calculating of \(d_{2,k}\) is similar as in **Pattern 2**:

\[
d_{2,k} = \frac{V_{in,k}}{V_{bus} - V_{in,k}} D_k = \frac{V_{in,k}}{2 (\frac{V_{bus} - V_{in,k}}{2})} \tag{2.14}
\]

Similar to **Pattern 2**, the average value of the input current in one switching cycle is determined by replacing \(D_k\) in equation (3.13) with 0.5:

\[
i_{Lin,ave} = i_{Lin,ave} (D_k = 0.5) = \frac{1}{4 L_m f_s} \left[ 0.5 V_{in,k} (V_{bus} - V_{in,k}) + \frac{1}{4} (V_{in,k})(0.5 V_{in,k}) \right] \tag{2.15}
\]

Figure 3.10 shows the input current during one half cycle of the input ac voltage. **Pattern 1** happens when the input ac voltage is low, **Pattern 2&3** happens when the input ac voltage is high. The boundary between two different patterns is \(\theta_{cr}\), which could be calculated by

\[
\theta_{cr} = \arcsin \left[ \frac{V_{bus} (1 - 2D_k)}{2V_m} \right] \tag{2.16}
\]

Figure 3.10. The input current during one half cycle of the input ac voltage

When \(0 < \omega t < \theta_{cr}\) and \((\pi - \theta_{cr}) < \omega t < \pi\), the input current is in **Pattern 1**. When \(\theta_{cr} < \omega t < (\pi - \theta_{cr})\), the input inductor is in **Pattern 2&3**. If the input ac voltage at each switching cycle is determined by:
$$V_{m,k} = V_m \sin(\omega_k t)$$

where $V_m$ is the maximum value of the input ac voltage. Combine equation (3.17) and equation (3.11), (3.13), (3.15), the average value of input power can be calculated by integral the input ac voltage and the average value of the input current over a half cycle of input ac voltage.

$$P_{in} = \frac{2}{\pi} \left( \int_{0}^{\theta_0} V_{m,k}i_{Lin(ave)}_{h,k} d(\omega_k t) + \int_{\theta_0}^{\pi/2} V_{m,k}i_{Lin(ave)}_{l,k} d(\omega_k t) \right)$$

(2.18)

### 3.4.2 DC Bus Capacitor Selection

When the duty cycle is less than 0.5, the voltages of the two dc bus capacitors are shown as Figure 3.11. The relation of peak to peak dc bus voltage ripple $V_{bus\_ripple}$ is similar to conventional boost PFC converter, which could be calculated as:

$$V_{bus\_ripple} = \frac{P_{out}}{2\pi f_{line} C_{eff\_bus} V_{bus}} = \frac{P_{out}}{\pi f_{line} C_{b1(b2)} V_{bus}}$$

(2.19)

where $P_{out}$ is the output power, $f_{line}$ is the line frequency of input ac power, The $C_{eff\_bus}$ is the equivalent dc bus capacitance, which is equal to half of the capacitance of one dc bus capacitor ($C_{b1(b2)}$) as the two dc bus capacitors are in series. Depending on different requirement of $V_{bus\_ripple}$, the minimum value of the dc bus capacitance could be calculated as:

$$C_{b1(b2)} \leq \frac{P_{out}}{\pi f_{line} V_{bus\_ripple} V_{bus\_avg}}$$

(2.20)

Another key ripple to be considered is the voltage difference between the two dc bus capacitors as Figure 3.7 shows. The voltages difference of the two dc bus capacitor $v_{cb1}(t) - v_{cb2}(t)$ is a sinusoid waveform with the same frequency of input ac voltage $v_{in}(t)$. The absolute maximum value of $v_{cb1}(t) - v_{cb2}(t)$ happens when $v_{in}(t)$ is zero, which is the end of every half-cycle of the input ac voltage.
When $t = t_1$, the voltages of two dc bus capacitors $v_{cb1}$ and $v_{cb2}$ are:

$$v_{cb1}(t_1) = \frac{1}{2}(V_{bus\_avg} + \Delta v)$$

$$v_{cb2}(t_1) = \frac{1}{2}(V_{bus\_avg} - \Delta v)$$

(2.21)

where $\Delta v$ is the amplitude of the peak-peak ripple of the voltage difference between the two dc bus voltages $(v_{cb1}(t) - v_{cb2}(t))$.

Therefore, when $t = t_2$, $v_{cb1}$ and $v_{cb2}$ could be presented as:

$$v_{cb1}(t_2) = \frac{1}{2}(V_{bus\_avg} - \Delta v)$$

$$v_{cb2}(t_2) = \frac{1}{2}(V_{bus\_avg} + \Delta v)$$

(2.22)
From \( t_1 \) to \( t_2 \), the energy stored in \( C_{b1} \) and \( C_{b2} \) has a change of \( \Delta E_{cb1} \) and \( \Delta E_{cb2} \) respectively, \( \Delta E_{cb1} \) and \( \Delta E_{cb2} \) could be calculated as:

\[
\Delta E_{cb1} = E_{cb1}(t_2) - E_{cb1}(t_1) = \frac{1}{2} C_{bus} (v_{cb1}^2(t_2) - v_{cb1}^2(t_1)) = \frac{1}{2} C_{bus} (v_{cb1}(t_2) + v_{cb1}(t_1))(v_{cb1}(t_2) - v_{cb1}(t_1))
\]

\[
\Delta E_{cb2} = E_{cb2}(t_2) - E_{cb2}(t_1) = \frac{1}{2} C_{bus} (v_{cb2}^2(t_2) - v_{cb2}^2(t_1)) = \frac{1}{2} C_{bus} (v_{cb2}(t_2) + v_{cb2}(t_1))(v_{cb2}(t_2) - v_{cb2}(t_1))
\]  

(2.23)

Plug equation (3.21) and equation (3.22) into equation (3.23), then the difference of \( \Delta E_{cb2} \) and \( \Delta E_{cb1} \) is given as:

\[
\Delta E_{cb2} - \Delta E_{cb1} = \frac{1}{2} C \Delta v_{bus\_avg} - \left( \frac{1}{2} C \Delta v_{bus\_avg} \right) = C_{bus} \Delta v_{bus\_avg} 
\]

(2.24)

The energy stored in a capacitor could also be calculated with the total charge it stores. Therefore, \( \Delta E_{cb1} \) and \( \Delta E_{cb2} \) could also be described as:

\[
\Delta E_{cb1} = \frac{1}{2} C_{bus} Q_{cb1}^2(t_2) - \frac{1}{2} C_{bus} Q_{cb1}^2(t_1) = \frac{1}{2} C_{bus} (Q_{cb1}(t_2) + Q_{cb1}(t_1))(Q_{cb1}(t_2) - Q_{cb1}(t_1))
\]

\[
\Delta E_{cb2} = \frac{1}{2} C_{bus} Q_{cb2}^2(t_2) - \frac{1}{2} C_{bus} Q_{cb2}^2(t_1) = \frac{1}{2} C_{bus} (Q_{cb2}(t_2) + Q_{cb2}(t_1))(Q_{cb2}(t_2) - Q_{cb2}(t_1))
\]  

(2.25)

where \( Q_{cb1} \) and \( Q_{cb2} \) are the charges stored in \( C_{b1} \) and \( C_{b2} \) respectively.

With equation (3.21) and equation (3.22), \( Q_{cb1}(t_2) + Q_{cb1}(t_1) \) and \( Q_{cb2}(t_2) + Q_{cb2}(t_1) \) could be rewritten as:

\[
Q_{cb1}(t_2) + Q_{cb1}(t_1) = C_{bus} \left( \frac{1}{2} (V_{bus\_avg} - \Delta v) + \frac{1}{2} (V_{bus\_avg} + \Delta v) \right) = C_{bus} V_{bus\_avg}
\]

\[
Q_{cb2}(t_2) + Q_{cb2}(t_1) = C_{bus} \left( \frac{1}{2} (V_{bus\_avg} - \Delta v) + \frac{1}{2} (V_{bus\_avg} + \Delta v) \right) = C_{bus} V_{bus\_avg}
\]  

(2.26)

Combine with equation (3.24) and equation (3.25), \( \Delta E_{cb1} \), \( \Delta E_{cb2} \) and \( \Delta E_{cb2} - \Delta E_{cb1} \) could be described as:

\[
\Delta E_{cb1} = \frac{1}{2} V_{bus\_avg} (Q_{cb1}(t_2) - Q_{cb1}(t_1)) = \frac{1}{2} V_{bus\_avg} \Delta Q_1
\]

\[
\Delta E_{cb2} = \frac{1}{2} V_{bus\_avg} (Q_{cb2}(t_2) - Q_{cb2}(t_1)) = \frac{1}{2} V_{bus\_avg} \Delta Q_2
\]

\[
\Delta E_{cb2} - \Delta E_{cb1} = \frac{1}{2} V_{bus\_avg} (\Delta Q_2 - \Delta Q_1)
\]  

(2.27)

where \( \Delta Q_1 \) and \( \Delta Q_2 \) are the changes of the charges stored in \( C_{b1} \) and \( C_{b2} \) respectively from \( t_1 \) to \( t_2 \).

Combine equation (3.24) and equation (3.27), \( \Delta v \) could be expressed as:
\[ \Delta V = \frac{1}{2C_{\text{bus}}} (\Delta Q_2 - \Delta Q_1) \]  

(2.28)

\(\Delta Q_2 - \Delta Q_1\) is the overcharge goes to \(C_{b2}\) from \(t_1\) to \(t_2\). This could be calculated by the integral of the overcharge current of \(C_{b2}\) from \(t_1\) to \(t_2\). Since the current go through the clamping diode \(D_{c2}\) is the same as the overcharge current of \(C_{b2}\), \(\Delta Q_2 - \Delta Q_1\) could be calculated as:

\[ \Delta Q_2 - \Delta Q_1 = \int_{t_1}^{t_2} i_{Dc2}(t)dt = \frac{1}{2\pi f_{\text{line}}} \int_{\pi}^{2\pi} i_{Dc2}(\omega t)d\omega t \]  

(2.29)

where \(i_{Dc2}\) is the current goes through the clamping diode \(D_{c2}\).

According to the analysis of different discharge pattern for the boost inductor in section 3.4.1, the average current go through \(D_{c2}\) during one switching cycle \(k\) is:

\[
\begin{aligned}
    i_{Dc2-avg}^k & = i_{\text{Lin_peak1}}^k (0.5 - D) \quad \text{when } \pi < \omega t < \pi + \theta_{cr} \text{ and } (2\pi - \theta_{cr}) < \omega t < 2\pi \\
    i_{Dc2-avg}^k & = \frac{1}{2} (0.5 - D) (i_{\text{Lin_peak2}}^k + i_{\text{Lin_peak1}}^k) \quad \text{when } \pi + \theta_{cr} < \omega t < 2\pi - \theta_{cr}
\end{aligned}
\]  

(2.30)

from \(\pi\) to \(2\pi\), \(i_{\text{Lin_peak1}}^k\) and \(i_{\text{Lin_peak2}}^k\) could be calculated with equation (3.2) and equation (3.11).

Therefore, the peak to peak voltage ripple of the voltage difference between the two dc bus capacitors is given as:

\[
V_{\text{diff pp}} = 2\Delta V = \frac{1}{4\pi f_{\text{line}} C_{\text{bus}}} \left[ \int_{\pi}^{\pi + \theta_{cr}} i_{Dc2-avg1}^k (\omega t) d\omega t + \int_{\pi + \theta_{cr}}^{2\pi} i_{Dc2-avg2}^k (\omega t) d\omega t \right]
\]  

(2.31)

Figure 3.8 and Figure 3.9 show \(V_{\text{diff pp}}\) for different duty cycle under 400V dc bus voltage and 800V dc bus voltage when \(f_s\) is 200kHz. \(V_{\text{diff pp}}\) reaches the maximum value when \(D\) is around 0.3. This is because although the conducting time of the clamp diode is longer when \(D\) is low, the amplitude of the conducting current is much lower, which result in a smaller \(\Delta Q_2 - \Delta Q_1\) compared to higher duty cycle.
Therefore, based on equation (3.20), (3.30) and (3.31), the capacitance of the dc capacitor could be properly selected with desired requirement of $V_{bus\_ripple}$ and $V_{diff\_pp}$.

Figure 3.12. peak to peak voltage difference between two dc bus capacitors ($V_{bus\_avg} = 400$V and $f_s = 200$ kHz)

Figure 3.13. peak to peak voltage difference between two dc bus capacitors ($V_{bus\_avg} = 800$V and $f_s = 200$ kHz)
3.4.3 DC-DC Resonant Converter Stage

Figure 3.10 shows the simplified circuit model of the DC-DC resonant converter stage of the proposed converter. The steady state analysis of this stage from dc bus to the output could be conducted with frequency domain analysis.

![Circuit Diagram]

Figure 3.14 Model of Resonant Converter with $v_{ab}$ and $i_s$

Since the LC filter is used in a series-parallel resonant converter, the equivalent ac load resistance $R_{ac}$ is determined by:

$$R_{ac} = \frac{\pi^2}{8} \left( \frac{N_1}{N_2} \right)^2 R_L$$

(2.32)

where $R_L$ is the load resistance, $N_1$ and $N_2$ are the turns of the primary side and secondary side of the high frequency transformer. $N_1:N_2$ is set to 1 to simplify the transformer design. The voltage across the resonant circuit $v_{ab}$ could be expressed as the following:

$$v_{ab} = \sum_{odd \, n} \frac{2}{n\pi} V_{bus} \sin(\pi D) \sin(2\pi nf_t t)$$

(2.33)

where $D$ is the duty cycle, $f_s$ is the switching frequency and $V_{bus}$ is the dc bus voltage generated by the rectifier stage.

The voltage across the parallel capacitor $v_{cp}$ is:

$$v_{cp} = \sum_{odd \, n} \frac{2}{n\pi} V_{bus} \left| \frac{Imp_{p(n)}}{Imp_{tot(n)}} \right| \sin(2\pi nf_st \, t + \phi_n)$$

(2.34)
where:

\[ \text{Imp}_{p(n)} = \frac{R_{ac}(1 - jnw_{r}R_{ac}C_{p})}{1 + n^{2}w_{r}^{2}R_{ac}^{2}C_{p}^{2}} \]  

(2.35)

\[ \text{Imp}_{\text{tot}(n)} = \frac{R_{ac}}{1 + n^{2}w_{r}^{2}R_{ac}^{2}C_{p}^{2}} + j \left( nw_{r}L_{r} - \frac{1}{nw_{r}C_{s}} - \frac{nw_{r}R_{ac}C_{p}}{1 + n^{2}w_{r}^{2}R_{ac}^{2}C_{p}^{2}} \right) \]  

(2.36)

\[ \varphi_{n} = \tan^{-1} \left( \frac{\text{Im}\left( \text{Imp}_{p(n)} \right)}{\text{Re}\left( \text{Imp}_{p(n)} \right)} \right) - \tan^{-1} \left( \frac{\text{Im}\left( \text{Imp}_{\text{tot}(n)} \right)}{\text{Re}\left( \text{Imp}_{\text{tot}(n)} \right)} \right) \]  

(2.37)

In order to simplify the calculation, \( v_{cp} \) could be approximated by only considering the fundamental frequency component (\( n=1 \) in equation (3.33-3.36)):

\[ v_{cp} \approx \frac{2}{\pi} V_{bus} \sin(\pi D) \left| \text{Imp}_{p(1)} \right| \sin(2\pi nfst + \varphi) \]  

(2.38)

the amplitude of \( v_{cp} \) could be presented as:

\[ V_{cp} = (v_{cp})_{\text{peak}} = \left( \frac{2V_{bus} \sin(\pi D)}{\pi} \right) \left[ (1 + K - K \left( \frac{f_{r}}{f_{s}} \right)^{2} + jQ \left( \frac{f_{r}}{f_{s}} - \frac{f_{r}}{f_{s}} \right) \right] \]  

(2.39)

The output dc voltage after the diode bridge and \( LC \) filter is the average of the absolute value of \( v_{cp} \), which could be calculated as:

\[ V_{out} = \frac{4V_{bus} \sin(\pi D)}{\pi^{2} \left[ (1 + K - K \left( \frac{f_{r}}{f_{s}} \right)^{2} + jQ \left( \frac{f_{r}}{f_{s}} - \frac{f_{r}}{f_{s}} \right) \right] \]  

(2.40)

where:

\[ f_{r} = \frac{1}{2\pi \sqrt{L_{r}C_{s}}}, \quad Q_{r} = \frac{2\pi f_{r}L_{r}}{R_{ac}}, \quad K = \frac{C_{p}}{C_{s}} \]  

(2.41)

\( Q_{r} \) is the quality factor of the resonant converter, \( f_{r} \) is the resonant frequency determined by the series inductor \( L_{r} \) and series capacitor \( C_{s} \), \( K \) is the ratio of the parallel capacitor \( C_{p} \) and series capacitor \( C_{s} \).
Figure 3.15. Output voltage for different $Q$ and $K$ ($V_{bus} = 400V$, $D = 0.5$, $P_{out} = 1kW$).
Normally, when the resonant frequency $f_r$ is fixed, higher value of $K$ results in a narrower switching frequency variation range but higher circulating current for the same change of the load. A carefully design trade-off should made between $K$ and the desired frequency variation range. While the value of $Q$ features the gain curve significantly. Higher vaule of $Q$ results in a low voltage gain. In order to achieve sufficient gain over all the load range, the worst case of maximum load and lowest dc bus voltage should be considered. Figure 3.15 shows the output voltage of the resonant convert for different $Q$ and $C_p/C_s$ with $V_{bus} = 400V$, $D = 0.5$ and 1kW output power. $f_r$ is chosen to be 160 kHz.

Although $V_{bus}$ varies in a wide ranged from 400V to 800V, the fundenmental component of $V_{ab}$ varies much less significantly compared to the dc bus voltage. This is because in order to transfer same amount of power, $D$ is normally much smaller when $V_{bus}$ is high compared to the $D$ when $V_{bus}$ is low. Based on equation (2.33), the change $V_{ab}$ is small since it is proportional to the product of $D$ and $V_{bus}$. Therefore, the voltage gain range and frequency variation range required for the DC-DC resonant converter stage is narrower and $K$ could have a smaller value. $K$ is chosen to be 1.5 for the prototype converter used in the simulation and experiment.

### 3.4.4 Decoupled Model of the Proposed Converter

As the converter has two control variables (duty cycle and switching frequency), steady state analysis and design of the proposed converter is complex as the two variables influence each other. However, since the dc bus capacitors is large and the dc bus voltage variation is much slower than the output voltage, the bandwidth of the duty cycle loop is much smaller than the switching frequency loop. The dc bus capacitor could be considered as a voltage source and the converter could be decoupled into two parts: a rectifier and a resonant DC-DC converter. This model is shown in Figure 3.16

The rectifier part generates a constant dc bus voltage. The resonant circuit and load are considered as an equivalent dc load $R_{eq}$ connected in parallel with the dc bus capacitors. The resistance of $R_{eq}$ determines the amount of power which the rectifier stage is delivering ($P(R_{eq})$).
The resonant converter part is very similar as the conventional DC-DC resonant converter, the input of this part is considered as a quasi-square voltage source, where the amplitude is determined by duty cycle and dc bus voltage. Assuming all converter losses are negleleted, power balance between the two parts should always be achieved: the resonant converter part should absorb exactly the same amount of power generated by the rectifier part.

The power delivered by the rectifier part can be calculated using equation (3.18). Figure 3.17 and Figure 3.18 show $P(Req)$ for different duty cycles under 110Vrms and 220Vrms input ac voltage. As the graph shows, the power delivered by the rectifier is mainly determined by the duty cycle. However, switching frequency also slightly affects the delivered power since the converter is in DCM. Normally, lower switching frequency delivered a higher amount of power. In order to maintain the dc bus voltage to a desired level (400V and 800V in Figure 3.17 and Figure 3.18), the switching frequency and output power of the resonant converter part should match the curves of. For an example, according to Figure 3.17. The output power of resonant converter part should be around 600W when its switching frequency and duty cycle are 210kHz and 0.4 respectively to maintain a 400V dc bus voltage.

![Figure 3.16. Decoupled model of the proposed converter](image)

$$V_{in} \rightarrow \text{Rectifier} \rightarrow V_{bus} \rightarrow R_{eq} \rightarrow P(Req) \rightarrow v_{ab}(fs,V_{bus}) \rightarrow \text{Resonant Converter} \rightarrow R_L$$
Figure 3.17. Power delivered by the Rectifier ($P(R_{eq})$) at $V_{in} = 110\text{Vrms}$, $V_{bus} = 400\text{V}$.

Figure 3.18. Power delivered by the Rectifier ($P(R_{eq})$) at $V_{in} = 220\text{Vrms}$, $V_{bus} = 800\text{V}$.
If duty cycle and dc bus voltage are already known, the power absorbed by the resonant converter could be calculated with equation (3.40). Figure 3.19 and Figure 3.20 show power absorbed by the resonant converter with different $Q$ (blue curves) and the power delivered by the rectifier (red curve) with a fixed duty cycle. For both figures, the output voltage is regulated at 380V. Because of the power balance feature discussed above, the proposed converter could only operate at the intersection of blue curves and red curve with the desired dc bus voltage and output voltage. All the operating point of the proposed converter can be found out with this method. Figure 3.21 shows the operating points for different output power with the chosen parameters in section 3.4.3. The dc bus voltage and output voltage are well regulated to the desired value for all the operating points. It could be noticed that the frequency variation is very narrow for a wide load range. The output power is higher than 1 kW and the switching frequency is higher than the resonant frequency. Therefore, the chosen parameters meet the design requirement of the proposed converter.

Figure 3.19. Operating area of the proposed converter when $D = 0.48$, $V_{bus} = 400V$
Figure 3.20. Operating area of the proposed converter when $D = 0.17$, $V_{bus} = 800V$.

Figure 3.21. Operating points for the proposed converter with the chosen parameters at $V_{in} = 110V$ rms.
3.5 Simulation Results

A 1kW, 380V bridgeless single stage AC-DC resonant converter prototype is designed to verify the effectiveness of the proposed topology. Table 3.1 shows the component parameters of the converter. The resonant frequency of the resonant circuit is set to 160 kHz and ZVS is achieved by operating the converter above the resonant frequency. The PSIM9.0 simulation schematic is in Appendix A. Turns ratio for the primary and secondary side of the high frequency transformer is set to 1:1. The output voltage is regulated as The dc bus voltage is regulated from 400V to 800V as equation (2.6) shows.

<table>
<thead>
<tr>
<th>Component Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>110-220Vrms</td>
</tr>
<tr>
<td>Output voltage</td>
<td>380V</td>
</tr>
<tr>
<td>DC bus capacitor ((C_{b1,2}))</td>
<td>2200µF</td>
</tr>
<tr>
<td>Boost inductor ((L_{in}))</td>
<td>10uH</td>
</tr>
<tr>
<td>Resonant series inductor ((L_o))</td>
<td>66uH</td>
</tr>
<tr>
<td>Resonant series capacitor ((C_s))</td>
<td>15nF</td>
</tr>
<tr>
<td>Resonant parallel capacitor ((C_p))</td>
<td>22.5nF</td>
</tr>
<tr>
<td>Transformer turns-ratio ((N_1:N_2))</td>
<td>1:1</td>
</tr>
<tr>
<td>Output filter inductor ((L_f))</td>
<td>200µH</td>
</tr>
<tr>
<td>Output filter capacitor ((C_f))</td>
<td>50µF</td>
</tr>
</tbody>
</table>

Table 3.1. Circuit component selection for the proposed converter.

The converter could achieve an almost unity power factor as Figure 3.22 shows. At the light load condition, since \(D\) is small, Pattern1 input current dominates the full cycle of the input ac voltage, which causes more
current distortion and decrease the power factor. Figure 3.23 and Figure 3.24 are the filtered input current and input voltage with 50% load under $V_{in} = 110\text{Vrms}$ and $V_{in} = 220\text{Vrms}$, the current harmonic components compliance with IEC1000-3-2 standards [30].

![Graph showing power factor with $V_{in} = 110\text{Vrms}$ and $V_{in} = 220\text{Vrms}$ under different load conditions (simulation)]

Figure 3.22 Power factor with $V_{in} = 110\text{Vrms}$ and $V_{in} = 220\text{Vrms}$ under different load conditions (simulation)

Figure 3.25 presents voltage of the two dc bus capacitor $V_{Cb1}$ and $V_{Cb2}$ and their difference under different load conditions with $V_{in} = 110\text{Vrms}$ and $V_{in} = 220\text{Vrms}$. When $V_{in} = 110\text{Vrms}$, the highest voltage difference between two dc bus voltages is 8V at 50% load when $D$ is around 0.3, which is around than 2% of total dc bus voltage and negligible. The voltage difference decrease to 5V at 20% load when $D$ is smaller than 0.3. This is coincident with the capacitor voltage difference analysis in section 3.3.2. When $V_{in} = 220\text{Vrms}$, since the duty cycle is already lower than 0.3 at the full load. The maximum voltage difference happens at full load and it keep decreasing with the load. The maximum voltage difference is around 10V, which is around 1.25% of the total dc bus voltage.
Figure 3.23. 110Vrms input voltage ($v_{in}$), filtered input current ($i_{emc}$) and its harmonics with 50% load

Figure 3.24. 220Vrms input voltage ($v_{in}$) and filtered input current ($i_{emc}$) and its harmonics with 50% load
Figure 3.25. $V_{cb1}$, $V_{cb2}$ and their difference under different load condition at $V_{bus} = 400$V.

Figure 3.26. $V_{cb1}$, $V_{cb2}$ and their difference under different load condition at $V_{bus} = 800$V.
In order to illustrate the ZVS operation for all four switches of the proposed converter. Figure 3.27 and Figure 3.28 show the switch voltage and current one of the upper switch ($S_2$) and one of the bottom switch ($S_3$) with 400V and 800V dc bus voltage receptively. The negative currents inside the circle guarantee the ZVS of $S_2$ and $S_3$. $S_1$ and $S_4$ also have ZVS as they are turned on at the same time of $S_2$ and $S_3$ respectively.

In Figure 3.27, it is obvious that the negative switch current inside the circle of $S_2$ is much larger than bottom switch during the dead time. This is because when the input ac voltage is at the positive half-cycle, the sum of resonant current and boost inductor current goes through $S_2$ to discharge the drain source capacitor of $S_2$. For bottom switch, only the difference between the resonant current and input inductor current is used for discharging the drain source capacitor. Figure 3.29 and Figure 3.30 present the resonant current and resonant circuit voltage under different load conditions with 400V and 800V dc bus voltage respectively. As discussed above, the duty cycle is much bigger with heavy load compared with light load. But in either situation, the resonant current is always lagging the resonant circuit voltage.

![Figure 3.27. ZVS operation illustration of upper switches ($S_2$) and bottom switch ($S_3$) with $V_{bus} = 400V$](image)

![Figure 3.27. ZVS operation illustration of upper switches ($S_2$) and bottom switch ($S_3$) with $V_{bus} = 400V$](image)
Figure 3.28. ZVS operation illustration of upper switches \((S_2)\) and bottom switch \((S_3)\) with \(V_{bus} = 400V\)

Figure 3.29. resonant current \(i_s\) and resonant circuit voltage \(v_{ab}\) when \(V_{bus} = 400V\)
Figure 3.30. resonant current $i_r$ and resonant circuit voltage $v_{ab}$ when $V_{bus} = 800\text{V}$.

3.6 Experimental Results

An experimental prototype converter is designed to verify the effectiveness of the proposed converter. The main power circuit is separated into two PCB boards. The first board contains the boost inductor, four main switchers and the two dc bus capacitors. The second board contains the resonant circuit, transformer and the output rectifier circuit. The schematic and PCB layouts for the two PCB boards are in Appendix B.

Since the three-level converter has four switches connected in series and the switch voltage is high. The traditional bootstrap half bridge gate driver is not applicable in the proposed converter. Four identical isolated driver circuit boards are designed. The four boards are designed as separated from the main power circuit. In order to decrease the intrinsic inductance of the gate driving loop, they are plugged very close to the four switches. The PCB schematic and layout for the gate driver board are also in Appendix B.
Since the converter switching frequency is high and it emit high amount of EM noise. Isolation is also preferred for the sampling circuit of the prototype converter to achieve a better accuracy. Two isolation amplifiers (TI AMC1200) are used for the sampling circuit. They are powered up by two isolating DC-DC modular converters. Digital control with TI TMS320F28335 DSP chip is implemented for the two control loops of the prototype converter.

Figure 3.31 (a) shows the input voltage, filtered input current and the two dc bus voltages. The input current is almost pure sinusoid waveform and a high power factor of 0.995 is achieved for the waveforms in Figure 3.31 (a). Figure 3.31 (b) shows the voltages of two dc bus capacitors. It is obvious that the two dc bus voltages almost same. That indicates the dc bus voltage is equally distribute on the two dc bus capacitors as analyzed before.

Figure 3.32 shows the AC coupling of voltages of the two dc bus capacitors under different duty cycles. The two dc bus capacitor voltage has a higher difference when $D = 0.3$ compared to $D = 0.18$. This is consistent with the above analysis. The voltage difference at $D = 0.3$ is less than 2V with a 140V dc bus voltage. This difference is less than 2% of the total dc bus voltage with the chosen capacitance. This tiny variation will not influence the operation of the converter and each dc bus capacitor could be considered as holding half of the total dc bus voltage.

Figure 3.33 shows the resonant current and the voltage applied to the resonant circuit at different duty cycles. The lagging current is ensured by operating the converter above the resonant frequency. Since the operation of top two switches and bottom two switches are symmetrical. Only the zero voltage switching operations of the top two switches $S_1$ and $S_2$ are illustrated by Figure 3.34. The drain source capacitor starts to discharge due to the lagging resonant current and input current. It is clear that the drain source voltage is very close to zero before the gate source voltage starts to increase for both switches.
Figure 3.31. (a) input voltage ($v_{in}$) and filtered input current ($i_{emc}$), (b) $V_{cb1}$ and $V_{cb2}$ (DC coupling)

Figure 3.32. $V_{cb1}$ and $V_{cb2}$ (AC coupling) and filtered input current when $V_{bus}$=140V at (a) $D = 0.3$, (b) $D = 0.18$
Figure 3.33. Resonant voltage ($V_{ab}$) and resonant current ($i_r$) at (a) high duty cycle, (b) low duty cycle.

Figure 3.34. Gate voltage ($v_{gs}$) and switch voltage ($v_{ds}$) to illustrate ZVS for (a) $S_2$, (b) $S_l$. 
Chapter 4

ZVS Bidirectional DC-DC converter

4.1 Introduction

In Chapter 3, a new single-stage AC-DC converter was proposed for the main AC-DC part of the new DC UPS proposed in Chapter 1. In this chapter, a ZVS bidirectional DC-DC converter will be presented as the battery side converter to charge and discharge the battery.

The isolated bidirectional DC-DC converter is a key part in DC UPS applications. When the input ac is on, this converter absorbs power from the input ac and charges the battery packs with a regulated battery charging current. When the input ac is off and the main AC-DC converter stops working, this converter starts delivering power from the battery packs to the output load with a regulated output voltage. Isolation is often required to separate the battery pack and the main power circuit for safety and reliability.

The outline of this chapter is as follows: Section 4.2 describes the principle operation and steady state analysis of the proposed converter. In Section 4.3, simulation results are provided to check the effectiveness of the proposed concept.

4.2 Proposed Battery Side Converter

Figure 4.1 shows the circuit diagram of the proposed converter. It consists of a full bridge and a series resonant tank. The isolation is provided by sharing the same high frequency transformer in the main AC-DC converter. The control of the proposed converter is very similar as the self-sustained oscillating control proposed in [72]. When the input ac is available, the proposed converter is in battery charging mode to charge the battery. When the input ac is off, the proposed converter is in battery discharging mode to deliver power from the battery to the load. In both modes, the frequency is used to achieved ZVS for all switches.
and the phase shift between two legs of the full bridge is used to regulate the output of the converter. In the rest of this section, the steady state operation and design of the proposed converter in both modes will be described in details

![Proposed battery side converter](image)

**Figure 4.1. Proposed battery side converter**

### 4.2.1 Battery Charging Mode

When the utility ac is available within its acceptable range, the main AC-DC converter is converting the ac input to a regulated dc output voltage. While the battery side converter absorbs power from the main AC-DC converter and regulating the battery charging current. Since the battery side converter and the main AC-DC converter are sharing one high frequency transformer, the parallel resonant capacitor $C_p$ in the main AC-DC converter is also delivering power to the battery side converter through the higher frequency transformer. The circuit diagram of the battery side converter is shown in Figure 4.2.

According to equation (3.39), when the output voltage is regulated at 380V, the amplitude of the input high frequency voltage $V_{cp}'$ is equal to:

$$V_{cp}' = \frac{N_3}{N_1} V_{cp} = 600 \frac{N_3}{N_1}$$

(3.1)

where $N_3$ and $N_1$ are the turns ratio of primary side and tertiary side of the high frequency transformer $V_{cp}$ is the high frequency voltage on the parallel capacitor of the main AC-DC converter. By controlling the full
bridge consists of $S_{b1}$ to $S_{b4}$, the battery charging current $i_b$ could be regulated and all four switches could have ZVS for a wide load range.

When utility ac is on and the output of main AC-DC converter is regulated, the amplitude of the high frequency voltage input $v'_{cp}$ to the battery side converter is also regulated and could be consider as a voltage source. Although the frequency of the $v'_{cp}$ is varying, this variation will not affect the power delivered to the battery. Assume the battery voltage is also a constant value. The equivalent circuit of the battery side converter is shown in Figure 4.3.

$$L_{eq}$$

![Equivalent circuit of the battery side converter in battery charging mode](image)

Figure 4.3. Equivalent circuit of the battery side converter in battery charging mode

The equivalent inductance $L_{eq}$ could be calculated as:

$$L_{eq} = \frac{f_{i2}^2}{f_{i2}^2 / f_{i2}^2} - 1$$

(3.2)
Where $f_{s2}$ is the switching frequency of the battery side converter and $f_{r2}$ is the resonant frequency determined by $L_{s2}$ and $C_{s2}$:

$$f_{r2} = \frac{1}{2\pi\sqrt{L_{s2}C_{s2}}}\quad (3.3)$$

$v_{ab2}$ is the voltage across the two legs of the full bridge consists of $S_{b1}$ to $S_{b4}$. It could be considered as the voltage difference $v_a - v_b$, where $v_a$ is the voltage of leg A and $v_b$ is the voltage of leg B as Figure 4.2 shows. $v_a$ is either battery voltage or ground depending on the gating signal of $S_{b1}$ and $S_{b3}$, similarly $v_b$ is depending on the gating signal of $S_{b2}$ and $S_{b4}$. Figure 4.4 shows the resonant current $i_{s2}$, $v_{ab}$ and the gating signal of the four switches.

![Diagram](image-url)

Figure 4.4. Operations of the battery side converter in charging mode
In Figure 4.4, $\theta_a$ is the phase difference between the resonant current $i_{s2}$ and leg A voltage $v_a$, while $\theta_b$ is the phase difference between the resonant current $i_{s2}$ and leg B voltage $v_b$. $\theta_b$ is kept close to zero degree to ensure the ZVS of all four switches and $\theta_a$ is varying to control the battery charging current. The gating signals of $S_{b1}$ to $S_{b4}$ are generated with two carrier voltages $v_{c1}$, $v_{c2}$ and the saw tooth voltage is based on the zero crossing point of resonant current $i_{s2}$.

The power transfer from $v'_{cp}$ to the battery could be calculated as the integral of $i_{s2}$ and $v_{ab}$ during one full period:

$$P_b = \frac{1}{2\pi f_s} \left( \int_{\pi/2}^{\pi} V_{\text{bat}} i_{s2} \sin \theta d\theta + \int_{\pi}^{2\pi} V_{\text{bat}} i_{s2} \sin \theta d\theta \right) \frac{T_s}{T_s} = \frac{1}{\pi} \left( V_{\text{bat}} I_{s2} \cos \theta_a + V_{\text{bat}} I_{s2} \cos \theta_b \right) \quad (3.4)$$

The amplitude of battery charge current $i_b$ is:

$$I_b = \frac{1}{\pi} \left( I_{s2} \cos \theta_a + I_{s2} \cos \theta_b \right) \quad (3.5)$$

$I_{s2}$ is the amplitude of $i_{s2}$ and $V_{\text{bat}}$ is the battery voltage. Since $I_{s2}$ is varying when $\theta_a$ changes, the relationship of $I_{s2}$ and $\theta_a$ should be found out. The following calculations shows the process to find the relationship.

The input voltage $v'_{cp}$ could be presented as:

$$v'_{cp} = V_{cp} \frac{N_1}{N_1} \sin(2\pi f_s t) = V_{cp} \sin(f_s t) \quad (3.6)$$

$f_s$ is the switching frequency of the main AC-DC converter in chapter 3.

Since the majority of the power is transferred at the fundamental frequency of $v_{ab2}$, only the fundamental component of $v_{ab2}$ is considered and it could be described as:

$$v_{ab2-f} = \frac{4}{\pi} V_{\text{bat}} \sin(\frac{\pi}{2} - \frac{\theta_a}{2}) \sin(2\pi f_s t + \theta_a) = V_{ab2-f} \sin(2\pi f_s t + \theta_a) \quad (3.7)$$
\[ \theta_s \] is the phase difference between \( v_{ab\_f} \) and \( v'_{cp} \), \( V_{ab\_f} \) is the amplitude of \( v_{ab\_f} \), \( f_{s2} \) is the switching frequency of the battery side converter. Because \( \theta_b \) is close to zero, \( f_s \) and \( f_{s2} \) are very similar, equation (3.6) could be rewritten as:

\[ v'_{cp} = V'_{cp} \sin(\omega_s t) = V'_{cp} \frac{N_3}{N_1} \sin(2\pi f_{s2} t) \]  

(3.8)

Combine equation(3.2), (3.7) and (3.8), the resonant current \( i_{s2} \) could be calculated as:

\[ i_{s2} = \frac{V'_{cp}}{j2\pi f_{s2} L_{eq}} + \frac{V_{ab\_f}}{j2\pi f_{s2} L_{eq}} = \frac{V'_{cp} \sin(2\pi f_{s2} t) + V_{ab\_f} \sin(2\pi f_{s2} t + \theta_s)}{j2\pi f_{s2} L_{eq}} \]  

(3.9)

Rewrite equation (3.9) to the phasor form:

\[ i_{s2} = \frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \sin \theta_s - \left( \frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \cos \theta_s + \frac{V_{cp}'}{2\pi f_{s2} L_{eq}} \right) j \]

\[ = \sqrt{\left( \frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \right)^2 + \left( \frac{V_{cp}'}{2\pi f_{s2} L_{eq}} \right)^2} + 2 \cos \theta_s \frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \frac{V_{cp}'}{2\pi f_{s2} L_{eq}} \angle \theta_y = I_{s2} \angle \theta_y \]  

(3.10)

where \( \theta_s \) is the phase difference between \( i_{s2} \) and \( \theta_y \). \( \theta_y \) could be presented as:

\[ \theta_y = \arctan \left( \frac{\frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \cos \theta_s + \frac{V_{cp}'}{2\pi f_{s2} L_{eq}}}{-\frac{V_{ab\_f}}{2\pi f_{s2} L_{eq}} \sin \theta_s} \right) \]  

(3.11)

From Figure 4.4, the phase difference between \( i_{s2} \) and \( v_{ab} \) is \( \frac{\theta_a}{2} \). Therefore, \( \theta_y \) could also be rewrite as

\[ \theta_y = \theta_x - \frac{\theta_a}{2} \]  

(3.12)

Since \( V_{ab\_f} \), \( V'_{cp} \), \( L_{eq} \) and \( \theta_a \) are all given, \( \theta_x \) and \( \theta_y \) could be calculated when combine equation (3.11) and (3.12). After that \( I_{s2} \) could be calculated with equation (3.10) and \( I_b \) could also be calculated using equation (3.5). Figure 4.5 and Figure 4.6 present two examples of \( I_{s2} \) and \( I_b \) with the increasing \( \theta_a \) at different \( L_{eq} \). It could noticed that although \( I_{s2} \) is not monotonous decreasing with the increase of \( \theta_a \), the
battery charge current $I_b$ is always decreasing with the increase of $\theta_a$. Therefore $I_b$ could be well regulated by varying value of $\theta_a$ with conventional PI control. Small $L_{eq}$ and higher $V'_{cp}$ give a higher battery charge current but also much higher resonant current $I_{s2}$ which increase the conduction loss of the converter. If the maximum battery charge current is set to be 10A and $V_{cp}$ is selected as 200V. $L_{eq}$ is chosen around 8µH according to Figure 4.6. Therefore the turns ratio $N_2 : N_1$ is set to 1:3 according to equation (4.1).

![Figure 4.5. resonant current (I_s) with different $\theta_a$ at $f_s = 220$kHz for (a) $V'_{cp} = 150$V (b) $V'_{cp} = 200$V](image1)

![Figure 4.6. battery charge current (I_b) with different $\theta_a$ at $f_s = 220$kHz for (a) $V'_{cp} = 150$V (b) $V'_{cp} = 200$V](image2)
The controller of the battery side converter in this mode is presented as Figure 4.7.

![Controller of the battery side converter (charging)](image)

**Figure 4.7.** Controller of the battery side converter in battery charging mode

### 4.2.2 Battery Discharging Mode

When the input ac is off, the battery starts to deliver power to the load. In this mode the battery side converter is working as a DC-DC series parallel resonant converter which utilized $C_p$ of the main AC-DC converter as its parallel resonant capacitor through the high frequency transformer. The circuit diagram is shown in Figure 4.8. The direction of $i_{s2}$ and $i_{s1}$ is the same as the direction in Figure 4.2 to keep the consistence for the analysis, but they should always be negative as the battery is discharging.
However, different with the main AC-DC converter, both frequency and phase shift are used to regulate the output voltage to achieve a better efficiency and smaller frequency variation in the battery side converter. As Figure 4.9 shows, the switch operations for the battery discharge mode is very similar as in the battery charge mode. When the battery is discharging, $-i_{s2}$ is lagging $v_{ab}$. The positive edge of $v_{ab}$ decides the converter has ZVS or not. Hence, $\theta_a$ should be kept close to 180 degree to ensure ZVS. While $\theta_b$ is changing from 0 to 180 degree to control the output power. According to equation (3.4), the range of transferred power in this mode is:

$$\frac{2}{\pi} I_{s2} V_{\text{batt}} < P_b < 0 \quad (0 < \theta_b < \pi, \theta_a \approx \pi) \quad (3.13)$$

The sign of $P_b$ is negative because the battery is delivering power. The generation of saw tooth waveform and control voltage $V_{c1}$ and $V_{c2}$ are identical as in the battery charging mode when $\theta_a$ and $\theta_b$ is well defined.
Figure 4.9. Operations of the battery side converter in the battery discharge mode

Figure 4.10. Equivalent circuit of the battery side converter in battery discharging mode

The equivalent circuit for the battery side converter is shown in Figure 4.10. Assume the high frequency transformer is ideal. The equivalent parallel capacitor $C_{p2}$ and equivalent ac resistor $R_{ac2}$ are:
\[ C_{ps} = \left( \frac{N_1}{N_3} \right)^2 C_p \]  

(3.14)

\[ R_{ac2} = \frac{\pi^2}{8} \left( \frac{N_3}{N_2} \right)^2 R_L \]  

(3.15)

Since \( N_1 = N_2 \) from the design in chapter 3, equation (3.15) could be rewrite as:

\[ R_{ac2} = \frac{\pi^2}{8} \left( \frac{N_3}{N_1} \right)^2 R_L \]  

(3.16)

The amplitude of the fundamental voltage of \( v_{ab} \) is \( V_{ab2-f} \):

\[ V_{ab2-f} = \frac{4}{\pi} V_{bas} \sin(\frac{\theta_b + \pi - \theta_a}{2}) \approx \frac{4}{\pi} V_{bas} \sin(\frac{\theta_b}{2}) \]  

(3.17)

since \( \theta_a \) is close to \( \pi \). Similar to the DC-DC Resonant Converter analysis in section 3.3.2, the output voltage of the battery side converter could be calculated as:

\[ V_{out2} = \frac{2V_{ab2-f}}{\pi \left[ 1 + K_2 - K_2 \left( \frac{f_s}{f_r} \right)^2 \right] + j Q_r \left( \frac{f_s}{f_r} \right) \left( \frac{f_s}{f_r} - f_r \right)} \]  

(3.18)

where:

\[ K_2 = \frac{C_{p2}}{C_{r2}} , \quad Q_r = \frac{\omega_r L_{b2}}{R_{ac2}} \]  

(3.19)

and \( f_s \) is the switching frequency of the battery side converter in battery discharge mode. Based on equation (3.2), \( K_2 \) and \( Q_{r2} \) could be rewritten as:

\[ K_2 = \frac{C_{p2}}{C_{r2}} = \left( \frac{N_1}{N_3} \right)^2 C_p \left( 2\pi f_{r2} \right)^2 L_{b2} = \left( \frac{N_1}{N_3} \right)^2 C_p \left( 2\pi f_{r2} \right)^2 \left( \frac{L_{eq} f_{r2}^2}{f_{s2}^2 - f_{r2}^2} \right) \]  

(3.20)

\[ Q_{r2} = \frac{2\pi f_{r2}}{R_{ac2}} \left( \frac{L_{eq} f_{r2}^2}{f_{s2}^2 - f_{r2}^2} \right) \]  

(3.21)
because \( C_p, N_1 / N_1, L_\text{eq} \) and \( f_{s2} \) are already known, the variables to determine the value of \( V_{\text{out,bs}} \) are only left to \( \theta_b, f_{s2} \) and \( f_{s3} \). The analysis procedure is very similar to the analysis in section 3.4.3. Therefore, the detailed analysis and calculation will not be presented here to reduce the redundancy of the thesis. Finally \( K_2 \) and \( f_{s2} \) is chosen as 3 and 150 kHz respectively.

The controller of the battery side converter in battery discharging mode is presented as Figure 4.11.

![Controller of the battery side converter (discharging)](image)

**Figure 4.11. Controller of the battery side converter in battery discharging mode**

### 4.3 Simulation Results

A prototype bidirectional ZVS DC-DC converter is designed to verify the effectiveness of the proposed topology. When the converter is in battery charge mode, the maximum battery charge current is around 10A. When the converter is in battery discharge mode, the output of the converter is well regulated to 380V DC and the rated power is 1kW. Table 3.1 shows the component parameters of the converter. The resonant frequency of the resonant tank is set to 160 kHz and ZVS is ensured by operating the converter above the
resonant frequency. The PSIM9.0 simulation schematic for both mode is given in Appendix B. Transformer
turns ratio is set to 3:1 and the ratio between parallel and series capacitor is 3.

<table>
<thead>
<tr>
<th>Component Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant series inductor (L_s2)</td>
<td>17uH</td>
</tr>
<tr>
<td>Resonant series capacitor (C_s2)</td>
<td>68nF</td>
</tr>
<tr>
<td>Resonant parallel capacitor (C_p2)</td>
<td>202.5nF</td>
</tr>
<tr>
<td>Transformer turns-ratio (N_i : N_3)</td>
<td>3:1</td>
</tr>
<tr>
<td>Battery side filter capacitor (C_bf)</td>
<td>500uF</td>
</tr>
</tbody>
</table>

Table 4.1. Component selected for the simulation of battery side converter

4.3.1 Battery Charging Mode

Figure 4.12 and Figure 4.13 present the battery charge current i_b and \( \theta_a \) when i_b is regulated at 9A and 5A. The battery charge current is well regulated in both cases. \( \theta_a \) is smaller when i_b is higher.

Figure 4.14 (a) and Figure 4.14 (b) show the resonant current and resonant voltage when I_b is regulated 9A and 5A respectively. It could be noticed that the resonant current is almost same in the two situations. That means the variation range of \( i_s \) is not wide when \( \theta_a \) is changing, which is very similar as the aforementioned analysis results. \( \theta_a \) decreases for a higher load and \( \theta_b \) is kept constant. The resonant current is always lagging the resonant circuit voltage. ZVS of all four switches is guaranteed due to the lagging resonant current.
Figure 4.12. Battery current $i_b$ and $\theta_a$ when $i_b$ is regulated at 9A.

Figure 4.13. Battery current $i_b$ and $\theta_a$ when $i_b$ is regulated at 5A.
4.3.2 Battery Discharging Mode

Figure 4.15 and Figure 4.16 present the output voltage and the control signal $\theta_b$ at full load (1kW) and 20% load (200W). The output voltage boosted and well regulated at 380V DC. the control variable is change to $\theta_b$ instead of $\theta_a$ in the battery charging mode. $\theta_b$ is proportional to the output power, where a high output power corresponds to a bigger value of $\theta_b$.

Figure 4.17 (a) and Figure 4.17 (b) show the resonant current and the voltage over the resonant circuit at 20% load and full load respectively. Similar to battery charging mode, the variation of resonant current is very small form 20% load to full load. $\theta_b$, or the phase shift between leg A and leg B is increasing with the output power. Since $\theta_a$ is kept a constant close to 180 degrees. A very smaller lagging is always found between the resonant current and the voltage over the resonant circuit. Hence, ZVS operations of all four switches are always achieved.
Figure 4.15. Output voltage of battery side converter and the control variable $\theta_b$ at full load.

Figure 4.16. Output voltage of battery side converter and the control variable $\theta_b$ at 20% load.
Figure 4.17. Resonant current $-i_{s2}$ and voltage $v_{ab2}$ when the output power is at (a) 20% load, (b) full load.
Chapter 5

Summary and Conclusion

5.1 Summary of Contributions

The main contributions of this thesis are as follows:

(i) A quantitative comparison of efficiency, reliability and cost between the 48V and 380V DC power distribution systems for the datacenters is presented. Although the 380V DC system is considered the most promising power distribution system choice for data centers due to its low cable loss and cost, the comparison shows that the 380V DC system has issues with reliability because of the large number of batteries connected in series. A new multi-port DC UPS is proposed to solve this problem. The proposed DC UPS has two output ports. When the input ac is available, the 380V DC port is used to deliver power to the load, while the 48V DC port is used to charge the battery. When the input ac is off, the 48V DC battery is boosted to 380V DC and delivers power to the load. High converter efficiency is achieved as only one converter is working in either situation. The proposed UPS has higher reliability and lower cost compared with traditional 380V DC system.

(ii) A new totem-pole bridgeless single-stage AC-DC converter is proposed to solve the unbalanced capacitor voltages which problem exists in previous topologies. By eliminating the rectified bridge diodes, the proposed converter has symmetrical operation for the two dc bus capacitors during one full cycle of the input ac voltage. One of the two dc bus capacitors is overcharged for one half-cycle of the input ac voltage. In the next half-cycle of input, the other dc bus capacitor receives exactly the same amount of overcharge. Hence, the voltages of the tow dc capacitors are naturally balanced during one full input cycle. Only a negligible low frequency voltage ripple is appeared on the two dc bus capacitors. The proposed converter has the same features of similar existing
topologies such as high power factor, zero voltage switching and low component stresses. Because the proposed converter removes two rectifying diode and the auxiliary circuit, it has higher efficiency and higher reliability compared to previous topologies.

(iii) The voltage ripple and voltage difference of the two dc capacitors in the proposed converter is analyzed and calculated. The relationship of the voltage difference between two dc capacitors and their capacitance is presented to optimize the capacitor selection. A decoupled model based on the power balance between the rectifying stage and the resonant DC-DC stage is proposed to simplify the design of the proposed converter.

(iv) A bidirectional ZVS DC-DC converter based on self-sustained oscillation control is proposed.

5.2 Conclusion
In this thesis, a quantitative analysis of the 48V DC and 380V DC power distribution systems for data centers has been conducted. Through the analysis, the advantages and disadvantages of both systems have been detailed. The 380V DC system A new DC UPS architecture has been proposed as a potential solution. This architecture combines the advantages of the 48V DC and 380V DC systems. Compared to the conventional 380V DC system, its reliability is 9.57% higher reliability and its cost is 21.3% lower. Since the new architecture has a very low cable loss and only one converter is working in either standard mode or backup mode. high over efficiency is also achieved.

A new bridgeless three-level single-stage AC-DC converter has been proposed. The proposed converter has a higher efficiency and higher reliability by removing the auxiliary circuit and two rectifying diodes found in previous topologies. A decoupled model, include detailed analysis of the steady state operation of the converter has been presented. High power factor and ZVS operation for all switches are also validated with simulation and experimental results. The voltages of two dc bus capacitors are well balanced without any auxiliary circuit. With two 2000uF capacitors, the maximum voltage difference between two dc bus capacitors is less than 2%, which is also validated with simulation and experimental results.
A bidirectional ZVS DC-DC converter based on self-sustained oscillating control has been proposed. When the input ac is available, it charges the battery. When the input ac is off, it discharges the battery and boosts the low battery voltage to powering the load. Both battery charge current and output voltage are well regulated across a wide range of ZVS for all switches. For both battery discharge and battery charge mode, a detailed analysis of their steady state operations has been presented. ZVS operation for all switches and well regulated outputs are validated with simulation result.

5.3 Suggested Future work

In the new DC UPS, control of main AC-DC converter and battery side converter are analyzed separately. However, it is possible to combine operations of the two controller. Advanced control techniques could be applied to improve the overall performance of the DC UPS. For an example, when the battery charge current increases, main AC-DC converter should drain more power form ac input immediately. With current controllers, this process is usually slow as main AC-DC converter only getting more power when load voltage decreases. An adaptive control based on battery charge current could be developed for the main AC-DC converter to increase its dynamic response.

In the proposed AC-DC converter, as the duty cycle is low and dc bus voltage is constant at light load, the equivalent input voltage to the resonant circuit decreases and large switching frequency variations are required to regulate the dc bus voltage. If the dc bus voltage is higher during light load instead of keeping constant, the equivalent input voltage to the resonant circuit is smaller and switching frequency variation is also reduced. Research into a variable dc bus voltage controlled by the load current should be carried out.

The resonant circuit used in the proposed AC-DC converter is a series-parallel resonant tank (LCC), which requires two resonant capacitors and one resonant inductor. It is possible to utilized the parasitic component of the high frequency transformer as part of resonant circuit, which could integrate all the resonant components and the high frequency transformer. Thus, reduced size could be achieved for the converter.
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Appendix A. PSIM Simulation Schematics

Figure A-1. PSIM schematic of the proposed three-level AC-DC converter and its two control loops
Figure A-2. PSIM schematic of battery side converter operating in battery charging mode.

Figure A-3. PSIM schematic of battery side converter operating in battery discharging mode.
Appendix B. PCB Schematic and Layout for the Proposed Single-Stage AC-DC converter

Figure B-1. PCB Schematic of the rectifier board of the prototype converter
Figure B-2. PCB Schematic of the dc bus voltage control loop for the prototype converter

Figure B-2. PCB layout of the rectifier board for the prototype converter
Figure B-3. PCB layout of the resonant circuit board for the prototype converter

Figure B-4. PCB layout of the output voltage control loop for the prototype converter
Figure B-5. PCB layout of the resonant circuit board for the prototype converter

Figure B-6. PCB schematic and layout of the gate driver board for the prototype converter