IMPROVING THE LIGHT LOAD PERFORMANCE OF POWER FACTOR CORRECTION CONVERTERS USING A DIGITAL CONTROLLER

by

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Abstract

AC-DC power conversion is the first power stage for all offline electronic devices. To maximize AC power transformer utilization, the power factor of AC-DC converters must be improved. The method that AC-DC converters use to improve the power factor is known as Power Factor Correction (PFC). This improvement of power factor, which can be quantified in terms of the total harmonic distortion (THD) of the converter, almost always is a trade-off for a reduction in overall converter efficiency. With increasing requirements for greater efficiency and lower THD, especially at output power loads much less than the rated output power of the AC-DC converter, new methods have been developed to meet either or both requirements. Many methods, however, can improve light load efficiency, but increase THD. Other methods, can reduce THD, but worsen light load efficiency. Some methods can reduce THD and improve light load efficiency, but at significant complexity and cost.

A new method for improving light load efficiency and THD, called Line Cycle Skipping (LCS) is proposed. This method improves the light load efficiency and THD without increasing complexity or cost. LCS can achieve this by conducting higher power over one or one-half line cycle, and then skipping or not conducting power over the next one or more line cycles. This allows the output power to remain constant at light load, while conducting higher input power over one or one-half line cycles. By conducting higher input power over a portion of the entire LCS period, the efficiency and the THD can be improved at lower output power levels, thus improving the light load performance of PFC converters.
LCS is implemented in digital control using a low-cost 8-bit microcontroller on a 100W PFC converter operating in critical conduction mode (CRM). Simulation results were verified by the experimental prototype waveforms. Experimental results showed significant improvement in efficiency and THD across the light load power range, proving that LCS has potential to be implemented in existing PFC converters with low cost to improve the light load efficiency and THD performance.
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Chapter 1

Introduction

Since the implementation of the alternating-current (AC) grid near the beginning of the twentieth century due in large part to Nikola Tesla and Westinghouse Electric & Manufacturing Company, AC power distribution has dominated as the main form of electrical energy transfer. This AC grid transferred and distributed electrical energy to linear loads, such as light bulbs and electric motors. However, these linear electrical loads of the past no longer will be the dominant form of energy usage on the AC power grid [1]. Increasingly, non-linear electronic loads are consuming every increasing amounts of power as a share of the total energy supplied by the AC power grid. These non-linear loads must convert AC into DC in order to power their downstream DC electronic loads. A large source of these non-linear electronic loads are desktop computers, notebook computers and large so called “server farms”, which are host to sometimes hundreds, if not thousands, of servers requiring a large amount of electricity for cooling and running continuously without interruption. This conversion process has become very taxing on the AC power distributors and the grids they maintain. This is due to the fact that this conversion process from AC to DC has heavily relied on rectification and large input capacitor filters, which create a distorted, non-sinusoidal current waveform drawn from the power distribution grid. These distorted current waveforms generate very large harmonic content and reactive power, limiting the amount of real power that can be effectively drawn from the grid, and making it more difficult for utilities to regulate the voltage of the AC source.
Figure 1.1 shows a simplified AC distribution system with both linear and non-linear loads. The linear AC loads draw a sinusoidal grid like current, and cause either a resistive loading or a combination of an inductive and resistive loading on the grid. The non-linear loads, however, draw a non-sinusoidal periodic current waveform, which is the result of rectifiers and capacitors used to convert from AC to DC to power the downstream DC devices. Figure 1.2 compares the linear and non-linear load current waveforms and their associated harmonic content. The linear load current waveform has a current amplitude at the fundamental frequency of 60Hz, which in this case is the power grid frequency. In contrast, the non-linear load has current amplitudes at 60 Hz, and at frequencies which are harmonics of fundamental 60Hz frequency. The harmonics currents caused by non-linear loads cause harmonic current distortion (THD$_i$) and harmonic voltage distortion (THD$_v$). Table 1.1 summarizes the effects of harmonic current and voltage distortion [2]. Significant current distortion can increase losses, reduce the lifespan, or lead to the failure of the point of load transformer distributing power. However, even minor voltage distortion can cause equipment failure and lifespan degradation of all equipment connected to the point of load transformer. In the distribution network, harmonic voltages are generated by harmonic currents passing through impedances within the network. By controlling the harmonic currents or impedances in the network, harmonic voltages can be limited or avoided altogether.
Figure 1.1 – AC Distribution System

Figure 1.2 – Harmonics Generated by Load Type

(a) Linear Loads and (b) Non-Linear Loads
1.1 Standards and Regulations

Due to issues related to power quality and harmonic emissions associated with AC-DC converters, multiple non-governmental and governmental bodies around the world have put in place standards and regulations to deal with these issues. Standards have been set by many organizations such as the Institute of Electronic and Electrical Engineers (IEEE), the International Electrotechnical Commission (IEC), and the U.S. Environmental Protection Agency (EPA). These standards were put into place by a general recognition that the utility companies producing the power would ensure good voltage quality, and consumers of power would limit their harmonic emissions.

Energy Star is an EPA voluntary program in which companies comply with the Energy Star standards set by the EPA [3]. If these standards are met and certified, the EPA then allows the applying product to carry the Energy Star label, such as the specification for external power supplies [4]. Energy Star labels can be found on notebook and desktop computer power supplies. This allows the consumers, whether they are end-users or product manufacturers, to know that the product meets certain
requirements for energy efficiency and power quality. Figure 1.3 shows a notebook computer external power supply with an Energy Star level 5 symbol on it, showing that it meets the highest level requirements set by the standard.

The IEC publishes international standards for all electrical and electronic equipment in order to reduce trade barriers by ensuring these standards are respected by different national governments and regulatory bodies, such as IEC 61000-3-2 which sets harmonic current emission limits for power electronic devices consuming less than 16A per phase [5]. Figure 1.4 shows the same notebook external power supply shown in Figure 1.3 containing the IEC standard symbol, to demonstrate that it complies with the most recent IEC standard associated with that device.

The IEEE has outlined harmonic current and voltage limit guidelines for utilities and industrial consumers, such as IEEE 519-1992, which set harmonic current and voltage emissions limits, but it is not intended for commercial and consumer use [6].

Figure 1.3 – Laptop AC Adapter with Energy Star Level 5 (V) Rating

Figure 1.4 – IEC Standards Certified Symbol
1.2 Power Factor Correction Converters

Non-linear loads draw non-sinusoidal current, which in turn creates harmonic current emissions. To prevent significant harmonic current emissions, power factor correction (PFC) is utilized to draw sinusoidal-like current from the grid, acting like a resistive load. A PFC converter effectively turns a non-linear load into a linear one, by correcting or improving the power factor (PF) of the converter. Typical input current waveforms of power supplies without PFC resemble the waveform in Figure 1.2(b). Without the use of PFC, the harmonic content generated limits the amount of real power available and can cause overloading, which will activate circuit breakers due to excessive currents.

There are two types of PFC: passive PFC and active PFC. Passive PFC employs a large input inductance to create a large low-pass filter in order to draw current that is more sinusoidal, as shown in Figure 1.5(a). It passes the current for frequencies close to the line frequency of the AC grid. Active PFC utilizes switched mode power supplies to shape in input current in such a way that it is linearly proportional to the input voltage source waveform, as shown in Figure 1.5(b). Essentially, it allows the non-linear load to mimic a resistive (linear) load. Both passive and active PFC improve the power factor of the converter and reduce the total number of harmonics of the line frequency, better known as total harmonic distortion (THD). However, this comes at the cost of efficiency, due to the additional switching circuit before the DC bus which contains more downstream DC-DC converters. Passive PFC, however, cannot achieve as high a PF as active PFC because of the limitations of the low pass filter design. Also, the passive PFC inductor is very large in comparison to the active PFC inductor because it is designed to
pass the 50/60 Hz line frequency. Because of the PF and size limitations, the applications for passive PFC become very limited.

1.2.1 Types of Common Active PFC Converters

There are three common active PFC converters types:

1) Single-stage PFC converters

2) Two-stage PFC converters

3) Multi-phase or Interleaved PFC converters
Single-stage PFC converters, like the one shown in Figure 1.6, consist of a rectifier stage and a AC-DC converter stage responsible for converting the high input line voltage to a lower DC voltage bus level. For example, this voltage could be around 20V for laptop power supplies, 48V for telecommunications equipment, 12V for generic wall charging devices, etc. One such single-stage PFC converter topology is a Flyback converter, shown in Figure 1.7.

**Figure 1.6 – Single-Stage PFC AC-DC Converter**

**Figure 1.7 – Single-Stage PFC Flyback Converter**

### 1.2.2 Benefits and Limitations of Active PFC Converters

 Passive PFC converters cannot provide the reduction of harmonics necessary at power levels exceeding 100W without either being prohibitively expensive, bulky, or both. As
the power level and PF requirements increase, the necessity for active PFC increases. Implementing active PFC, however, can be beneficial and is not necessarily a negative trade-off.

Active PFC converters offer many benefits which include:

- Drastically reducing THD, by improving the PF
- Better real power utilization by limiting reactive power generated by harmonics
- Universal input voltage compatibility without transformer winding switches
- Input voltage transients, interruption detection, and compensation
- Reduction in size and number of bulk energy storage capacitors
- Better offline DC bus voltage regulation

Active PFC converters, however, have some limitations:

- Reduced overall efficiency due to additional switching
- Increases cost due to additional front-end converter
- Increased EMI from additional switching

1.2.3 Design and Trade-offs in PFC converters

There are many factors that are taken into account when one decides to utilize a PFC converter, but there are three general ones. A PFC converter must balance efficiency, THD, and economic value. The lower the price point, the worse the efficiency and THD performance tend to be. Also, increasing the efficiency will usually come at the cost of worsening the THD performance and vice a versa. Power electronic engineers spend much time and effort trying to balance these three areas depending on the application for the device.
To summarize, because a PFC converter’s purpose is to reduce the THD by improving the power factor, in order for a power electronics engineer to increase the efficiency of such a converter, they must try not to reduce the THD of the device to a point where it defeats the purpose of utilizing it in the first place. Any improvement, therefore, must increase the efficiency while retaining the ability to meet the standards and regulations, without any additional cost when compared to current technology.

1.3 Light Load Performance of PFC Converters

The nameplate or rated power of a PFC converter is the maximum output power that it can deliver to the load. However, the rated load is not always the load at which the operating efficiency of the PFC converter is highest. This is illustrated in Figure 1.8, where a typical efficiency vs. load characteristic for a PFC converter is shown. The efficiency vs. load characteristic curve is broken down into three sections including the heavy load, medium load and light load regions. The medium load region is where the converter operates at its highest efficiency, where as the heavy load region shows a slight drop in efficiency, which is usually due to design constraints and operating conditions of the load. This is mainly due to not overdesigning the PFC converter to handle higher current stresses, and the fact that the PFC converter, although capable of delivering the maximum rated power, generally performs best at a power level less than the rated power. Hence, the efficiency is higher in the medium load condition where most of the energy is consumed.
Figure 1.8 – Efficiency vs. Load Regions

Of particular interest in Figure 1.8 is the light load region, because it exhibits a large decrease in efficiency as the load decreases. This large decrease in efficiency is due to many reasons including:

- Switching loss and reverse recovery loss become a higher percentage of overall losses
- High current peaks caused by the PFC converter entering discontinuous conduction mode (DCM) from continuous conduction mode (CCM)
- Increasing switching frequency leading to higher switching losses for critical conduction mode (CRM)

Interestingly, the THD vs. load curve, seen in Figure 1.9 is nearly the inverse of the efficiency vs. load curve. This is because at medium and heavy loads the PFC converter experiences less current distortion, allowing the current waveform to follow the voltage waveform generating fewer harmonics. However, in the light load region, due to DCM
operation and low signal amplitudes for control sensors, the current distortion increases as the load decreases.

![THD vs. Load Regions](image)

Figure 1.9 – THD vs. Load Regions

### 1.4 Motivation

The motivation of this thesis is to improve the light load efficiency and THD of PFC converters. The solution should balance the three general trade-offs of efficiency, THD and cost. It should consist of a simple and easy to implement design that is capable of being very robust, but also very cost effective. The motivation of this thesis is summarized in three key points:

1. Increase the light load efficiency of PFC converters
2. Decrease the THD of PFC converters
3. Use a low cost microcontroller to implement a robust digital control scheme

#### 1.4.1 Increase the Light Load Efficiency of PFC Converters

The objective for the increase in light load efficiency is ideally to maintain peak efficiency throughout the light load range, as shown in Figure 1.10. Chapter 3 will
propose a method in order to achieve this light load efficiency improvement. The method must not decrease THD for efficiency improvement. The method must also be able to be implemented with practical cost constraints.

![Light Load Efficiency Improvement Objective](image)

Figure 1.10 – Light Load Efficiency Improvement Goal for PFC Converters

1.4.2 Decrease the THD of PFC converters

The decrease in THD of PFC converters is linked directly to the increase in the light load efficiency, because the method used to achieve this will simultaneously do both. The objective decrease in THD is shown in Figure 1.11. The power level at peak efficiency is the starting point for the improvement of THD down into the light load range.
1.4.3 Use a Low Cost Microcontroller to Implement a Robust Digital Control Scheme

The cost of a microcontroller unit (MCU) has substantially decreased since their introduction [7]. Although MCUs are universal in their applications, they have been and continue to be used in the control of power supplies [8]. Using a low cost MCU can be very cost effective, due to the standardized nature of their architecture and manufacturing. The control consists of lines of code of a widely recognized language, usually the C programming language, which can be easily understood and modified. This makes the design extremely flexible and amenable to modification. It also allows for the use of digital control, because the control will be implemented digitally instead of using analog components. Digital control can enable the use of non-linear and adaptive control techniques that would be very difficult to realize using analog control due to the sheer number of analog components required to replicate the digital control algorithm.
The proposed control method in Chapter 3 will utilize a low cost microcontroller in order to show the simplicity of the control scheme when compared to previous control schemes discussed in Chapter 2.

1.5 Thesis Outline

This thesis consists of six chapters. Chapter 1 provides the introduction to the objective and challenges in creating a low cost solution for improving the light load efficiency and the THD of PFC converters. Chapter 2 provides a description and an analysis of the light load performance of PFC converters, and discusses past work in the literature that tries to improve the light load efficiency and/or the THD of such PFC converters, as well as similar intermittent line commutation techniques. Chapter 3 introduces the Line Cycle Skipping (LCS) method, its suitability in PFC converters as well as an analysis its efficiency, output voltage ripple, and harmonics. Chapter 4 provides an overview of LCS control, its control process, and implementation requirements. Chapter 4 will also provide an overview of MCUs suited for implementing LCS control, how to adapt them to a CRM PFC boost converter, as well as input voltage slop detection techniques and look-up table design for LCS implementation. Chapter 5 presents the simulation and experimental results obtained from a universal input voltage boost PFC converter prototype implementing LCS. As a result, significant increases in light load efficiency and reductions in THD are presented. Chapter 6 provides a summary of the current work and ideas for future work on and related to this topic.
Chapter 2

Light Load Performance Improvement in Power Factor Correction Converters and Intermittent Control Methods

Light load performance of PFC converters has been the focus of much research in the recent literature. This has been motivated by the wide load range of many devices including lighting and computer electronics. It is no longer the case that a power supply needs only be designed for the stand-by and full-load conditions. Take the examples of a dimmable ballast for a LED lamp or a notebook computer’s power supply. Both devices may be operating at any point in their load range depending on their current use. Also, many power electronic devices are required by certain standards and regulations, as discussed in Chapter 1, to meet minimum average efficiency and no-load power consumption levels, while meeting harmonic limitations. However, a power supply for a notebook computer having a similar efficiency vs. load profile, as shown in Figure 1.9, may not be able to meet both minimum average efficiency and the less than ultra low power consumption requirement set by [4], while keeping harmonic levels below the limits set by the IEC [5].

This section contains the literature review for light load efficiency improvement in power factor correction converters and highlights the fact that light load efficiency generally comes at the cost of THD in these proposed control schemes. To begin, a summary and analysis of light load efficiency, power factor and THD, and their relationship in PFC converters is presented to better understand the reasons why such a converter suffers from poor light load performance. This chapter then discusses previous
work to improve the light load performance. And, finally, the last part of this chapter will
describe previous intermittent line commutation techniques used in power converters.

2.1 Light Load Efficiency, Power Factor and THD

2.1.1 Light Load Efficiency

PFC converter power supplies suffer from poor light load efficiency if the converter
maintains high power factor as the load is decreasing. This happens depending on the
topology and control method. The general equation for efficiency of a power supply is
given in equation 2.1. The efficiency, therefore, is a ratio between the output power of the
converter and the output power in addition to the total loss generated from the operation
of the converter. If the output power decreases and the losses increase proportionally, this
will result in a severe loss in efficiency as shown in Figure 1.9.

\[
Eff = \frac{P_o}{P_o + P_{loss}}
\]  
(2.1)

The power loss of the circuit, \( P_{loss} \), can be expanded to equation, where \( P_{conv} \) is the
power conversion loss of the circuit and \( P_{ctrl} \) is the controller losses. \( P_{conv} \) depends on
the circuit topology and components, as well as switching patterns defined by the control
scheme. \( P_{ctrl} \) changes with the different controller circuit components and control
schemes.

\[
P_{loss} = P_{conv} + P_{ctrl}
\]  
(2.2)

At light loads even a small controller loss is significant. Lower power controllers,
especially digital controllers, tend to be less powerful (i.e. lower clock frequency and
lower computation capabilities for digital controllers). The lower power consumption requirements for the controller lead to less powerful the controllers that can be utilized, which cause more limitations for possible control schemes.

2.1.2 Power Factor and THD

Power factor (PF) is a 0 to 1 measurement of how effectively power is transmitted from the source to the load [9]. It can be described generally as the average power transferred to the load divided by the RMS of the source current and voltage, as in equation 2.3 [9].

\[
\text{power factor} = \frac{(\text{average power})}{(\text{rms voltage})(\text{rms current})} \quad \text{(2.3)}
\]

A linear resistive load that is sourced by a purely sinusoidal voltage always conduct a purely sinusoidal current, and thus has a PF of 1, meaning all of the power from the source is transferred to the load. This would be considered the ideal case for power transfer. For non-linear loads sourced by purely sinusoidal voltage, however, the PF must be broken down into two components: displacement PF and distortion PF. Displacement PF is generally described as the cosine of the phase angle difference between the voltage and current waveforms, shown in Figure 2.1, where \( \theta_{PF} \) is the phase angle difference, represented by equation 2.4.

\[
P_{PF_{disp}} = \cos \theta_{PF} = \cos(\theta_v - \theta_i) \quad \text{(2.4)}
\]

This phase displacement is a problem cause by linear loads that are considered capacitive or inductive (not purely resistive). The distortion PF, however, is created by non-linear loads, has a direct relationship to THD, and is represented by equation 2.5. \( THD_i \) is
calculated using equation 2.6, where the amplitudes of the harmonics, $I_{krms}$, are squared and summed, before being divided by the amplitude of the fundamental signal amplitude, $I_{1rms}$.

\[
PF_{dist} = \frac{1}{\sqrt{1 + THD_i^2}} \quad \text{(2.5)}
\]

\[
THD_i = \sqrt{\sum_{k=2}^{\infty} \frac{I_{krms}^2}{I_{1rms}^2}} \quad \text{(2.6)}
\]

True power factor, therefore, is the product of $PF_{disp}$ and $PF_{dist}$, as in equation 2.7.

\[
PF_{true} = PF_{disp} \cdot PF_{dist} \quad \text{(2.7)}
\]

Figure 2.1 – Power Factor (PF) as a Function of Phase Difference

2.1.3 Efficiency vs. THD in PFC Converters

AC-DC converters that do not address PFC generally take the form shown in Figure 2.2, where the AC line is rectified, the peak is held by a large capacitor bank, and the DC voltage is regulated by a DC-DC converter. This allows the input voltage to the DC-DC converter to have a smaller input voltage swing, making it easier to regulate the output DC bus voltage with high conversion efficiency. However, this type of AC-DC converter
comes at the cost of PF and THD, because the input current waveform does not follow the voltage waveform, and thus produces many current harmonics. To eliminate these harmonics while regulating the DC bus voltage, either a single-stage or two-stage PFC AC-DC converter is used conduct current that will follow the voltage from the AC line source. Their architectures are shown in Figure 2.3(a) and Figure 2.3(b). This effectively allows the load presented to the AC line source to change from a non-linear harmonic dense load into a linear harmonic-less load.

Although PFC converters reduce the harmonics generated by the input current, thereby lowering the THD, it prevents the AC-DC converter stage from being designed to handle a small input voltage range. In order for the AC-DC converter to follow the voltage waveform, it must operate from zero to the peak voltage of the line. This large input voltage range creates non-ideal conditions for the output voltage regulation of the AC-DC converter, which affect the efficiency of the converter, especially light load efficiency.

Figure 2.2 – AC-DC Converter without PFC
Converter control schemes affect the light load efficiency and overall efficiency of the PFC converter discussed in section 2.1.4 below. These control schemes coupled with the large input voltage range that a PFC converter must handle, presents many challenges to achieve both high power factor, and thus lower THD and high efficiency.

2.1.4 Converter Control Schemes Affecting Light Load Efficiency

The control of the converter is a significant factor when determining the light load efficiency. Most PFC converter control schemes, if not all, can be described by either three basic modes of operation; continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CCM) – sometimes called...
transition mode or boundary mode. Figure 2.4(a) shows the inductor current waveform for a boost PFC converter. CCM type control methods continuously draw current – the inductor current does not fall to zero after every switching cycle – with some ripple that depends on the switching frequency and size of the inductor for a constant load. The efficiency starts to decrease as the load decreases because the converter will enter into DCM. DCM, shown in Figure 2.4(b), is when the inductor current falls to zero after the switch turns off in each switching cycle, and remains at zero until the switch turns on again at the end of each switching cycle. This will cause the input peak currents to become much higher than in the CCM case, in order for the average current to remain equal. Higher peak currents cause additional losses in the switch and in the inductor’s core, especially in proportion to a smaller load, therefore, increasing the light load losses. CRM, shown in Figure 2.4(c), like DCM, allows the current to fall to zero after the switch is turned on. However, as soon as the current reaches zero the switch is immediately turned back on. The average current in CRM is always half of the peak current, which means that the switching frequency, therefore, is variable as opposed to fixed in the case of both CCM and DCM. This means that as the load decreases the switching frequency increases, further increasing losses at light load.
2.2 Existing Light Load Performance Strategies for PFC in the Literature

Light load performance strategies for PFC converters are appearing in the literature with more frequency, along with the increasing awareness of poor THD performance and efficiency for consumer electronics. This is due, in part, to the growth of non-linear electronics and the standards, such as Energy Star, meant to improve them [10].

Various methods have been used to improve either the light load efficiency, THD, or both. Some control techniques for PFC converters use variable frequency to reduce distortion near the edges of the line voltage waveform at lighter loads, when the converter would normally enter DCM [11-14]. Other control schemes would avoid the edges of the
input voltage waveform at lighter loads using a windowing technique [15, 16]. When
PFC converters are interleaved or have multiple phases to handle higher power, phase
shedding techniques are used at lighter loads to shutdown one or more stages to reduce
overall losses [11, 17-23]. PFC converters that change its control based on the load are
known adaptive control schemes [24-28]. Some adaptive control schemes change the
conduction mode of the PFC converter as the load or input voltage changes [21, 29-34].
Earlier techniques to address the regulation issue of PFC converters at very light loads or
standby-by conditions is to turn the PFC converter and allow switching to occur during
very small portions of the input voltage line cycle, sometimes known as burst mode [25,
26, 35, 36]. Digital control has been used to control PFC converters and many of these
techniques implement presented in the literature use digital control exclusively to
implement such techniques [11, 13, 20, 21, 30, 31, 37-41]. Resonant switching, non-
linear inductance, and various methods have also been used to either improve efficiency
or harmonic distortion [42-44].

2.2.1 Burst Mode and Burst Mode PFC

One way to improve the light load efficiency is to turn-off the PFC control of the
converter completely or intermittently, when the load is less demanding on the
converter’s output. For a conventional burst mode control found in DC-DC converters,
the switching control circuit is turned on and off periodically to regulate the output
voltage between a hysteretic band – an upper and lower voltage threshold [45]. In burst
mode control for a PFC converter, the input current reference becomes a DC signal,
effectively operating the converter as a DC-DC converter, regulating the output voltage
The switching frequency is constant, and the gate driver is turned on using a hysteretic voltage control to regulate the output voltage. Figure 2.5 shows the switching control signal and the output voltage waveforms for the conventional burst mode operation, where $V_{TH+}$ and $V_{TH-}$ are the upper and lower threshold voltages for the hysteretic voltage control, respectively. The area between the two voltage thresholds make up what is sometimes known as the hysteric voltage band. This method is extensively used in DC-DC converters to reduce the switching losses when the converter is in the light load region.

A modified version of burst mode control for PFC converters uses the same concept, but instead of disabling the PFC and operating as a DC-DC converter, the PFC control is disabled intermittently over many input line cycles and then enabled, while remaining within the hysteretic output voltage band. A good example of this is presented in [49].
Figure 2.6 shows the input line current waveform overlaid on the input line voltage. The PFC is turned on and off intermittently, allowing for the output voltage – shown in the lower figure – to be regulated within a hysteretic voltage band. This type of burst mode allows the PFC converter to maintain at least a portion of PFC while in the light load region, while at the same time maintaining a higher efficiency by avoiding DCM or an increased switching frequency depending on the current control method.

There are two primary problems with this technique. One problem with using this burst-mode PFC technique shown in Figure 2.6, is that output voltage’s upper and lower threshold is triggered independent of phase of the input voltage line cycle, because it is actually dependent on the load applied to the PFC converter. This means that, depending on the load, the burst-mode PFC technique could be turning on and off the PFC anywhere in the line cycle, causing additional distortion and losses, as well as signal noise. The
second problem is that, because of the first problem, this technique is restricted to the very light load region, or the no-load operation of the converter due to the high distortion, slow response, and limited regulation.

2.2.2 Adaptive current conduction mode and frequency switching

There are many research papers in the literature that utilize some form of what is called “adaptive control” and can include some type of variable switching frequency scheme [50-52]. These control schemes use some threshold or predefined transition window to transition from one conduction mode of operation to another and may adjust the switching frequency based on the line cycle waveform and load. Adaptive control can be accomplished by using either an analog or a digital method. The more complex the adaptive control – by having multiple transition phases – the more likely such a method will be devised digitally using some type of microcontroller or DSP due to the added complexity of such multi-modal control schemes.

As the PFC converter enters into light load, the objective of these control schemes as the angle of the line cycle changes is to either change the conduction mode from CCM to DCM, change from constant frequency to constant on-time, or a combination of both. The adaptive CCM/DCM control input current waveform as it transitions from DCM to CCM and back to DCM during the half line cycle is shown in Figure 2.7(a). Figure 2.7(b) displays an example of a switching frequency and an on-time profile as the load and line cycle angle changes for an adaptive frequency/on-time control scheme.

While adaptive control schemes of these types do improve the performance of a PFC converter by changing the conduction mode or switching mode over different portions of
the line cycle and load, they are still inherently limited to the direct benefits that such conventional modes can provide in that operating region. But, they do so at considerable complexity and cost.

![Diagram](attachment:image.png)

**Figure 2.7 – Adaptive PFC Control Schemes**

(a) Adaptive CCM/DCM and (b) Adaptive Frequency/On-time

2.3 **Intermittent AC Line Conduction**

Conducting AC line current over an intermittent period relative to the line voltage has been a strategy since the utilization of thyristors in power electronics. Unlike phase-angle controlled thyristor applications, the goal of the intermittent AC line conduction technique is to connect and disconnect the load from the AC source over a number of
specified line cycles in order to control the average voltage and/or average power received by the load. This can be done to regulate either the power or voltage applied to the load. At least two techniques employing this strategy have appeared in power electronics literature: Integral Line Cycle Control and Line Frequency Pulse Density Modulation (LFPDM).

2.3.1 Integral Line Cycle Control

Integral Line Cycle Control consists of controlling the firing angle of one or more thyristors, depending on the configuration and number of phases, such that the number of voltage line cycles that appears at the load is reduced. Usually used in the application of variable direct voltage for resistive loads and speed control of series connected DC motors, Integral Line Cycle Control is an alternative to the more popular phase-angle controlled AC circuits [53-55]. Figure 2.8(a) shows a typical single phase thyristor controlled circuit. The thyristor firing angles are controlled such that the complete line cycles or half line cycles are removed from appearing at the load. This can be seen in Figure 2.8(b) where the conduction period, N, is commutated to the load over the period, T, such that T minus N is the period that is removed from appearing at the load.
2.3.2 Line Frequency Pulse Density Modulation (LFPDM)

Similar to Integral Line Cycle Control, Line Frequency Pulse Density Modulation, or LFPDM, controls the amount of commutated line cycles to regulate the voltage or power to a resistive or inductive load. The difference being that LFPDM is used with high frequency switches in a bridge configuration, instead of thyristors in line commutation, to create a high frequency switched-mode power supply (SMPS) operating from rectified line voltage [56, 57].
An example of LFPDM control is given in Figure 2.9 above. A high frequency half-bridge driver circuit, Figure 2.9(a), is used to drive an inductive load with high frequency switching inside commutated line cycles. During the power injection cycle, the driver...
operates in its conventional high switching frequency operation. However, during the inactive cycle, the switching is disabled causing the line current, $i_{IN}$, and load current, $i_{LOAD}$, to go to zero. This duty cycle of LFPFM can continue to repeat as desired.
Chapter 3

A Line Cycle Skipping Method to Improve the Light Load Performance of PFC Converters

From the previous chapter in section 2.2, many methods of improving light load efficiency, THD, or both were presented. The light load performance of a PFC converter should be described as containing both elements. Improving both can be quite difficult, and without the right control method, a trade-off can exist between the two. The objective would be to devise a method that would not trade between light load efficiency and THD, while maintaining a practical solution with a low cost. In this chapter, with reference to previous methods devised in section 2.3, a Line Cycle Skipping (LCS) method is proposed to improve the light load performance of PFC converters.

First to be discussed in this chapter will be section 3.1, The Proposed Line Cycle Skipping Method. In this section, the operating principle of the proposed LCS method and an analysis will be presented along with derived equations, used to establish the principle behind the light load efficiency and THD improvement for PFC converters. Also, included in the section are some design considerations which discuss a few different ways a designer can go about achieving the fundamental requirements needed to implement LCS. The second section of this chapter, section 3.2, will analyze and propose some methods to address the effect of LCS on the output voltage ripple. The final section, section 3.3, will go into detail on the harmonic effects when implementing LCS.
3.1 The Proposed Line Cycle Skipping Method

3.1.1 Operating Principle

The LCS control method is used to increase the light load efficiency while maintaining, or improving THD. Its entire purpose is *not* to trade-off between two elements contained within light load performance – light load efficiency and THD. It does this using the following procedure:

1) The PFC converter will sense the output power

2) When the PFC converter enters into a pre-defined “light load” region, LCS is triggered

3) The PFC converter will turn the PFC off for one or more line cycles depending on the output power, and conduct power for one or one-half of a line cycle at the power corresponding to peak power efficiency

The above procedure is described by Figures Figure 3.1, Figure 3.2, and Figure 3.3 respectively.
Figure 3.1 – LCS Trigger Point

Figure 3.2 – Simplified LCS Control Diagram
In practice, however, an increase in THD cannot be avoided, but the amount increased can be substantially reduced. The analysis of THD is presented in chapter 3.3. There are two primary methods to achieve light load skipping. Both are described in the following two sections.

3.1.2 Full Line Cycle Conduction (FLCC)

The first method to achieve line cycle skipping is called Full Line Cycle Conduction (FLCC). This is achieved by activating PFC for a full line cycle, or $2 \pi$, and then deactivated or turned-off for another full line cycle. This method is illustrated in Figure 3.4, where the conduction period and skipping period are both components that comprise.
of one LCS period. Each conduction period is for one or more full line cycle. The skipping period comprises of one or more line cycles.

![Diagram](image)

**Figure 3.4 – Full Line Cycle Conduction (FLCC)**

The average power of FLCC can be expressed by equation 3.1, where the average power, $P_{FLCC}$, during LCS is the sum average of the conduction power, $P_{COND}$, during the number of conduction cycles, $N_{COND}$, with the skipping power $P_{SKIP}$, and the number of skipping cycles, $N_{SKIP}$, divided by the total number of line cycles, $N_{TOTAL}$. Where every $N$ is an integer multiple of a full line cycle.

$$P_{FLCC} = \frac{P_{COND} \cdot N_{COND} + P_{SKIP} \cdot N_{SKIP}}{N_{TOTAL}} \quad (3.1)$$

For example, in Figure 3.5, LCS is activated using the FLCC method. Their conduction period is one full line cycle, or $N_{COND} = 1$, and the conduction power, $P_{COND} = 50W$. The skipping period is assumed, ideally, to be 0W for one full line cycle.
Therefore, the LCS period is two full line cycles and the calculation to determine $P_{FLCC}$ is as follows:

$$P_{FLCC} = \frac{50W \cdot 1 + 0W \cdot 1}{2} = 25W$$

(3.2)

Figure 3.5 – FLCC Example

3.1.3 Half Line Cycle Conduction (HLCC)

The second method to achieve line cycle skipping is called half line cycle conduction (HLCC). Similar to FLCC, HLCC is achieved by activating PFC for a half line cycle, or $\pi$, and then deactivated or turned-off of the switching converter for an additional full line cycle, or $2\pi$. This method is illustrated in Figure 3.6, where the conduction period and skipping period are both components that comprise of one LCS period, but the conduction period alternates between positive and negative half line cycles. This is to avoid a DC bias and additional harmonics, which is a phenomenon that occurs in half line cycle rectification. The skipping period comprises of one or more full line cycles, which
allows for the conduction period to alternate between positive and negative half line cycles.

Figure 3.6 – Half Line Cycle Conduction (HLCC)

HLCC can be expressed by equation 3.3, where the average power, $P_{HLCC}$, during LCS is the sum average of the conduction power, $P_{COND}$, during the number of conduction cycles, $M_{COND}$, with the skipping power $P_{SKIP}$, and the number of skipping cycles, $M_{SKIP}$, at divided by the total number of line cycles, $M_{TOTAL}$. Where every $M$ is an integer multiple of a half line cycle.

$$P_{HLCC} = \frac{P_{COND} \cdot M_{COND} + P_{SKIP} \cdot M_{SKIP}}{M_{TOTAL}} \quad (3.3)$$

For example, in Figure 3.7, LCS is activated using the HLCC method. Their conduction period is one half line cycle, or $M_{COND} = 1$, and the conduction power, $P_{COND} = 30W$. 
The skipping period is assumed, ideally, to be 0W for two half line cycles. Therefore, the LCS period is three half line cycles and the calculation to determine $P_{HLCC}$ is as follows:

$$P_{HLCC} = \frac{30W \cdot 1 + 0W \cdot 1}{3} = 10W$$  (3.4)

Figure 3.7 – HLCC Example

3.2 Light Load Efficiency Analysis of LCS

The intended effect of LCS is to enhance the light load efficiency of PFC control schemes. As demonstrated in section 3.1, the proposed line cycle skipping methods conduct a discontinuous amount of power that is greater than the average power over the LCS period. As shown in Figure 1.9, the medium load of a typical AC-DC converter is usually where the highest efficiency is achieved. Because of this, LCS allows for the converter to conduct power in the medium load, and due to the skipping period, the average power over the LCS period is less than the power being conducted during the
conduction period. Ideally, this allows for the medium or full load efficiencies to be realized in the light load efficiency region of Figure 1.9. In the following sections, the light load efficiency of both LCS methods will be analyzed to show the benefit of LCS control schemes.

### 3.2.1 Light Load Efficiency Analysis for FLCC

Efficiency for power converters are generally calculated using a simple equation, as in equation 3.5.

\[
Eff = \frac{P_{\text{OUT}}}{P_{\text{IN}}} \times 100\%
\]  

(3.5)

Combining equations 3.5 and 3.1, yields equation 3.6 for the efficiency for FLCC.

\[
Eff = \frac{P_{\text{OUT}}}{\left(\frac{P_{\text{COND}} \cdot N_{\text{COND}} + P_{\text{SKIP}} \cdot N_{\text{SKIP}}}{N_{\text{TOTAL}}}\right)} \times 100\%
\]  

(3.6)

Combining equations 3.3 and 3.5, yields equation 3.7:

\[
Eff = \frac{P_{\text{OUT}}}{\left(\frac{P_{\text{COND}} \cdot M_{\text{COND}} + P_{\text{SKIP}} \cdot M_{\text{SKIP}}}{M_{\text{TOTAL}}}\right)} \times 100\%
\]  

(3.7)

To simply the calculations and reduce the number of equations in the analysis, because \( N = M \times 2 \), equations 3.6 and 3.7 can be just simplified by using half line cycles for measuring the period:

\[
\eta_{\text{AC-DC}} = \frac{P_{\text{OUT}}}{\left(\frac{P_{\text{COND}} \cdot 2 \times M_{\text{COND}} + P_{\text{SKIP}} \cdot 2 \times M_{\text{SKIP}}}{2 \times M_{\text{TOTAL}}}\right)} \times 100\%
\]  

(3.8)
\[ \eta_{AC-DC} = \frac{P_{OUT}}{2 \left( \frac{P_{COND} \cdot M_{COND} + P_{SKIP} \cdot M_{SKIP}}{M_{TOTAL}} \right)} \times 100\% \quad (3.9) \]

\[ \eta_{AC-DC} = \frac{P_{OUT}}{\left( \frac{P_{COND} \cdot M_{COND} + P_{SKIP} \cdot M_{SKIP}}{M_{TOTAL}} \right)} \times 100\% \quad (3.10) \]

Therefore, for the equation for efficiency calculation for FLCC is the same as HLCC when using half line cycles to measure the conduction, skipping, and LCS periods. So, from this point forward, equation 3.10 will be used to calculate the efficiency of all LCS control schemes.

To demonstrate the improved efficiency for LCS control schemes, equation 3.10 will be used in the following example:

The efficiency for a conventional PFC converter operating continuously (not using LCS) is,

\[ \eta_{AC-DC}^{Pout=50W} = 95\% \quad (3.11) \]

\[ \eta_{AC-DC}^{Pout=25W} = 90\% \quad (3.12) \]

FLCC is activated when \( P_{OUT} = 25W \), and the efficiency of FLCC at 25W can be calculated using equation 3.7 and then solving to achieve equation 3.15, as seen in Figure 3.5.

\[ \eta_{FLCC} = \frac{P_{OUT}}{\left( \frac{P_{COND} \cdot M_{COND} + P_{SKIP} \cdot M_{SKIP}}{M_{TOTAL}} \right)} \times 100\% \quad (3.13) \]
\[ \eta_{FLCC}^{Pout=25W} = \frac{25W}{\left( \frac{50W}{\eta_{AC-DC}^{Pout=50W}} \cdot (2) + 0W \cdot (2) \right)} \times 100\% \] (3.14)

\[ \eta_{FLCC}^{Pout=25W} = \frac{25W}{25W} \times 100\% \] (3.15)

The result of equation 3.15 is 95% efficiency. This is not only greater than the efficiency at 25W for a AC-DC converter operating continuously, but the FLCC efficiency at 25W is equal to the efficiency at for the AC-DC converter operating continuously at 50W.

\[ \eta_{FLCC}^{Pout=25W} = 95\% \] (3.16)

\[ \eta_{AC-DC}^{Pout=50W} = \eta_{FLCC}^{Pout=25W} > \eta_{AC-DC}^{Pout=25W} \] (3.17)

As can be seen in from equations 3.16 and 3.16, the efficiency for FLCC at 25W is equal to the efficiency for the AC-DC converter at 50W during continuous PFC operation. This is a substantial increase in efficiency, and proves that Figure 1.11 is theoretically possible. However, because there are non-ideal losses that factor in to equation 3.7, the efficiency of FLCC would have to account for such losses when calculating the efficiency.

### 3.2.2 Light Load Efficiency Analysis for HLCC

The same calculation can be done for HLCC, where:

The efficiency for a conventional PFC converter operating continuously (not using LCS) is,
HLCC is activated when $P_{OUT} = 10\text{W}$, and the efficiency of LCS at 10W can be calculated using equation 3.7 and then solving to achieve equation 3.22, as seen in Figure 3.7.

\[
\eta_{HLCC} = \left( \frac{P_{OUT}}{P_{COND} \cdot M_{COND} + P_{SKIP} \cdot M_{SKIP}} \right) \times 100\% \quad (3.20)
\]

\[
\eta_{HLCC}^{Pout=10W} = \left( \frac{10W}{\frac{30W}{\eta_{AC-DC}^{Pout=30W}} \cdot (1) + 0W \cdot (2)} \right) \times 100\% \quad (3.21)
\]

\[
\eta_{HLCC}^{Pout=10W} = \frac{10W}{10W \cdot 0.90} \times 100\% \quad (3.22)
\]

The result of equation 3.22 is 90% efficiency. This is not only greater than the efficiency at 10W for a AC-DC converter operating continuously, but the HLCC efficiency at 10W is equal to the efficiency at for the AC-DC converter operating continuously at 30W.

\[
\eta_{AC-DC}^{Pout=30W} = \eta_{HLCC}^{Pout=10W} > \eta_{AC-DC}^{Pout=10W} \quad (3.23)
\]

As can be seen in from equations 3.23 and 3.24, the efficiency for HLCC at 10W is equal to the efficiency for the AC-DC converter at 30W during continuous PFC.
operation. Again, this is a substantial increase in efficiency, and proves that Figure 1.11 is theoretically possible for HLCC as well as FLCC. However, because there are non-ideal losses that factor in to equation 3.7, the efficiency of HLCC would also have to account for such losses when calculating the efficiency.

### 3.3 Output Voltage Ripple Analysis of LCS

Due to the non-continuous nature of LCS, the output voltage ripple is affected. Like other discontinuous control schemes, some of which were shown in Figure 2.5 and Figure 2.6, this creates a trade-off between light load efficiency and output voltage ripple. Generally, the minimum output capacitance is determined by the hold-up time required to prevent the output voltage dropping below a certain threshold, and is usually greater than the minimum capacitance required to limit the amplitude of the low frequency ripple at the output voltage. Because of this, the maximum voltage ripple can be determined using equation 3.26. This equation is used to determine the minimum output capacitance to limit the low frequency ripple at the output voltage,

$$C_{OUT} \geq \frac{P_{OUT}}{2 \cdot \pi \times f_{LINE} \times V_{OUT} \times \Delta V_{OUT}}$$

where $f_{LINE}$ is frequency causing the low frequency ripple at the output of the PFC converter, and $\Delta V_{OUT}$ is the maximum output voltage ripple, peak to peak, that is permitted. By calculating $C_{OUT}$ from equation 3.26 and rearranging the same equation for $\Delta V_{OUT}$, equation 3.26 is used to determine the output voltage ripple of the PFC converter for a particular value of $C_{OUT}$.
\[ \Delta V_{OUT} = \frac{P_{OUT}}{2 \cdot \pi \times f_{LINE} \times V_{OUT} \times C_{OUT}} \]  

(3.26)

It is useful to observe that equation 3.26 is used to determine the magnitude of the low frequency ripple, or in practical terms, the effect of the input variation on the output of the PFC converter. In Figure 3.8, the low frequency ripple of a conventional PFC converter is shown. Due to the inductor between the input and output, the output voltage lags the input voltage by approximately 90°. Also, the output voltage ripple frequency is twice that of the input voltage frequency due to the effect of the rectification stage, shown previously in Figure 1.6.

![Figure 3.8 – Low Frequency Output Voltage Ripple Waveform from Rectification](image)

3.3.1 Output Voltage Ripple Analysis for FLCC
The output voltage ripple waveform for FLCC is shown in Figure 3.9 below. The AC coupled output voltage ripple waveform, $v_{\text{OUT}_{\text{ac}}}$, is quite different from the output voltage waveform in a conventional PFC converter. Because the low frequency ripple is discontinuous during LCS, the output voltage ripple is quite similar to other discontinuous control schemes. However, unlike the control schemes in Figure 2.5 and Figure 2.6, there is no need to control either the upper or lower voltage thresholds. The reason for this is demonstrated in equation 3.27,

$$\Delta V_{\text{OUT}} = \frac{n \times P_{\text{OUT}}}{f_{\text{LINE}} \times V_{\text{OUT}} \times C_{\text{OUT}}}, \text{ where } n = 1, 2, 3, \ldots$$

(3.27)

which is a modified version of equation 3.26. This equation estimates the output voltage ripple of the PFC converter operating in LCS. To fix the output voltage ripple for each LCS period, $n$, at each output power, $P_{\text{OUT}}$, equation 3.27 can be rearranged to solve for $P_{\text{OUT}}$, giving equation 3.28.

$$P_{\text{OUT}} < \frac{f_{\text{LINE}} \times \Delta V_{\text{OUT}} \times V_{\text{OUT}} \times C_{\text{OUT}}}{n}$$

(3.28)
3.3.2 Output Voltage Ripple Analysis for HLCC

The output voltage ripple waveform for HLCC is shown in Figure 3.10 below. The AC coupled output voltage ripple waveform, $v_{OUTac}$, resembles more closely to a sawtooth waveform, similar to what is seen in DCM control scheme waveforms of DC-DC converters.
Figure 3.10 – LCS HLCC Output Voltage Ripple

Similar to the analysis of the output voltage ripple for FLCC, the output voltage ripple for HLCC is given in equation 3.29,

$$\Delta V_{OUT} = \frac{m \times P_{OUT}}{f_{LINE} \times V_{OUT} \times C_{OUT}}, \text{ where } m = 1, 2, 3, \ldots$$  \hspace{1cm} (3.29)

which is a modified version of equation 3.26. This equation estimates the output voltage ripple of the PFC converter operating in LCS. Again, the output voltage ripple can be fixed for each $m$ at each $P_{OUT}$ by solving for $P_{OUT}$ to obtain equation 3.30.

$$P_{OUT} < \frac{f_{LINE} \times \Delta V_{OUT} \times V_{OUT} \times C_{OUT}}{m}$$  \hspace{1cm} (3.30)
3.4 Harmonic Analysis of LCS

In order to improve light load efficiency, many control schemes must make a necessary trade-off by improving such efficiency at the cost of the total harmonic distortion. LCS attempts to mitigate or even eliminate any trade-off between light load efficiency and THD. LCS effectively accomplishes this by pushing the harmonics of the fundamental frequency, 50-60Hz in the case of AC-DC power converters, into the sub-harmonic frequency range.

Figure 3.11 is an illustration of a harmonic spectrum for a conventional AC-DC converter with PFC. The harmonics of the fundamental frequency, where the fundamental frequency usually is referred to as the line frequency, are distributed in odd multiples of the line frequency, where the amplitude of the harmonics decreases with increasing harmonics of the fundamental frequency. An amplitude distribution of the harmonics is easily represented in a chart similar to Figure 3.12.

![Figure 3.11 – Harmonic Amplitudes and Distribution in a Conventional PFC Converter](image)
LCS harmonic analysis is different than the approach normally taken to calculate and measure THD for conventional PFC converters. Equation 2.6 can be used calculate THD$_i$ or THD$_v$ if voltage is substituted for current. Due to the symmetrical property of AC sinusoidal waveforms, even harmonics are not present and odd harmonics are only considered in such waveforms in order to determine THD. Not all converter topologies or control schemes contain sinusoidal voltages or currents, which affect the AC power distribution grid negatively. For example, half-wave rectifier circuits, Figure 3.13 (a), conduct non-sinusoidal current because current is only conducted during either the positive or negative cycle of the AC voltage source depending of the direction of the rectifier. This results in a non-symmetrical current waveform, as shown in Figure 3.13 (b), causing a DC offset in the harmonics due to the average current being greater than zero, as shown in Figure 3.13 (c). Full-wave rectifier circuits, Figure 3.14 (a), conduct sinusoidal current because current is conducted in both the positive and negative cycles of the AC voltage source.
Figure 3.13 – (a) Half-wave Rectifier Circuit, (b) Voltage and Current Waveforms for a Half-wave Rectifier, and (c) Harmonic Amplitudes for a Half-wave Rectifier
Figure 3.14 – (a) Full-wave Rectifier Circuit, (b) Voltage and Current Waveforms for a Full-wave Rectifier, and (c) Harmonic Amplitudes for a Full-wave Rectifier.
Voltage and current distortions are limited by certain industry standards such as IEEE Std 519-1992, which limits not only odd harmonics, but even harmonics as well to the limit of 25% of their corresponding odd harmonic amplitudes for current distortion only [6]. Voltage harmonic distortion, as it relates to SMPSs, is a byproduct of current harmonic distortion and unlike current harmonic distortion which has limits based on the harmonic number, IEEE Std 519-1992 limits THD$_{v}$ to 5% for bus voltages less than 69kV, where each harmonic is limited to less than 3%.

LCS generates current harmonic distortion like any other PFC converter scheme aimed at improving light load efficiency. However, in LCS, current harmonic distortion or THD$_{i}$, is generated in two ways. First, THD$_{i}$ is generated by non-sinusoidal currents drawn during the line cycle in the conduction period. And second, THD$_{i}$ is generated by what is known as sub-harmonic currents created during the LCS period, caused by partial conduction of the sinusoidal waveform. Sub-harmonic current limits are not specified in the IEEE Std 519-1992 standard, but such harmonics do contribute to THD$_{i}$.

### 3.4.1 Harmonic Analysis for FLCC

The current harmonics generated from FLCC can be separated into two contributing components: conduction period harmonics and LCS period harmonics. As seen in Figure 3.5, the conduction period is the active PFC portion of the LCS period. It generates harmonics currents proportionate to the power conducted during the conduction period. If only the conduction period is considered, the THD caused by the harmonics in the conduction period can be reflected in equation 3.31.
The LCS period generates harmonics due to the combination of the conduction period and skipping period, generating sub-harmonics and inter-harmonics. If the harmonic amplitudes are known, equation 3.32 can be used to calculate the THD for harmonic currents of LCS with LCS period $2N$ for all $k$ except when $k$ is equal to $2N$, where $N$ is a half line cycle.

$$THD_{\text{COND}} = \sqrt{\sum_{k=3,5,7,...}^{\infty} \frac{I_{k\text{rms}}^2}{I_{1\text{rms}}}}$$

(3.31)

$$THD_{\text{FLCC}} = \sqrt{\sum_{k=1}^{\infty} \frac{I_{k\text{rms}}^2}{2N_{\text{rms}}}} \cdot 2N \notin k$$

(3.32)

3.4.2 Harmonic Analysis for HLCC

Similar to FLCC, HLCC generates current harmonics from the conduction period and LCS period. Similar to FLCC, if only the conduction period is consider – half line cycles in this case – the THD can be calculated using equation 3.31. To calculate the THD for HLCC, equation 3.32 is modified to account for half line cycles giving equation 3.33.

$$THD_{\text{HLCC}} = \sqrt{\sum_{k=1}^{\infty} \frac{I_{k\text{rms}}^2}{N_{\text{rms}}}} \cdot N \notin k$$

(3.33)

The symmetry of the HLCC waveform must reflect Figure 3.6 in order to pass the IEEE Std 519-1992 – Table 10.3, where it states that a dc offset from half-wave converters are not allowed. Therefore, the harmonics with a DC offset will not be analyzed.
Chapter 4

Line Cycle Skipping Control Implementation in PFC Converters using Digital Control

This chapter will discuss the design implementation of LCS control method in a PFC converter using digital control. The first part of this chapter will list the requirements to implement LCS and describe the LCS control method. The second part of this chapter described the digital control implementation of LCS control and that features are required from microcontrollers. Finally, the third part of this chapter will discuss the practical implementation of LCS in a low cost MCU, and the techniques required to adapt it to a CRM PFC boost converter. This chapter will show that most low-cost microcontrollers can implement LCS on any PFC topology, demonstrating the low computational requirement for a LCS control scheme.

4.1 LCS Control Implementation for PFC Converters

The implementation of LCS control requires two parameters:

1. Zero-crossing of input line voltage
2. Output power

In order to avoid additional harmonic distortion and to ensure proper line cycle detection, the zero crossing of the input line voltage must be sensed. The output power of the PFC converter must also be measured, either directly or indirectly. The output power is a feedback parameter to the LCS control used to determine the conduction period and the skipping period for either FLCC or HLCC.
4.1.1 LCS Control Flow Diagram

Figure 4.1 below is the control flow diagram for LCS.

![LCS Control Flow Diagram](image-url)
Before LCS is activated, the output power is being measured. When the output power, $P_{\text{OUT}}$, is measured to be less than power threshold to active LCS, $P_{\text{LCS}}$, the LCS control scheme is activated. Based on the measured output power, the number of conduction cycles, $N_{\text{COND}}$ and $N_{\text{SKIP}}$ skipping cycles is selected. If $P_{\text{OUT}}$ is greater than $P_{\text{LCS}}$, at any point, LCS is disabled. The input line voltage is measured to detect the zero crossing in order to count the line cycles. When a zero crossing is detected, a counter variable, $n$, is incremented. When $n$ is greater than $N_{\text{COND}}$, $n$ is reset, the conduction period ends, and the skipping period begins. Again, the input line voltage is measured to detect a zero-crossing to increment $n$ until it is greater than $N_{\text{SKIP}}$, and end of the skipping period. Once the skipping period ends, the conduction period begins again.

**4.1.2 LCS Conduction Period and Skipping Period**

LCS operates as a function of line cycles, and is inherently discrete. The conduction period and skipping period is quantified by a number of line cycles. The LCS period is the sum of these two periods. Therefore, in order to calculate $N_{\text{COND}}$ and $N_{\text{SKIP}}$, an array or table of values may be used. An example of such a table is given in Table 4.1 below. It is up to the designer to determine for each output power level below the LCS power threshold, $P_{\text{LCS}}$, based on efficiency, harmonics and output voltage ripple requirements.
The boundaries between the output power levels are also determined by the designer. As illustrated in Figure 4.2 and Figure 4.3 for FLCC and HLCC, when the threshold for the next power level is crossed, a new set of conduction period and skipping period is determined.

<table>
<thead>
<tr>
<th>Output Power ($P_{OUT}$)</th>
<th>Conduction Period Function ($N_{COND}[P_{OUT}]$)</th>
<th>Skipping Period Function ($N_{SKIP}[P_{OUT}]$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{OUT_1}$ to $P_{OUT_2}$</td>
<td>$N_{COND_1}$</td>
<td>$N_{SKIP_1}$</td>
</tr>
<tr>
<td>$P_{OUT_2}$ to $P_{OUT_3}$</td>
<td>$N_{COND_2}$</td>
<td>$N_{SKIP_2}$</td>
</tr>
<tr>
<td>$P_{OUT_3}$ to $P_{OUT_4}$</td>
<td>$N_{COND_3}$</td>
<td>$N_{SKIP_3}$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

Table 4.1 – LCS Lookup Table

Figure 4.2 – LCS Output Power Boundaries for Conduction and Skipping Periods for FLCC
There are many ways a designer can implement LCS. One such method is to create a controller using a digital control scheme programmed on a general purpose microcontroller unit (MCU). This controller is used to control an AC-DC PFC converter. Using a low-cost general purpose MCU to implement the control scheme demonstrates the simplicity of the LCS control method.

**4.2 LCS Control Using a Microcontroller**

There are many ways a designer can implement LCS. One such method is to create a controller using a digital control scheme programmed on a general purpose microcontroller unit (MCU). This controller is used to control an AC-DC PFC converter. Using a low-cost general purpose MCU to implement the control scheme demonstrates the simplicity of the LCS control method.

**4.2.1 General Purpose Microcontroller (MCU)**

A general purpose microcontroller unit (MCU) differs from a microprocessor unit (MPU), typically found in personal computers and other electronics, in several ways. Typically, MCUs have embedded permanent and temporary memory, which is used to store and execute a program that been saved onto the device, whereas MPUs separate their memory from their processing core [58]. Because MCUs combine both the processing core and memory on one chip, they have much less memory than a typical MPU application. This embedded permanent and temporary memory, also known as
Electrically Erasable Programmable Read-Only Memory (EEPROM) and Random Access Memory (RAM), respectively, is where the program is stored and executed. It allows the MCU to start-up very quickly and begin to execute its pre-programmed code. Also, MCUs have an embedded power supply in order to operate off a single rail voltage external to the device, whereas an MPU requires several different voltages to power its core and other peripherals [58].

There are many features amongst MCUs. They can be differentiated by instruction size, such as 8-Bit, 16-Bit, or 32-Bit. They can be differentiated by central processing core (CPU) clock frequency, which determines the speed at which the instructions can be executed or how fast memory is read. This speed can range from a few megahertz to hundreds of megahertz depending on the MCU and vendor. Another feature of MCUs is the embedded peripherals. Such peripherals can include Analog to Digital Converters, Digital Input and Output ports, Digital Timers, etc. Peripherals vary amongst the many MCUs on the market.

4.2.2 MCU Requirements for LCS in a PFC Converter

As outlined in section 4.1, the output power and zero-crossing of the input line voltage are key sensory parameters for LCS. Therefore, the microcontroller must be capable of detecting both. Many modern general purpose MCUs include at least one Analog-to-Digital Converter (ADC). An ADC is capable of converting a voltage into its digital representation interpreted by the MCU. An ADC channel can be shared for multiple voltage inputs using a Multiplexor (MUX) device if the MCU has only one ADC.
channel. Table 4.2 contains the minimum features needed from the MCU to implement LCS in PFC converters.

Table 4.2 – Minimum MCU Requirements for LCS in a PFC Converter

<table>
<thead>
<tr>
<th>Requirement</th>
<th>MCU Feature(s)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCS Program</td>
<td>EEPROM, RAM</td>
<td>With sufficient space for program and temporary variables</td>
</tr>
<tr>
<td>Input Voltage Sensing</td>
<td>ADC</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Sensing</td>
<td>ADC</td>
<td></td>
</tr>
<tr>
<td>Output Current Sensing</td>
<td>ADC</td>
<td>Current can be converted to voltage before ADC sensing</td>
</tr>
<tr>
<td>Switching Signal</td>
<td>Digital I/O</td>
<td>Using an I/O to either generate the PWM or as an EN signal for the gate driver(s)</td>
</tr>
</tbody>
</table>

4.3 LCS Implementation in a PFC Converter using a MCU

No matter the topology of the PFC converter, it is possible to implement LCS using a MCU. Consider a black-box PFC converter, as shown in Figure 4.4, which uses a MCU to implement LCS. The MCU has three inputs measured through the ADC channels: line input voltage, PFC converter output voltage, and transduced PFC converter output current into voltage. A single output to the PFC converter from the MCU that is required is a switching signal: either a single digital line to enable or disable the gate driver, or the PWM signal itself that provides the necessary frequency and duty cycle information that may be either enabled or disabled.
4.3.1 CRM PFC Converter using an 8-Bit MCU

An application where a PFC converter operating in CRM is controlled by an 8-Bit MCU has been published by STMicroelectronics [59]. The MCU in the application, with part number ST7FLIT19B, contains general purpose MCU features as well as an integrated analog comparator and an internal programmable voltage reference [60]. These features allow the MCU to be able to implement CRM on a PFC converter with a closed voltage loop.

LCS control can be implemented in a CRM PFC converter using the ST7FLIT19B. Figure 4.5 shows the interconnection of a CRM PFC converter with a ST7FLIT19B MCU programmed and configured for CRM and LCS control. The CRM voltage loop regulates the output voltage of the PFC converter and remains relatively unchanged from the circuit in [59]. The LCS control loop regulates the output power to the load. Because current is not measured in Figure 4.5, it is inferred from the on-time. Look-up tables (LUTs) are used to match the on-time, generated by the CRM voltage loop’s PID, with
the output power delivered to the load. Because this CRM PFC converter is intended to be universal for all line voltage inputs, an input voltage detection block is used to switch LUTs depending on the AC mains type. Once output power is determined to be less than the threshold needed for LCS, then LCS is activated until the threshold is surpassed. Once LCS is activated, the control flow outlined in Figure 4.1 is followed.

![Diagram of PFC Converter Implementing LCS with ST7FLIT19B](image)

**Figure 4.5 – PFC Converter Implementing LCS with ST7FLIT19B**

### 4.3.2 Digital Line Cycle Detection

The zero-crossing point of the input line voltage is critical to LCS algorithm in order to determine when a new line cycle occurs. The zero-crossing point of the input line voltage is when the positive line cycle transitions to the negative line cycle, or vice versa, at zero volts, as shown in Figure 4.6. Counting line cycles will allow LCS to determine...
when the conduction period and the skipping period have expired, so that it may switch between them.

![Graph of Zero-crossing Point of Input Line Voltage](image)

**Figure 4.6 – Zero-crossing Point of Input Line Voltage**

The input voltage is measured by the MCU through an ADC channel. However, most MCUs, including the ST7FLIT19B MCU, do not measure AC voltage. In order to detect the zero-crossing point, a circuit can be used to rectify and scale the AC input line voltage. An example of such a circuit is shown in Figure 4.7 below, where the AC input line voltage is rectified and scaled in order to connect to the ADC of the MCU. Once $v_{IN}$ has been scaled to $V_{IN,SCALED}$, it can be read by the MCU to implement the line cycle detection algorithm in order to implement LCS.
The sampling of the input line voltage by the MCU is not likely to sample a zero-voltage due to DC offset errors and sampling rate. Setting a voltage threshold may work, but it will only determine a new cycle too early or too late relative to the actual zero-
crossing voltage. A more reliable method for detecting the zero crossing is to determine the change in slope of the $V_{IN,SCALED}$ signal.

Figure 4.9 is a control flow diagram for line cycle detection using the slope of the waveform. The ADC of the MCU samples the input voltage and compares it to the previous value. If the current value is less than the previous value, the waveform is determined to have a negative slope, or greater than $T_{LINE}/4$ of the input voltage waveform. If the current value is greater than the previous value and a negative slope has been registered in previous cycles, then a positive slope is detected and the zero-crossing point has occurred. The line cycle count, n, is incremented and the slope variable is set to a positive value. If the current value was greater than the previous value but the slope variable was registered to be positive in the previous cycles, then the input voltage waveform is less than $T_{LINE}/4$ portion and must wait for the slope to go negative before detecting a new line cycle.
4.3.3 LCS Output Power LUT with Indirect Current Measurement

Once the designer has decided what voltage ripple, THD, and efficiency are permitted at light load, a lookup table can be generated that maps the output power range with the conduction period and skipping period pairs, as seen in Table 4.1. Because the circuit described in Figure 4.5 does not measure current directly, the output power must be inferred from the on-time generated by the CRM voltage loop. The on-time for a PFC CRM boost converter can be calculated from equation 4.1 below,

\[ t_{ON} = \frac{2 \cdot L \cdot P_{IN}}{(V_{IN,RMS})^2} \]  \hspace{1cm} (4.1)
where $L$ is the boost inductance and $V_{IN,RMS}$ is the RMS of the input line voltage. If the efficiency of the converter, $\eta$, is known,

$$P_{IN} = \frac{P_{OUT}}{\eta}$$  \hspace{1cm} (4.2)

then equation 4.2 can be substituted into equation 4.1 to produce equation 4.3.

$$t_{ON} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot (V_{IN,RMS})^2}$$  \hspace{1cm} (4.3)

Solving for output power, $P_{OUT}$, as a function of on-time, $t_{ON}$, yields equation 4.4.

$$P_{OUT}(t_{ON}) = \frac{t_{ON} \cdot \eta \cdot (V_{IN,RMS})^2}{2 \cdot L}$$  \hspace{1cm} (4.4)

With equation 4.4, $P_{OUT}$ can be calculated based on the $t_{ON}$ generated by the voltage loop and the calculated $V_{IN,RMS}$, measured by the ADC of the MCU.

With $P_{OUT}$ determined by $t_{ON}$, the MCU can determine when the LCS threshold, $P_{LCS}$, has been crossed. However, when the LCS control is activated by the MCU, the $t_{ON}$ is based on the input power, $P_{IN}$, conducted during the conduction period. Therefore, in order to map the $t_{ON}$ with the actual $P_{OUT}$, it must be scaled based on the conduction period and skipping period set by the LCS algorithm. This is done by substituting equation 3.1 into equation 4.1 to produce equation 4.5.

$$t_{ON,SCALED} = \frac{2 \cdot L \cdot \left( \frac{P_{COND} \cdot N_{COND}}{N_{COND} + N_{SKIP}} \right)}{(V_{IN,RMS})^2}$$  \hspace{1cm} (4.5)
Because $P_{COND}$ is the $P_{IN}$ used by the CRM voltage loop to determine $t_{ON}$, equation 4.5 can be rearranged to equation 4.6,

$$t_{ON, SCALED} = \frac{2 \cdot L \cdot P_{COND}}{(V_{IN, RMS})^2} \left( \frac{N_{COND}}{N_{COND} + N_{SKIP}} \right)$$  \hspace{1cm} (4.6)$$

and then simplified into equation 4.7.

$$t_{ON, SCALED} = t_{ON} \cdot \left( \frac{N_{COND}}{N_{COND} + N_{SKIP}} \right)$$  \hspace{1cm} (4.7)$$

With the ability to calculate $t_{ON, SCALED}$ from $t_{ON}$ and the conduction period, $N_{COND}$, and skipping period, $N_{SKIP}$, the MCU can then determine the actual $P_{OUT}$ value. With the correct $P_{OUT}$, the MCU can use the LCS lookup table to determine the appropriate $N_{COND}$ and $N_{SKIP}$ for that output power range.
Chapter 5

Simulations and Experimental Results

This chapter will show that the LCS method can be implemented on an existing boost PFC converter operating in CRM by simulation and experimental prototype. The agreement between the simulated and experimental waveforms will demonstrate the feasibility for a PFC converter operating using LCS control. Experimental results using the CRM PFC boost converter prototype, will show that LCS can dramatically improve the light load performance of PFC converters.

5.1 PFC Converter Design

A PFC boost converter operating in CRM was designed with reference to [59-61], shown in Figure 5.1 and Table 5.1.

![Figure 5.1 – PFC Boost Converter Operating in CRM with a ST7FLIT19B MCU](image-url)

Figure 5.1 – PFC Boost Converter Operating in CRM with a ST7FLIT19B MCU
A simulation of the CRM PFC converter from Figure 5.1 and Table 5.1 was created using PSIM. The results are shown from Figure 5.2 to Figure 5.8 below.

**Table 5.1 – CRM PFC Boost Converter Design Specifications**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Switching Frequency</td>
<td>22 kHz</td>
</tr>
<tr>
<td>Input Line Voltages, $V_{in_{AC}}$</td>
<td>85-265 V$_{RMS}$</td>
</tr>
<tr>
<td>Output Voltage, $V_o$</td>
<td>400 V$_{DC}$</td>
</tr>
<tr>
<td>Output Power</td>
<td>100 W</td>
</tr>
<tr>
<td>Boost Inductor, $L_{boost}$</td>
<td>1 mH</td>
</tr>
<tr>
<td>Boost Inductor Aux. Winding</td>
<td>1:12 Turns</td>
</tr>
<tr>
<td>Input Filter Capacitor, $C_{in}$</td>
<td>0.47 uF ± 20%</td>
</tr>
<tr>
<td>Output Boost Capacitor, $C_{out}$</td>
<td>120 uF ± 20%</td>
</tr>
<tr>
<td>Boost MOSFET</td>
<td>STD10NM60N (600V, 8A)</td>
</tr>
<tr>
<td>Boost Diode</td>
<td>S8KC-13 (800V, 8A)</td>
</tr>
<tr>
<td>Diode Bridge Rectifier</td>
<td>GBU6J-BP (600V, 6A)</td>
</tr>
<tr>
<td>MCU</td>
<td>ST7FLIT19B, 8MHz</td>
</tr>
<tr>
<td>Low Side MOSFET Driver</td>
<td>MCP1407-E</td>
</tr>
</tbody>
</table>

**5.2 LCS PFC Converter Simulation**

A simulation of the CRM PFC converter from Figure 5.1 and Table 5.1 was created using PSIM. The results are shown from Figure 5.2 to Figure 5.8 below.
Figure 5.2 – Simulated CRM PFC Boost Results: $P_{IN,AVG} = 50W$

Figure 5.3 – Simulated FLCC: $P_{IN,AVG} = 25W$, $P_{COND} = 50W$, $N_{COND} = 1$, $N_{SKIP} = 1$
Figure 5.4 – Simulated HLCC: $P_{IN,AVG} = 10W$, $P_{COND} = 50W$, $M_{COND} = 1$, $M_{SKIP} = 4$

Figure 5.5 – Simulated FLCC w/ $V_{OUT}$ Ripple: $P_{IN,AVG} = 16W$, $P_{COND} = 32W$, $N_{COND} = 1$, $N_{SKIP} = 1$
Figure 5.6 – Simulated FLCC FFT: $P_{IN,AVG} = 16W$, $P_{COND} = 32W$, $N_{COND} = 1$, $N_{SKIP} = 1$

Figure 5.7 – Simulated HLCC w/ $V_{OUT}$ Ripple: $P_{IN,AVG} = 16W$, $P_{COND} = 48W$, $M_{COND} = 1$, $M_{SKIP} = 2$

$\Delta V_O = 6.40V$
5.3 LCS Experimental Results

A 100W AC-DC CRM PFC boost converter prototype was built and implemented with a ST7FLIT19B MCU according to Figure 5.1 and Table 5.1 in order to implement the LCS control method to improve the light load efficiency and reduce the THD. Figure 5.9, below, is a photo of the experimental prototype. This prototype is intended to be the first stage of a two-stage power supply for a Class D power supply meeting Class D harmonics requirements listed in [5]. The AC input line voltage was supplied by a California Instruments AC Power Supply and an Agilent DC Electronic Load.
5.3.1 Validating LCS Simulations with Experimental Results

Figure 5.10, Figure 5.11, and Figure 5.12 are the prototype’s experimental input voltage and current waveforms operating without LCS at 50W, with FLCC at 50W, and with HLCC at 50W, respectively. These waveforms closely resemble Figure 5.2, Figure 5.3, and Figure 5.4 from the simulated results in section 5.2. The output voltage ripple and input power waveforms are given for FLCC and HLCC in Figure 5.13 and Figure 5.14, which produce the expected output given from the simulations in Figure 5.5 and Figure 5.7. The FFT of the input current waveforms for FLCC and HLCC are shown in Figure 5.15 and Figure 5.16, which match the distribution and proportion of harmonics in Figure 5.6 and Figure 5.8. With Table 1 describes the specifications, components and the values of the components used for the boost converter prototype. Fig. 8 shows the input line voltage and the input line current for the prototype at 50W load operating in conventional BCM with constant on-time. Fig. 9 shows the prototype operating with LCS
using Method 1 for an average output power of 25W. Sinusoidal line current is conducted for 1 line cycle at a power level of 50W. The total average power is 25W. Fig. 10 shows input voltage and current waveforms using Method 2 for 10W.

Figure 5.10 – Experimental CRM PFC Boost without LCS: $P_{IN\text{AVG}} = 50W$
Figure 5.11 – Experimental FLCC: \( P_{\text{COND}} = 50\text{W}, N_{\text{COND}} = 1, N_{\text{SKIP}} = 1, P_{\text{IN,AVG}} = 25\text{W} \)

Figure 5.12 – Experimental HLCC: \( P_{\text{COND}} = 50\text{W}, M_{\text{COND}} = 1, M_{\text{SKIP}} = 4, P_{\text{IN,AVG}} = 10\text{W} \)
Figure 5.13 – Experimental FLCC: $\Delta V_O = 6.65\text{V}_{pk-pk}$, $N_{COND} = 1$, $N_{SKIP} = 1$, $P_{IN,AVG} = 16.7\text{W}$

Figure 5.14 – Experimental HLCC: $\Delta V_O = 6.70\text{V}_{pk-pk}$, $M_{COND} = 1$, $M_{SKIP} = 2$, $P_{IN,AVG} = 16.21\text{W}$
Figure 5.15 – Experimental FLCC FFT: NC\text{OND} = 1, N\text{SKIP} = 1, P_{IN,AVG} = 16.70W

Figure 5.16 – Experimental HLCC FFT: M\text{COND} = 1, M\text{SKIP} = 2, P_{IN,AVG} = 16.21W
5.3.2 LCS Efficiency and THD<sub>i</sub> Results – Open-loop without Output Voltage Ripple Limit

Light load and THD<sub>i</sub> results for LCS using FLCC are shown below. When output voltage ripple isn’t critical, the maximum light load efficiency and THD<sub>i</sub> results can be realized. Open-loop control results are given over the entire input voltage range of the 100W CRM PFC converter prototype. For an input voltage of 265V<sub>RMS</sub>, Figure 5.17 and Figure 5.18, light load efficiency gains up to 10% and THD<sub>i</sub> reductions up to 32.6% from 40W down to 10W output power are achieved. For an input voltage of 220V<sub>RMS</sub>, Figure 5.19 and Figure 5.20, light load efficiency gains up to 8.3% and THD<sub>i</sub> reductions up to 17.8% can be seen. For an input voltage of 120V<sub>RMS</sub>, Figure 5.21 and Figure 5.22, light load efficiency gains up to 7.2% and THD<sub>i</sub> reductions up to 15.3% can be seen. And, finally, in Figure 5.23 and Figure 5.24, for an input voltage of 85V<sub>RMS</sub> both light load efficiency and THD<sub>i</sub> are improved by 6% and 12.9% respectively.

![Efficiency Graph](image-url)

Figure 5.17 – Efficiency Results for FLCC: V<sub>IN</sub> = 265V<sub>RMS</sub>
Figure 5.18 – THD Results for FLCC: $V_{IN} = 265V_{RMS}$

![Graph showing THD results for FLCC with 265Vrms input, comparing Conventional PFC and LCS PFC.]

Figure 5.19 – Efficiency Results for FLCC: $V_{IN} = 220V_{RMS}$

![Graph showing efficiency results for FLCC with 220Vrms input, comparing Conventional PFC and LCS PFC.]

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Figure 5.20 – THD Results for FLCC: $V_{IN} = 220V_{RMS}$

Figure 5.21 – Efficiency Results for FLCC: $V_{IN} = 120V_{RMS}$
Figure 5.22 – THD Results for FLCC: $V_{IN} = 120V_{RMS}$

Figure 5.23 – Efficiency Results for FLCC: $V_{IN} = 85V_{RMS}$
5.3.3 LCS Efficiency and THD Results – with Output Voltage Ripple Limit

When the output voltage ripple is a constraint in the design, equation 3.28 is used to calculate the maximum output power for each increment in skipping period. The output voltage ripple limit – peak to peak – is selected to be below 6V. From those calculations a LUT can be generated as shown in Table 5.2, below. The LUT is then programmed into the ST7FLIT19B’s LCS algorithm. The closed-loop efficiency results for LCS using FLCC with an output voltage ripple limit and 120V\textsubscript{RMS} input voltage is given in Figure 5.25. When the output power reaches 16W, the LCS threshold is reached, and the LCS algorithm begins with $N_{\text{SKIP}}=1$. From 16W to 1W, $N_{\text{SKIP}}$ increases from 1 to 15 full line cycles. A specific advantage of LCS for CRM PFC converters is the ability to limit the maximum frequency over the line cycle at light load, eliminating the need for minimum loading to prevent an overvoltage condition.
With a limit on the output voltage ripple, the light load efficiency is still significantly improved. At \( P_{\text{OUT}} = 16W \), the light load efficiency is increased by 5.6%. THD\(_i\) results for closed-loop LCS control using FLCC are also measured in Figure 5.26 below. At \( P_{\text{OUT}} = 16W \), the THD\(_i\) is decreased by 11.7%.

### Table 5.2 – LCS Lookup Table

<table>
<thead>
<tr>
<th>Output Power ((P_{\text{OUT}}))</th>
<th>Conduction Period Function ((n_{\text{COND}}[P_{\text{OUT}}]))</th>
<th>Skipping Period Function ((n_{\text{SKIP}}[P_{\text{OUT}}]))</th>
</tr>
</thead>
<tbody>
<tr>
<td>16W to 8W</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8W to 5.3W</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>5.3W to 4W</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>4W to 3.2W</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>3.2W to 2.7W</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>2.7W to 2.3W</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>2.3W to 1.5W</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>1.5W to 1W</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>&lt;1W</td>
<td>1</td>
<td>15</td>
</tr>
</tbody>
</table>

With a limit on the output voltage ripple, the light load efficiency is still significantly improved. At \( P_{\text{OUT}} = 16W \), the light load efficiency is increased by 5.6%. THD\(_i\) results for closed-loop LCS control using FLCC are also measured in Figure 5.26 below. At \( P_{\text{OUT}} = 16W \), the THD\(_i\) is decreased by 11.7%.
Figure 5.25 – Closed-loop LCS Efficiency Results for FLCC with $V_{\text{RIPPLE}}$ Limit: $V_{\text{IN}} = 120V_{\text{RMS}}$

Figure 5.26 – Closed-loop LCS THD Results for FLCC $V_{\text{RIPPLE}}$ Limit: $V_{\text{IN}} = 120V_{\text{RMS}}$
5.3.4 IEC 61000-3-2 Class D Harmonic Current Results

Comparisons of harmonic currents of the PFC converter prototype operating with and without LCS are measured according to the IEC 61000-3-2 harmonic current limit for Class D equipment [5]. In Figure 5.27, the harmonic current limits for Class D equipment is given along the harmonic current measurements for LCS operating in FLCC and HLCC, and without LCS, operating as a conventional PFC converter. As can be seen from Figure 5.27, the 3\textsuperscript{rd} harmonic current for LCS is substantially less than the same converter operating without LCS, with a 62\% reduction for FLCC and a 71.5\% reduction for HLCC. Every LCS harmonic, up to the 39\textsuperscript{th} harmonic with the exception of the 7\textsuperscript{th} harmonic, is the same or less when compared to the converter operating without LCS.

Class D harmonic currents limits for FLCC with $N_{\text{SKIP}} = 1$ and $N_{\text{SKIP}} = 2$ are compared in Figure 5.28, where the output power is 16W and 8W respectively. With more line cycles skipped, the percentage of the harmonic amplitude increases slightly. Both remain significantly under the limit for that power level. The same observation can be made in HLCC from Figure 5.29, where $M_{\text{SKIP}} = 2$ and $M_{\text{SKIP}} = 4$ for output power levels 16W and 8W respectively.

From these results, it can be concluded that LCS can improve the light load THD of according to the IEC 61000-3-2 harmonic currents standard when compared to a conventional PFC converter control scheme.
Figure 5.27 – IEC 61000-3-2 Class D THD, Results Comparison: $P_{\text{OUT}} = 16\,\text{W}$

Figure 5.28 – IEC 61000-3-2 Class D THD, Results for FLCC: $P_{\text{OUT1}} = 16\,\text{W}$, $P_{\text{OUT2}} = 8\,\text{W}$
5.3.5 Very Light Load LCS Results and Waveforms

At very light load, the power loss due to the MCU and MOSFET driver IC become a larger proportion of the overall loss if operating continuously. With LCS, however, not only are the converter losses lower due to the higher efficiency during $P_{\text{COND}}$, but the MOSFET driver IC loss is reduced due to intermittent operation. Table 5.3 shows the converter, MCU, and driver IC losses for 1W, 2W, and 5W output power. As $N_{\text{SKIP}}$ increases, the average converter and MOSFET driver IC losses over the LCS period decrease. The MCU losses, however, remain constant in order to implement the LCS algorithm. The THD$_i$ still remains very low due to the $P_{\text{COND}}$ over one line cycle drawing a higher current with less distortion than would be normally be present at lighter loads.
The input line voltage and input current waveforms for LCS operating in FLCC at 1W output power are shown in Figure 5.30. A zoomed-in waveform of Figure 5.30 is given in Figure 5.31. The expected $I_{IN}$ waveform for $P_{COND} = 30W$ is observed, showing that LCS can conduct clean input current waveforms at very light load with a large amount of skipping cycles.

Table 5.3 – Very Light Load Efficiency Results at 120V$_{RMS}$

<table>
<thead>
<tr>
<th>Output Power ($P_{OUT}$)</th>
<th>Skipping Period ($N_{SKIP}$)</th>
<th>Converter Loss</th>
<th>MCU Loss</th>
<th>Driver IC Loss</th>
<th>Efficiency</th>
<th>THD$_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1W</td>
<td>29</td>
<td>72.4 mW</td>
<td>47.7 mW</td>
<td>1.8 mW</td>
<td>87.3%</td>
<td>13.4%</td>
</tr>
<tr>
<td>2W</td>
<td>14</td>
<td>150 mW</td>
<td>47.7 mW</td>
<td>3.5 mW</td>
<td>90.2%</td>
<td>13.6%</td>
</tr>
<tr>
<td>5W</td>
<td>5</td>
<td>420 mW</td>
<td>47.7 mW</td>
<td>8.7 mW</td>
<td>91.6%</td>
<td>13.4%</td>
</tr>
</tbody>
</table>

The input line voltage and input current waveforms for LCS operating in FLCC at 1W output power are shown in Figure 5.30. A zoomed-in waveform of Figure 5.30 is given in Figure 5.31. The expected $I_{IN}$ waveform for $P_{COND} = 30W$ is observed, showing that LCS can conduct clean input current waveforms at very light load with a large amount of skipping cycles.

Figure 5.30 – Very Light Load FLCC $V_{IN}$ and $I_{IN}$: $N_{COND} = 1, N_{SKIP} = 29, P_{OUT} = 1W$
Figure 5.31 – Zoomed-In Very Light Load FLCC $V_{IN}$ and $I_{IN}$: $N_{COND} = 1$, $P_{COND} = 30W$
Chapter 6

Conclusion and Future Work

6.1 Conclusions

Power distribution by AC electricity requires the use of AC-DC converters to power a wide range of power electronics. As the number of non-linear electronic devices connected to the AC electricity grid increases, more emphasis has been placed on improving the efficiency and harmonic distortion caused by such devices. The light load performance of AC-DC PFC converters is an important design consideration for power electronics engineers. There are many methods to improve the light load efficiency of PFC converters, but often come at the cost of additional harmonic distortion or increased cost and complexity. Using similar principles to previous line cycle commutation techniques, a Line Cycle Skipping method is proposed to increase the light load efficiency and reduce the THD for a universal line input voltage AC-DC PFC converter.

The principles of LCS allow the PFC converter to achieve increased light load performance by the introduction of a conduction period and a skipping period, which make up the LCS period. LCS can achieve this by conducting higher power over one or one-half line cycle, and then skipping or not conducting power over the next one or more line cycles. This allows the output power to remain constant at light load, while conducting higher input power over one or one-half line cycles. By conducting higher input power over a portion of the entire LCS period, the efficiency and the THD can be improved at lower output power levels, thus improving the light load performance of PFC converters.
LCS was realized using a digital controller without increasing the complexity or cost to a conventional AC-DC PFC converter. Using a low cost 8-bit MCU, the LCS control algorithm requires measurement of only the input line voltage and output power. LCS control is then programmed with a LUT for each input line voltage range to determine the conduction period and skipping period for each output power level measured. With these very basic requirements for implementation, LCS control can be easily adopted or adapted to any PFC converter.

Simulated and experimental waveforms from a 100W CRM PFC converter prototype have shown that LCS is feasible. The experimental results show that LCS can dramatically increase the light load efficiency and reduce the THD, over the entire light load range, getting closer to the goals set out by Figure 1.11 and Figure 1.12. Section 5.3.2 demonstrated that light load efficiency and THD, improvement results held across the universal input line voltage. Light load efficiency and THD, improvements at an input line voltage of 265V_{RMS} have shown an improvement of 10% and 32.6%, respectively, over the PFC converter operating in a conventional CRM control scheme. Compared to a conventional PFC converter control scheme, LCS can drastically reduce the harmonic currents regulated by the IEC 61000-3-2 harmonics standard. A 3rd harmonic reduction of 62% for FLCC and 71.5% for HLCC can be achieved over the conventional PFC control scheme.

6.2 Future Work

The application of LCS can be expanded to other PFC topologies and conduction mode types. Some of the weaknesses in LCS, such as output voltage ripple increase and
sub-harmonic generation that could prevent it from being implemented in higher output power applications, can be addressed with multi-phase implementation. With multi-phase PFC converters implementing LCS, the conduction period and skipping period can be alternated to cancel the input power ripple. This allows the PFC converter to still benefit from LCS’s improved light load performance while eliminating the increased output voltage ripple and generation of sub-harmonics.

Current harmonic standards do not directly address the generation of sub-harmonics in AC-DC converters. More exploratory research on sub-harmonics and its impacts is required in order to address potential concerns with LCS. However, due to the line voltage synchronization built into LCS, a Monte Carlo simulation or similar technique can give insight into the harmonic analysis of the distribution point of load affected by N sub-harmonic generating devices.
References


F. Gaillard. (2013, Microprocessor (MPU) or Microcontroller (MCU)? What factors should you consider when selecting the right processing device for your next design. 4. Available: http://www.atmel.com/Images/MCU_vs_MPU_Article.pdf

