MODIFYING THE THREE-PHASE SYNCHRONOUS REFERENCE FRAME PHASE-LOCKED LOOP TO REMOVE UNBALANCE AND HARMONIC ERRORS

by

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Abstract

As an increasing number of distributed power generation systems (DPGS) are being connected to the utility grid, there is a growing requirement for the DPGS to be able to ride through short grid disturbances. This requires improvements to be made to the grid-side control scheme of the DPGS. An important part of the grid-side control scheme is the grid synchronization method, which is responsible for tracking the phase angle of the grid voltage vector. The state-of-the-art grid synchronization methods being used today are phase-locked loops.

This thesis presents a modified phase-locked loop which is more robust towards grid disturbances. It consists of a multi-block adaptive notch filter (ANF) integrated into a conventional three-phase synchronous reference frame phase-locked loop (SRF-PLL). The addition of the multi-block ANF to the system allows it to become frequency adaptive. Also, since the multi-block ANF consists of multiple ANF blocks in parallel with one another, the system is able to remove multiple input signal distortions. Thus, the proposed system is able to eliminate the double frequency ripple that is caused in the conventional three-phase SRF-PLL by input unbalance, as well as harmonic errors, despite the presence of frequency variations in the input signal.

Simulation results found using Matlab/Simulink, and experimental results found using the dSPACE DS1103 DSP board, demonstrate the feasibility of the modified SRF-PLL. Also, the modified SRF-PLL is compared to a conventional three-phase SRF-PLL, as well as to a conventional three-phase SRF-PLL with a simple notch filter, and the advantages of the modified SRF-PLL are discussed.

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List of Abbreviations

AC	Alternating Current
ANF	Adaptive Notch Filter
DC	Direct Current
DPGS	Distributed Power Generation System
Hz	Hertz
LPF	Low Pass Filter
NF	Notch Filter
PI	Proportional Integrator
PLL	Phase-Locked Loop
PV	Photovoltaic
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
WT	Wind Turbine

Chapter 1

Introduction

1.1 Introduction

The demands made on traditional power systems are changing globally. These demands include a need for more sources of energy due to load growth, a need for renewable energies due to changing environmental policies, and a need for geographically distributed power sources due to dispersed populations. This has naturally brought about an increase in the development of alternative energies as a possible solution to these dilemmas. Wind turbines (WT) and photovoltaic (PV) power generation, for example, have both seen dynamic growth in the last decade [1, 2] (refer to Fig.1-1 and Fig. 1-2). The average annual growth rate of wind energy capacity in Canada during the years 2000 to 2006 was 51% [3]. This alternative energy growth trend is leading to a change in the setup of traditional power systems.

In traditional power systems power is generated at a relatively small number of large power generation plants which are located at a great distance to the consumers. The generators operate at a fixed speed and fixed grid frequency. At these large power generation plants the voltage is stepped up to high voltage, and the power is then transferred over high-voltage long distance transmission lines. The voltage is then stepped down to medium voltage or low voltage and distributed through the uni-directional (radial) distribution network until it reaches a user. Power system control centers monitor and control the quality of the power that is delivered.

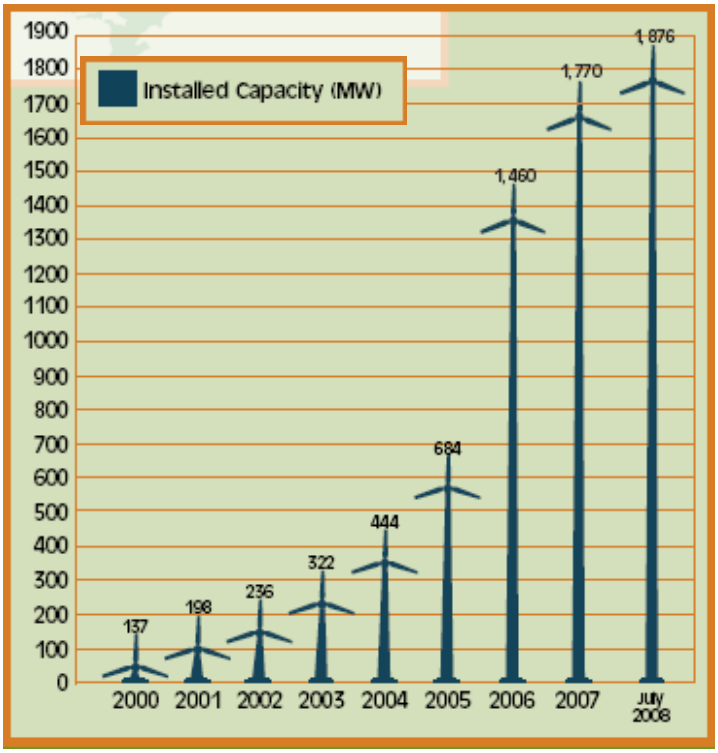

Figure 1–1: Canada's installed wind capacity to the end of July 2008 [3]

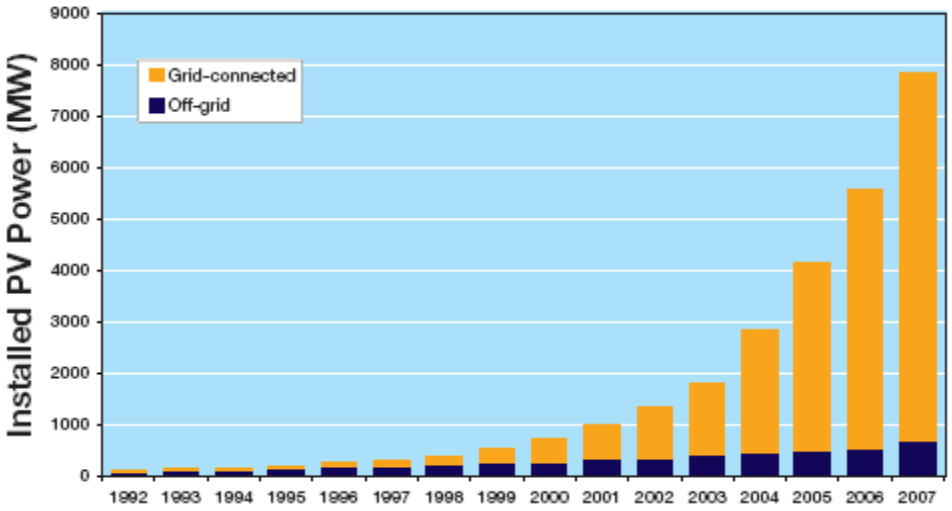

Figure 1–2: Cumulative installed grid-connected and off-grid PV power in the reporting countries [4][1]

[1] Australia, Austria, Canada, Switzerland, Denmark, Germany, Portugal, Spain, France, Great Britain, Israel, Italy, Japan, Korea, Mexico, Netherlands, Norway, Sweden, United States of America.

1.1.1 Distributed Power Generation Systems

Modern power systems do not have the same structure as traditional power systems, because distributed power generation systems (DPGS) are being integrated into the utility grid. A DPGS is a small scale power generation system that produces electrical energy at or near the load site and it is connected to either the medium or low voltage grid. It can range in size from several kW to hundreds of MW and can use both renewable and non-renewable energy sources (e.g., wind turbines, photovoltaic cells, fuel cells, small hydro, combined heat and power stations), but there is a definite inclination towards using renewable energies given the recent emphasis placed on developing environmentally friendly sources of energy. The distributed power generation system is not a new concept; a small number of consumers have been installing their own on-site generation for decades [5]. However, it is the recent technological advances in alternative energies which have enabled distributed power generation systems to be used on a larger scale. It is important that modern power systems have the same cost and reliability as traditional power systems in order for the grid integration of distributed power generation systems to be worthwhile.

In addition to the environmental benefits that arise from using renewable energy sources, a DPGS is also advantageous because it is located nearer to the customer, thus producing less transmission losses. They can be especially advantageous to customers who reside in rural areas, or in microgrids, with limited access to reliable and uninterruptible sources of energy. Finally, they can help support the traditional power system by providing power during periods of peak demand. However, renewable energy

sources can be problematic due to their high cost and their variable nature, which arises from their dependence on seasonal patterns of energy. These seasonal patterns of energy availability may not match the seasonal patterns of customer demand. Another concern is that the grid-connected DPGS can cause bi-directional power flows to occur in the utility grid. Bi-directional reactive power flows, for example, can cause voltage fluctuations, which threatens the stability of the utility grid. The distribution network is not designed to accommodate bi-directional power flows, and thus must be carefully managed by well-designed controllers.

1.1.2 Control Requirements of a Distributed Power Generation System

The increasing usage of DPGS units has caused the grid connection requirements to become more stringent, in order to prevent grid instability from occurring [6-9]. Grid connection requirements place an emphasis on power quality and robustness to grid disturbances. For example, if there are short grid disturbances, the DPGS should be able to continue operating without having to disconnect from the grid. Using power electronics to help interface the DPGS with the grid has been the means for allowing the grid connection requirements to be met [10, 11]. There are many different types of control methods implemented to achieve controllability of the power electronics interface [10]. Also, different types of control must be implemented for the different operation modes of the DPGS. Although there has been focus on connecting the DPGS to the utility grid as a supplemental source of power, it is also possible to have the DPGS run in stand-

alone mode in which case it supplies only private loads and is disconnected from the utility grid. Stand-alone systems are especially popular in rural areas in developing countries where low-cost access to the grid is impractical [12]. Another possibility, called islanding, is a case in which the DPGS becomes the only source of power for a local load (e.g., a city) in the case of grid failure. Finally, there are microgrids which are entities that coordinate DPGSs in a decentralized manner, thereby reducing the control burden on the grid and permitting the DPGS to yield its full benefits [13]. Microgrids are capable of operating safely and efficiently both within the local distribution network, as well as in islanding mode. Stand-alone operation, islanding, and microgrids may each require unique control schemes.

There are two main categories of control when it comes to the DPGS. Power electronics technology requires that the DPGS be connected to the grid through power converters [10]. There is an input-side converter (e.g, for wind turbines this is an AC-DC converter) and a grid-side converter (e.g., for wind turbines this is a DC-AC converter). Thus, the first control category is related to the input-side converter. The main job of the input-side controller is to ensure that the maximum power is extracted from the input source, generally achieved through the use of maximum power point tracking algorithms. Also, if grid failure occurs, the input-side controller should be able to protect the input source. The second control category is related to the grid-side converter. The grid-side controller has many jobs. It must ensure that the quality of the output power to the grid is maintained by controlling the output current. Some common power quality problems that must be mitigated are voltage dips/swells, flicker, voltage unbalance, harmonics, and

transients. The grid-side controller must also regulate the DC-link voltage (i.e., the DC-link that is between the two power converters) such that the power flow in the system is balanced. It must control the active power generated to the grid as well as the reactive power exchanged between the DPGS and the grid. Another task of the grid-side controller is that it is required to have a monitoring unit that is continuously measuring the grid voltage amplitude and frequency so that it can disconnect the DPGS in the requested amount of time in case of major grid disturbances. And finally it must ensure that the output current is synchronized with the grid voltage. Please refer to Figure 1-3 to see the structure of a DPGS. The grid-side controller may also be required to perform some extra tasks, depending on the requirements of the grid operator. These include providing ancillary services such as local voltage and frequency regulation, voltage harmonic compensation, and active filtering [10].

1.1.3 Grid Synchronization

An important part of the controllability required in order to fulfill these grid connection requirements is achieved by having a robust grid synchronization technique. The grid synchronization algorithm is mainly responsible for detecting the phase angle of the grid voltage vector, which can then be used to synchronize the control variables of the system. The grid synchronization technique should ideally be able to output a clean synchronization signal despite the presence of noise, harmonic distortions, voltage unbalance, and frequency variations in the input signal [14]. Harmonic distortions are

periodic sinusoidal distortions of the supply voltage. Voltage unbalance commonly results during grid faults and occurs if the input signals have unequal magnitudes or phase-displacements that are unequal to 120 degrees. The grid frequency can have considerable fluctuations in power systems containing a large amount of DPGS during transient grid faults. The grid frequency can also display significant fluctuation if the DPGS is operating in stand-alone or islanding mode. All of these drawbacks need to be considered when designing the grid synchronization technique.

To achieve grid synchronization, there are many different techniques that can be employed. The most primitive technique is the zero-crossing detection method [15]. This method finds the zero-crossing points of the grid voltage in order to determine the phase information. However, this technique is not satisfactory because the phase information can only be detected at each half cycle, which considerably slows its performance. Also, harmonics and notches can affect the quality of the synchronization. Another technique is the filtering method, where the phase angle of the grid voltage is obtained by filtering the grid voltages in the dq or αβ reference frames. As with all methods which use filters, a certain amount of delay is introduced when using this method. Thus, the filter must be properly designed in order to mitigate the filter delay. Nevertheless, depending on the type of filter in question, filtering can be a viable grid synchronization method.

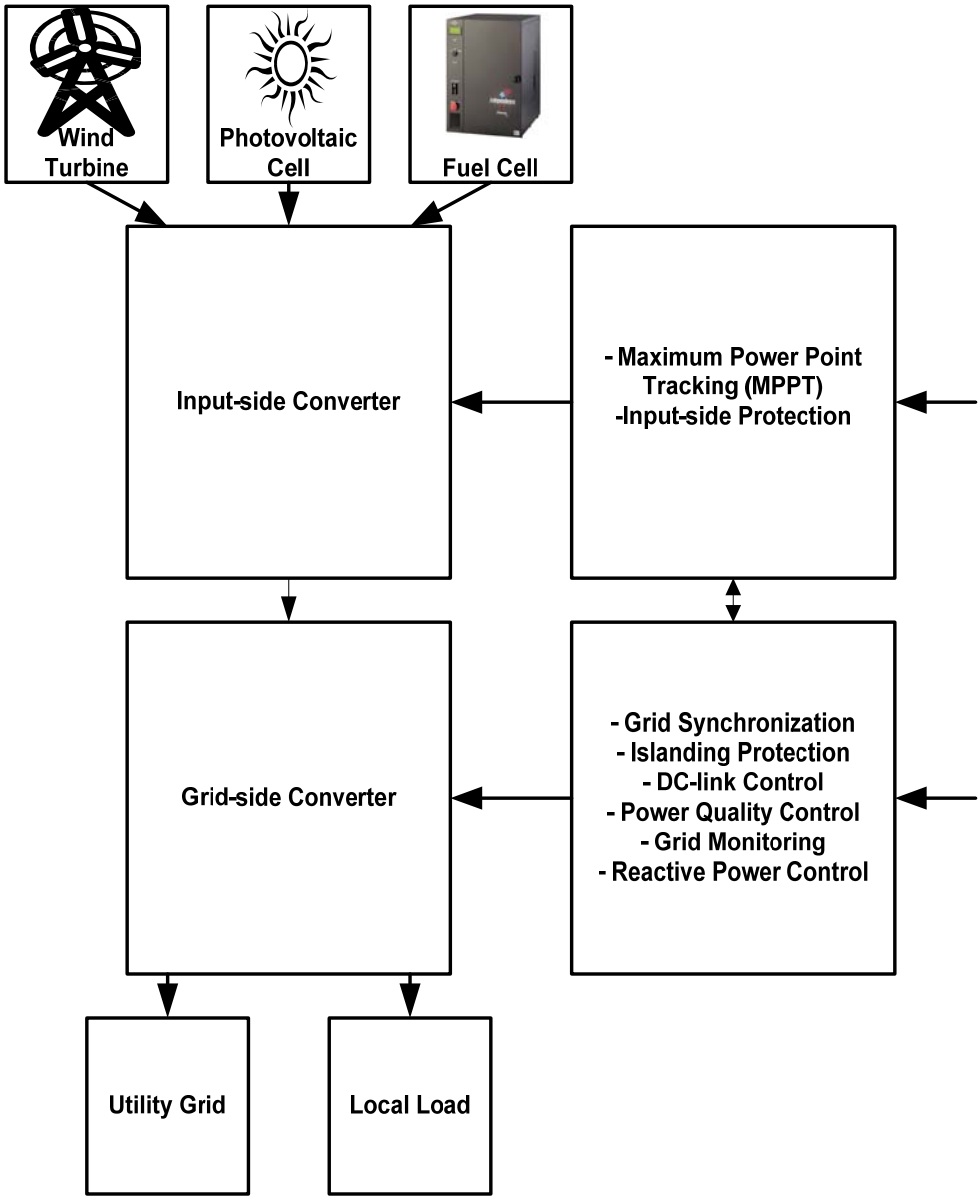

Figure 1–3: Structure of a DPGS

The most state-of-the-art technique that can be used for grid synchronization is the phase-locked loop (PLL). The single-phase PLL operates by generating an output signal whose phase angle tracks the phase angle of the input signal. It is used for single-

phase systems, but it has two main drawbacks: (1) three-phase power systems are more common, (2) it produces a double frequency ripple in its output. For three-phase systems in particular, the synchronous reference frame phase-locked loop (SRF-PLL) is used [16]. However, when the grid is not operating under ideal conditions, the SRF-PLL technique becomes inadequate. For example, the input voltage unbalances resulting from grid faults cause a double frequency ripple to be generated by the SRF-PLL. Previous papers have focused on modifying the PLL or control techniques of grid-connected power converters such that they could remove this inadequacy to some degree of success. In [17], notch filters are added to the control system of a grid-connected voltage source converter to remove the double frequency ripple caused by input unbalance. Although this system gives good results, since the notch filters are not frequency adaptive, the proposed system would be unable to handle frequency variations in the input signal. A decoupled double synchronous reference frame phase-locked loop is proposed in [18], which is used to detect the positive-sequence component of an unbalanced voltage vector. The results given by this modified PLL are very good, but there is some room for improvement when the input signal is distorted with harmonics.

The main contribution of this thesis is to modify the SRF-PLL such that it can work ideally even when voltage unbalance, frequency variations, and harmonic distortions are present in the input signal. This is achieved by placing an adaptive notch filter (ANF), proposed in [19, 20], in the control loop of the three-phase SRF-PLL such that it filters out the distortions. The ANF is frequency-adaptive, and thereby is able to continue filtering distortions even when there are frequency variations in the input signal.

Another advantage of the ANF is that many ANF blocks can be placed in parallel such that it can remove many distortions simultaneously without affecting the time response of the system. This is especially useful for removing harmonic distortions in the signal, which can be introduced into the system through grid-connected power electronics devices. The multi-block ANF configuration can frequency-adaptively remove multiple harmonics in addition to removing the double frequency ripple caused by unbalance.

1.2 Thesis Outline

Chapter 1 provides a brief background on the challenges faced by modern power systems due to the integration of distributed power generation systems into the grid. It reviews the basic control requirements of a grid-connected DPGS. Finally, it provides a brief description of how grid synchronization is important for the control of a grid-connected DPGS, and it provides a brief review of the available grid synchronization techniques. This chapter establishes the motivation behind the research presented in this thesis.

Chapter 2 presents a review of existing grid synchronization techniques. A general overview of the zero-crossing method, filtering method, and both the single-phase and three-phase phase-locked loop method is covered in the review. Advantages and disadvantages of each of these methods are also covered. Finally, a review of current improvements made to the conventional three-phase phase-locked loop is presented.

Chapter 3 proposes a modified phase-locked loop method, which is an improvement on the conventional three-phase phase-locked loop method. The modified PLL is equipped with an adaptive notch filter (ANF), and thus characteristics of the ANF are also covered in this chapter. Next, simulation and experimental results are provided which verify the effectiveness of the modified PLL method. The provided simulation and experimental results examine the performance of the modified PLL method when the input signal contains voltage unbalance, frequency variations, and harmonic distortions. There are also simulations results provided which verify its frequency tracking capabilities and which compare its performance with the conventional synchronous reference frame phase-locked loop (SRF-PLL), as well as with a SRF-PLL equipped with a notch filter.

Chapter 4 concludes the thesis. A summary of the results and contributions of the modified SRF-PLL is included as well as possible suggestions for future work.

Chapter 2
Review of Grid Synchronization Techniques

2.1 Background

Most grid-connected static converter applications require that there is synchronization between the grid voltage and the voltage or current synthesized by the converter. Such applications include the grid-connected DPGS, active power line conditioners, and FACTS and Custom Power devices (e.g., DVR, STATCOM, and active filters). The grid synchronization algorithm is chiefly responsible for detecting the phase angle of the grid voltage vector. The phase angle of the grid voltage vector can then be used to synchronize the control variables of a grid-connected converter. For grid-connected DPGS applications, one of the most important uses of the phase angle is to control the power flow. The power flow is controlled by adjusting the phase of the output current relative to the grid voltage. Generally, the grid-connected DPGS is required to deliver active power to the grid, which means that it operates at unity power factor. However, it must also be able to inject or absorb reactive power from the grid as well.

Accurate phase angle information is essential in order for the grid-connected converter to provide power factor correction, reactive power compensation, harmonic current cancellation, etc. Without grid synchronization, the grid-connected converter can suffer from poor performance or even instability. Preferably, the grid synchronization technique should be able to provide a clean synchronization signal despite the presence of

noise, harmonic distortions, voltage unbalance, and frequency variations in the input signal.

There are many different techniques that can be used to achieve grid synchronization. The most elemental technique available is the zero-crossing detection method [15]. Mathematically, zero-crossing occurs when the sign of any given function switches from positive to negative, or vice versa. On a plot of any particular function, this can be seen as the point where the function crosses the axis, or in other words is at a zero value. When using this method for grid synchronization, the zero-crossing points for the grid voltage must be found. Since the grid voltage is an AC voltage, this is the instantaneous point at which the grid voltage is zero. For an AC voltage, which is sinusoidal by nature, zero-crossing occurs twice during each cycle. By finding the zero-crossing points of the grid voltage, the phase angle information can also be determined.

However, this technique is not satisfactory because the phase angle information can only be detected at each half cycle, which considerably slows its performance. The synchronization technique should be able to gather the phase angle information continuously over the entire signal cycle in order to have fast performance. Also, if there are harmonics or notches present in the grid voltage, these will affect the performance of the system. For example, a notch present in the grid voltage could possibly cause the grid voltage to cross the zero value momentarily when it is not supposed to, thus distorting the quality of the information being gathered. This disadvantage of the zero-crossing technique is demonstrated in Figure 2-1, where notches in the input signal cause spikes in the output signal.

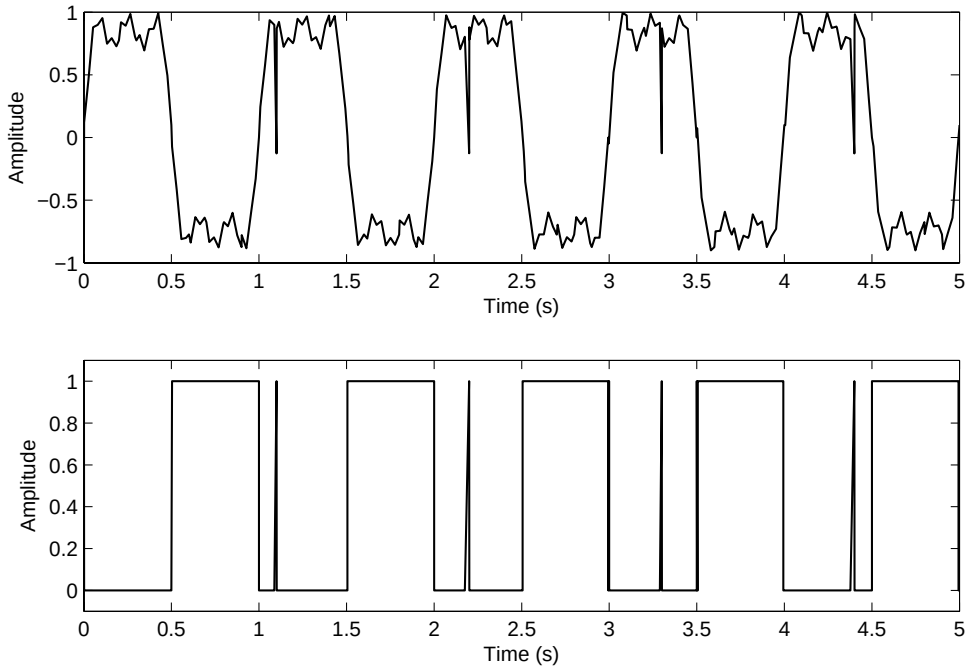

Figure 2–1: Zero-crossing technique, (a) Input signal contains third harmonics, fifth harmonics, noise, and notches, (b) Zero-crossing technique operation is faulty because the notches cause spikes in the output signal

Filtering can be used to remove these notches and harmonics from the input signal so that a reliable zero-crossing detection signal can be obtained. Nevertheless, it has been shown that analog solutions to this problem are insufficient. The reason for this is that if the input signal is filtered before reaching the zero-crossing detector, it is challenging to avoid introducing a phase lead or lag into the filtered waveform, which degrades the accuracy of the zero-crossing detection signal [21]. However, solutions to this dilemma have been proposed, such as the use of the discrete Fourier transform and various other

digital techniques, which have been successful at improving the zero-crossing detection method [22].

Another open-loop technique used to achieve synchronization is the filtering method, where the phase angle of the grid voltage is obtained by filtering the grid voltages in the dq or $\alpha\beta$ reference frames [10, 23]. Refer to Figure 2-2 to see an example of one possible filtering method that can be used to achieve synchronization, the low-pass filtering method [23]. In this method, the utility voltages are transformed from the natural abc frame to the $\alpha\beta$ reference frame, and then low-pass filters are used to remove distortion. Finally the filtered signals are normalized and pass through a rotation matrix R in order to compensate for the phase lag caused by the low-pass filters. The low-pass filtering method is an improvement on the zero-crossing method, but as with all methods which use filters, a certain amount of delay is introduced when using this method. If the filter is sharp, less distortion is permitted to pass through. However, in such a case the rate of transient convergence is very slow and this causes a delay. Conversely, if the filter is not sharp, the rate of convergence is quick, but more distortion is present in the output. Thus, the filter must be properly designed in order to mitigate the filter delay; filter delay may be compensated to a degree. Another shortcoming of the filtering method is that if the filters being used are not frequency-adaptive, they are sensitive to variations in the center frequency. Although many different types of filters have been proposed to be used for the filtering method, some of the most common are the low-pass filter, the space-vector filter, and the extended Kalman filter [23, 24].

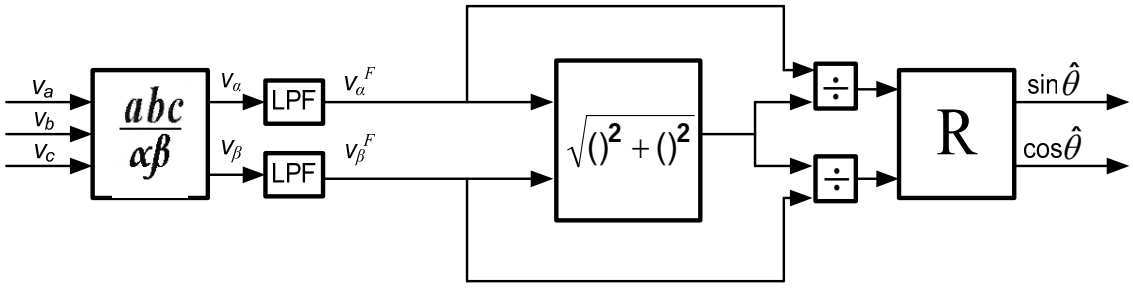

Figure 2–2: Low-Pass Filtering Method for Grid Synchronization

The best and most commonly used grid synchronization technique available at present is the phase-locked loop (PLL). The conventional three-phase synchronous reference frame phase-locked loop (SRF-PLL), for example that seen in [16], is generally sufficient for removing distortion during balanced operating conditions. However, it becomes inadequate when unbalance, harmonic errors, and frequency variations exist in the input signal, which are to be expected during grid operation.

2.2 Phase-Locked Loop

2.2.1 Single-Phase PLL Techniques

The single-phase phase-locked loop consists of three main components (Fig. 2-3): a phase detection scheme, loop filter (LF), and voltage controlled oscillator (VCO). The phase detection scheme, generally implemented using a multiplier, is responsible for finding the difference between the phase angle of the input signal and the output signal.

The output of the phase detection scheme consists of two components. The first component is a function of the phase difference between the input signal and output signal and the second component is at a frequency of twice the signal frequency (this is called the double frequency ripple). Since the second component of the phase detection scheme output is not useful, it can be partially removed using the loop filter. The bandwidth of the loop filter should be small so that it can remove both the double frequency ripple as well as any unwanted noise. However, if the bandwidth is too small, then this will affect the dynamics of the system. Thus, choosing a proper filter bandwidth is an important PLL design consideration.

The output of the loop filter then contains only the first component which is a function of the phase difference between the input and the output signals, otherwise called the phase error. This error signal is then used to drive the voltage-controlled oscillator to generate an output signal. Ideally, the phase error should be zero, so that the phase angle of the output signal is identical to the phase angle of the input signal. The VCO produces a periodic output signal, the frequency of which changes depending on the applied control signal. When the phase error signal is zero the VCO generates an output signal at the center frequency. However, when the phase error is not equal to zero, the VCO responds by changing its operating frequency. Since the phase angle of the output signal is a function of its frequency (the phase angle is equivalent to the integral of the frequency over a certain period of time), and vice versa, the phase angle of the output signal can be modified to become equal to the phase angle of the input signal by changing the operating frequency of the output signal. Essentially, the VCO is able to drive the

phase error to zero by modifying its operating frequency. It generates an output signal with a phase angle equivalent to the phase angle of the input signal.

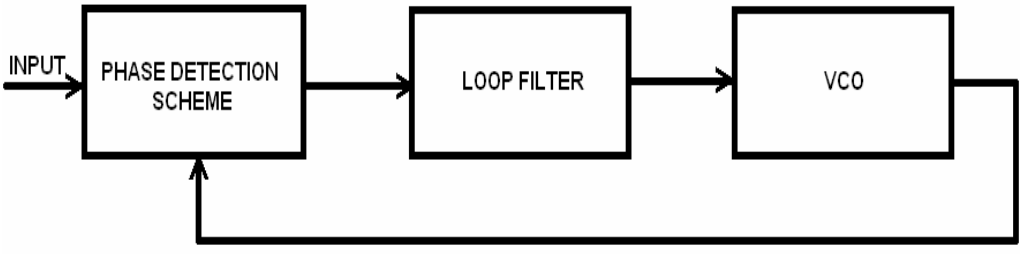

Figure 2–3: General Structure of the Single-Phase Phase-Locked Loop

The main drawback of the single-phase PLL is that the loop filter is not able to completely eliminate the double frequency ripple without noticeably slowing its performance. Another important drawback of the single-phase PLL is that three-phase power systems are more common than single-phase power systems, so it may not be as relevant a technique as those grid synchronization techniques which are designed for three-phase power systems.

There have been various works proposed to improve the performance of the single-phase PLL [25-28]. Since the single-phase PLL has no internal harmonic cancellation and generates a double frequency ripple, these works have focused on rectifying this problem. In [25], an enhanced single-phase PLL (EPLL) is introduced, and its applications are further discussed in [26]. The EPLL furnishes the conventional single-phase PLL with a magnitude estimation strategy (Fig. 2-4). This modification enables it to cease producing a double frequency ripple. In addition to eliminating the double

frequency ripple, the EPLL is also able to directly estimate the magnitude, phase-angle, and frequency. In [26], a multi-unit EPLL structure is proposed which has not only the advantageous features of the single-unit EPLL, but which is also able to remove harmonic components from the output (Fig. 2-5).

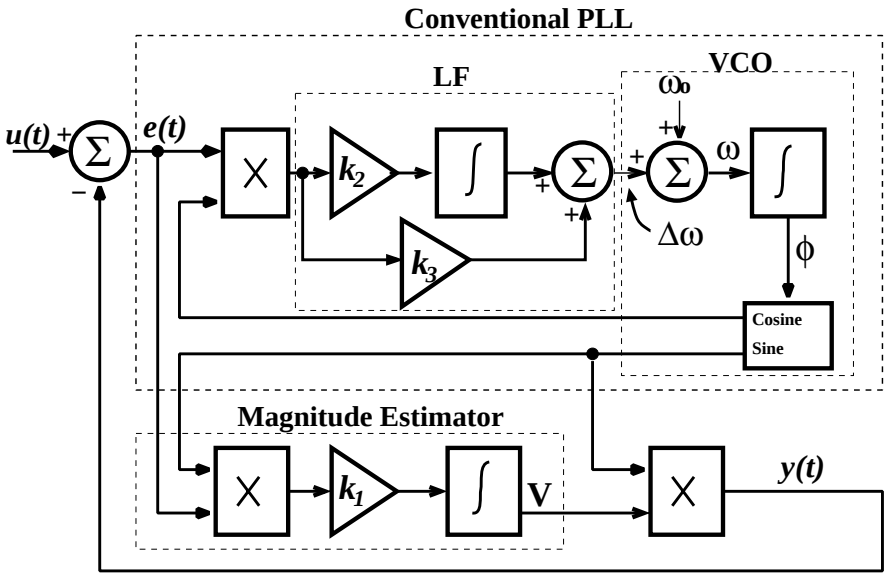

Figure 2–4: Structure of Enhanced Phase-Locked Loop (EPLL) [25]

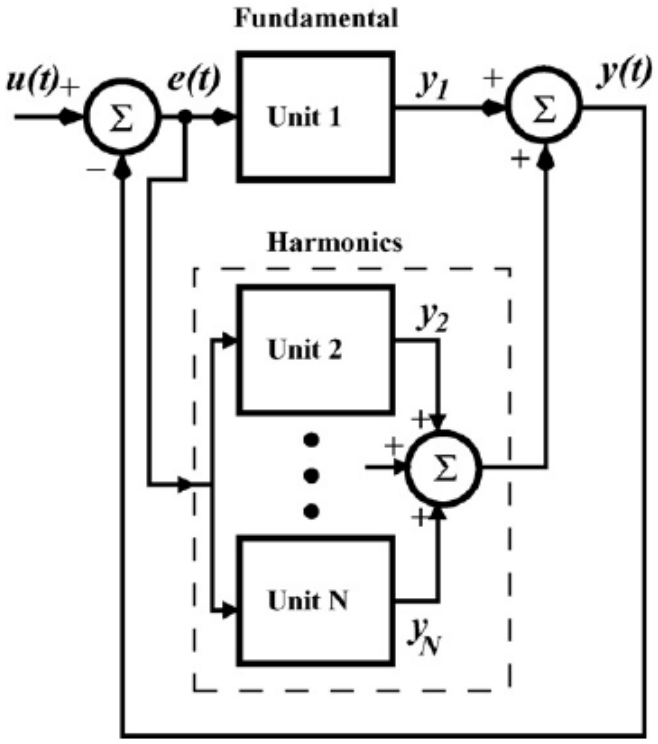

Figure 2–5: Structure of multi-unit single-phase PLL [26]

2.2.2 Three-Phase PLL Techniques

Three-phase PLL techniques are used more often for grid synchronization than single-phase PLL techniques since three-phase power systems are more common than single-phase power systems. The most commonly used three-phase PLL technique is the synchronous reference-frame PLL [16, 29]. The SRF-PLL, seen in Fig. 2-6, converts the input signal from the natural abc frame to the stationary $\alpha\beta$ frame and then to the synchronous dq frame. This is achieved using the linear transformations seen in equation set (1), where T_{dq} represents the Park transformation and $T_{\alpha\beta}$ represents the Clarke

transformation. By converting from the abc frame to the dq frame, the input signal variables become dc values, making them easier to filter and control [30].

$$\left[T_{dq}\right]=\begin{bmatrix}\cos\theta & \sin\theta\\ -\sin\theta & \cos\theta\end{bmatrix}, \text{ where } \theta = \omega t+\delta,$$

$$\left[T_{\alpha\beta}\right]=\begin{bmatrix}\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3}\\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}}\end{bmatrix} \quad (1)$$

Then through the use of a closed-loop control system it regulates the q component, representative of the error signal, to zero by generating a phase angle that is equal to the phase angle of the input signal. In the closed-loop control system there is a PI controller (loop filter) which is responsible for providing a filtered output. When adjusting the control parameters of the loop filter it is important to consider that there is a tradeoff between the speed of the response and the accuracy of the filtering. Thus, if the control parameters of the loop filter are set such that it is designed to perform as a very sharp filter, then the speed of the system response will suffer. Conversely, an increase in the speed of the system response requires a sacrifice in the quality of the filtering. In practice, the filtering is sharp enough such that it is able to eliminate high order harmonics, but not sharp enough to eliminate the low-order harmonics (i.e., 3^{rd}, 5^{th}, 7^{th}, etc.) because this would cause the system to become too sluggish [31]. Finally, after the

signal passes through the loop filter, it is converted from a frequency value to a phase angle value through integration. This integration can be implemented through the use of a voltage-controlled oscillator (VCO). The approximated transfer function of the closed-loop system is given in equation (2).

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{2}$$

where,

$$\omega_n = \sqrt{\frac{K_p V}{\tau}}, \varsigma = \frac{K_p V}{2\omega_n} \tag{3}$$

If the grid is operating at an ideal utility voltage (e.g., balanced, constant frequency, no harmonics) then the phase-locked loop provides a highly fast and accurate synchronizing signal. However, when the input signal to the SRF-PLL becomes unbalanced, double frequency ripples are generated [31]. Unbalance occurs if the input signals have unequal magnitudes or phase-displacements that are unequal to 120 degrees. When unbalance is present in the input signal, the input signal can be decomposed into three components; the positive-sequence, negative-sequence (see equation set (4)), and the zero-sequence. The zero-sequence term which is present in the input signal is not considered in equation set (4).

$$v = \begin{bmatrix} v^+ \cos(\omega t) \\ v^+ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v^+ \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} + \begin{bmatrix} v^- \cos(\omega t) \\ v^- \cos\left(\omega t + \alpha + \frac{2\pi}{3}\right) \\ v^- \cos\left(\omega t + \alpha - \frac{2\pi}{3}\right) \end{bmatrix} \quad (4)$$

Since the SRF-PLL first transforms the input signal into the $\alpha\beta$ frame, the input signal becomes separated into the following two components,

$$v_\alpha = v^+ \cos(\omega t) + v^- \cos(\omega t + \alpha)$$

$$v_\beta = v^+ \sin(\omega t) - v^- \sin(\omega t + \alpha) \quad (5)$$

Finally, the signal is transformed from the $\alpha\beta$ into the dq frame, and the q component becomes the error signal. Since the input signal had a negative-sequence component, there is double frequency ripple present in the q component, which can be seen in the following equation,

$$v_q = v^+ \sin(\delta) - v^- \sin(2\omega t + \alpha + \delta) \quad (6)$$

Simulations in Matlab/Simulink demonstrate that when there is input voltage unbalance (i.e., when there is a negative-sequence component in the input signal), a significant double frequency ripple is present (Figure 2-7) in the error signal of the SRF-PLL. Harmonic distortions in the input signal also lead to distortions in the phase and

frequency output. For example, an nth harmonic leads to harmonics of the degree (n-1) and (n+1) in the error signal (v_q) (refer to Equation set 7).

Because if,

$$v = \begin{bmatrix} v_n \cos(n\omega t + \beta_1) \\ v_n \cos(n\omega t + \beta_2) \\ v_n \cos(n\omega t + \beta_3) \end{bmatrix}$$

Then given that,

$$[T_{\alpha\beta}] = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix}$$

And,

$$[T_{dq}] = \begin{bmatrix} \cos(\omega t + \delta) & \sin(\omega t + \delta) \\ -\sin(\omega t + \delta) & \cos(\omega t + \delta) \end{bmatrix}$$

We find that,

$$\begin{aligned} v_q &= -\frac{1}{3} v_n \left[\sin((n+1)\omega t + \beta_1 + \delta) - \sin((n-1)\omega t + \beta_1 - \delta)\right] \\ &+ \frac{1}{6} v_n \left[\sin((n+1)\omega t + \beta_2 + \delta) - \sin((n-1)\omega t + \beta_2 - \delta)\right] \\ &+ \frac{1}{6} v_n \left[\sin((n+1)\omega t + \beta_3 + \delta) - \sin((n-1)\omega t + \beta_3 - \delta)\right] \\ &+ \frac{1}{2\sqrt{3}} v_n \left[\cos((n-1)\omega t + \beta_2 - \delta) + \cos((n+1)\omega t + \beta_2 + \delta)\right] \\ &- \frac{1}{2\sqrt{3}} v_n \left[\cos((n-1)\omega t + \beta_3 - \delta) + \cos((n+1)\omega t + \beta_3 + \delta)\right] \end{aligned} \tag{7}$$

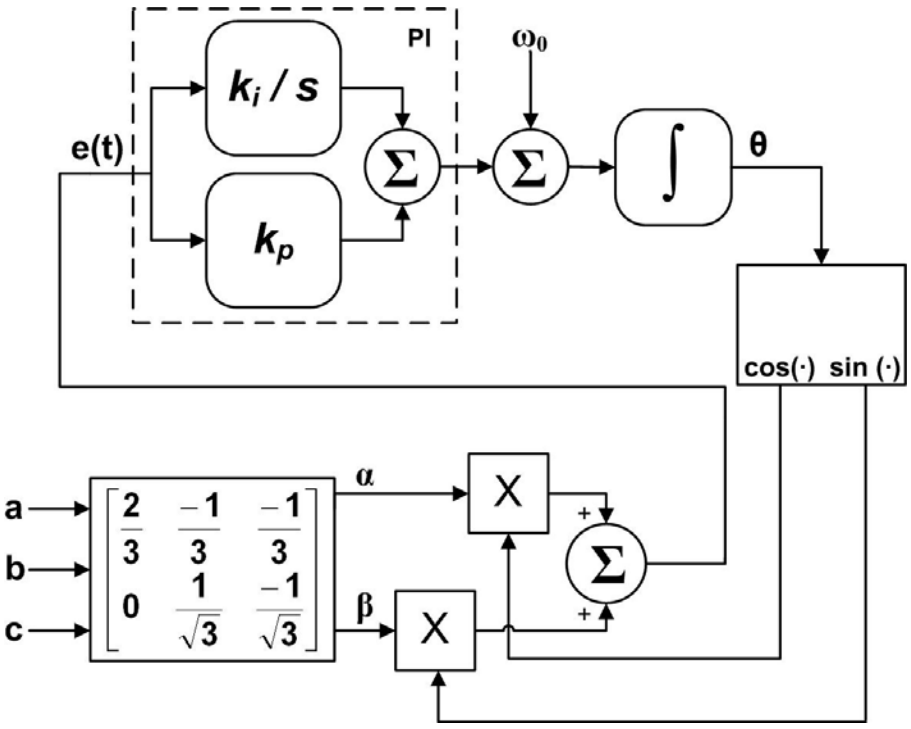

Figure 2–6: Three-phase synchronous reference frame phase-locked loop

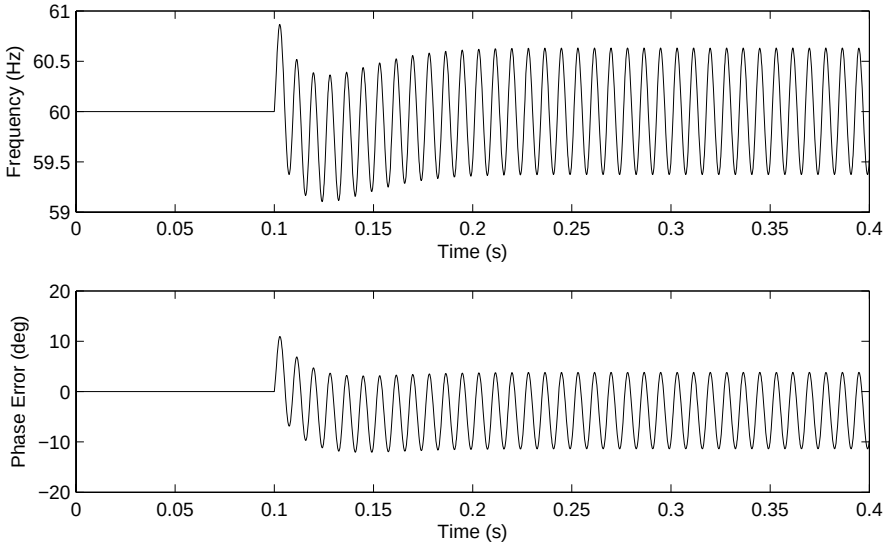

Figure 2–7: Frequency (Hz) and phase error (°) output of conventional three-phase SRF-PLL. At t = 0.1s the input voltage becomes unbalanced.

Previous papers have focused on modifying the phase-locked loop or control techniques of grid-connected power converters to remove its inadequacies, and they have reached some degree of success. In [17], notch filters are added to the control system of a grid-connected voltage source converter to remove the double frequency ripple caused by input unbalance. Although this system gives good results, since these notch filters are not frequency adaptive, the proposed system would be unable to handle frequency variations in the input signal. Matlab simulations demonstrate that an SRF-PLL equipped with a notch filter (Figure 2-8) is able to remove the double frequency ripple caused by input voltage unbalance (Figure 2-9). Matlab simulations also demonstrate that when a frequency variation occurs, the notch filter is no longer able to remove the double frequency ripple adequately (Figure 2-10).

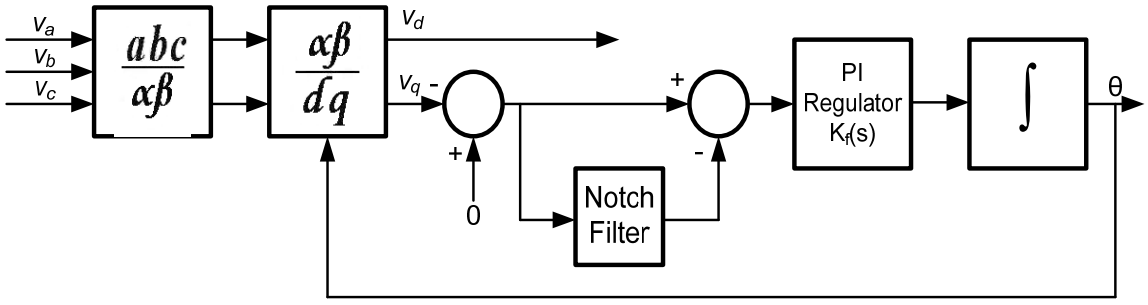

Figure 2–8: Conventional three-phase SRF-PLL with a notch filter.

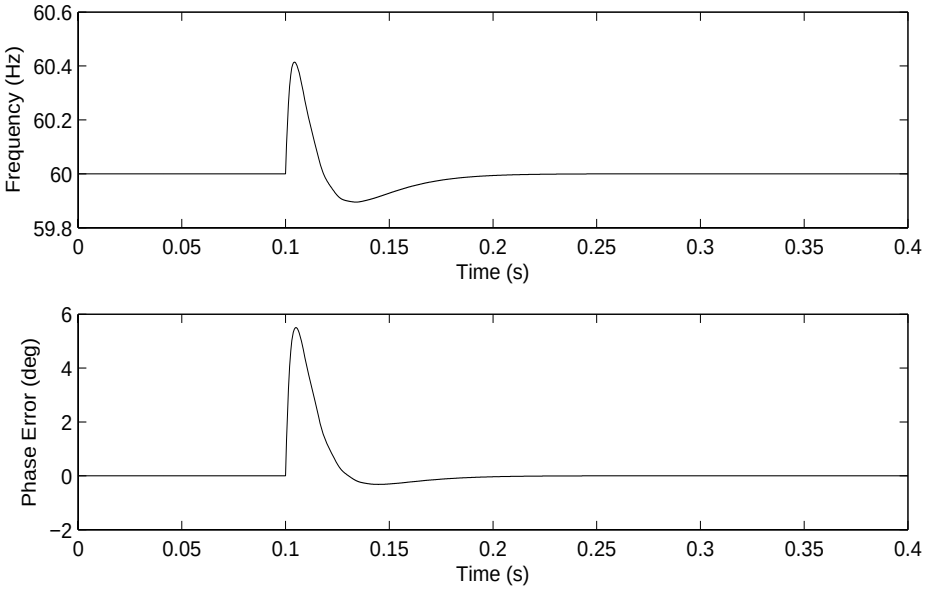

Figure 2–9: Conventional three-phase SRF-PLL with a notch filter. At t=0.1s the input voltage becomes unbalanced.

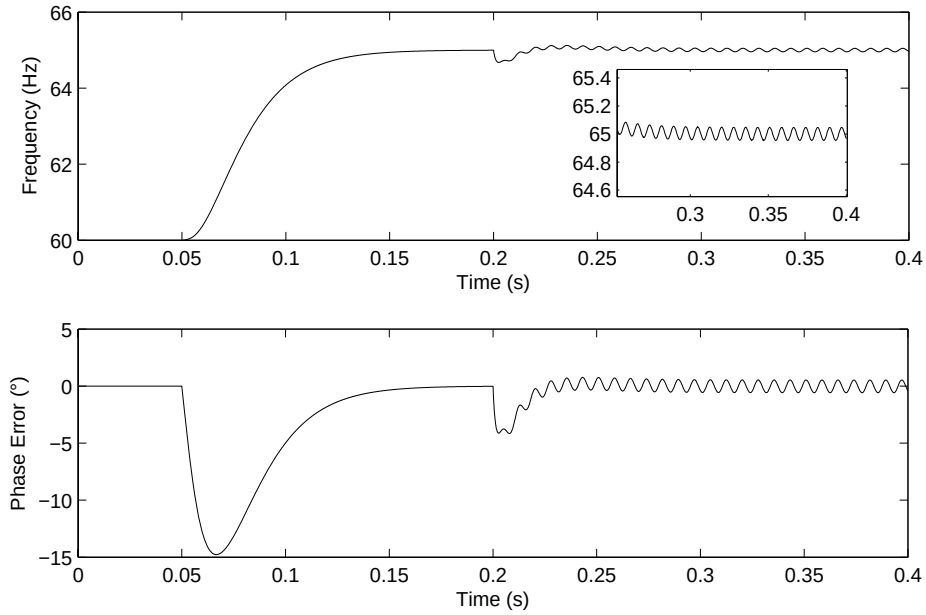

Figure 2–10: Conventional three-phase SRF-PLL with a notch filter. There is a frequency jump (from 60Hz to 65Hz) at t=0.05s and the input voltage becomes unbalanced at t=0.2s.

Most of the proposed PLL methods in the literature focus on removing the negative-sequence from the three-phase input signal. One of the most recognized PLL methods of this kind is the decoupled double synchronous reference frame phase-locked loop proposed in [18], which is used to detect and extract the positive-sequence component of an unbalanced voltage vector thereby eliminating the negative-sequence component causing the voltage unbalance. It does this by expressing both the positive- and negative-sequence components on the double synchronous reference frame (Fig. 2-11). The results given by this modified PLL are very good, but there is some room for improvement when the input signal is distorted with harmonics.

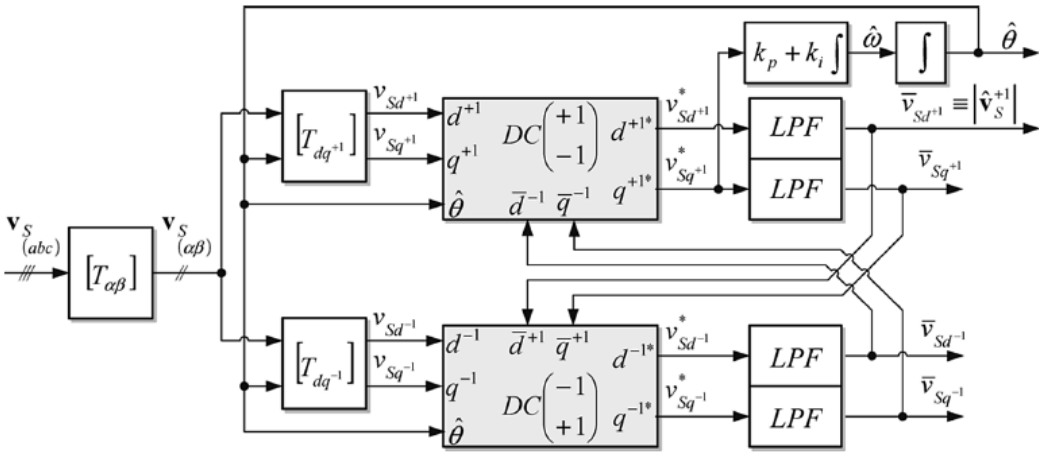

Figure 2–11: Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) [18]

In [14] a three-phase PLL is proposed which is able to operate under unbalanced conditions, with very good results. This work is an extension of a previous work proposed in [32], where an enhanced three-phase PLL (EPLL) is introduced. An

advantage of the EPLL over the conventional three-phase PLL is its ability to estimate the magnitude of the fundamental component, in addition to the frequency and phase angle. The work in done in [14], however, places three of these EPLL in parallel with each other. Each EPLL is responsible for processing one of the sequence components of a three-phase set of input signals. Thus, the system decomposes the input signal into its positive-sequence, negative-sequence, and zero-sequence components. Simulation results show that it is able to perform well under conditions of unbalance and it removes the double frequency ripple completely. Simulation results also show that it is able to do so in the presence of frequency variations in the input signal. Finally, simulation results show that it is able to perform well within the presence of a 5^{th} harmonic, and it is able to remove the effects of this harmonic. However, so far no simulations have been presented which show its performance in the presence of multiple harmonics.

Another method proposes placing a repetitive controller into the conventional SRF-PLL in order to cope with the double frequency ripple caused by unbalance [33]. The repetitive controller is cascaded with the PI controller, and it acts as a bandpass filter such that the even harmonics have no attenuation and the odd harmonics are filtered out. When even harmonics appear due to unbalance, they pass through the filter and are added to the d-axis voltage reference. Thus, the proportional gain of the PI controller is artificially increased at that particular frequency, which allows better rejection of these harmonics to be achieved. Simulation and experimental results show good performance when there are frequency jumps, unbalance, and input harmonic distortion individually occurring. However, there are no results which show how the system rejects unbalance

and input harmonics once there has already been a frequency jump. In conclusion, there is a need for an improved PLL which is able to produce an undistorted synchronization signal despite the presence of noise, multiple harmonic distortions, voltage unbalance, and frequency variations in the input signal.

2.3 Chapter Summary

In summary, a grid synchronization technique is responsible for tracking the phase-angle of the input signal. There are several grid synchronization techniques available for usage but many of these still have noticeable limitations. The most elemental technique is the zero-crossing detection technique, which detects the zero-crossing points of a signal in order to determine its phase angle. There are speed limitations of the zero-crossing technique since it can only detect the phase angle at every half cycle of the signal. Another limitation is that distortions and notches in the signal can cause the signal to display a momentary zero-crossing. Since this technique is unable to distinguish the zero-crossings caused by the sinusoidal nature of the signal and those caused by distortions and notches, it can cause faulty operation.

Another common grid synchronization technique is the filtering technique, where the phase angle is obtained by filtering the grid voltage in either the dq or αβ frames. A wide variety of filters have been proposed for this method (e.g., low-pass filter, space vector filter, Kalman filter), some more successful than others. The filtering technique is an improvement upon the zero-crossing technique.

The most state-of-the-art grid synchronization technique, however, is the phase-locked loop. The conventional single-phase PLL is able to swiftly generate an output signal with a phase angle equivalent to the phase angle of the input signal. However, it also generates a double frequency ripple which can not be removed without the single-phase PLL losing a significant amount of speed. The conventional three-phase PLL tracks the phase angle of the input signal quickly and accurately. Its limitations are that it can not remove harmonic distortions, nor can it remove the double frequency ripple which it generates when the input signal is unbalanced. Finally, it is unable to operate satisfactorily when there are changes in the input frequency. Various modifications have been proposed in the literature to the PLL to deal with these limitations, and they have had varying degrees of success.

Chapter 3

Modified Synchronous Reference Frame Phase-Locked Loop

3.1 Modeling and Analysis

The proposed system is a modification of the SRF-PLL such that it is able to remove double frequency ripple caused by input voltage unbalance, as well as multiple harmonics, in spite of the presence of possible frequency variations in the input signal. This modification consists of placing an ANF before the PI controller in the SRF-PLL control loop.

3.1.1 Review of ANF Structure

Before reviewing the structure of the ANF, a basic understanding of the notch filter (NF) is required. The ideal notch filter has a frequency response with unity gain for all frequencies except a specific frequency called the notch frequency; the notch frequency has a gain of zero. Practically speaking, building an ideal notch filter is not feasible. However, the notch filter can be made to resemble an ideal notch filter by having a sharp bandwidth. The notch filter is defined by the transfer function given in equation (8).

$$H(s) = K\frac{s^2 + (2\pi f)^2}{s^2 + 2\pi f\frac{s}{Q} + (2\pi f)^2} \tag{8}$$

The notch filter is able to filter out or extract a chosen sinusoidal component of a given signal, provided that this component has a constant frequency. If the sinusoidal component that is to be filtered out does not have a constant frequency, the notch filter can become less efficient or even inoperative if it has a very sharp bandwidth. In such a case the adaptive notch filter (ANF) is more suitable since it is able to track the frequency variations of the input signal, and accordingly modify the notch frequency. The ANF model that is of interest for this thesis was proposed in [19]. Structurally, this ANF is composed of a conventional NF with an added frequency estimation loop. While a conventional NF is linear, the ANF is a nonlinear filter because of the frequency estimation loop present in the structure.

The structure of the ANF can be seen in Fig. 3-1, where *y(t)* represents the input signal, $\dot{x}$ represents the output signal, and θ represents the estimated frequency. ζ_i and γ are positive and real parameters that effect the accuracy and convergence speed of the ANF. An improved ANF structure can be seen in Fig. 3-2(a) with multiple ANF units, each built like the one seen in Fig. 3-2(b), connected in parallel, which allows the ANF to decompose a signal into its harmonics [20]. This parallel structure is also advantageous in terms of the filtering delay. Since the ANF units in a multi-block ANF operate simultaneously because they are in parallel, a multi-block ANF and a single-block ANF have the same filtering delay. The dynamic behavior of the multi-block ANF can be characterized by the differential equations given in equation set (9).

$$\ddot{x}_i + i^2\theta^2 x_i = 2\zeta_i\theta(y(t) - \dot{x})$$

$$\dot{\theta} = -\gamma x_1\theta(y(t) - \dot{x}) \quad (9)$$

Where the value of *i* corresponds to the number of units, and where $\dot{x}$ is defined as the following,

$$\dot{x} = \dot{x}_1 + \dot{x}_2 + \ldots + \dot{x}_N \quad (10)$$

When the ith filter of Fig. 3-2(b) is in steady state, the output is given by,

$$\dot{x}_i = A_i \sin(i\omega_0 t + \phi_i) \quad (11)$$

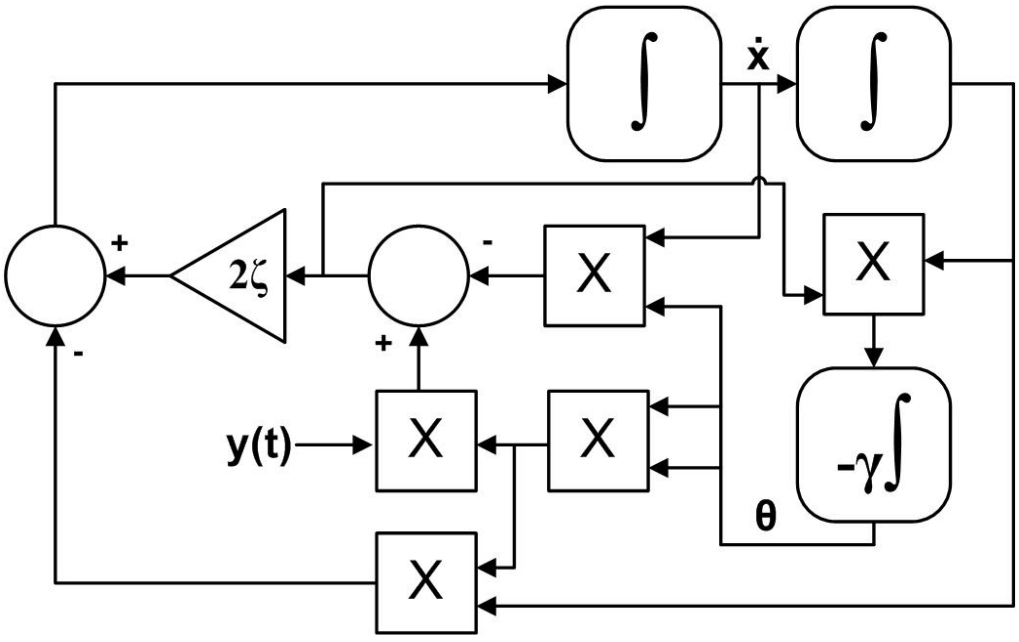

Figure 3–1: Adaptive Notch Filter [19]

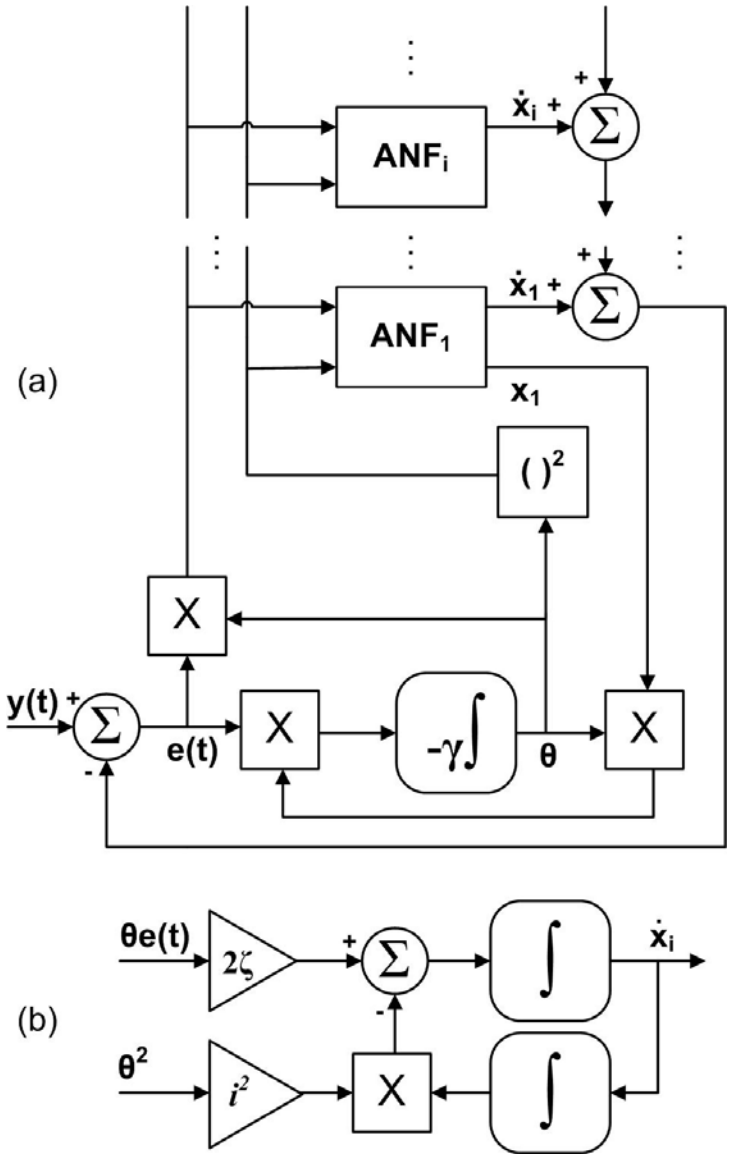

Figure 3–2: (a) Multiple-unit ANF structure, (b) Structure of the ANF building block [20]

3.1.2 Proposed Structure

The proposed PLL, seen in Fig. 3-3, has an ANF structure in its control loop, which allows it to remove double frequency ripple as well as harmonics. It filters out

input signal distortions and removes them from the input signal going into the PI controller. If the PLL input contains only a double frequency ripple, then a one-block ANF is sufficient to remove the distortion. This ANF will filter out the double frequency ripple so that it does not propagate through the phase-locked loop. If the PLL input contains harmonics as well, then a multi-block ANF should be used. In this case, each block removes at most only one harmonic component.

Since the ANF can continue to filter accurately during input frequency variations, the proposed structure is able to continue removing double frequency ripple and harmonics even if there are frequency variations present in the input signal. In terms of applications, this is an especially important feature for a DPGS operating autonomously. This is because frequency variations are negligible when a DPGS is connected to the utility grid, but are amplified when the DPGS operates in islanding mode or in stand-alone mode.

Another important feature of the proposed PLL is its ability to remove harmonic distortions. The IEEE standards require that the total harmonic distortion (THD) in a utility grid with a DPGS connected must be less than 2.5 percent [6]. However, this can be challenging because the power electronic converters present in a DPGS can be a source of harmonic distortions. The proposed PLL is advantageous because the multi-block ANF configuration can be used to remove multiple harmonics, where one or more ANF units can be assigned the task of removing a particular harmonic. Another advantage of the multi-block ANF configuration is that the ANFs are placed in parallel

with each other. Therefore, no matter how many different harmonics are present in the signal, the system response time will not increase.

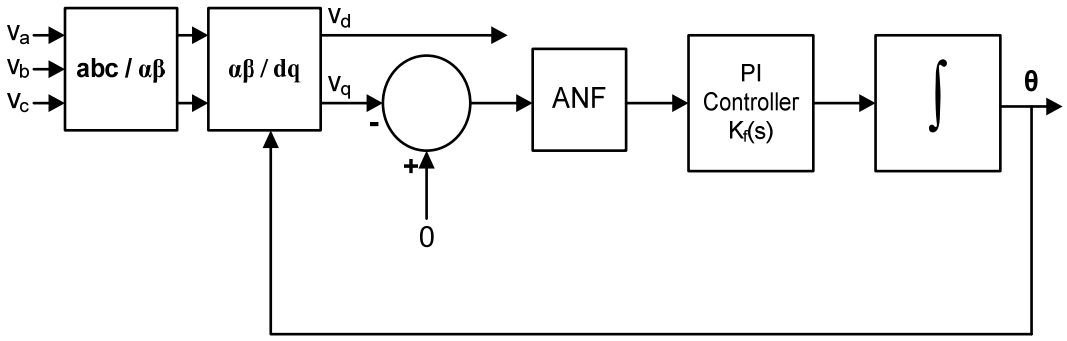

Figure 3–3: Enhanced Synchronous Reference Frame PLL

3.2 Simulation Results

The performance of the modified PLL has been studied by conducting computer simulations using Matlab/Simulink. The Matlab depiction of the proposed PLL, as well as the single-block and multi-block ANF subsystems, can be seen in Fig. 3-4 - 3-6.

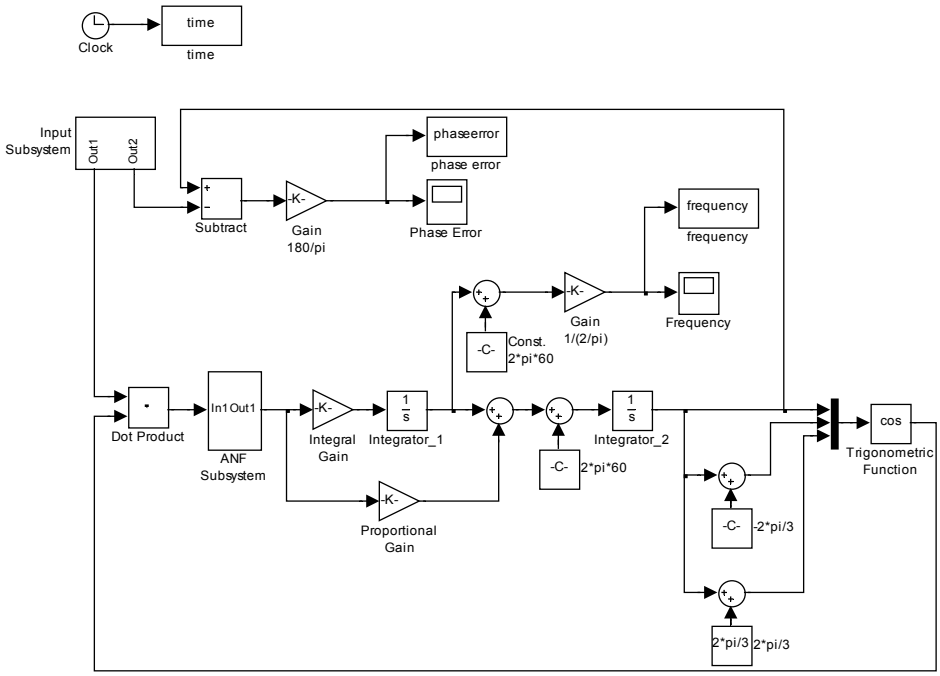

Figure 3–4: Proposed PLL Structure implemented in Matlab/Simulink

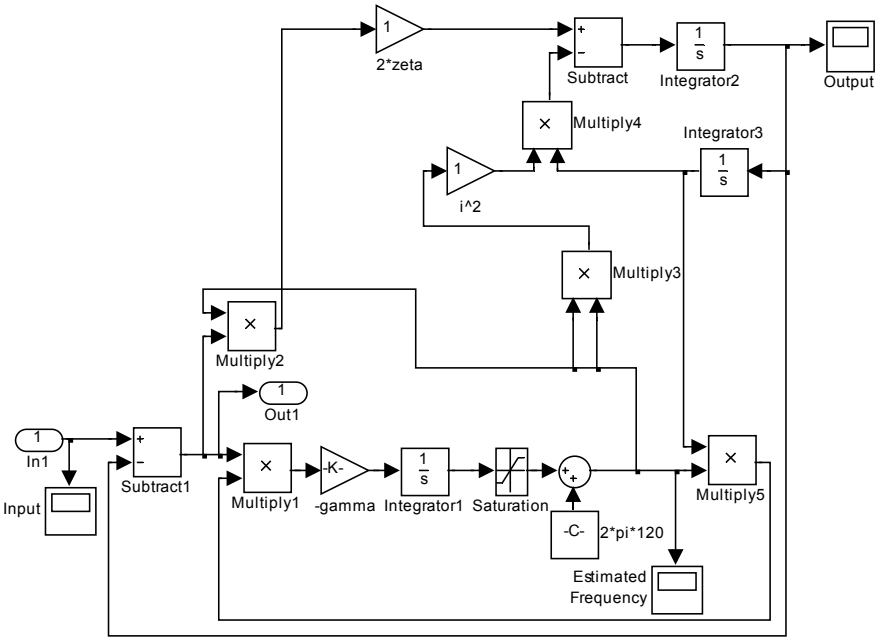

Figure 3–5: Single-block ANF structure implemented in Matlab/Simulink

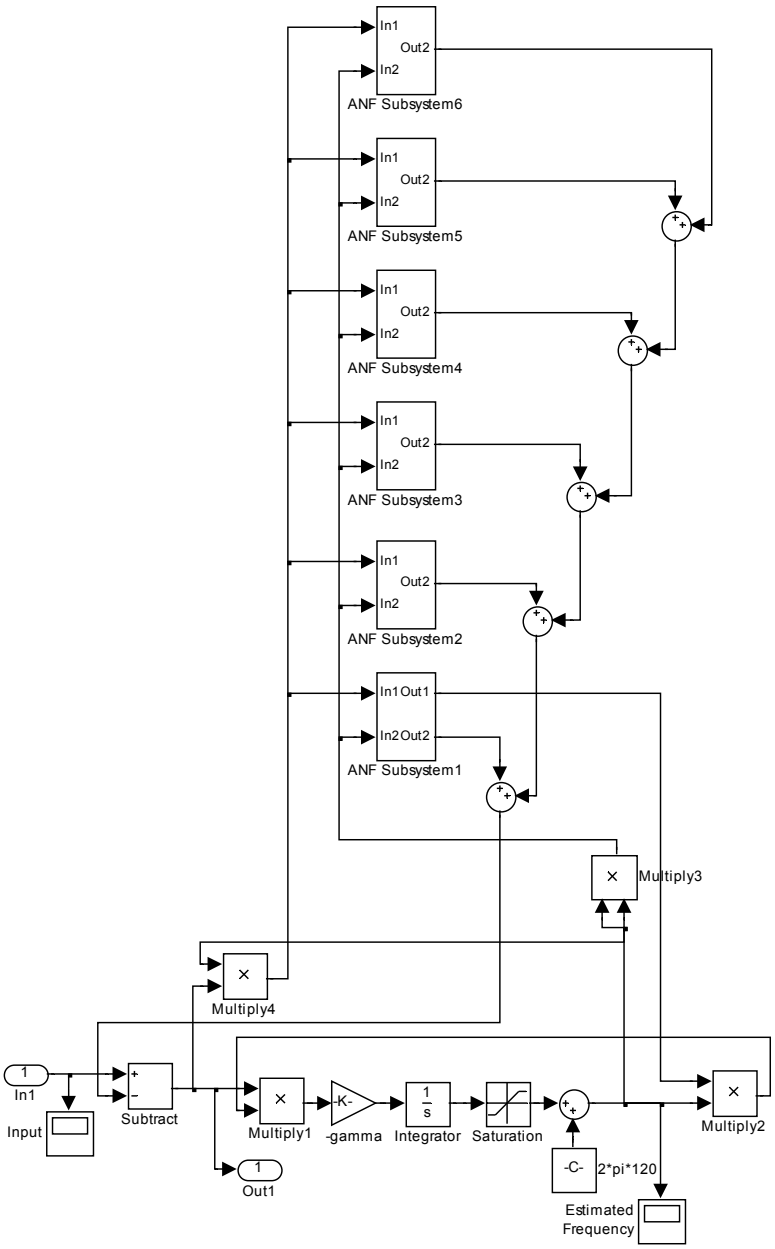

Figure 3–6: Multi-Block ANF structure implemented in Matlab/Simulink

For the first simulation, seen in Fig. 3-7, the parameters of the one-block ANF are set to $\zeta = 0.5$, $I = 1$, and $\gamma = 1 \times 10^6$. The gains of the PI controller in the PLL are set to

$K_i = 10000$ and $K_p = 150$. All gain values for both the PLL and the ANF were adjusted through trial and error. For this simulation, there is a frequency jump from 60Hz to 65Hz occurring at t = 0.05s. Then subsequently an input voltage unbalance occurs due to the injection of a negative sequence with an amplitude of 0.3 at t = 0.2s. As seen in the figure, the modified PLL is able to continue tracking the phase angle, with no visible error, 0.05s (three cycles) after the frequency jump occurs. Also, once the voltage unbalance is introduced, the modified PLL is again able to continue tracking the phase angle with no visible error and with the transient lasting less than 0.05s (three cycles).

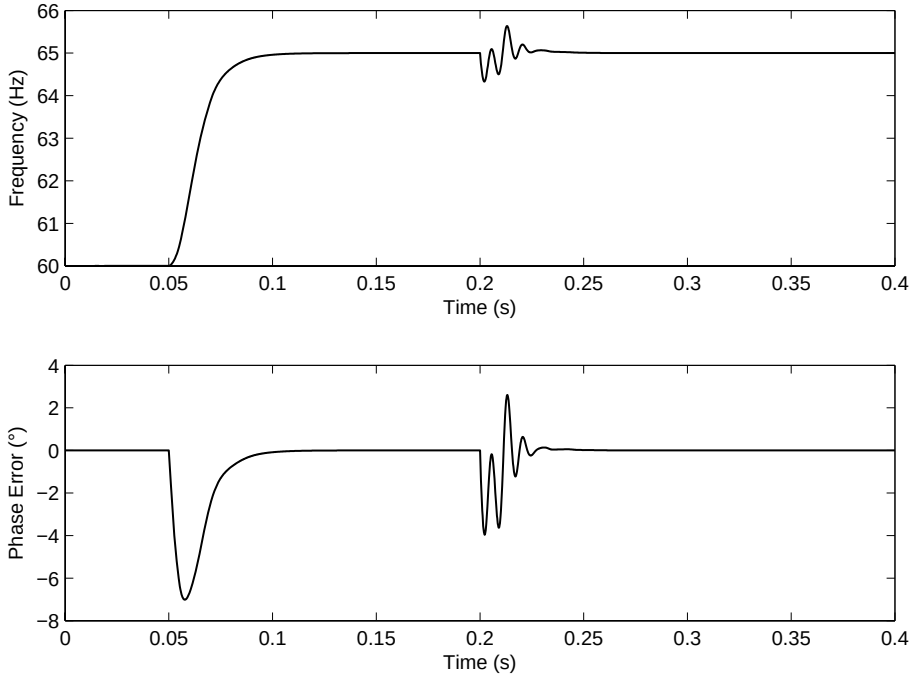

Figure 3–7: Conventional three-phase SRF-PLL with a one-block ANF. There is a frequency jump (from 60Hz to 65 Hz) at t = 0.05s and the input voltage becomes unbalanced at t = 0.2s.

The second simulation is used to analyze the effects of harmonics on the modified PLL with a one-block ANF. For this simulation, seen in Fig. 3-8, the parameters of the one-block ANF are set to $\zeta = 0.5$, $I = 1$, and $\gamma = 1 \times 10^6$. For this simulation, there is a frequency jump from 60Hz to 65Hz occurring at t = 0.05s. Then subsequently an input voltage unbalance occurs due to the injection of a negative sequence with amplitude of 0.3 at t = 0.2s. Harmonics (i.e., 30 % of the third harmonic and 20% of the fifth harmonics) are also injected into the system at t = 0.2s. Predictably, the results of this simulation demonstrate that the modified PLL with a one-block ANF is unable to remove the harmonics injected into the input, since the one-block ANF is only designed to remove the double-frequency ripple. To remove the distortion seen in this simulation, a multi-block ANF should be used inside the modified PLL, instead of a single block.

The third simulation, seen in Fig. 3-9, is used to demonstrate how efficiently a multi-block ANF is able to remove input harmonics. In this case a six-block ANF is used, and its parameters are set to $\zeta = 0.5$, $I = 1, 2 \ldots 6$, and $\gamma = 1 \times 10^6$. For this simulation, as with the previous one, there is a frequency jump from 60Hz to 65Hz occurring at t = 0.05s. Then subsequently an input voltage unbalance occurs due to the injection of a negative sequence with amplitude of 0.3 at t = 0.2s. Harmonics (i.e., 30 % of the third harmonic and 20% of the fifth harmonics) are also injected into the system at t = 0.2s. A six-block ANF is used because when there is a harmonic to the nth degree in the input of the SRF-PLL, two harmonics to the (n+1)th and (n-1)th degree will be present in the SRF-PLL control. Thus, since there are two harmonics in the input, there will be four harmonics circulating in the control loop. In order to remove both the double frequency

ripple, as well as the four harmonics, at least five ANF blocks are required. Thus, a six-block ANF is used in order to remove the maximum possible amount of distortion. The simulation results show that the PLL modified with a multi-block ANF is able to track the frequency jump within three cycles. The simulation results also show that the multi-block ANF is able to successfully remove both the double frequency ripple as well as the harmonics injected into the system within three cycles of the occurrence of the voltage unbalance.

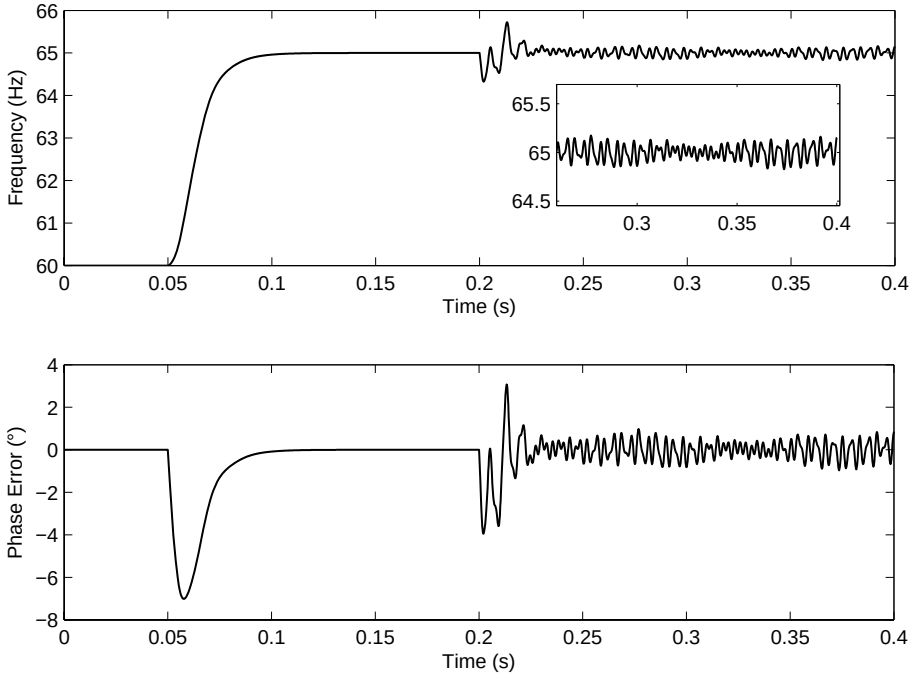

Figure 3–8: Conventional three-phase SRF-PLL with a one-block ANF. There is a frequency jump (from 60Hz to 65Hz) at t = 0.05s. Input voltage unbalance, third, and fifth harmonics are input into the system at t = 0.2s.

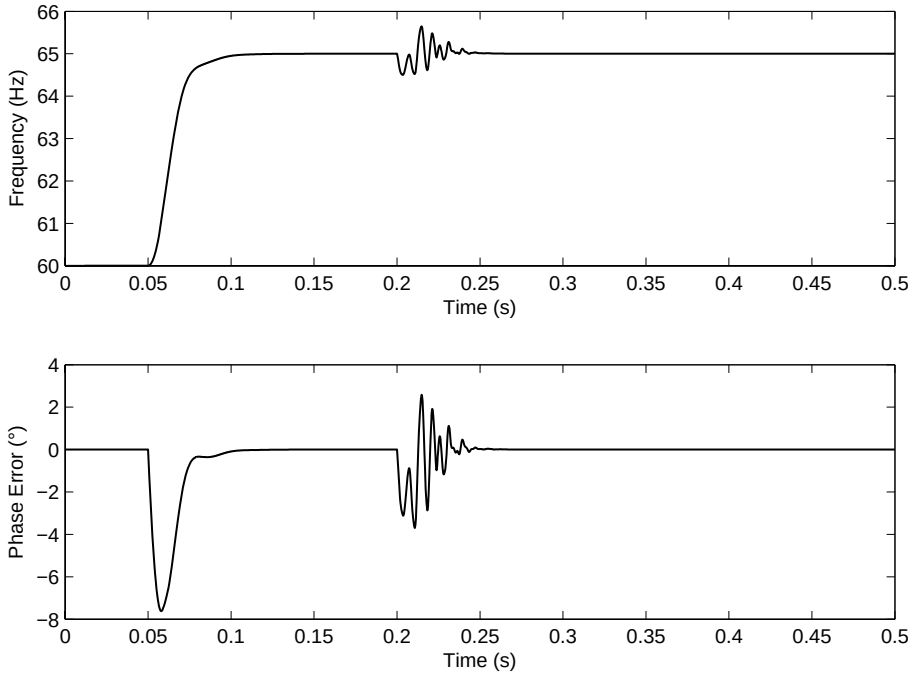

Figure 3–9: Conventional three-phase SRF-PLL with a six-block ANF. There is a frequency jump (from 60Hz to 65Hz) at t = 0.05s. Input voltage unbalance, third, and fifth harmonics are input into the system at t = 0.2s.

Two simulations are done using the single-block ANF to examine how quickly this modified PLL is able to track and respond to changes in the input. The first simulation, seen in Fig. 3-10, demonstrates how the modified PLL responds to an input frequency ramp. At t = 0.1s, an input frequency ramp occurs with a slope of 1. It can be seen that modified PLL tracks this change with very negligible delay. Next, an input voltage unbalance occurs at t = 0.2s. As can be seen, the modified PLL not only continues to track the ramp, but also removes the double frequency ripple that would be caused by an input voltage unbalance within three cycles.

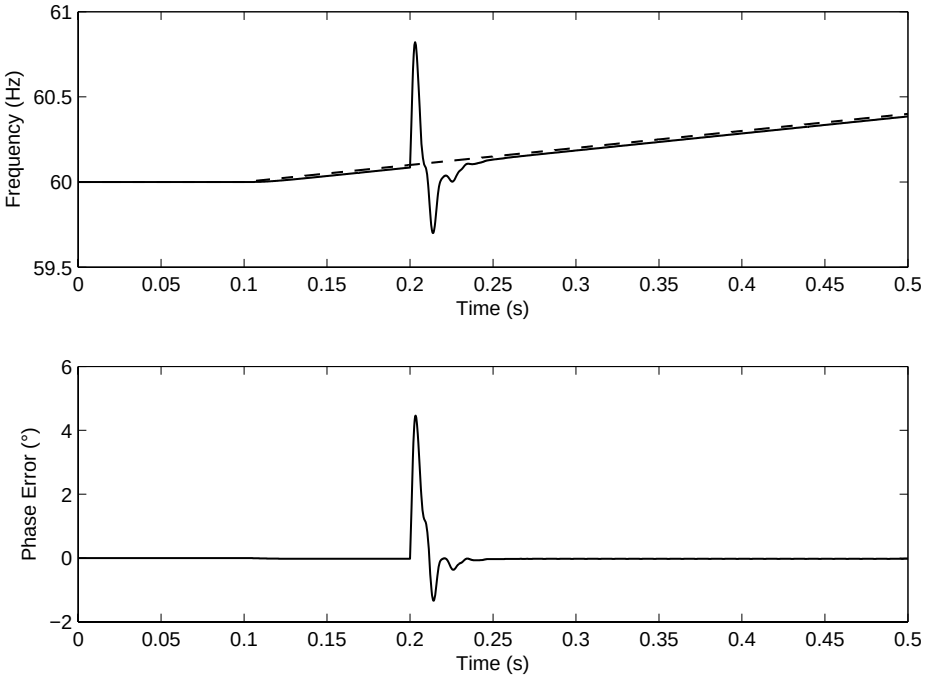

Figure 3–10: Conventional three-phase SRF-PLL with a one-block ANF. Input frequency ramp of slope = 1 occurs at t = 0.1s. Input voltage unbalance occurs at t = 0.2s. The dashed line on the frequency plot represents the input frequency ramp applied to the system.

The second simulation, seen in Fig. 3-11, demonstrates how the modified PLL responds to an input frequency ripple. In this simulation there is an input frequency ripple of 5Hz. It can be seen that modified PLL tracks this change with a very tiny delay. Next, an input voltage unbalance occurs at t = 0.2s. As can be seen, the modified PLL not only continues to track the ripple, but also removes the double frequency ripple that would be caused by an input voltage unbalance within 0.075s (four and a half cycles).

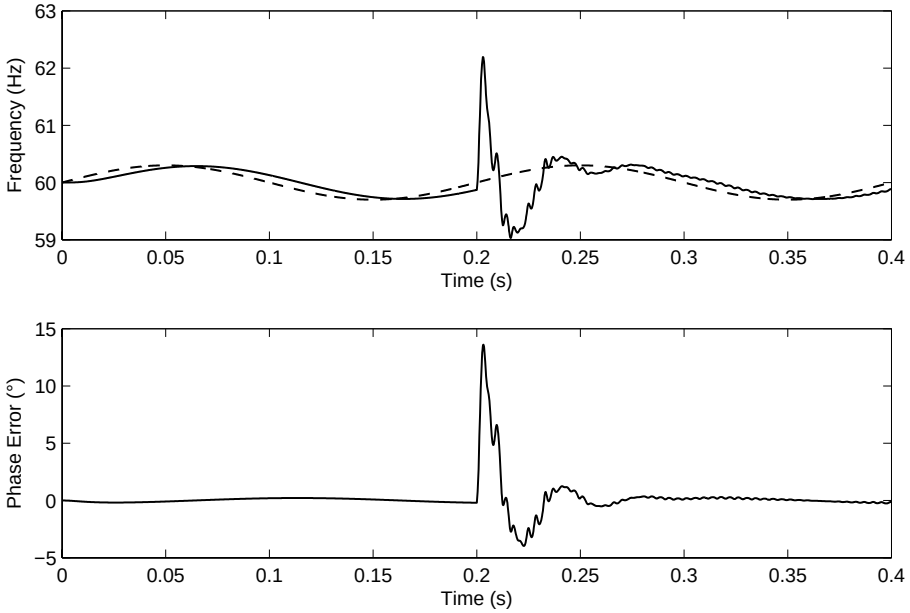

Figure 3–11: Conventional three-phase SRF-PLL with a one-block ANF. There is an input frequency ripple of 5 Hz. Input voltage unbalance occurs at t = 0.2s. The dashed line on the frequency plot represents the input frequency ripple applied to the system.

3.2 Experimental Results

The performance of the modified PLL has also been evaluated experimentally through the use of dSPACE. The dSPACE DS1103 DSP board was used to implement the proposed structure. In Fig. 3-13, a three-phase positive-sequence input, produced by a three-phase programmable source, is fed into a conventional PLL with a one-block ANF (see Fig.3-12). There is a frequency jump in the input from 60Hz to 65Hz, and 100 ms later a 30% negative-sequence is added to the input signal. Fig. 3-14 shows the output signals of the conventional PLL with a one-block ANF, in response to this input. Results show that the PLL is able to recover to steady-state, with no distortion in the output, in

approximately 20-30ms. Note that in Figure 3-14 the frequency (CH2) is multiplied by 0.1.

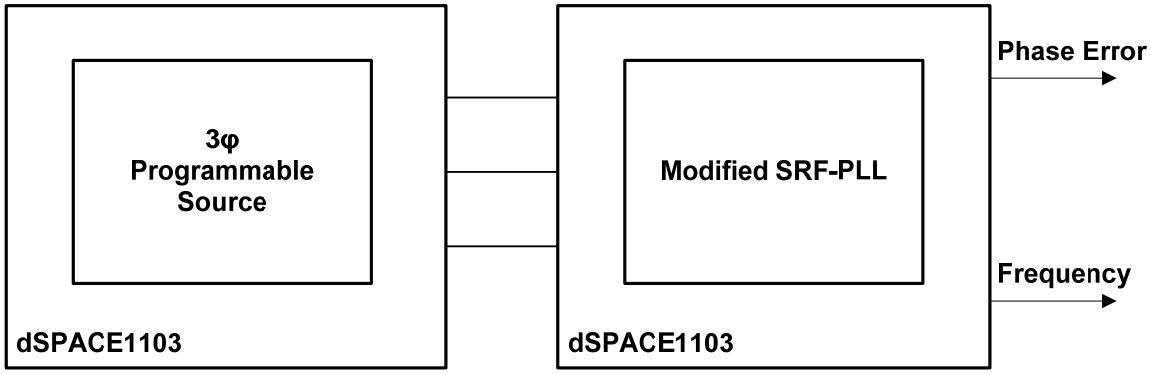

Figure 3–12: Setup used to obtain experimental results

In Fig. 3-15, a three-phase positive-sequence input is fed into a conventional PLL with a six-block ANF. There is a frequency jump in the input from 60Hz to 65Hz, and 100 ms later a 30% negative-sequence, a 30% third harmonic, and a 20% fifth harmonic are added to the input signal. Fig. 3-16 shows the output signals of the conventional PLL with a six-block ANF, in response to this input. Results show that the PLL is able to recover to steady-state, with no distortion in the output, in approximately 30ms. Note that in this figure the frequency (CH2) is multiplied by 0.1.

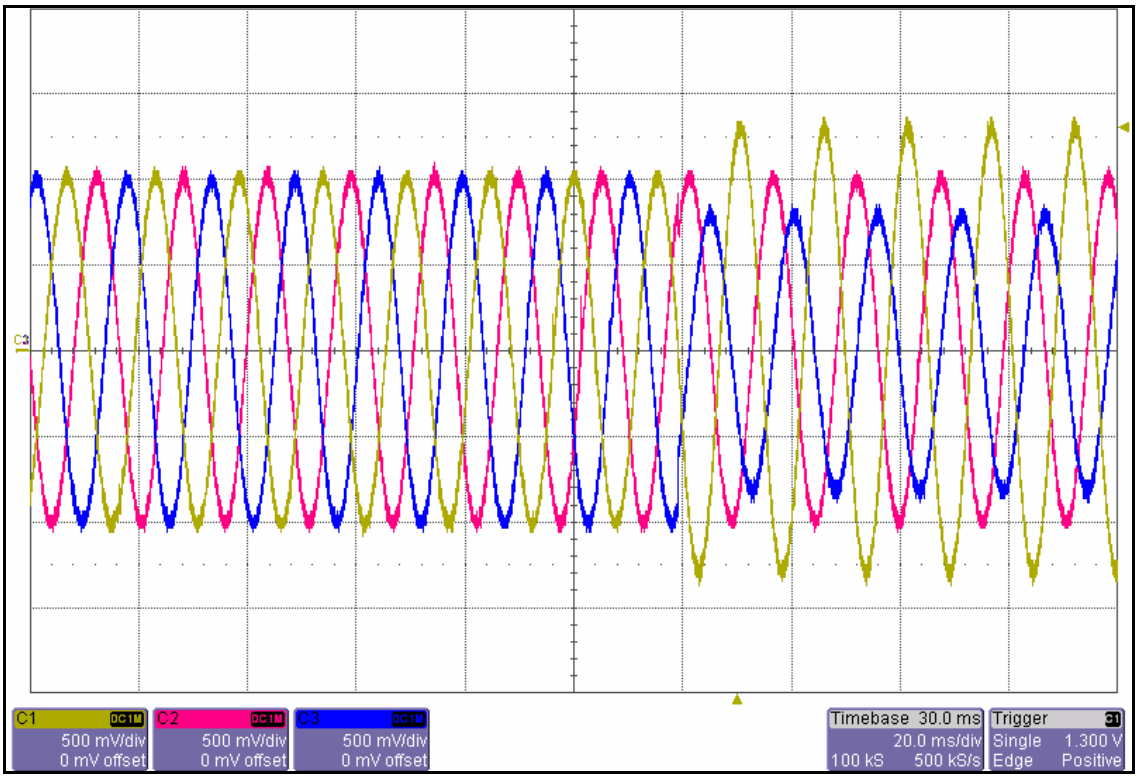

Figure 3–13: Three-phase input into conventional three-phase SRF-PLL with a one-block ANF.

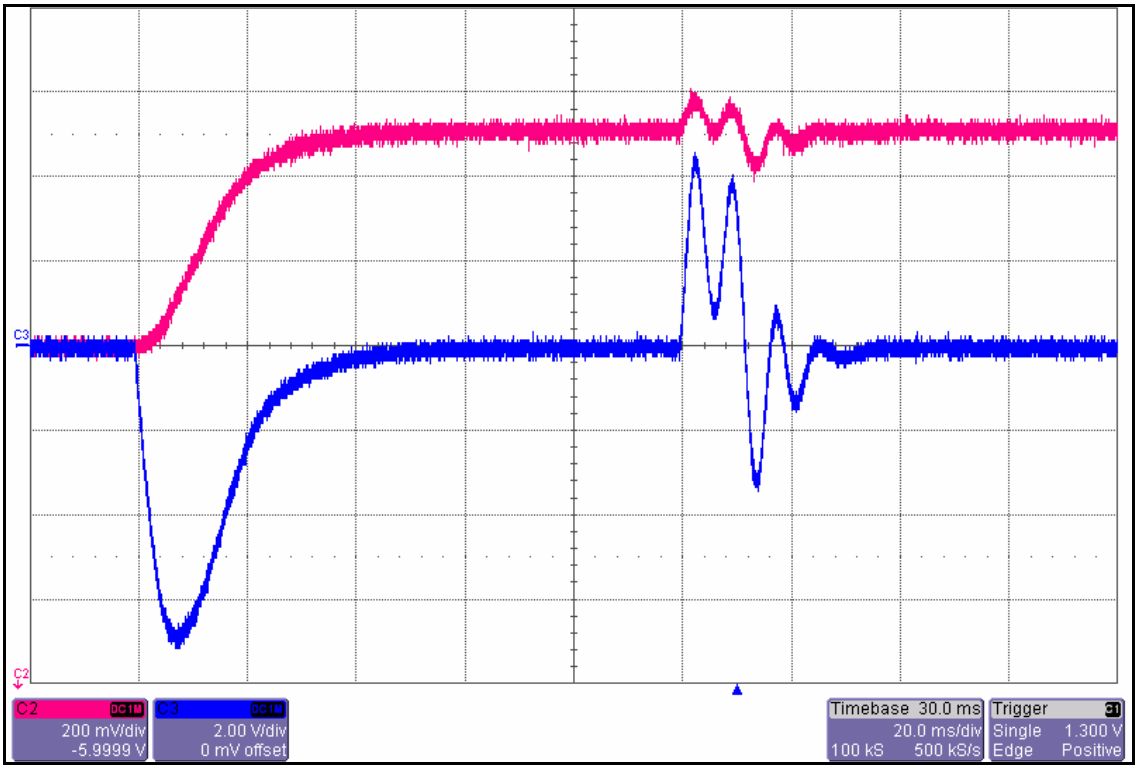

Figure 3–14: These are the output signals of a conventional three-phase SRF-PLL with a one-block ANF in response to the input signals shown in Fig. 3-13. The outputs are the phase error (CH3) and frequency (CH2).

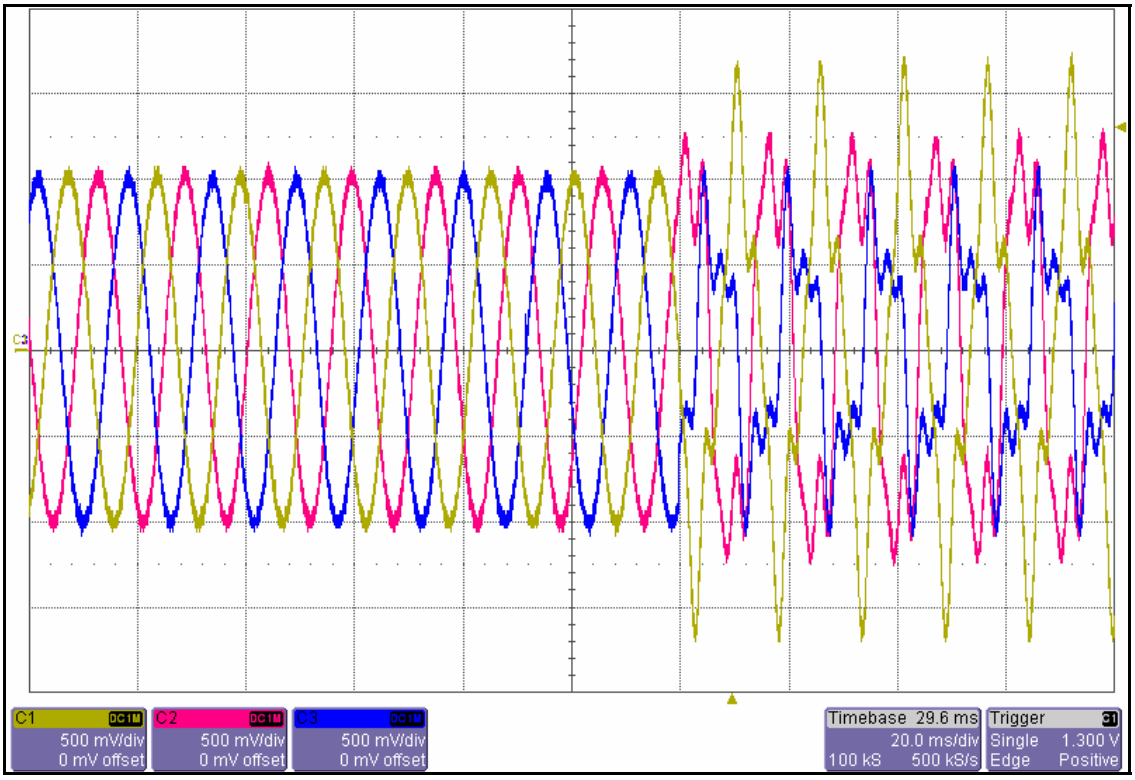

Figure 3–15: Three-phase input into conventional three-phase SRF-PLL with a six-block ANF.

In Fig. 3-17, a three-phase positive-sequence input is fed into a conventional PLL with a one-block ANF. There is a frequency ramp in the input with a slope of 1, and 100 ms later a 30% negative-sequence is added to the input signal using a step function. Fig. 3-18 shows the output signals of the conventional PLL with a one-block ANF, in response to this input. Results show that the PLL is able to recover to steady-state, with no distortion in the output, in approximately 30ms.

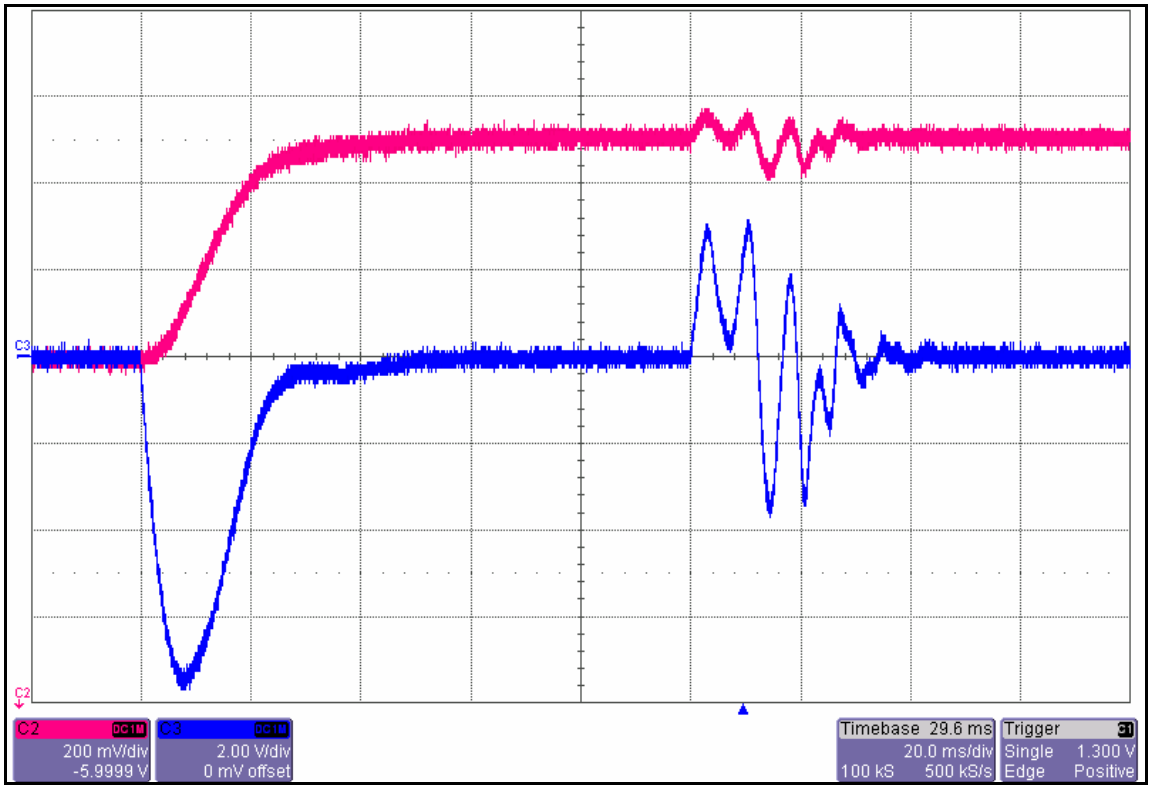

Figure 3–16: These are the output signals of a conventional three-phase SRF-PLL with a six-block ANF in response to the input signals shown in Fig. 3-15. The outputs are the phase error (CH3) and frequency (CH2).

In Fig. 3-19, a three-phase positive-sequence input is fed into a conventional PLL with a one-block ANF. There is a sinusoidal frequency ripple in the input with a frequency of 5Hz and amplitude of 0.3, and 100 ms later a 30% negative-sequence is added to the input signal using a step function. Fig. 3-20 shows the output signals of the conventional PLL with a one-block ANF, in response to this input. Results show that the PLL is able to recover to steady-state, with no distortion in the output, in approximately 30ms.

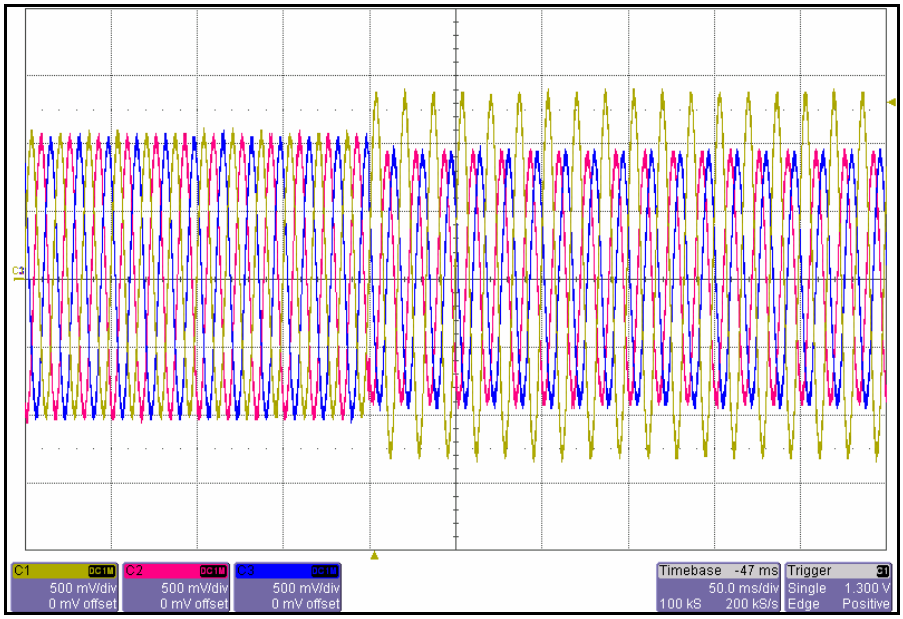

Figure 3–17: Three-phase input into conventional three-phase SRF-PLL with a one-block ANF. There is a frequency ramp in the input.

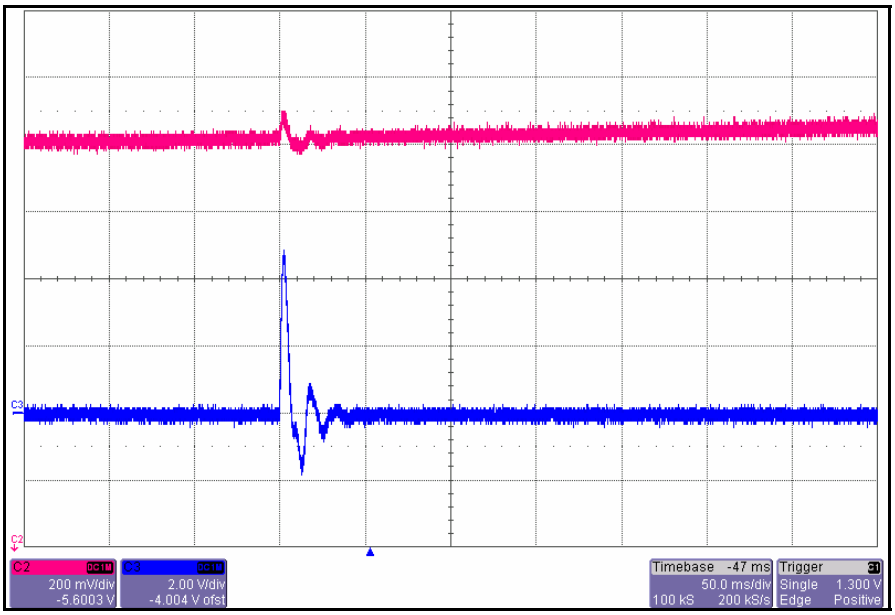

Figure 3–18: These are the output signals of a conventional three-phase SRF-PLL with a one-block ANF in response to the input signals shown in Fig. 3-17. The outputs are the phase error (CH3) and frequency (CH2).

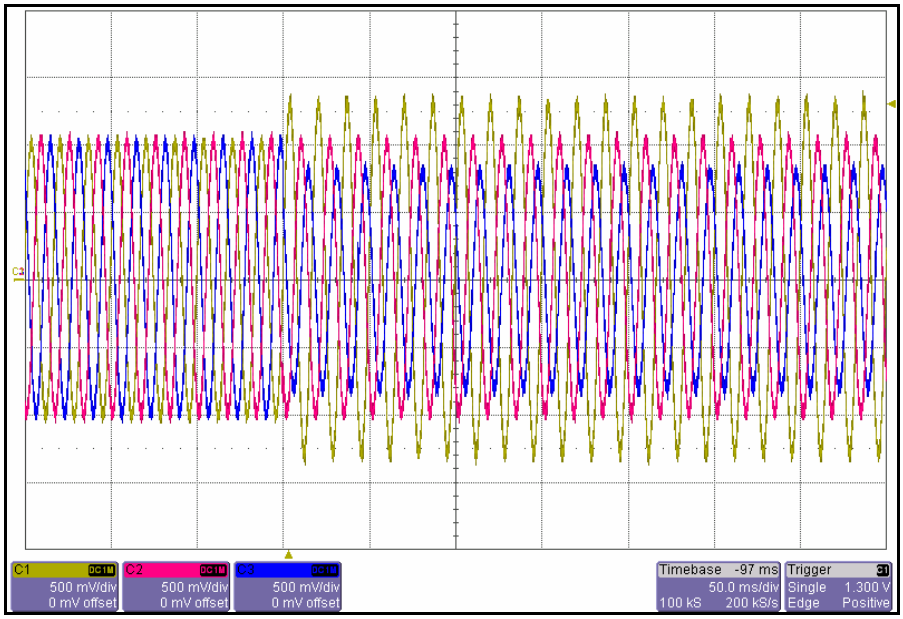

Figure 3–19: Three-phase input into conventional three-phase SRF-PLL with a one-block ANF. There is a sinusoidal frequency ripple in the input.

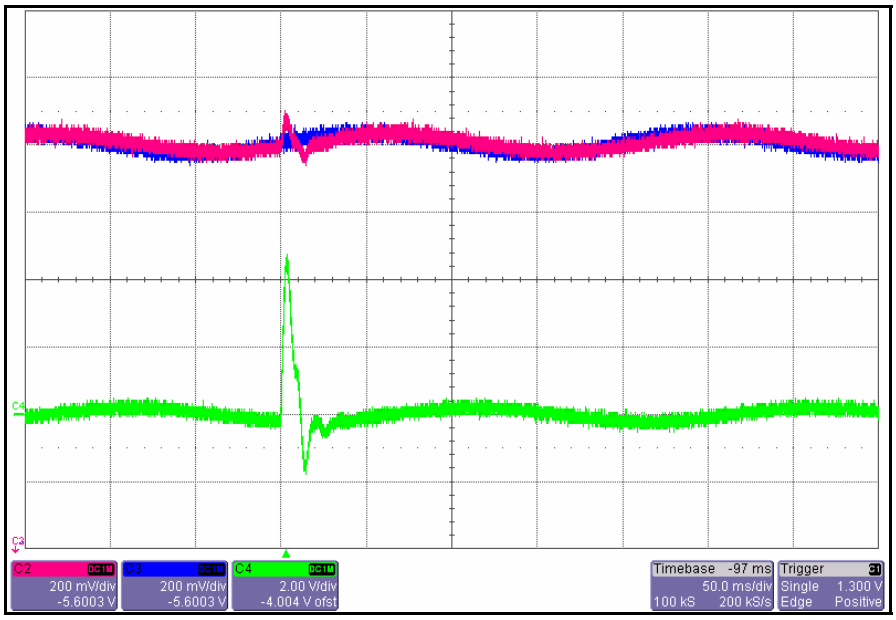

Figure 3–20: These are the output signals of a conventional three-phase SRF-PLL with a one-block ANF in response to the input signals shown in Fig. 3-19. The outputs are the phase error (CH4) and the extracted frequency (CH3). CH2 represents the actual frequency.

3.4 Chapter Summary

The proposed PLL integrates an adaptive notch filter into a conventional three-phase PLL. The adaptive notch filter is similar to a notch filter but has an added frequency estimation loop. The adaptive notch filter is also capable of removing multiple distortions simultaneously. This allows it to successfully remove the double frequency ripple caused by input signal unbalance as well as multiple harmonic distortions. Since the ANF has a frequency estimation loop, the proposed PLL can successfully remove these distortions even when there are frequency variations in the input signal. Simulations were performed on Matlab/Simulink, and experimental results were obtained using DSpace, which verify the good performance of the proposed PLL. The simulation and experimental results verify that the proposed PLL is able to adjust to frequency variations and continue to extract multiple distortions.

Chapter 4
Conclusion

4.1 Summary

The importance of effective signal-processing and control techniques for distributed power generation systems (DPGS) was discussed, along with the need for a robust grid synchronization technique. It was observed that the phase-locked loop is the state-of-the-art technique used to achieve grid synchronization. It was also observed that three-phase PLL techniques were more widely used than single-phase PLL techniques. The conventional three-phase PLL technique was presented in detail, as well as its shortcomings.

This thesis proposed a modified phase-locked loop technique with grid synchronization as its intended application. The proposed PLL structure combined the conventional synchronous reference frame phase-locked loop (SRF-PLL) with the adaptive notch filter (ANF) to overcome the shortcomings present in the SRF-PLL when grid conditions were not ideal. The modified SRF-PLL was successful in removing the double frequency ripple (caused by a three-phase input signal unbalance) from the phase angle and frequency output. The ANF used in the modified SRF-PLL also had a multi-unit structure which allowed it to remove multiple harmonic distortions from the phase angle and frequency output as well. Since the ANF is frequency adaptive, it could continue to remove these distortions even when there were frequency variations in the input signal. Simulations results were included which demonstrated that the modified

SRF-PLL could execute the aforementioned features. The modified SRF-PLL was able to detect the phase angle quickly and accurately, and the setup of the system was fairly straightforward. Also, the modified SRF-PLL was able to remove the double frequency ripple caused by unbalance as well as multiple harmonic distortions even after an input frequency variation had occurred. Simulation results also confirmed that the performance of the proposed system was notably superior to the performance of a conventional SRF-PLL, as well to the performance of an SRF-PLL equipped with a simple notch filter. Experimental results were also included which verified the validity of the simulation results, and were executed using the dSPACE DS1103 DSP board.

4.2 Contributions

The development of a robust and effective three-phase phase-locked loop for grid-connected DPGS synchronization applications is the key contribution of this dissertation. Through simulation and experimental analyses it has been shown that the modified SRF-PLL can detect the phase angle and frequency of a three-phase input signal quickly and accurately in the presence of frequency variations. It is also able to remove the double frequency ripple generated by input signal unbalance from the phase angle and frequency output such that it becomes negligible. Finally, it is able to remove multiple harmonic distortions from the phase angle and frequency output. Thus, the modified SRF-PLL can perform well in the presence of a variety of grid disturbances, and would be well-suited for grid-connected DPGS applications.

4.3 Future Works

The following are suggestions for future works:

(1) Make further changes to the modified SRF-PLL which enables it to detect the amplitude of the input signal in addition to the frequency and phase angle.

(2) Place the modified SRF-PLL into the control scheme of a grid-side converter for power quality as well as monitoring and protection purposes.

(3) Investigate possible applications of the modified SRF-PLL for islanding detection.

(4) Find an algorithm to optimize the parameters of the multi-block ANF used in the modified SRF-PLL.

(5) Consider an application-specific integrated circuit (ASIC) implementation of the modified SRF-PLL.

References

[1] "New World Record in Wind Power Capacity," World Wind Energy Association (WWEA), Press Release, January 2007.

[2] "Renewable 2007 Global Status Report," Renewable Energy Policy Network for the 21st Century, December 2007.

[3] CANWEA, *Canada's Current Installed Capacity*. [Online]. Available: http://www.canwea.ca

[4] IEA-PVS, *Trends in photovoltaic applications: Survey report of selected IEA countries between 1992 and 2007*, [Online]. Available: http://www.iea-pvps.org

[5] P. A. Daly and J. Morrison, "Understanding the potential benefits of distributed generation on power delivery systems," *IEEE Rural Electric Power Conference*, pp. A2-1 – A2-13, 2001.

[6] IEEE Standard 1547-2003: IEEE Standard for interconnecting distributed resources with electric power systems.

[7] IEEE Standard 929-2000: IEEE Recommended practice for utility interface of photovoltaic (PV) systems.

[8] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible Active Power Control of Distributed Power Generation Systems During Grid Faults," *IEEE Transactions on Power Electronics*, Vol. 57, No. 5, pp. 2583-2592, Oct. 2007.

[9] F. Blaabjerg, A. Consoli, J. A. Ferreira, and J. D. van Wyk, "The Future of Electronic Power Processing and Conversion (Special Feature)," *IEEE Transactions on Industry Applications*, Vol. 41, No. 1, pp. 3-8, Jan.-Feb. 2005.

[10] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, Vol. 53, No. 5, pp. 1398-1409, October 2006.

[11] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, Vol. 19, No. 5, pp. 1184-1194, Sep. 2004.

[12] R. Teodorescu and F. Blaabjerg, “Flexible Control of Small Wind Turbines with Grid Failure Detection Operating in Stand-Alone and Grid-Connected Mode,” *IEEE Transactions on Power Electronics*, Vol. 19, No. 5, pp. 1323-1332, September 2004.
[13] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, “Microgrids,” *IEEE Power and Energy Magazine*, pp. 78-94, July/August 2007.
[14] M. Karimi-Ghartemani and H. Karimi, “Processing of Symmetrical Components in Time-Domain,” *IEEE Transactions on Power Systems*, Vol. 22, No.2, pp. 572-579, May 2007.
[15] F. M. Gardner, *Phase Lock Techniques*. New York: Wiley, 1979.
[16] S.-K. Chung, “A Phase Tracking System for Three Phase Utility Interface Inverters,” *IEEE Transactions on Power Electronics*, Vol. 15, No. 3, pp. 431-438, 2000.
[17] A. Yazdani and R. Iravani, “A Unified Dynamic Model and Control for theVoltage-Sourced Converter Under Unbalanced Grid Conditions,” *IEEE Transactions on Power Delivery*, Vol. 21, No. 3, pp. 1620-1629, July 2006.
[18] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, “Decoupled Double Synchronous Reference Frame PLL for Power Converters Control,” *IEEE Transactions on Power Electronics*, Vol.22, No. 2, pp. 584-592, March 2007.
[19] M. Mojiri and A. Bakhshai, “An Adaptive Notch Filter for Frequency Estimation of a Periodic Signal,” *IEEE Transactions on Automatic Control*, Vol. 49, No. 2, pp. 314-318, February 2004.
[20] M. Mojiri, M. Karimi-Ghartemani, and A. Bakhshai, “Time-Domain Signal Analysis Using Adaptive Notch Filter,” *IEEE Transactions on Signal Processing*, Vol. 55, No. 1, pp. 85-93, January 2007.
[21] R. Weidenbrug, F. P. Dawson, and R. Bonert, “New synchronization method for thyristor power converters to weak AC-system,” *IEEE Transactions on Industrial Electronics*, Vol. 40, No. 5, pp. 505-511, Oct. 1993.
[22] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, “Power converter line synchronization using a Discrete Fourier Transform (DFT) based on a variable sample rate,” *IEEE Transactions on Power Electronics*, Vol. 20, No. 4, pp.877-884, July 2005.

[23] M. Karimi-Ghartemani and M. R. Iravani, "A Method for Synchronization of Power Electronic Converters in Polluted and Variable-Frequency Environments," *IEEE Transactions on Power Systems*, Vol. 19, No. 3, pp. 1263-1270, August 2004.
[24] J. Svensson, "Synchronization methods for grid-connected voltage source converters," *Proc. Inst. Elect. Eng. Generation, Transmission, Distribution*, Vol. 148, pp. 229-235, May 2001.
[25] M. Karimi-Ghartemani and M. R. Iravani, "A nonlinear adaptive filter for on-line signal analysis in power systems: applications," *IEEE Transactions on Power Delivery*, Vol. 17, No. 1, pp. 617-622, 2002.
[26] M. Karimi-Ghartemani, "A Distortion-Free Phase-Locked Loop System for FACTS and Power Electronic Controllers," *Electric Power System Research (77)*, pp. 1095-1100, 2007.
[27] D. Jovcic, "Phase Locked Loop System for FACTS," *IEEE Transactions on Power Systems*, Vol. 18, No. 3, pp. 1116-1124, Aug. 2003.
[28] M. Karimi-Ghartemani, H. Karimi, and M. Iravani, "A Magnitude/Phase-Locked Loop System Based on Estimation of Frequency and In-Phase/Quadrature-Phase Amplitudes," *IEEE Transactions on Industrial Electronics*, Vol. 51, No. 2, pp. 511-517, April 2004.
[29] V. Kaura and V. Blasko, "Operation of phase loop system under distorted utility conditions," *IEEE Transactions on Industrial Applications*, Vol. 33, No. 1, pp.58-63, 1997.
[30] M. Kazmierowski, R. Krishnan, and F. Blaabjerg, *Control in Power Electronics – Selected Problems*. New York: Academic, 2002.
[31] S.-J. Lee, J.-K. Kang, and S.-K. Sul, "A New Phase Detecting Method for Power Conversion Systems Considering Distorted Conditions in Power System," *Proc. IAS Annual Meeting*, p.2167-2172, 1999.
[32] M. Karimi-Ghartemani, "A Novel Three-Phase Magnitude-Phase-Locked Loop System," *IEEE Transactions on Circuits and Systems*, Vol. 53, No. 8, pp. 1792-1802, August 2006.

[33] A. V. Timbus, R. Teodorescu, F. Blaabjerg, M. Liserre, and P. Rodriguez, "PLL Algorithm for Power Generation Systems Robust to Grid Voltage Faults," *37th IEEE Power Electronics Specialists Conference 2006 (PESC'06)*, pp.1-7, June 2006.