ANALYSIS, DESIGN & CONTROL OF LOW-*Q* LLC DC-DC RESONANT CONVERTER FOR WIDE INPUT VOLTAGE AND LOAD RANGE APPLICATIONS

by

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Abstract

Constant frequency LLC converters reported in literature guarantees optimal efficiency only at nominal operating conditions and lose zero voltage switching (ZVS) at reduced load and high-end of the input voltage range. Traditional variable frequency LLC resonant converter requires wide switching frequency range and a high quality-factor (Q) of resonant circuit for voltage regulation at light loads. A high Q results in large size of the resonant circuit, increased magnetic losses and high circulating current for a wide range of load and input voltage variations. Low-Q LLC resonant circuits may allow efficient operation of the converters due to low voltage stress across the magnetics and capacitors, but they will lose ZVS operation at light loads. This thesis presents the analysis of low-Q LLC resonant converters and also proposes a new control technique.

Frequency domain modeling of the low-Q LLC resonant circuit is not possible without considerably sacrificing the accuracy of the design results. This is because for low-Q LLC resonant circuit, the voltage waveform at the output of the circuit is not defined. An accurate time-domain analysis of the resonant converter is, therefore, required and proposed in this thesis.

A novel light-load modulation scheme is proposed for achieving ZVS operation from part-load to extremely light-load conditions at high end of the input voltage range. In the proposed scheme, both duty cycle and switching frequency of the full bridge inverter are varied. A time domain model has been developed and resulting non-linear transcendental equations solved using Newton Raphson method.

An experimental prototype of 380V/300W LLC converter operating between input voltage 20-40V, is developed for validating the analysis and performance of the proposed LLC converter. An efficiency improvement of upto 6% is observed for the loads below 10% of the full-load.

Dedicated to

Maa, Papa & Bhai

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a	Steinmetz co-efficient
A_e	Effective core area
b	Steinmetz co-efficient
ΔB	Peak-peak flux density
c	Steinmetz co-efficient
C_1	Core factor
C_d	Distributed capacitance of high frequency isolation transformer
C_{oss}	Junction capacitance of MOSFET
C_s	Series resonant capacitance
C_{sn}	Snubber capacitance
D	Duty cycle
f_r	Series resonant frequency
f_{sw}	Switching frequency
f_{sw_max}	Maximum allowable switching frequency
f_{sw_min}	Minimum allowable switching frequency
G_{FHA}	DC gain derived using fundamental harmonic approximation
G_{max}	Maximum required dc gain of LLC converter
G_{min}	Minimum required dc gain of LLC converter
G_{NP}	DC gain of NP mode
G_{PO}	DC gain of PO mode
i_{Ls}	Series inductor current
I_{base}	Base current value
I_o	Average output current

I_{RMS_O}	RMS current for O stage
I_{RMS_P}	RMS current for P stage
I_{RMS_PO}	RMS current for PO mode
K	Ratio of magnetizing inductance and series inductance
L_{lkg}	Transformer leakage inductance
L_m	Magnetizing inductance
L_s	Series resonant inductance
n	Transformer turns ratio
N_p	Primary winding turns
N_s	Secondary winding turns
P_{base}	Base power
P_{core}	Core power loss
Q_{rated}	Rated quality factor
R_{ac}	Equivalent ac load
R_l	Load resistance
t_d	Time ratio of rectifier diode conduction to switch conduction
v_{Cs}	Series capacitor voltage
v_{ab}	Voltage across mid-point of full bridge switching network
V_c	Core volume
V_{in_max}	Maximum input voltage of PV voltage range
V_{in_min}	Minimum input voltage of PV voltage range
V_{in_nom}	Nominal input voltage
V_o	Output voltage
Z_{in}	Input impedance of LLC resonant tank
Z_0	Characteristic impedance of series L_s and C_s

Z_1	Characteristic impedance of L_s, C_s and L_m
ω	Normalized switching frequency of switching network
ω_{max}	Maximum normalized switching frequency of switching network
ω_{min}	Minimum normalized switching frequency of switching network
ω_{nom}	Nominal normalized switching frequency of switching network
ω_r	Series resonant frequency, in radians
ω_{r1}	Resonant frequency of L_s, C_s and L_m, in radians
ω_s	Switching frequency, in radians
ϕ_{NP}	ZVS angle of NP mode
ϕ_{PO}	ZVS angle of PO mode
ρ_i	Current form factor
μ_{eff}	Effective permeability of ferrite core material

Chapter 1

Introduction

1.1 Background and Challenges

In the past decade, there has been a major overhaul of the traditional coal-based utility grid across the world. The rise of cost-effective renewables, such as solar PV and wind, has led to grid parity for customers [1,2]. PV energy systems will make up more than 32% of the total electricity supply by 2022 as estimated by the European Photovoltaic Industry Association [3]. Efficient power conversion architectures are an important link between the renewable energy power source and the end-user.

Several power architectures exist for photovoltaic power applications [4-8]. A grid-interfaced micro-system, illustrated in Figure 1-1, has smaller power ratings (150W-2kW) but are often preferred due to extra flexibility for large-scale applications [9]. The biggest challenge is imposed by the dc-dc converter stage. For a PV application, the dc-dc converter stage must withstand fluctuations in input voltage and output loading conditions while maintaining good power conversion efficiency levels. Additionally, it is required that the chosen power converter topology should be compact, light weighted, possess high power density.

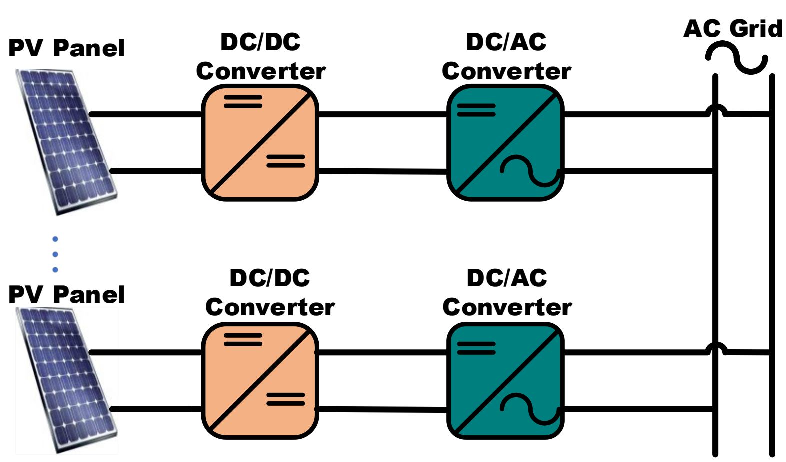


Figure 1-1: Grid interface microsystem

Hence, it is desirable for the converters to operate at high switching frequencies to minimize the size of bulky passive components such as transformers, inductors and capacitors. Apart from selection of suitable power converter topology, reliable mathematical modeling of the selected topology is also a crucial aspect to be considered for analysis during design procedure.

DC-DC converters can be categorized broadly into two categories:

1.1.1 Pulse-Width Modulated (PWM) Switched Mode Converter

PWM switched mode converters [10-12] utilize a square wave pulse width input for output voltage regulation. Due to attractive features such as simple mathematical modeling, easy-to-design circuit, fixed frequency operation and high efficiency for a wide line and load control range, PWM converters are commercially viable. However, hard switching of semiconductor components causes increased power loss. Such hard-switching conditions restrict application at high operating frequencies. Large dv/dt and di/dt causes switching stress due to Electro-Magnetic Interference (EMI) issues. In order to ensure excellent performance at high operating frequencies, soft switching is necessary.

1.1.2 Soft Switched Converter

Soft-switched converters [15-78] introduce a resonant network (made up of inductors and capacitors) with a designed quality factor (Q) to conventional PWM converters due to which zero voltage switching (ZVS) and zero current switching (ZCS) can be achieved. Incorporating soft-switching technique reduces switching losses, improves power density and efficiency. Moreover, resonant converters exhibit lower EMI due to minimum noise generated by converter components as a result of soft switching.

Generally, a resonant converter consists of a switching network, a resonant tank network, high frequency (HF) isolation transformer with turns ratio $n(N_p/N_s)$ and rectifier network as seen in Figure 1-2. The supply voltage is modulated by a half-bridge or full- bridge switching network. Depending on the resonant tank configuration, these converters provide an inherent input/output

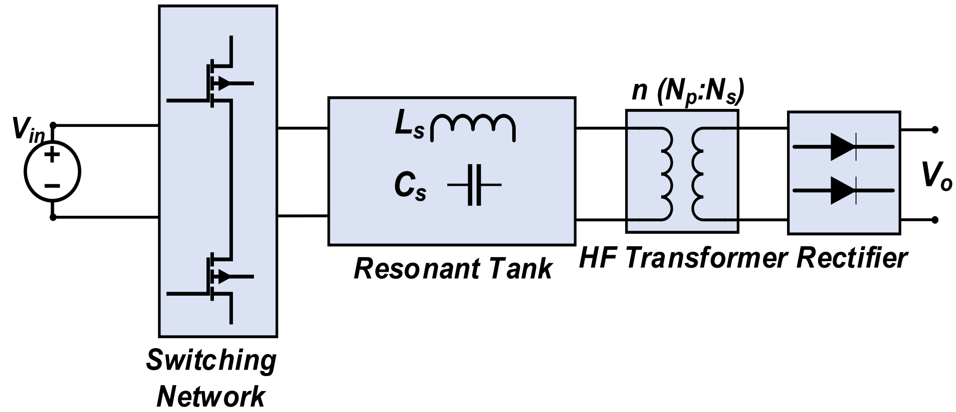


Figure 1-2: General structure of a DC-DC resonant converter

gain which is a function of excitation frequency. Varying the switching frequency and loading conditions changes magnitude of ac waveforms applied to the resonant tank circuit, thereby achieving desired voltage and/or current regulation. The high frequency transformer provides isolation between the primary and secondary side. Depending on which configuration is used, the leakage inductance of the transformer can be used partially or wholly as an element of the resonant tank. It also provides the necessary voltage step-up/step down feature.

Depending on number of passive tank elements (*L* and/or *C*) present, any number of tank configurations are possible [18,19]. The most commonly used resonant converter topologies are series resonant converter (SRC) [20-25], parallel resonant converter (PRC) [27-33] and series parallel resonant converter (SPRC) [34-44]. SRC has the simplest structure amongst all three and guarantees maximum power transfer from full load to part load. However, it requires wide switching frequency variation to maintain ZVS for output regulation at light loads. Apart from these resonant tank configurations, LLC converter has gained a lot of attention in recent years [45-89] due to its ability to maintain ZVS for primary MOSFETs and ZCS for secondary-side rectifier diodes for a wide input/load range. However, due to their characteristic non-linear behavior and existence of multiple modes due to 3 element tank configuration, analysis, design and control of LLC resonant converters is a challenge.

1.2 Analysis of Low *Q* LLC Resonant Converters

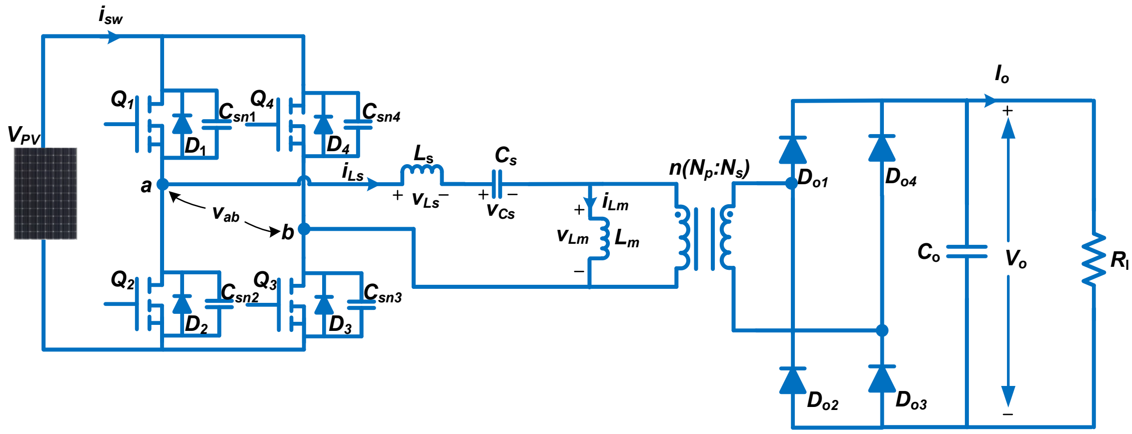


Figure 1-3: Typical architecture of a full bridge LLC resonant converter.

As shown in Figure 1-2, resonant tank is excited by a modulated supply voltage which is further rectified and filtered into DC output. A capacitive filter is preferred for a micro-converter application since it is less bulky than an inductive filter. A typical full bridge LLC resonant converter for solar PV application is shown in Figure 1-3. A full bridge architecture of the inverter allows for flexibility in choosing modulation technique over a half-bridge architecture. It also permits higher power to be processed through the same transformer design. A full-bridge secondary rectifier reduces voltage stress for high voltage output applications.

Unlike PWM converters, switching frequency of a resonant converter is comparable to the resonant frequency of the L-C resonant tank network. Therefore, the voltage or current variation during one switching cycle has higher amplitude compared to low-frequency ripple of hard switched PWM converter. Hence, small-signal based transfer function analysis method [13,14] isn't an appropriate tool for modeling resonant converters. Several analysis techniques for LLC converter have been developed. In the following subsection, these methods are discussed in detail.

1.2.1 Frequency- Domain Method

Approximation methods based on using few harmonics of the waveforms Fourier series gives closed form solutions but is highly inaccurate A popular approximation based technique which uses only the waveform's fundamental component of the Fourier series, known as Fundamental Harmonic Approximation (FHA) [26], [55-59] can be utilized for analysis of high *Q* LLC resonant tank circuits. A representation of the same is given in Figure 1-4. A high Q circuit implies good filtering characteristics. Hence, all current and voltage waveforms are assumed to be sinusoidal for a high *Q* loaded resonant tank. Consequently, the rectifier stage can be replaced by a resistor [26]. However, this method is not applicable when operating away from the series resonant frequency and gives poor results for gain calculation. Application on low-Q circuits leads to highly inaccurate results as well. An improved technique which considers harmonics of the source and load end by means of a continuous square wave applied across both input and output voltage end of series resonant tank was used to model a SRC [25]. This technique can be applied to a circuit of any *Q*-factor value but becomes difficult to implement when the secondary rectifier current goes to zero during LLC converter operation, making the output load-side reflected square wave discontinuous. Hence, frequency domain-based modeling methods aren't reliable for analyzing 3 or more element resonant converter with multiple modes of operation occurring within one switching cycle.

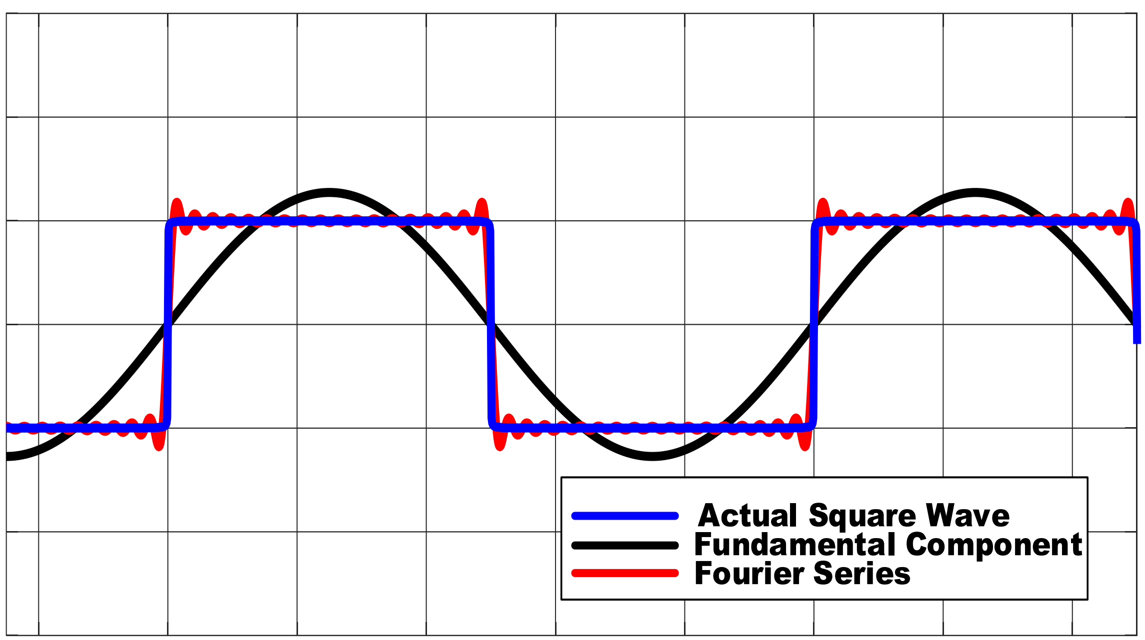


Figure 1-4: Approximation method for LLC converter analysis

1.2.2 Time Domain Method

Time domain methods requires prior knowledge of desired mode of operation and its equivalent circuit. Ordinary differential equations of equivalent circuit for each mode of operation are solved for one switching cycle, with the initial conditions as unknown parameters [61-70]. Equating initial and final states of the converter, the steady state response can be obtained. For converter operation with variable duty cycle, non-linear equations are formed which can only be solved using numerical techniques [71]. These methods are highly accurate but lack closed form solutions. Additionally, the Q value of LLC resonant tank doesn't have any influence over the accuracy of gain calculations.

1.3 Design of Low Q LLC Resonant Converters for Wide Input Range

Design focus for wide input range applications includes meeting gain requirement at all loading conditions while maintaining ZVS. Design characteristics of LLC resonant converter depend only on values of selected rated quality factor, Q and inductance ratio, K. For high output voltage, low output current micro-inverter application, it is necessary to choose such K and Q values that minimizes primary side circulating current as much as possible.

1.3.1 Significance of *Q* in Resonant Tank Design

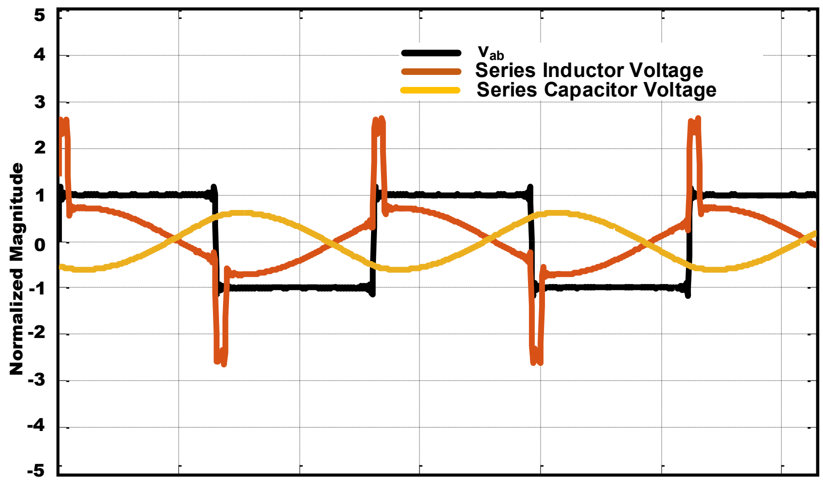
The Q factor of a resonant tank describes how under-damped the resonant circuit is; higher the Q factor the less damping there is. The Q factor is described as:

$$Q(\omega) = \omega \frac{\text{Maximum Energy Stored}}{\text{Power Loss}} \tag{1.1}$$

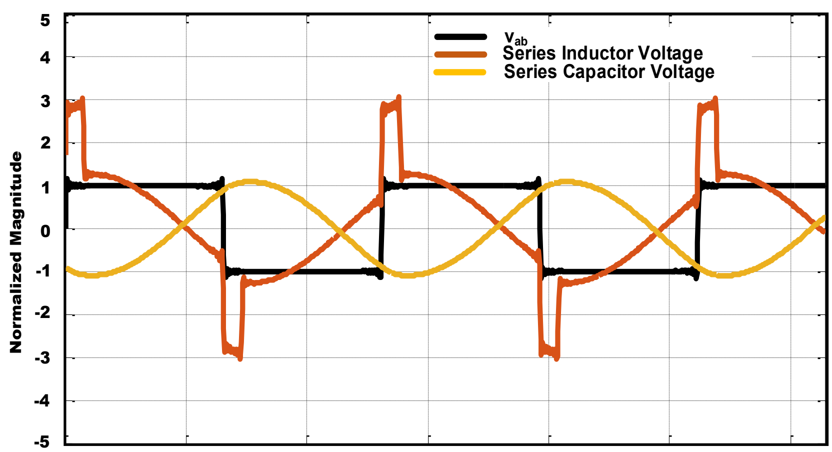
Since no energy is consumed by an ideal LLC resonant circuit, energy is circulated between the tank elements. Maximum energy stored in the resonant tank is either the maximum energy stored in the inductor or the maximum energy stored in the capacitor. The relevant equations are:

$$\text{Maximum energy stored} = LI_{Lrms}^2 = CV_{Crms}^2 \tag{1.2}$$

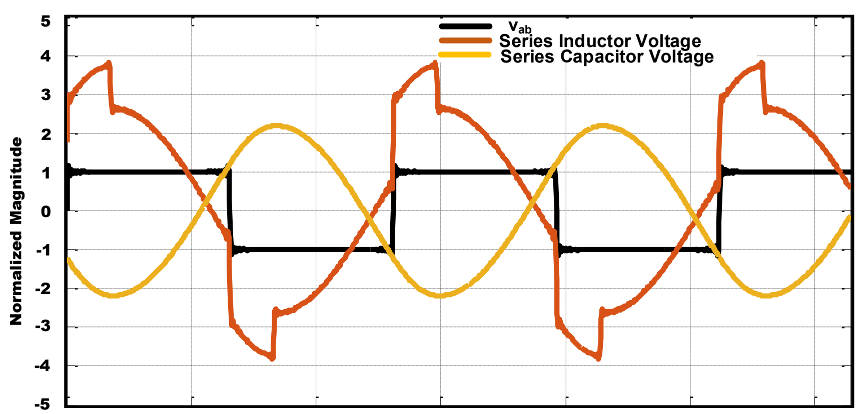
As implied by (1.2), higher the Q, higher would be the stress on the resonant tank components. This feature is depicted in Figure 1-5 for operation above resonance at various values of Q.



(a)



(b)



(c)

Figure 1-5: Component voltage stress above resonance for (a) *Q*=0.5, (b) *Q*=1, (c) *Q*=3

It is evident that a low-Q designed LLC resonant tank leads to lower component stress and eventually, smaller component size. Hence, for micro-inverter application which demands compact size and high-power density, it is extremely important that a low-Q resonant circuit is designed. However, analysis of low Q LLC resonant tank cannot be done reliably using the FHA method. It is because a high Q resonant tank implies better tank filtering characteristics than a low loaded Q tank. Under such a condition, the voltages and currents of the switching network with a high loaded Q LLC tank is nearly sinusoidal. The series inductor current and series capacitor voltage waveform can be assumed to be approximately sinusoidal which makes its analysis using FHA easier. Hence, it is necessary to use the suitable modeling method depending on Q value of resonant circuit.

1.3.2 Significance of *K* in Resonant Tank Design

Choice of inductor ratio K, which is the ratio of magnetizing inductance to resonant inductance, is crucial in deciding whether the converter can operate at very light load conditions for the given input voltage and load range. If K is too small, the magnetizing current relative to the primary side referred load current increases. This leads to a smaller switching frequency range and PRC like operating characteristics are demonstrated. However, since the magnetizing current represents the circulating current in the circuit, it generates high conduction losses in primary side MOSFETs and isolation transformer. If K is too large, conduction losses are drastically reduced but the required gain range cannot be achieved for light loading conditions within a narrow switching frequency range using variable frequency control. Hence, optimized efficiency relies heavily on choice of K value.

1.4 Control of Low-*Q* LLC Converter for Wide Input Range

Control of low-Q LLC converter for wide input range and load range applications is difficult since the dynamic characteristics vary significantly with any change in line/load condition. Control of resonant converters involves using different modulation schemes on inverter switching network such that a lagging current flows in the circuit for designed converter.

1.4.1 Variable Frequency Control

As mentioned in Section 1.1, varying the operating frequency of the converter with respect to the resonant frequency of series components L_s and C_s, output voltage of any dc-dc resonant converter can be controlled. The variable frequency modulation (FM) based LLC resonant converter requires relatively high Q that results in physically large size of the resonant circuit, increased magnetic losses and significantly higher circulating current for a wide range of load and input voltage variations [54-64]. Operation well above the resonant frequency results in significant de-rating of the converter. Large frequency variation inhibits optimization of magnetics, EMI filters and gate drive circuitry.

1.4.2 Fixed Frequency Control

Fixed frequency PWM based LLC resonant converters, like conventional phase shift modulation (PSM), asymmetrical pulse width modulation (APWM) and asymmetrical clamped mode (ACM) control reported in [72-77] demonstrate better ZVS range than variable frequency control for a wider input range. However, the proposed designs have high-Q and lose zero-voltage-switching (ZVS) at reduced load and high-end of the input voltage range, Burst mode control schemes are popular for improving extremely light load efficiency but suffers from filter design, noise problems and startup response after a burst mode cycle [78-83].

1.4.3 Hybrid Control

These techniques employ variable frequency control from medium to high power levels within narrow frequency range. At low power levels in order to minimize frequency variation above resonant frequency, it fixes maximum optimal switching frequency and switches to duty cycle control. Hybrid modulation techniques which combine FM and PWM technique [84] or variable frequency-based phase shift control [85], [86] have either been implemented on LLC resonant converter with a high Q design or requires wide switching frequency. Therefore, the need for a simple modulation technique which ensures ZVS and output voltage regulation for a wide input range from partial load to extremely light load for a low Q based LLC resonant converter within a narrow switching frequency range is required.

1.5 Thesis Objectives

An effort has been made in this research work to tackle the challenges related to LLC converter mentioned earlier in this section. The objectives of this thesis are as follows:

1) To present an accurate, time domain analysis method of LLC dc-dc resonant converter for micro-inverter applications (i.e., high output voltage, low output current) for low Q resonant circuit operating under variable frequency control. The analysis should be valid for any possible mode of operation both below and above resonance frequency without any restriction on operating conditions.
2) To propose a novel light load modulation technique for low-Q LLC converter based on simultaneous variation of both duty cycle and switching frequency to achieve ZVS at light load conditions for specified wide input voltage range (2:1 for micro-inverter applications).
3) To propose a time-domain based analytical method for the proposed light load modulation technique and solve the resultant transcendental equations using a numerical iterative technique. Resulting performance characteristic curves such as voltage gain, turn-off current as a function of duty cycle and normalized switching frequency are used to optimize operation at light load conditions. Mode boundary conditions were established to guarantee ZVS performance at light load conditions.
4) To establish a design procedure for selecting values of L_s, C_s and L_m, based on achieving optimal efficiency at rated load conditions and ZVS at light load conditions for low Q LLC converter throughout the desired input voltage range.
5) To verify the proposed time domain-based analysis of LLC converter operation under variable frequency control and proposed modulation technique using MATLAB to generate analytical curves.

6) To build an experimental prototype based on the design values and compare ZVS performance over specified input voltage range. Verification of ZVS operation at light load with conventional PSM, APWM and proposed modulation technique with proposed mathematical analysis is to be performed.

1.6 Thesis Outline

The layout for this thesis is as follows:

Chapter 2 deals with time domain modeling of a low- Q LLC resonant converter operating at, above or below resonant frequency under fixed duty cycle, variable frequency control. A brief description of the possible stages of operation in an LLC converter is given with emphasis on their suitability for the proposed application. Based on the qualitative analysis, time domain modeling of two dominant modes occurring below and above resonant frequency is performed. Due to wide switching frequency requirement of variable frequency control, two different modes of operation of asymmetrical duty cycle control are analyzed for obtaining additional gain below resonant frequency. A design example, representative of dc-dc stage of micro-inverter is studied. Simulation and experimental results below resonant frequency validate the proposed mathematical analysis.

Chapter 3 proposes a novel hybrid modulation technique for achieving ZVS at light load conditions within a narrow switching frequency range when operating above resonant frequency. It is based on the concept of modulating the full bridge output voltage waveform by varying duty cycle and switching frequency simultaneously. Modulating the waveform by changing the effective duty cycle changes the RMS value which allows for decreasing the switching frequency range required. Accurate time domain analysis using Newton Raphson technique has been performed to derive voltage gain, turn-off current expressions as a function of duty cycle D. Lack of literature dealing with maintaining ZVS of a low Q LLC converter for wide line and load variations while regulating output voltage simultaneously has been mentioned. Shortcomings of existing modulation schemes, such as variable frequency modulation, phase shift modulation and asymmetrical pulse-width modulation (APWM) have been briefly discussed and their ZVS performance demonstrated on an experimental prototype of 300W LLC converter.

Chapter 4 focuses on a design procedure of LLC resonant converter based on fulfilling low-Q and minimum primary resonant current form factor criterion. The design procedure is illustrated by a design flowchart which outlines the procedure to select minimum possible rated quality factor, Q_{rated} and inductor ratio, K of LLC converter. Design curves were generated to showcase the procedure for a specific design example of 300W LLC converter. Criterion for selecting high frequency isolation transformers, resonant capacitors and external resonant inductor is addressed since they play a crucial role in design optimization at light load conditions.

Chapter 5 concludes the present research work with key outcomes and suggests the possible areas of future research on this topic.

Chapter 2

Time- Domain Analysis of Low-*Q* Full Bridge LLC Converter

2.1 Introduction

Time domain modeling of LLC resonant converters provides an accurate method to analyze different modes of operation of LLC converter without any constraint on selected value of Q, operating frequency or variable duty cycle of modulated source voltage. Using different modulation schemes on LLC converter can lead to existence of any number of modes within one switching cycle. The biggest advantage that a time domain-based model has over frequency domain-based model is in solving as many numbers of modes which can co-exist during one switching cycle. Each mode can be represented by an equivalent circuit which can be analyzed using ordinary differential equations over half (symmetrical waveforms) or full switching cycle (asymmetrical waveforms). Each switching cycle can have various modes occurring in any given order, every one of which can be represented by an equivalent circuit under certain assumptions.

2.2 Equivalent Circuits of LLC Resonant Converter

There is a total of six equivalent circuits which can exist during one complete switching cycle of a full bridge LLC converter as shown in Figure 2-1. The following assumptions hold true for the equivalent circuits.

2.2.1 Assumptions

The following assumption are made in analysis of steady-state behaviour of the converter.

1) The semiconductor MOSFET switches along with the rectifier diodes and high frequency transformer are ideal.
2) MOSFET capacitances are negligible.
3) The output filter capacitor is large enough to keep the output voltage constant.
4) Dead time between switches is neglected.

Following quantities are defined for analysis purposes:

$$Z_0 = \sqrt{\frac{L_s}{C_s}} \qquad Z_1 = \sqrt{\frac{L_s + L_m}{C_s}} \qquad \omega_r = \frac{1}{\sqrt{L_s C_s}} \tag{2.1}$$

$$\omega_{r_1} = \frac{1}{\sqrt{(L_s + L_m) C_s}} \qquad \omega = \frac{\omega_{sw}}{\omega_r} \qquad K = \frac{L_m}{L_s}\,.$$

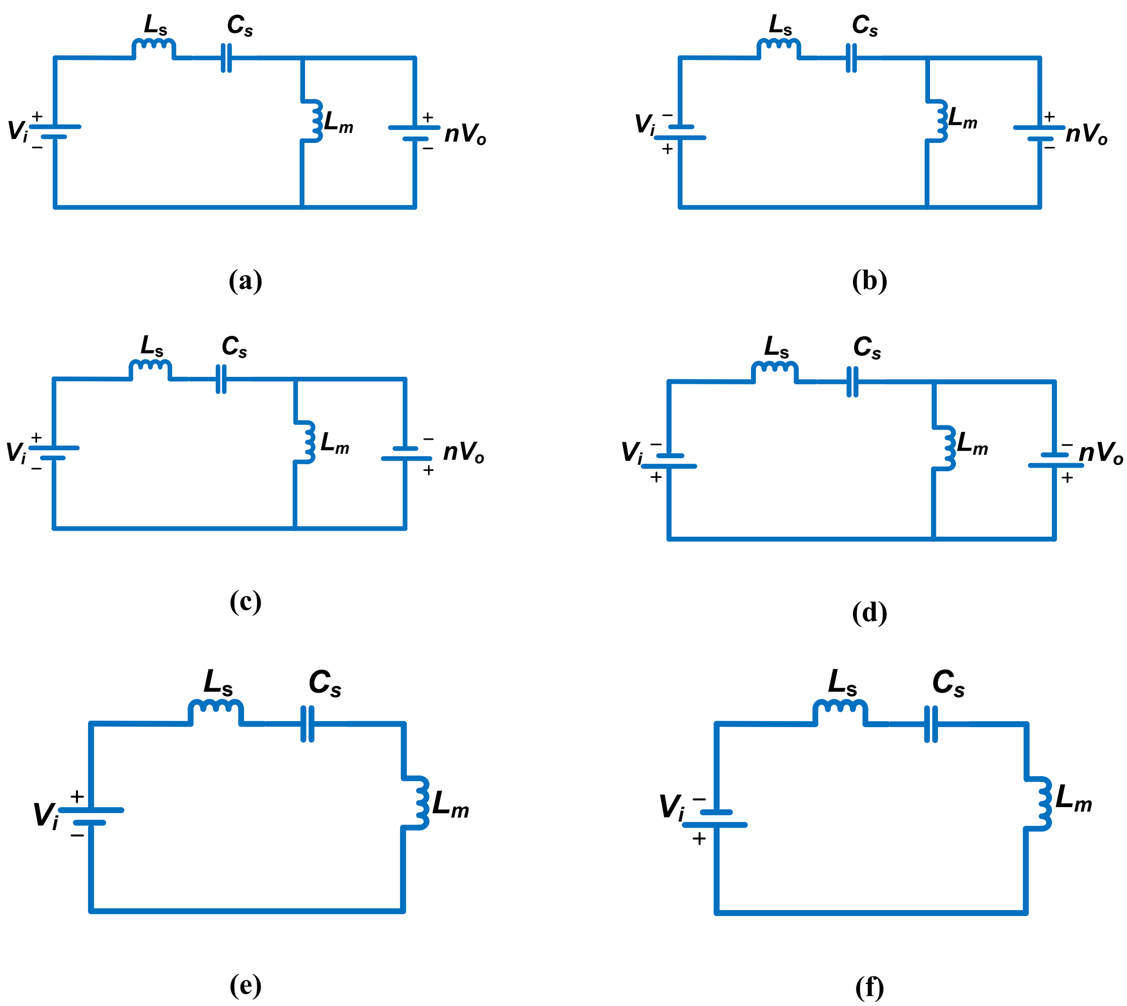


Figure 2-1: Equivalent circuits of six possible resonant stages of LLC converter

2.3 Operation Stages of LLC Converter

Depending upon chosen modulation technique, the number of equivalent circuits to be analyzed within a switching cycle can vary. Conventional variable frequency modulation uses a duty cycle of 0.5 for the LLC converter which leads to anti-half wave symmetry of voltages and currents in the resonant circuit. Under such conditions, the analysis can be restricted to analyzing the equivalent circuits over half switching cycle only. Based on whether L_m is clamped to either $\pm nV_o$ or starts resonating with series L_s and C_s and loses clamping, there can be 3 possible stages of operation within one half switching cycle under variable frequency control. Feature of these stages and the resulting equivalent circuits are given in the next sub-section.

2.3.1 Positively clamped power delivery stage (v_m=nV_o)

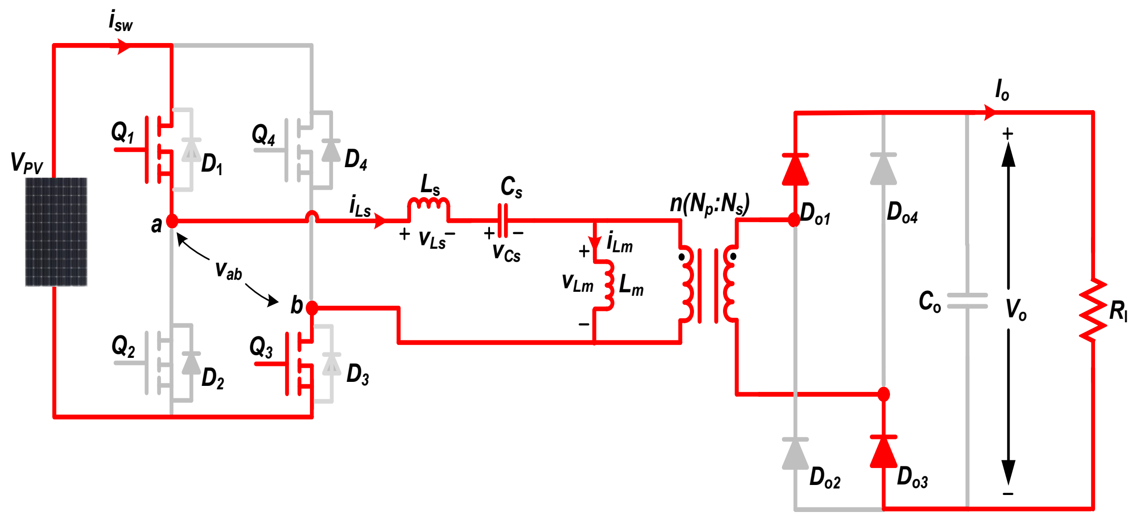


Figure 2-2: LLC circuit during power delivery positive clamped stage

Popularly known as stage P, L_s and C_s are in resonance and power is delivered via the conducting secondary side rectifier diodes D_{o1} and D_{o3} by positive output current, I_o. Resonant current, i_{Ls} lags the square wave voltage, v_{ab} thereby ensuring ZVS. Secondary rectifier current, I_o is continuous throughout this stage. As a result of this feature, magnetizing inductor L_m is clamped by the primary side reflected output voltage, nV_o, due to which i_{Lm} increases linearly. Figure 2-2 shows the different converter current with their direction during this stage.

2.3.2 Negatively clamped power delivery stage (v_m=-nV_o)

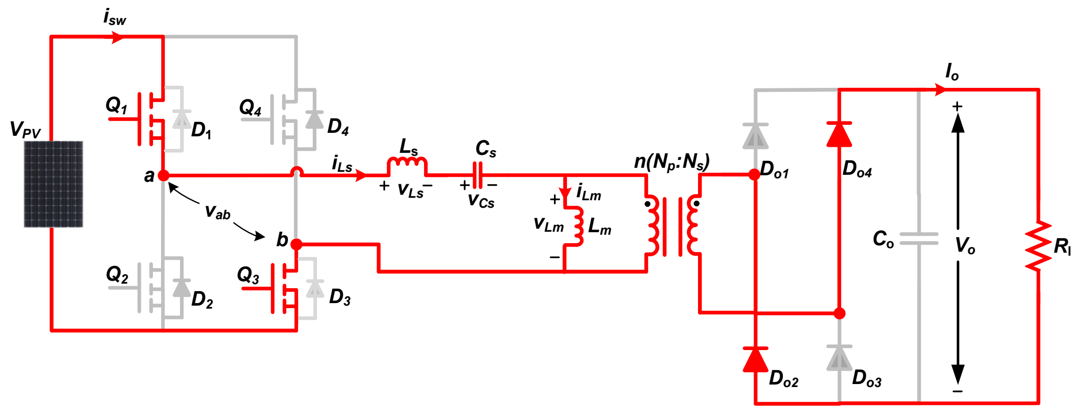


Figure 2-3: LLC circuit during power delivery negative clamped stage

This power delivery stage is similar to stage P described in Section 2.3.2. L_s and C_s resonate with each other with the only difference that current flows through D_{o2} and D_{o4} secondary diodes. This causes clamping of L_m by a negative output reflected voltage -$nV_{o.}$ instead of a positive output reflected output voltage, nV_o as shown in Figure 2-3. The magnetizing current decreases linearly during this power delivery stage, also known as stage N.

2.3.3 Freewheeling stage (-nV_o<v_m<nV_o)

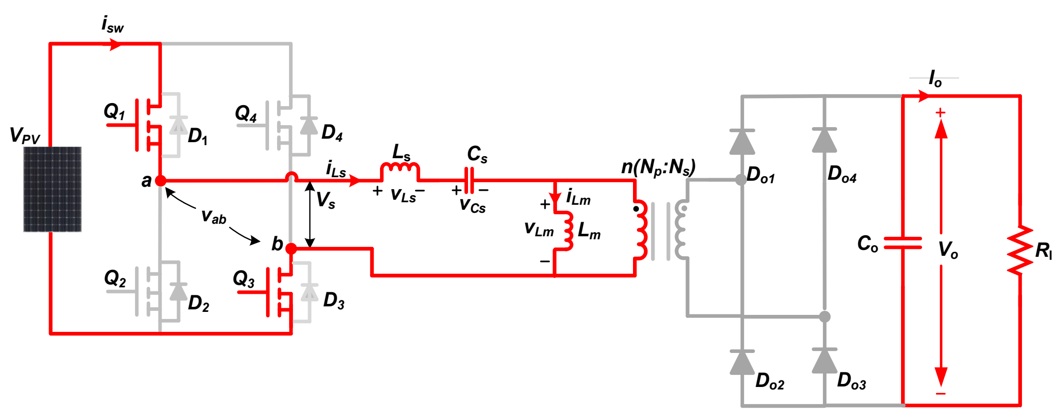


Figure 2-4: LLC circuit during freewheeling stage

Due to light loading conditions, the series resonant current, i_{Ls} becomes equal to transformer magnetizing current, which causes the secondary rectifier diodes to stop conducting. At this instant, magnetizing inductor L_m is no longer clamped by the reflected output voltage and starts resonating with L_s and C_s as shown in Figure 2-4.

Occurrence of any of these stages within one switching cycle can constitute various operating modes of variable frequency LLC converter. LLC converter can exhibit different modes depending on the loading conditions of the converter. N, NP, OP, NOP, OPO, PON, PO, PN, P are some of the popular modes that have been studied in existing literature. Since PO and NP mode gives voltage boost and buck property to the variable frequency LLC converter while maintaining ZVS, these two modes are most preferable for wide input range PV applications which require a variable DC gain. Hence, for the purpose of this study, time domain modeling of PO and NP mode has been performed in upcoming sections.

2.4 Analysis

This section presents the steady-state time domain analysis of variable frequency operated LLC resonant converter operating with a constant duty cycle of 0.5 as shown in Figure 2-5. MOSFET switches, Q_1-Q_4 produce a bipolar square wave, V_s with switching frequency, f_s with a duty cycle of 0.5 for each diagonal switch pair. The bipolar square wave drives the LLC resonant tank and produces ac currents and voltages in the resonant tank. High frequency isolation transformer with turns ratio, n (N_p:N_s) steps up to primary ac voltage to the desired output voltage. Secondary rectifier produces a dc output current, $I_{o.}$

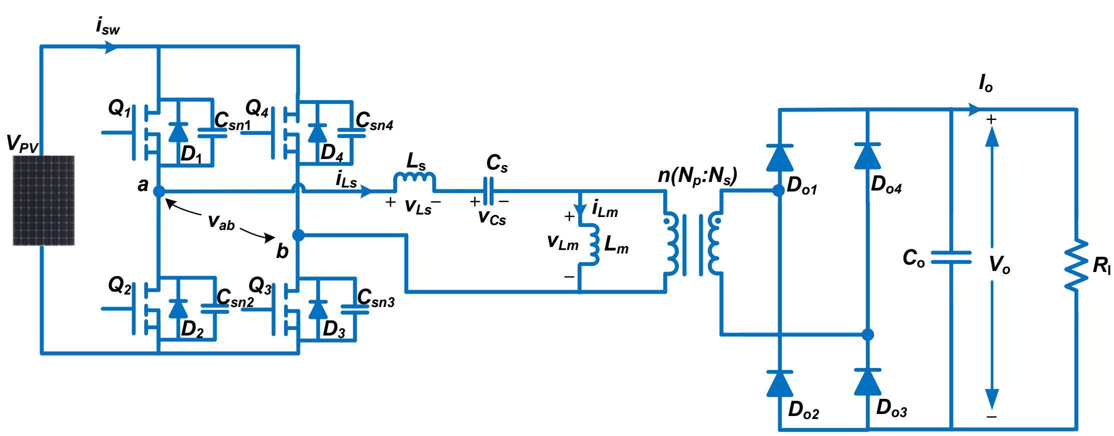


Figure 2-5: Typical full bridge LLC resonant converter

The following assumptions have been made for the purpose of proposed time domain analysis:

2.4.1 Assumptions

1) The semiconductor MOSFET switches along with the rectifier diodes and high frequency transformer are ideal.
2) MOSFET capacitances are negligible.
3) The output filter capacitor is large enough to keep the output voltage constant.
4) Dead time between switches is neglected.

2.4.2 Analysis for Operation Below Resonant Frequency using Variable Frequency Modulation

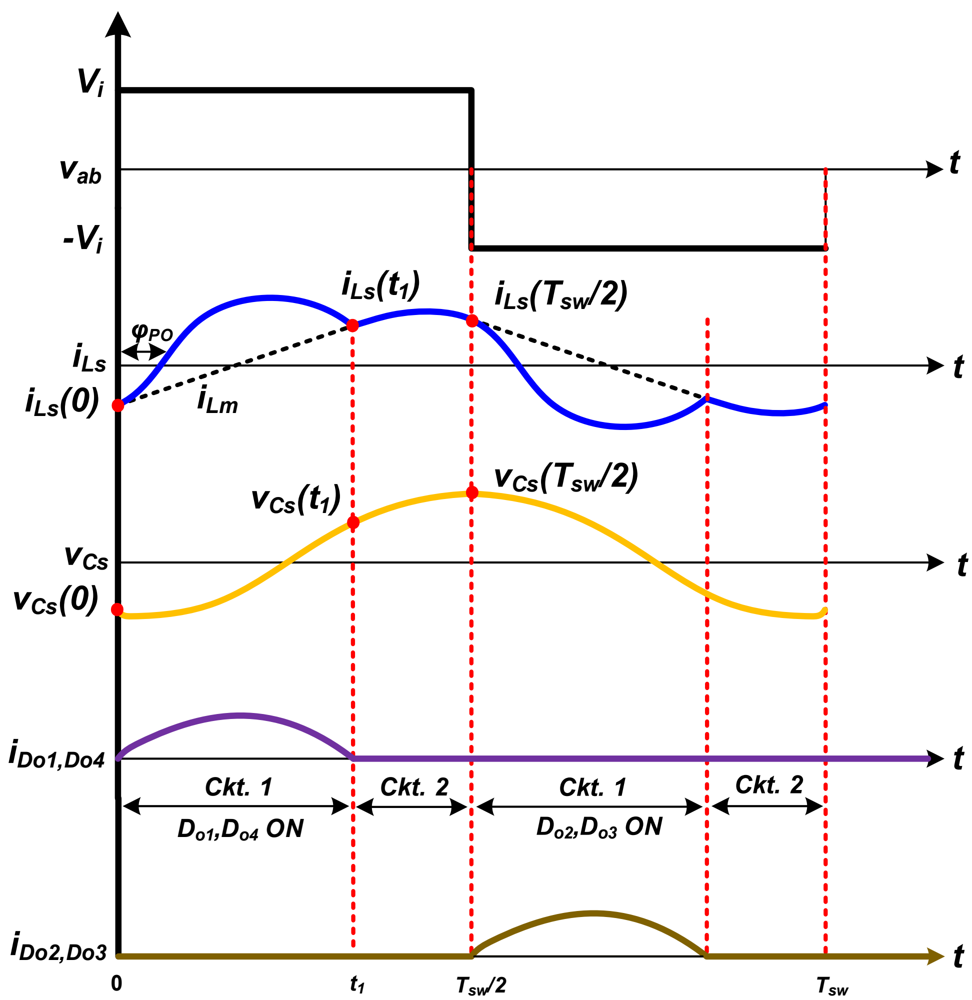


Figure 2-6: Steady state waveforms of LLC converter in PO mode

This mode exhibits stage P and stage O during each half switching cycle. It starts with stage P and culminates with stage O and exhibits characteristic boost mode. Figure 2-6 shows the key operational waveforms of LLC resonant converter operating below resonant frequency under variable frequency control. The variable switching frequency controlled full bridge provides a square wave input which drives the resonant tank. Output rectifier diodes conduct for time duration t_1 as shown in Figure 2-6. t_d represents the rectifier diode to switch conduction ratio, φ_{PO} is ZVS angle, which is a measure of true ZVS. Differential equations for each mode using KVL/KCL have been formulated below.

Power Delivery Interval [0-t_1]

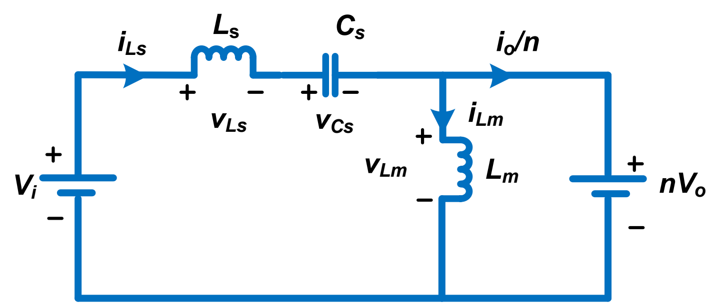


Figure 2-7: Equivalent LLC circuit (*Ckt. 1*) during energy transfer period (0-t_1)

Figure 2-7 shows the equivalent LLC circuit operating in PO mode during power delivery interval. The resonant tank current, i_{Ls} and magnetizing current, i_{Lm} have the same initial value. Since the series inductor, L_s and capacitor, C_s are resonating, and the magnetizing inductance is clamped to the output voltage, the currents show different wave shapes and diverge. Magnetizing current, i_{Lm} rises linearly under the effect of clamped output voltage, $+nV_o$. i_{Ls} originates from a negative initial value, it passes zero crossing point and eventually becomes equal to i_{Lm} at t_1. By KCL, it is evident that remaining current is supplied to the load through the output rectifier. This interval lasts till $t_1=t_dT_{sw}/2$, where t_d is the rectifier diode to switch conduction ratio. The resulting steady state dynamics can be represented through the following differential equations.

$$
\begin{aligned}
&V_i - nV_o = L_s \frac{di_{Ls}(t)}{dt} + v_{Cs}(t) \\
&i_{Ls}(t) = C_s \frac{dv_{Cs}(t)}{dt} \\
&i_{Lm}(t) = \frac{1}{L_m} \int_0^t nV_o dt + i_{Lm}(0)
\end{aligned}
\tag{2.1}
$$

Solving (2.1),

$$i_{Ls}(t) = i_{Ls}(0)cos(\omega_r t) + \left[\frac{V_i - nV_o - v_{Cs}(0)}{Z_0} \right] sin(\omega_r t) \tag{2.2}$$

$$i_{Lm}(t) = \frac{nV_o}{L_m} t + i_{Lm}(0) \tag{2.3}$$

$$v_{Cs}(t) = Z_0 i_{Ls}(0) sin(\omega_r t) + v_{Cs}(0) cos(\omega_r t) + \left[V_i - nV_o \right] \left[1 - cos(\omega_r t) \right] \tag{2.4}$$

$$\frac{i_o(t)}{n} = i_{Ls}(t) - i_{Lm}(t) \tag{2.5}$$

This solution is valid only if $0 \leq t_1 < T_{sw}/2$ and $t_o=0$

Freewheeling Interval [$t_1 - T_{sw}/2$]

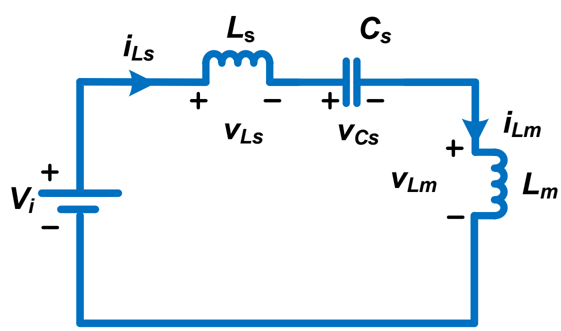


Figure 2-8: Equivalent LLC circuit (*Ckt. 2*) during freewheeling period (t_1-$T_{sw/2}$)

When magnetizing current, i_{Lm} and series resonant current, i_{Ls} become equal at the end of the first interval, the diodes of the output rectifier are reverse biased, and no energy is transferred to the output. L_m is no longer clamped to the output voltage and starts resonating with the series L_s and C_s in series, thereby allowing the series resonant current to flow through L_m. The resonant frequency changes from ω_r to ω_{r1}. The differential equations representative of the equivalent circuit during this period shown in Figure 2-8 is:

$$
\begin{aligned}
V_i &= L_s \frac{di_{Ls}(t)}{dt} + v_{Cs}(t) + v_{Lm}(t) \\
i_{Ls}(t) &= C_s \frac{dv_{Cs}(t)}{dt} \\
v_{Lm}(t) &= L_m \frac{di_{Lm}(t)}{dt}
\end{aligned} \tag{2.6}
$$

Solution to (2.6) is given by (2.7), (2.8) and (2.9)

$$
i_{Ls}(t) = i_{Ls}(t_1)cos\left[\omega_{r1}(t-t_1)\right] - \frac{v_{Cs}(t_1)}{Z_1} sin\left[\omega_{r1}(t-t_1)\right] + \frac{V_i}{Z_1} sin\left[\omega_{r1}(t-t_1)\right] \tag{2.7}
$$

$$
v_{Cs}(t) = Z_1 i_{Ls}(t_1) sin\left[\omega_{r1}(t-t_1)\right] + v_{Cs}(t_1)cos[\omega_{r1}(t-t_1)] + V_i\left[1-cos(\omega_{r1}(t-t_1))\right] \tag{2.8}
$$

$$
i_{Ls}(t) = i_{Lm}(t) \tag{2.9}
$$

This solution is valid only if $t_1<t\leq T_{sw}/2$, where t_1 equals $t_d T_{sw}/2$.

Since energy transfer takes place only during $0<t\leq t_1$, where t_1 is dependent on rectifier diode to switch conduction ratio, t_d. Hence, t_d cannot be taken as a constant for calculating the voltage gain, initial current or voltage values for LLC resonant converter as it varies with the loading conditions. Mathematical expressions cannot be closed form since t_d is an unknown quantity. Hence, for accurate time domain analysis, voltage gain, initial values of resonant current and capacitor voltage will be shown to be an implicit function of t_d, $Q(R_l)$ and ω, instead of being an explicit function of only ω.

Average output current can be written as:

$$
\begin{aligned}
I_o &= \frac{2}{T_{sw}} \int_0^{t_1} \left(i_{Ls}(t) - i_{Lm}(t)\right) dt \\
&= \frac{2}{T_{sw}\omega_r}\left[i_{Ls}(0) sin(\omega_r t_1) + \left[\frac{V_i - nV_o - v_{Cs}(0)}{Z_0}\right]\left(1-cos\left(\omega_r t_1\right)\right) - \frac{nV_o\omega_r^2}{\omega_r L_m}\frac{t_1^2}{2} - i_{Ls}(0)\omega_r t_1 \right]
\end{aligned} \tag{2.10}
$$

Since the steady-state waveforms have anti-half wave symmetry, the analysis can be performed over half switching cycle with the following conditions:

$$\begin{aligned} &i_{Ls}(0)=i_{Lm}(0)=-i_{Ls}(T_{sw}/2)\\ &v_{Cs}(0)=-v_{Cs}(T_{sw}/2)\\ &i_{Ls}(t_1)=i_{Lm}(t_1) \end{aligned} \tag{2.11}$$

Simplifying the resulting set of equations for evaluating the voltage gain, initial series resonant current, $i_{Ls}(0)$ and initial resonant capacitor voltage, $v_{Cs}(0)$ closed form expressions are found. The resulting expressions has the form of:

$$i_{Ls}(0)=-V_i\alpha_1+\frac{GV_i}{n}\beta_1 \tag{2.12}$$

$$v_{Cs}(0)=-V_i\alpha_2+\frac{GV_i}{n}\beta_2 \tag{2.13}$$

where,

$$\begin{aligned} \alpha_1&=\frac{2(Z_1\sin x\cos y+Z_0\cos x\sin y)}{L}\\ \beta_1&=\frac{Z_1\sin x\cos y+Z_0\cos x\sin y+Z_1\sin x-Z_0\sin y}{L} \end{aligned} \tag{2.14}$$

$$\begin{aligned} \alpha_2&=\frac{\sin x\sin y(Z_1^2-Z_0^2)}{L}\\ \beta_2&=\frac{Z_1^2\sin x\sin y-Z_1Z_0(1-\cos x-\cos y)}{L} \end{aligned} \tag{2.15}$$

$$L=2Z_1Z_0+2Z_1Z_0\cos x\cos y-\sin x\sin y(Z_1^2+Z_0^2) \tag{2.16}$$

$$\begin{aligned} x&=\frac{\omega_r}{\omega_{sw}}t_d\pi\\ y&=\frac{\omega_{r_1}}{\omega_{sw}}(1-t_d)\pi \end{aligned} \tag{2.17}$$

Finally, voltage gain, G for DCM boost mode operation can be derived using the average output current expression (2.10) and has the form of:

$$G_{PO}=\frac{nV_o}{V_i}=\frac{\left[\sin(x)+\alpha_1Z_0(1-\cos(x))+\alpha_2\sin(x)\right]}{[t_d\frac{T_{sw}}{2}\frac{Z_0}{L_m}+\sin(x)+\beta_2\sin(x)+\beta_1Z_0(1-\cos(x))]}=f(t_d,\omega) \tag{2.18}$$

which is a function of both ω and t_d.

$$G = f(t_d, \omega) \tag{2.19}$$

Now, in DCM mode of operation,

$$t_d = f(Q, \omega) \tag{2.20}$$

As opposed to

$$G = f(Q, \omega) \tag{2.21}$$

which means that when transformer secondary current is in continuous conduction mode, G is an explicit function of Q (load) but when transformer secondary current goes into DCM mode, G becomes an implicit function of Q.

Substituting initial value of resonant current in (2.12), $i_{Ls}(0)$ to zero and $Z_1=(1+K)Z_0$ in (2.14)-(2.16), peak gain for PO mode can be calculated as:

$$G_{peak} = \frac{2}{1 + \dfrac{\sqrt{1+K}\left(\sin x - \sin y\right)}{\left(1+\sqrt{1+K}\right)\sin\left(x+y\right)}} \tag{1.1}$$

Negative $i_{Ls}(0)$ is the turn off current as shown in (2.11) due to anti-half wave symmetry of the steady state waveforms. Substituting (2.17) in (2.10), and simplifying the resulting equation, average output current has the form,

$$I_o = \left(A_1 \sin(x) + B_1(1-\cos(x)) - \frac{GV_i x^2}{2n\omega_r L_m} - i_{Ls}(0)x \right)\frac{\omega}{\pi} \tag{2.22}$$

where

$$\begin{aligned} A_1 &= i_{Ls}(0) \\ B_1 &= \frac{\left[V_i - \dfrac{GV_i}{n} - v_{Cs}(0) \right]}{Z_0} \end{aligned} \tag{2.23}$$

Expression for output voltage can be used to calculate equivalent ac load,

$$V_o = I_o R_l \tag{2.24}$$

$$R_l = \frac{V_o}{\left(A_1 sin(x) + B_1(1-cos(x)) - \frac{GV_i x^2}{2n\omega_r L_m} - i_{Ls}(0)x\right)\frac{\omega}{\pi}} \tag{2.25}$$

Noticeably, R_l is the expression for equivalent load for DCM operation and is dependent on diode to switch conduction ratio, t_d and ω as compared to the conventional expression given by $R_{ac}=8n^2/\pi^2 R_l$ which is valid only for CCM operation above resonance. Figure 2-9 shows the dependence of ratio t_d with respect to value of load resistance (R_l) at K=6. Depending on the output voltage and power, R_l can be calculated and plotted against t_d for various values of ω. Value of t_d is plugged in the remaining expressions with unknown x and y variables.

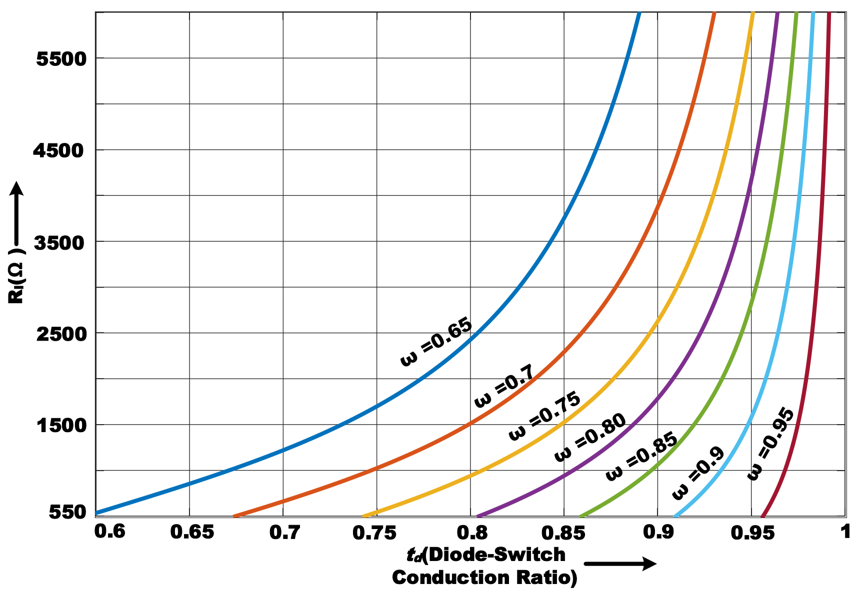


Figure 2-9: Diode-Switch Conduction Ratio vs Load at *K*=6.

Phase difference between the input square wave voltage, v_{ab} and primary resonant current, i_{Ls} is evaluated using the expression

$$\varphi_{ZVS} = \frac{\pi}{\omega} tan^{-1}\left(-\frac{A_1}{B_1}\right) \tag{2.26}$$

RMS value of resonant tank inductor current is given by

$$i_{RMS\_PO} = \sqrt{\frac{\pi}{\omega}\left(I_{RMS\_P} + I_{RMS\_O}\sqrt{1+K}\right)} \tag{2.27}$$

where,

$$I_{RMS\_P} = \left(A_1^2 + B_1^2\right)\left[\frac{x}{2} - \frac{1}{4}\left(sin\left[2\left(x + tan^{-1}\left(\frac{A_1}{B_1}\right)\right)\right] + sin\left(2\,tan^{-1}\left(\frac{A_1}{B_1}\right)\right)\right)\right] \text{ and}$$

$$I_{RMS\_O} = \left(A_2^2 + B_2^2\right)\left[\frac{y}{2} - \frac{1}{4}\left(sin\left[2\left(y + tan^{-1}\left(\frac{A_2}{B_2}\right)\right)\right] + sin\left(2\,tan^{-1}\left(\frac{A_2}{B_2}\right)\right)\right)\right]$$

is the respective RMS current for mode P and mode O. Variables for mode O are defined as:

$$\begin{aligned} A_2 &= i_{Ls}(t_1) \\ B_2 &= \frac{V_i - v_{Cs}(t_1)}{Z_1} \end{aligned} \tag{2.28}$$

The proposed time domain analysis evaluates the performance of LLC converter without any approximations. It is known that variable frequency LLC converter operating in this mode offers attractive features such as ZVS of primary MOSFETs for a certain frequency range below resonant frequency, ZCS of secondary rectifier diodes below resonant frequency and boost operation. However, during O stage, the converter does not transfer energy to the secondary side. For a low-line voltage, high line current application, such as PV micro-converters, this feature causes high circulating current losses, thereby severely degrading power efficiency. Hence, there is always a trade-off between losses incurred due to primary circulating current and losses avoided due to reduced reverse recovery loss in rectifier diodes.

2.4.3 Analysis for Operation Below Resonant Frequency using Asymmetrical Duty Cycle Modulation

Variable frequency control of LLC converter below resonant frequency gives voltage gain greater than unity. Depending on chosen K and Q value of LLC resonant tank, wide variation below resonant frequency causes difficulty in optimizing board magnetics. It was observed in [88], that applying asymmetrical duty cycle control below resonant frequency can provide additional voltage boost at selected switching frequency, thereby requiring lower switching frequency variation below resonant frequency. However, the analysis performed would be valid only for high Q resonant circuits. In this section, operation of LLC resonant converter operating below resonant frequency under asymmetrical duty cycle control has been analyzed using the same principles developed in Section 2.4.2.

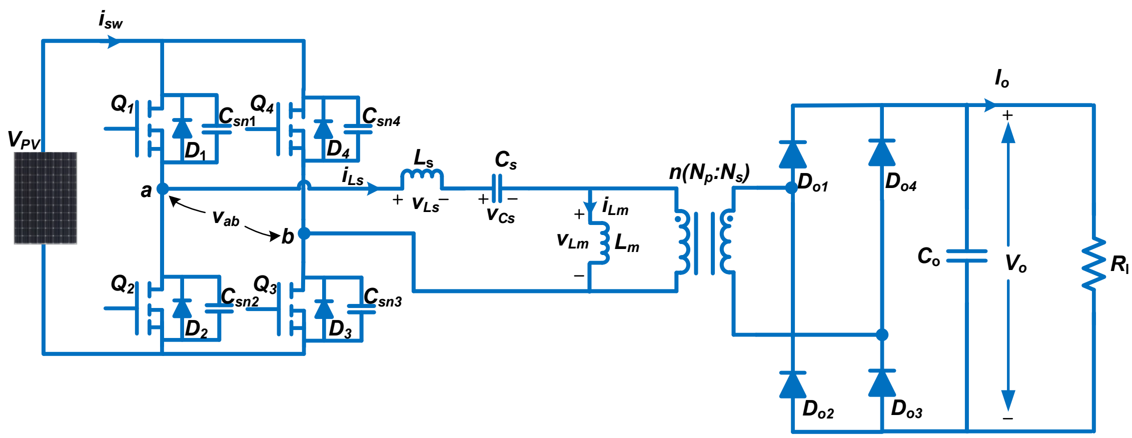


Figure 2-10: LLC converter for APWM operation below resonant frequency

2.4.3.1 Assumptions

In addition to the assumptions mentioned in Section 2.4.1, it is assumed that $Q_{1,3}$ pair is switched ON with duty cycle D, whereas $Q_{2,4}$ pair is switched ON with duty cycle $1\text{-}D$ at switching frequency, f_{sw} as shown in Figure 2-10. Power transfer duration over a switching cycle via secondary diode rectifier (D_{o1}-D_{o4}) is taken as t_p.

2.4.3.2 Mode Analysis

Two modes of operation are possible depending upon the time duration of power conduction of secondary diodes, t_p {$t_p \leq DT_s$ [Mode A] and $t_p > DT_s$ [Mode B]} when operating LLC converter using asymmetrical duty cycle control below resonant frequency. Both modes are explained in detail below.

Mode A [$t_p < DT_s$]

Figure 2-11 shows the principal steady state waveforms occurring during Mode A operation under APWM operated LLC resonant converter. This stage occurs when the secondary side rectifier is turned OFF before switch pair Q_1, Q_3 is turned off at DT_s leading to the operating condition $t_p < DT_s$.

Operating under this mode leads to ZCS of rectifier diodes and ZVS of primary MOSFETs but also causes higher circulating energy losses within the system. Different stages of operation are examined in the next sub-section.

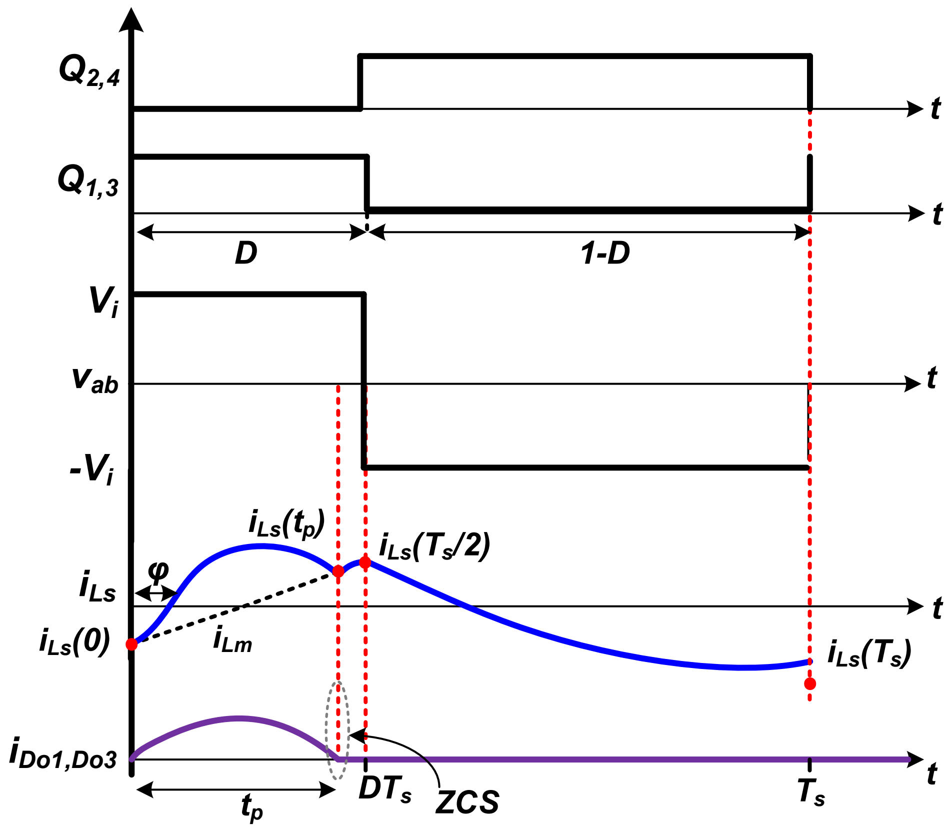


Figure 2-11: Key steady state waveforms during Mode A

Stage 1 [0, t_p]

Figure 2-12 presents the equivalent circuit arising due to operation in mode A during time interval 0-t_p.

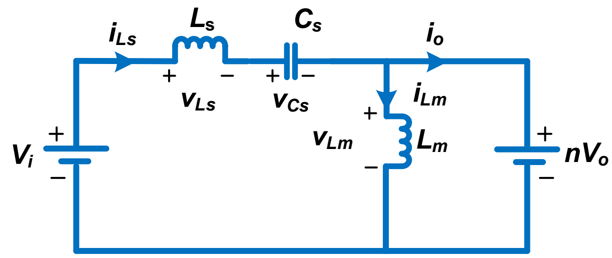


Figure 2-12: Mode A equivalent LLC circuit during stage 1 operation

Switches $Q_{1,3}$ are turned ON at t=0 and kept ON until time DT_s. Magnetizing inductor L_m is clamped to the output voltage whereas rectifier diode current is equal to the algebraic sum of series resonant current, i_{Ls} and magnetizing current, i_{Lm}. This stage ends when diode rectifier current becomes discontinuous at time t_p. Currents i_{Ls}, i_{Lm} and resonant capacitor voltage v_{Cs} can be written as:

$$
\begin{aligned}
& i_{Ls}(t) = i_{Ls}(0)\cos(\omega_r t) - \frac{v_{Cs}(0)}{Z_0}\sin(\omega_r t) + \left[\frac{V_i - nV_o}{Z_0}\right]\sin(\omega_r t) \\
& i_{Lm}(t) = \frac{nV_o}{L_m}t + i_{Lm}(0) \\
& v_{Cs}(t) = Z_0 i_{Ls}(0)\sin(\omega_r t) + v_{Cs}(0)\cos(\omega_r t_1) + [V_i - nV_o][1 - \cos(\omega_r t)]
\end{aligned}
\tag{2.29}
$$

Stage 2 [t_p, DT_s]

This stage begins when L_m is no longer clamped to the output voltage and the rectifier diodes are turned OFF as shown by the equivalent circuit in Figure 2-13.

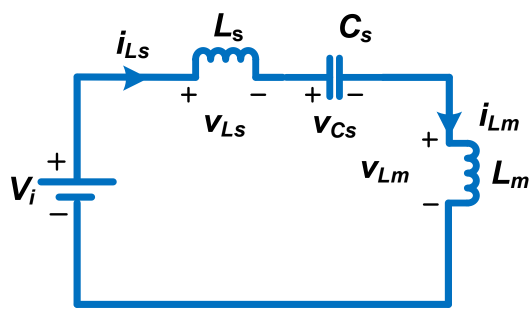


Figure 2-13: Mode A equivalent LLC circuit during stage 2 operation

Current i_{Ls} becomes equal to i_{Lm} at t=t_p. This mode usually occurs when load is increased with the switching frequency held constant. The steady-state expressions during this stage are written as:

$$
\begin{aligned}
& i_{Ls}(t) = i_{Ls}(t_p)\cos\left[\omega_{r_1}(t - t_p)\right] - \frac{v_{Cs}(t_1)}{Z_1}\sin\left[\omega_{r_1}(t - t_p)\right] + \frac{V_i}{Z_1}\sin\left[\omega_{r_1}(t - t_p)\right] \\
& v_{Cs}(t) = Z_1 i_{Ls}(t_p)\sin\left[\omega_{r_1}(t - t_p)\right] + v_{Cs}(t_p)\cos[\omega_{r_1}(t - t_p)] + V_i\left[1 - \cos(\omega_{r_1}(t - t_p))\right]
\end{aligned}
\tag{2.30}
$$

This stage ends when switches Q_1 and Q_3 are turned OFF at time t=DT_s

Stage 3 [DT_s, T_s]

Switch Q_2 and Q_4 are turned ON at time t= DT_s. Since voltage across magnetizing inductor L_m is less than output voltage, the secondary rectifier diodes remain turned OFF ensuring no power delivery during this stage. Equivalent circuit representing this stage dynamics is shown in Figure 2-14.

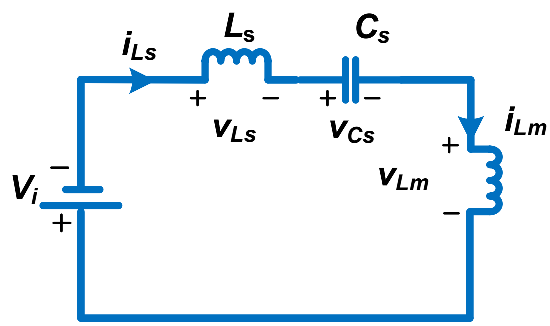


Figure 2-14: Mode A equivalent LLC circuit during stage 3 operation

The resulting equations to represent this stage are:

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(DT_s)cos\left[\omega_{r_1}(t-DT_s)\right]-\frac{v_{Cs}(DT_s)}{Z_1}sin\left[\omega_{r_1}(t-DT_s)\right]-\frac{V_i}{Z_1}sin\left[\omega_{r_1}(t-DT_s)\right] \\ v_{Cs}(t) &= Z_1 i_{Ls}(DT_s)sin\left[\omega_{r_1}(t-DT_s)\right]-v_{Cs}(DT_s)cos[\omega_{r_1}(t-DT_s)]-V_i\left[1-cos(\omega_{r_1}(t-DT_s))\right] \end{aligned} \tag{2.31}$$

Mode B [t_p>DT_s]

Figure 2-15 shows the principal steady state waveforms occurring during Mode B operation under APWM operated LLC resonant converter.

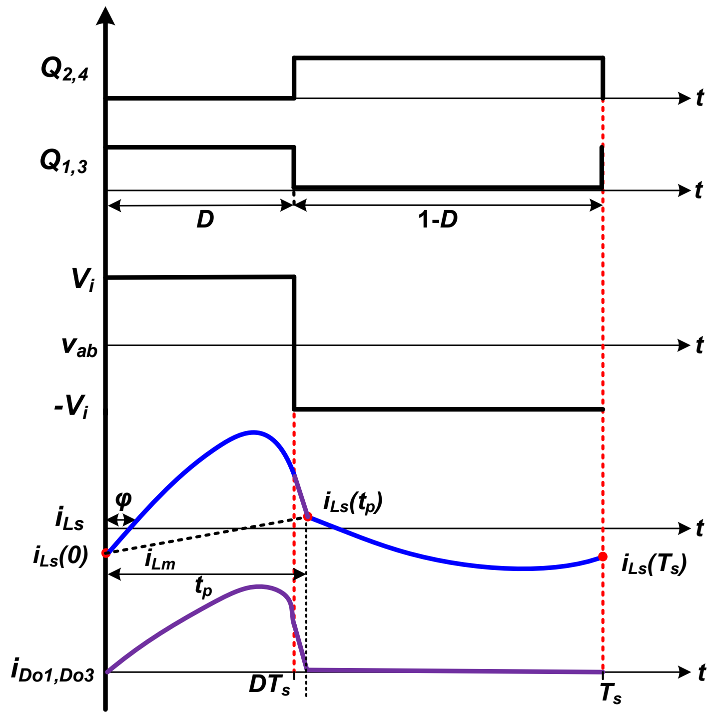


Figure 2-15: Key steady state waveforms during Mode B

This stage occurs when the secondary side rectifier is turned OFF after switch pair Q_1, Q_3 is turned off at DT_s leading to the operating condition $t_p>DT_s$. Since power transfer takes place during the complete ON time period, DT_s of switch pair, Mode B has lower circulating energy losses compared to Mode A. However, Mode B incurs higher turn-off currents than Mode A. Lossless snubber capacitors placed across MOSFET can reduce turn-off switching losses.

Stage 1 [0, DT_s]

This stage is similar to stage 1 in Mode A as shown in Figure 2-16.

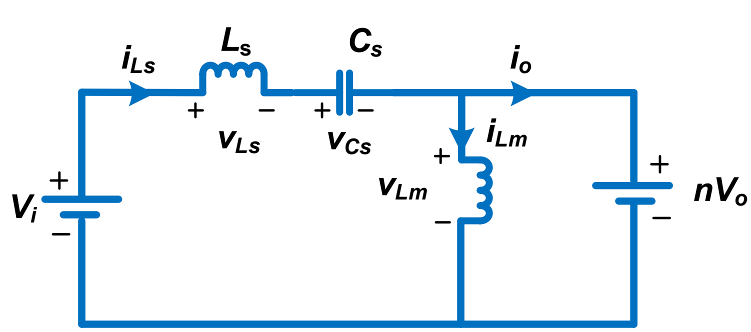


Figure 2-16: Mode B equivalent LLC circuit during stage 1 operation

The resultant steady-state dynamics can be represented by

$$
\begin{aligned}
& i_{Ls}(t)=i_{Ls}(0)\cos(\omega_r t)-\frac{v_{Cs}(0)}{Z_0}\sin(\omega_r t)+\left[\frac{V_i-nV_o}{Z_0}\right]\sin(\omega_r t) \\
& i_{Lm}(t)=\frac{nV_o}{L_m}t+i_{Lm}(0) \\
& v_{Cs}(t)=Z_0 i_{Ls}(0)\sin(\omega_r t)+v_{Cs}(0)\cos(\omega_r t_1)+\left[V_i-nV_o\right]\left[1-\cos(\omega_r t)\right]
\end{aligned}
\tag{1.2}
$$

Stage 2 [DT_s, t_p]

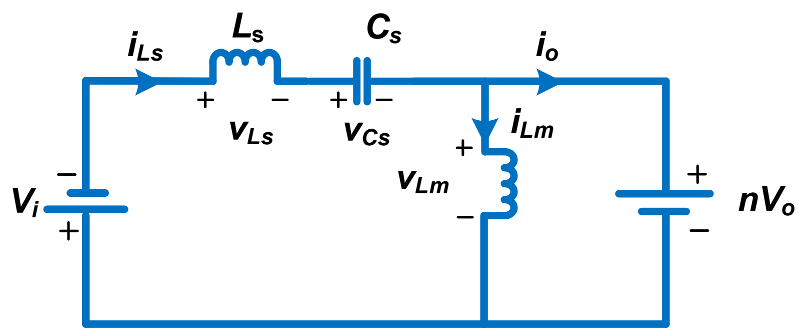


Figure 2-17: Mode B equivalent LLC circuit during stage 2 operation

At time instant DT_s, the switches Q_1 and Q_3 are turned off but the rectifier diodes still conduct current till time instant t_p. The expressions representing the dynamics of this stage can be derived from equivalent circuit in Figure. 2-17:

$$
\begin{aligned}
& i_{Ls}(t)=i_{Ls}(DT_s)\cos(\omega_r(t-DT_s))-\frac{v_{Cs}(DT_s)}{Z_0}\sin(\omega_r(t-DT_s))-\left[\frac{V_i+{}^{V_o}\!/\!_{n}}{Z_0}\right]\sin(\omega_r(t-DT_s)) \\
& i_{Lm}(t)=\frac{{}^{V_o}\!/\!_{n}}{L_m}(t-DT_s)+i_{Lm}(DT_s) \\
& v_{Cs}(t)=Z_0 i_{Ls}(DT_s)\sin(\omega_r(t-DT_s))+v_{Cs}(DT_s)\cos(\omega_r(t-DT_s))-\left[V_i+\frac{V_o}{n}\right]\left[1-\cos(\omega_r(t-DT_s))\right]
\end{aligned}
\tag{2.32}
$$

Stage 3 [t_p, T_s]

This stage is similar to stage 3 in Mode A as shown in Figure 2-18.

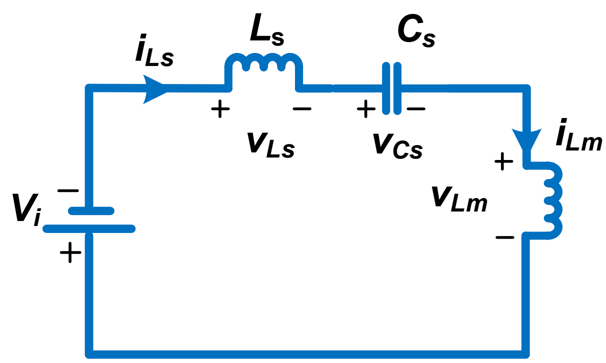


Figure 2-18: Mode B equivalent LLC circuit during stage 3 operation

The steady state dynamics can be represented by the following equations.

$$\begin{aligned} i_{Ls}(t) &= i_{Ls}(t_p)cos\left[\omega_{r_1}(t-t_p)\right] - \frac{v_{Cs}(t_p)}{Z_1}sin\left[\omega_{r_1}(t-t_p)\right] - \frac{V_i}{Z_1}sin\left[\omega_{r_1}(t-t_p)\right] \\ v_{Cs}(t) &= Z_1 i_{Ls}(t_p)sin\left[\omega_{r_1}(t-t_p)\right] - v_{Cs}(t_p)cos[\omega_{r_1}(t-t_p)] - V_i\left[1-cos(\omega_{r_1}(t-t_p))\right] \end{aligned} \tag{1.3}$$

In order to find the unknown quantities at time t_p and DT_s, the initial resonant inductor current, i_{Ls} (0), initial capacitor voltage, $v_{Cs}(0)$ needs to be derived. Applying the following set of conditions.

$$\begin{aligned} & i_{Ls}(0) = i_{Lm}(0) = i_{Ls}(T_{sw}) \\ & v_{Cs}(0) = v_{Cs}(T_{sw}); i_{Ls}(t_1) = i_{Lm}(t_1) \end{aligned} \tag{2.33}$$

Solving (2.33), we obtain the expressions for initial resonant inductor current, $i_{Ls}(0)$, initial capacitor voltage, $v_{Cs}(0)$, expressed in (2.34) and (2.35) respectively.

$$i_{Ls}(0) = \frac{V_i\alpha_1 - nGV_i\beta_1}{L} \tag{2.34}$$

$$v_{Cs}(0) = \frac{V_i\alpha_2 - nGV_i\beta_2}{L} \tag{2.35}$$

Voltage gain due to operation in APWM under resonant frequency and average output current is given in (2.36) and (2.37) respectively.

$$G_{APWM}(t_p,\omega,D) = \frac{V_o}{nV_i} = \frac{\left[\frac{\alpha_1}{L}\left(cos(x)-1\right) + \frac{sin(x)}{Z_0}\left(1-\frac{\alpha_2}{L}\right)\right]}{\left[\frac{x}{\omega_r L_m} + \frac{\beta_1}{L}\left(cos(x)-1\right) + \frac{sin(x)}{Z_0}\left(1-\frac{\beta_2}{L}\right)\right]} \tag{2.36}$$

$$I_o = \frac{2}{T_{sw}}\int_0^{t_p}\left(i_{Ls}(t)-i_{Lm}(t)\right)dt \Rightarrow \frac{2}{T_{sw}\omega_r}\left[i_{Ls}(0)sin(\omega_r t_p)+\left[\frac{V_i-\frac{V_o}{n}-v_{Cs}(0)}{Z_0}\right]\left(1-cos\left(\omega_r t_p\right)\right)-\frac{V_o\omega_r^2}{n\omega_r L_m}\frac{t_p^2}{2}-i_{Ls}(0)\omega_r t_p\right] \tag{2.37}$$

ZVS angle, φ can be written as

$$\varphi_{ZVS} = \frac{2\pi}{\omega}tan^{-1}\left[-\frac{i_{Ls}(0)}{\left(\frac{V_i-nGV_i-v_{Cs}(0)}{Z_0}\right)}\right] \tag{2.38}$$

α_1, β_1 α_2, β_2 variables used for expressing the various quantities above have been defined for Mode A and Mode B respectively in Appendix A.

2.4.4 Analysis for Operation Above Resonant Frequency using Variable Frequency Modulation

This mode consists of stages N and P occurring within half switching cycle. NP mode occurs when operating frequency of LLC resonant tank is above series resonant frequency, due to which a lagging p.f. is obtained. Magnetizing inductance, L_m remains clamped to the reflected square wave output voltage. This mode imparts buck property to the LLC converter.

Figure 2-19 shows the principal steady state waveforms arising during NP mode. t_1 is the duration of N stage, ϕ_{NP} is the true ZVS angle. Differential equations for each mode using KVL/KCL have been formulated.

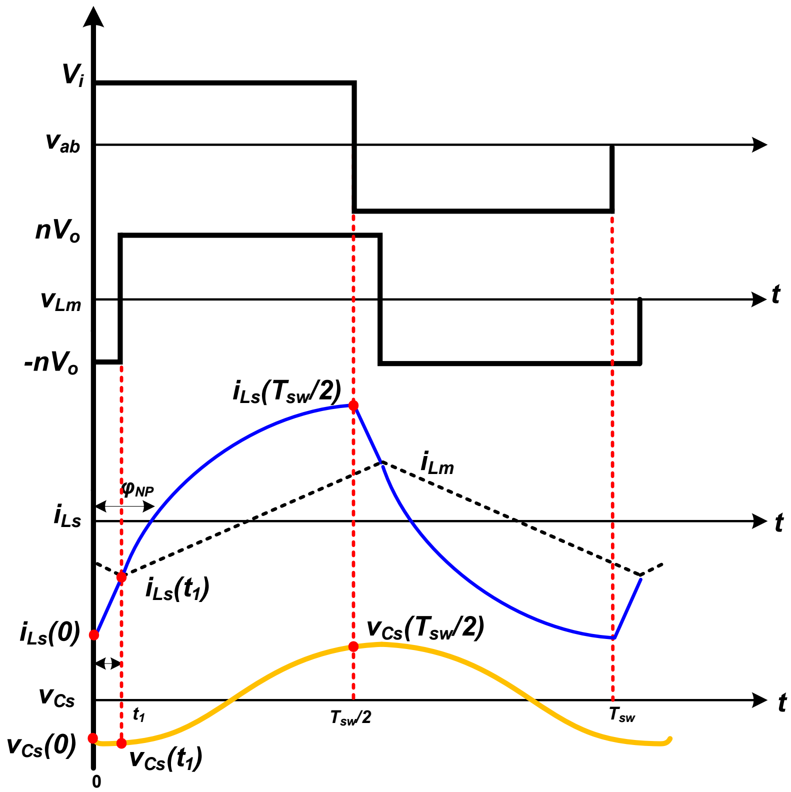


Figure 2-19: Steady state waveforms of LLC converter in NP mode

Power Delivery Interval 1 [$0 - t_1$]

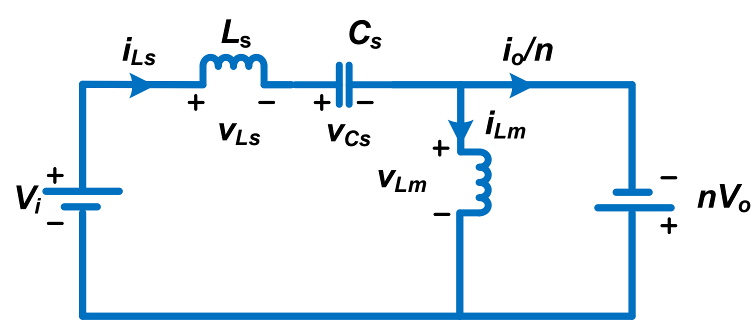


Figure 2-20: Equivalent LLC circuit in NP mode during energy transfer period (0-t_1)

Absolute magnitude of resonant current, i_{Ls} is greater than i_{Lm} at the end of half switching cycle. Like P mode, the magnetizing current is linear shaped due to constant magnitude of reflected bipolar square wave output voltage applied on the magnetizing inductor, L_m. Resonant current, i_{Ls} becomes equal to i_{Lm} at the end of this interval at time instant $t=t_1$. Applying KCL/KVL to the equivalent LLC circuit shown in Figure 2-20, the following differential equations are obtained:

$$
\begin{aligned}
V_i + nV_o &= L_s \frac{di_{Ls}(t)}{dt} + v_{Cs}(t) \\
i_{Ls}(t) &= C_s \frac{dv_{Cs}(t)}{dt} \\
i_{Lm}(t) &= \frac{1}{L_m} \int_0^t -nV_o dt + i_{Lm}(0)
\end{aligned}
\tag{2.39}
$$

Solving (2.39) gives

$$i_{Ls}(t) = i_{Ls}(0)cos(\omega_r t) + \left[\frac{V_i + nV_o - v_{Cs}(0)}{Z_0}\right] sin(\omega_r t) \tag{2.40}$$

$$i_{Lm}(t) = -\frac{nV_o}{L_m} t + i_{Lm}(0) \tag{2.41}$$

$$v_{Cs}(t) = Z_0 i_{Ls}(0) sin(\omega_r t) + v_{Cs}(0) cos(\omega_r t) + \left[V_i + nV_o\right]\left[1 - cos(\omega_r t)\right] \tag{2.42}$$

Power Delivery Interval 2 [$t_1 - T_{sw}/2$]

Figure 2-21 exhibits the equivalent LLC circuit in NP mode during energy transfer period. Resonant tank current, i_{Ls} and magnetizing current, i_{Lm} are equal at the beginning of this interval. Magnetizing current, i_{Lm} starts rising linearly under the effect of positive reflected square wave output voltage, $+nV_o$.

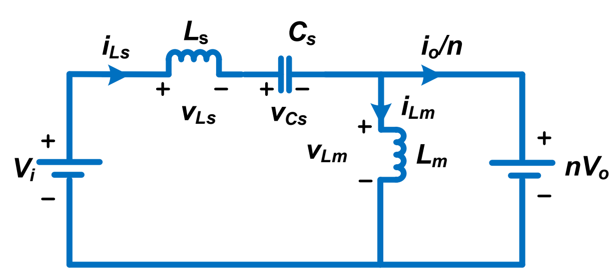


Figure 2-21: Equivalent LLC circuit in NP mode during energy transfer period (t_1-$T_{sw/2}$)

This interval lasts till $t=T_{sw}/2$. The final solution for current and voltage is given as

$$i_{Ls}(t) = i_{Ls}(t_1)cos(\omega_r(t-t_1)) + \left[\frac{V_i - nV_o - v_{Cs}(t_1)}{Z_0}\right] sin(\omega_r(t-t_1)) \tag{2.43}$$

$$i_{Lm}(t) = \frac{nV_o}{L_m}(t-t_1) + i_{Lm}(t_1) \tag{2.44}$$

$$v_{Cs}(t) = Z_0 i_{Ls}(t_1) sin(\omega_r(t-t_1)) + v_{Cs}(t_1) cos(\omega_r(t-t_1)) + \left[V_i - nV_o\right]\left[1 - cos(\omega_r(t-t_1))\right] \tag{2.45}$$

Since the steady-state waveforms have anti-half wave symmetry, the analysis can be performed over half switching cycle with the following conditions:

$$\begin{aligned} &i_{Ls}(0) = -i_{Ls}(T_{sw}/2) \\ &v_{Cs}(0) = -v_{Cs}(T_{sw}/2) \\ &i_{Ls}(t_1) = i_{Lm}(t_1) \end{aligned} \tag{2.46}$$

Simplifying the resulting set of equations for evaluating the voltage gain, initial series resonant current, $i_{Ls}\,(0)$ and resonant capacitor voltage, $v_{Cs}\,(0)$ closed form expressions are found. The resulting expressions has the form of:

$$i_{Ls}(0) = -V_i\alpha_1 - \frac{GV_i}{n}\beta_1 \tag{2.47}$$

$$v_{C_s}(0) = -\frac{GV_i}{n}\beta_2 \tag{2.48}$$

where,

$$\alpha_1 = \frac{\sin x}{1+\cos x} \tag{2.49}$$

$$\beta_1 = \frac{\sin y - \sin(x-y)}{1+\cos x} \tag{2.50}$$

$$\beta_2 = \left(\frac{\cos(x-y)+\cos y}{1+\cos x}\right) - 1 \tag{2.51}$$

and

$$\begin{aligned} &x = \left(\frac{\omega_r}{\omega_s}\pi\right) \\ &y = t_1\frac{\omega_r}{\omega_s}\pi \end{aligned} \tag{2.52}$$

Output voltage gain for NP mode is given by

$$G_{NP} = \frac{-\alpha_1 b + c}{a\beta_2 + \beta_1 b - d} \tag{2.53}$$

where,

$$a = -2\sin y + \sin x \tag{2.54}$$

$$b = -\cos x - 1 + 2\cos y \tag{2.55}$$

$$c = 2\sin(y) - \sin(x) \tag{2.56}$$

$$d = 2\sin y - \sin x + 2\sin(x - y) \tag{2.57}$$

This mode ensures a lagging p.f. for frequency variation above resonant frequency, thereby achieving ZVS of primary MOSFETs. Since, magnetizing inductor, L_m is clamped, L_s and C_s act as a voltage divider. This mode causes reverse recovery turn-off losses of rectifier diodes which is a major concern at high switching frequency. However, this mode guarantees highest efficiency during converter operation as the secondary rectifier current is always continuous, ensuring energy is always transferred to the load with minimum circulating energy losses.

The major issue with operating in this mode above resonance that a wide switching frequency variation above resonance frequency is required for voltage regulation at light loads for low Q designed LLC resonant tank. This requirement leads to degraded power efficiency, magnetic core losses and EMI interference. Hence, it is necessary to develop and analyze a modulation scheme which can enhance light load efficiency when operating above the nominal voltage.

2.5 Design Example

In order to validate the mathematical analysis of operation below resonant frequency using variable frequency control and asymmetrical duty cycle control proposed in this chapter, a design example will be described and evaluated in this section.

2.5.1 Converter Specifications

An LLC resonant converter will be designed to represent the dc-dc stage of PV micro-inverters. The specifications are tabulated in Table 2-1. Wide input range requirement for the converter demands LLC converter operation under variable frequency control. ZVS performance of asymmetrical duty cycle control below resonant frequency will be evaluated to reduce the required switching frequency variation.

Table 2-1:LLC resonant micro-inverter specifications

Parameter	Value
Input Voltage Range	20-40V (V_{in_nom}=30V)
Output Voltage (V_{out}):	380V
Output Power (P_{out}):	300W
Switching Frequency (f_{sw})	150kHz

2.5.2 Converter Design

The design process has been thoroughly described in Chapter 4. Resonant parameters of K=6 and Q_{rated}=0.34 are selected for the design which achieves optimal trade-off between voltage regulation capability and light load ZVS performance within a narrow switching frequency range. Operation at series resonant frequency for nominal input voltage conditions guarantees the most efficient performance of LLC converter. Hence, the desired switching frequency is taken to be the resonant frequency for the designed LLC resonant converter. For a resonant frequency of 150kHz, these parameters translate to resonant component values: L_s=1μH, C_s=1.1μF and L_m=6μH with turns ratio, n=14. Therefore, for the given input range, converter operates below resonant frequency when input voltage varies between 20-30V. Operation below resonant frequency provides additional voltage gain due to LLC resonant tank. Verification of proposed mathematical analysis and resulting LLC converter design via MATLAB generated analytical waveforms will be performed at two possible worst-case operating conditions. These analytical results will be compared with experimental results obtained on a laboratory converter prototype. If the converter operates with ZVS at these two operating conditions, then ZVS is guaranteed at all other possible operating conditions.

2.5.3 Analytical Result

Table 2-2 lists the ideal parameters of LLC converter used for proposed mathematical analysis in MATLAB platform.

Table 2-2: Analytical parameters for LLC converter

Parameters	Value
Input Voltage Range	20-40 V
Output Voltage (V_o)	380 V
Output Power (P_o)	300 W
Resonant Frequency (f_r)	150 kHz
Switching Frequency Range	91.2-180 kHz
Series Resonant Inductor (L_s)	1µH
Series Resonant Capacitor (C_s)	1.1µF
Magnetizing Inductor (L_m)	6µH
Transformer Turns Ratio (n)	1:14

2.5.3.1 At Minimum Input Voltage, Rated Load Condition Below Resonant Frequency

2.5.3.1.1 Using Frequency Modulation

Frequency modulation varies the effective impedance offered by the LLC resonant tank by varying the operating frequency. First worst-case condition for verifying ZVS performance is at minimum input voltage (V_{in_min}=20V) and rated load condition (P_o=300W). From proposed analysis in Section 2.4.2, it is estimated that a switching frequency of 91.2kHz is required for voltage gain equal to 1.4 while operating under PO mode. Figure 2-22. shows the analytical steady state operating waveforms of input square voltage, v_{ab} with series resonant current, i_{Ls} and magnetizing current, i_{Lm} generated using MATLAB® 2018b. As calculated in Chapter 4, the converter is operating in PO mode with ZVS of all primary MOSFETs. Analytical values were a close match with simulated design on PSIM®. Although, the required gain was achieved under variable frequency control for selected K and Q values, the switching frequency variation required is too wide. It is necessary to optimize the ZVS performance by narrowing the operating frequency using APWM.

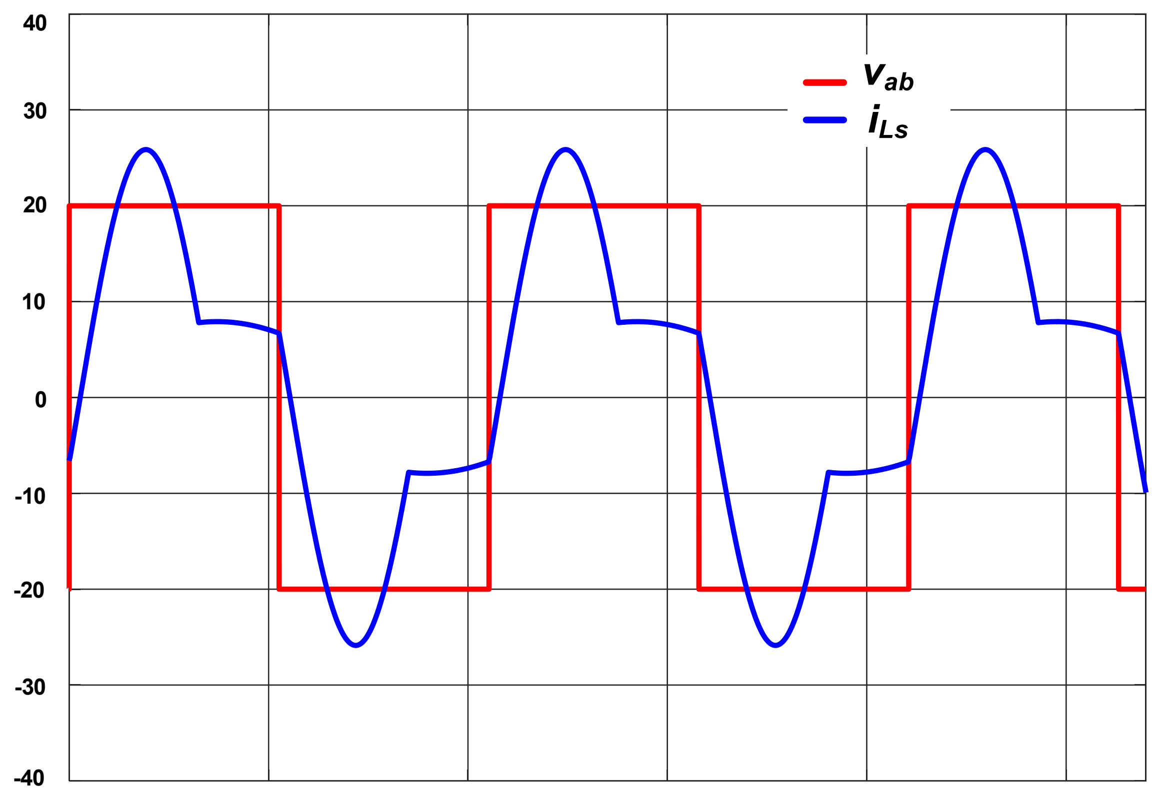


Figure 2-22: MATLAB generated steady state LLC converter operation at V_{in_min}=20V, rated load(300W) under variable frequency control (ω=0.6)

2.5.3.1.2 Using Asymmetrical Pulse-Width Modulation

Asymmetrical duty cycle control allows Required switching frequency variation below resonant frequency for achieving necessary voltage gain of 1.4 can be further narrowed by using asymmetrical duty cycle control at a pre-defined minimum switching frequency. Section 2.4.3 discussed proposed time-domain analysis for asymmetrical duty cycle control below resonance. Using the APWM voltage gain expression (2.36), it is evaluated that switching to asymmetrical duty cycle variation at f_{sw}=114kHz (ω=0.75) would provide voltage regulation at V_o=380V at D=0.3. Figure 2-23 shows the resultant steady state waveforms of primary resonant current and input ac voltage generated using MATLAB®. Primary MOSFETs exhibited zero turn-on losses while achieving the required output voltage. The only drawback of using APWM is high peak currents which leads to high losses at rated load conditions. Analytical values were a close match with simulated design on PSIM®.

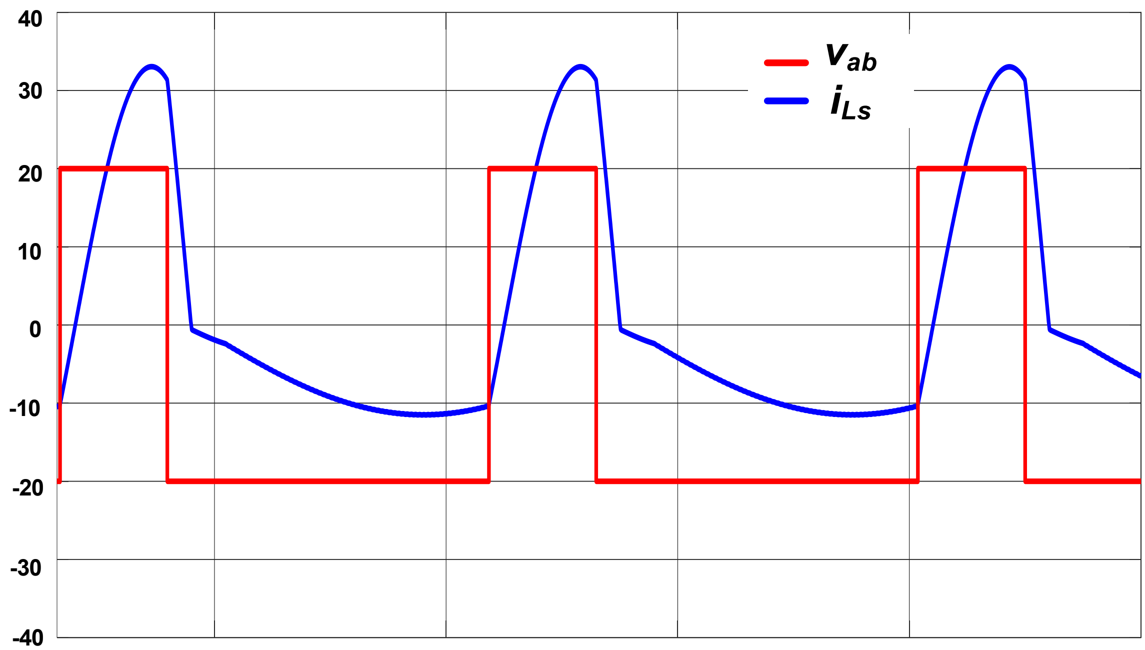


Figure 2-23: MATLAB generated steady state LLC converter operation at V_{in_min}=20V, rated load(300W) under APWM (ω=0.75).

2.5.3.2 At Nominal Input Voltage, Rated Load Condition

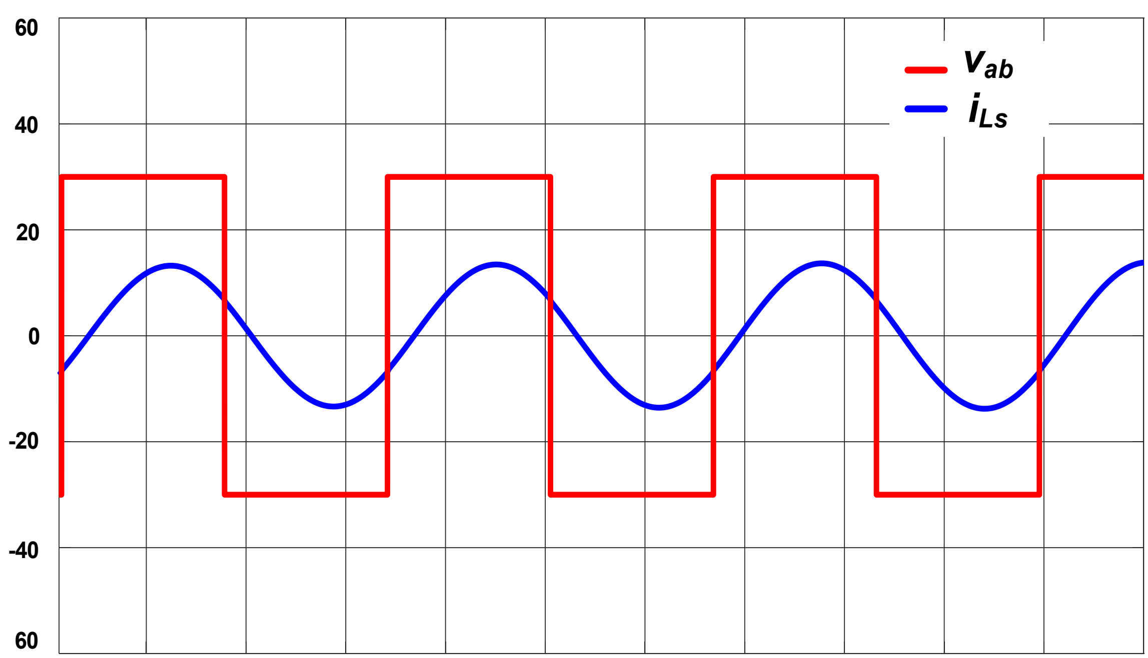


Figure 2-24: MATLAB generated steady state LLC converter operation at V_{in_min}=20V, rated load(300W) under variable frequency control (ω=1).

2.5.4 Experimental Results

Table 2-3 lists the experimentally measured parameters of the developed prototype. The desired design parameters are constrained by the size of the capacitor bank, due to which the designed value comes out to C_s=0.99µF. Total resonant inductance value was increased to 1.1µH to keep the resonant frequency, f_r=152.8kHz which is close to the simulated resonant frequency of 150kHz. Measured transformer turns are also measured to be 1:13.

Table 2-3: LLC experimental prototype parameters

Parameters	Measured Value
Input Voltage Range	20-40 V
Output Voltage (V_o)	380 ±10V
Output Power (P_o)	300 W
Resonant Frequency (f_r)	152.8 kHz
Switching Frequency Range	90-180 kHz
External Series Resonant Inductor (L_s)	0.89µH
Leakage Inductor	0.21 µH
Series Resonant Capacitor (C_s)	0.99 µF
Rated Quality Factor	0.37
Magnetizing Inductor (L_m)	6 µH
Transformer Turns	1:13
DC Bus Capacitor	20 µF
Snubber Capacitance (C_{sn})	1 nF (each MOSFET)

The converter is designed to operate over an input voltage range of 20-40V (2:1 input voltage range) with a primary motive of maintaining good efficiency throughout the whole line/load operating range. Operation below resonant frequency was performed on the experimental prototype using variable frequency control and APWM. From analytical results, lower bound on the switching frequency for operation between 20-30V input voltage is 91.2kHz (ω= 0.6) and 114kHz (ω=0.75) using variable frequency control and APWM respectively.

2.5.4.1 At Minimum Input Voltage, Rated Load Condition Below Resonant Frequency

2.5.4.1.1 Using Frequency Modulation

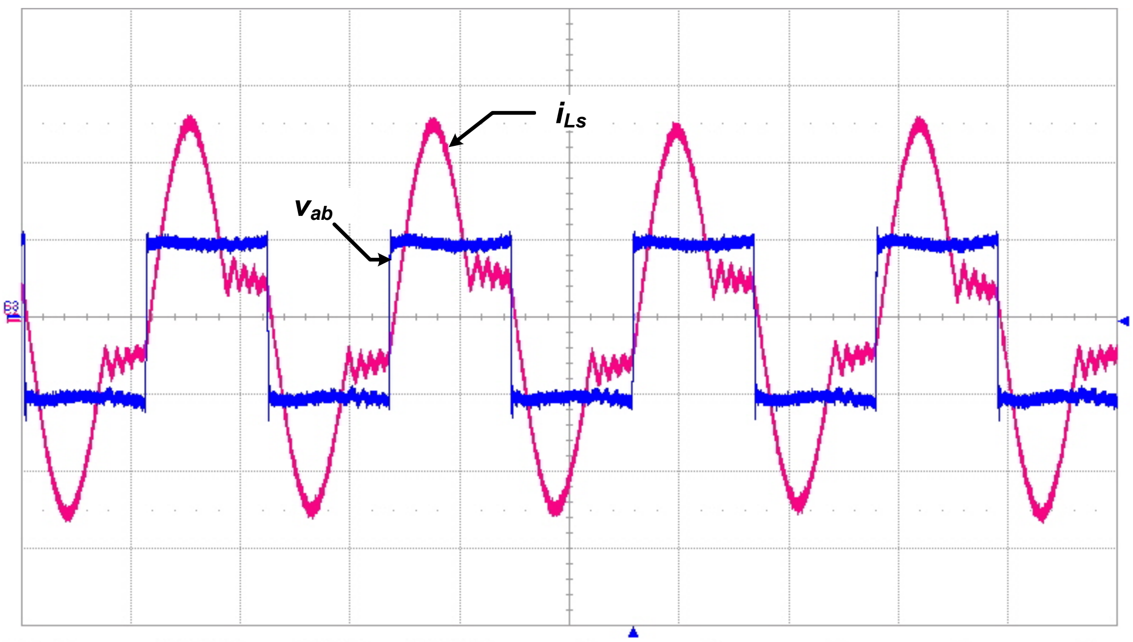


Figure 2-25: Experimental waveforms of input voltage and resonant current operating below resonant frequency at V_{in_min}=20V, Rated Load (300W) using Frequency Modulation at f_{sw}=90kHz (ω=0.59) [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 5µs/div]

Experimental waveforms for operation at worst case condition of V_{in_min}=20V, P_o=300W using variable frequency modulation scheme is shown in Figure 2-25. The proposed design achieves ZVS of primary MOSFETs at f_{sw}=90kHz (ω=0.59), which is extremely close to the analytically calculated value of f_{sw}=91.2kHz (ω=0.60).

2.5.4.2 Using Asymmetrical Pulse Width Modulation

ω_{min} and D were selected based on minimum-turn-off current for required gain value calculations done using proposed analysis in Section 2.4.3. Figure 2-26 shows experimental waveforms for APWM based LLC converter at f_{sw}=114kHz (ω=0.75), D=0.25 which demonstrates ZVS for a

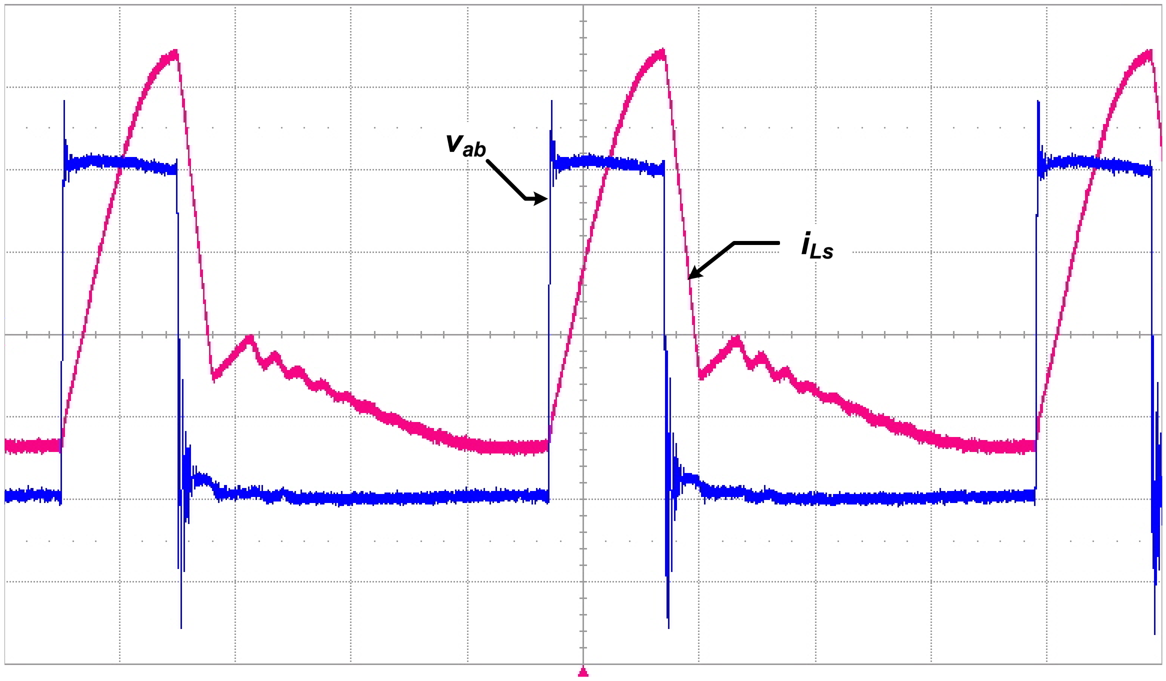


Figure 2-26: Experimental waveforms of input voltage and resonant current operating below resonant frequency at V_{in_min}=20V, Rated Load (300W) using APWM at f_{sw}=114kHz (ω=0.75), D=0.25 [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2µs/div]

2.5.4.3 At Nominal Input Voltage, Rated Load Condition

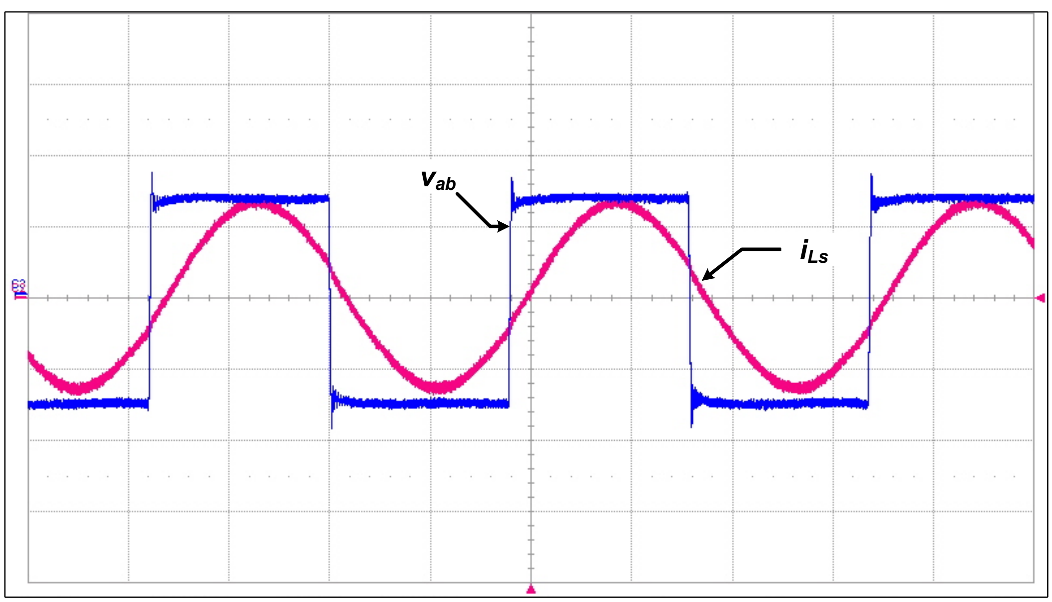


Figure 2-27: Experimental waveforms of input voltage and resonant current operating at resonant frequency at V_{in_nom}=30V, rated load (300W) using Frequency Modulation at f_{sw}=151kHz [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2µs/div]

smaller frequency variation below resonant frequency while achieving required output voltage V_o= 380V. Figure 2-27 shows the experimental waveforms of input square wave voltage, v_{ab} and primary side resonant current, i_{Ls} at nominal input voltage V_{in_nom}=30V, rated load (300W) condition with f_{sw}=151kHz.

Switching currents, ZVS angle and peak current values inferenced from experimental results matched closely with the analytical results demonstrated in previous section. Similarly, operation at other loading conditions for input voltage range 20-30V showed good corroboration between analytically calculated and experimentally measured values.

2.6 Summary

Different possible resonant stages of LLC converter and their equivalent circuits were presented in this chapter. Dynamic characteristics of the three most commonly occurring resonant stages were described in detail. The underlying assumptions used for time-domain modeling of full bridge LLC dc-dc resonant converter for PV applications were mentioned. The proposed analysis is independent of chosen Q value of LLC resonant tank, unlike previous existing work in literature. PV applications demands wide input range operation which translates to wide gain requirement. Therefore, operation below and above resonant frequency is essential. Time domain analysis for variable frequency control below (PO mode) and above (NP mode) resonant frequency was performed. A qualitative comparative analysis of general features of each mode was also performed However, it was observed that operation in these modes for the given input range led to a wide switching frequency range requirement on both sides of the unity gain resonant point. Narrowing switching frequency variation below resonant frequency can be achieved by operating the LLC converter under asymmetrical duty cycle control at a pre-defined minimum switching frequency. Such duty cycle modulation leads to additional voltage gain. However, the reported literature which proposed the above-mentioned feature performed analysis valid only for high Q resonant circuits. Hence, time domain analysis of the same technique was performed which would be valid at any Q

value. Experimental observation showed a close match with the analytical values for voltage gain, ZVS angle and primary RMS current. Experimental verification of APWM based LLC converter was done.

Chapter 3

Proposed Hybrid Modulation Technique for Improved Light Load Efficiency

3.1 Introduction

Chapter 2 discussed time domain modeling of frequency modulated full bridge-based LLC type series resonant converter. Variable frequency modulation is the simplest technique to regulate output voltage. However, it is required to use LLC converter for applications which require zero voltage switching (ZVS) and tight output voltage regulation for wide input and load range variation. One such application which requires a wide range of input voltage operating conditions is dc-dc stage of solar PV micro-inverters. Maintaining high conversion efficiency and ZVS of all four switches at worst case operating conditions of maximum input voltage and light load condition is a major challenge with LLC converter. Switching losses (due to loss of ZVS and MOSFET turn -off losses) account for a major share of the total losses. This is due to a wide range of switching frequencies required for output voltage regulation which makes it difficult to optimize the magnetics for the wide range. Constant transformer core losses at light loads significantly degrades efficiency. Core losses can be reduced by decreasing flux swing and switching frequency. Turn-off losses are also proportional to switching frequencies. Hence, load independent losses at light loading conditions dominates the total loss, thereby degrading the output efficiency. Conventional frequency modulation (FM) method requires wide range of switching frequencies above resonance to achieve required output voltage gain at light loading conditions which leads to large core losses and MOSFET turn-off loss. Asymmetrical pulse width modulation (APWM) with voltage doubler rectifier was implemented in [84] which considerably improved light load efficiency by decreasing flux swing but led to increase of turn-off losses for switch pair conducting during duty ratio D. This is due to high peak magnetizing current arising due to asymmetrical operation. Phase shift modulation (PSM) is a popular method which has been favored in industry [75] and academia [85] due to ease of implementation and good efficiency performance at nominal rated conditions. However, at worst case operating conditions such as maximum input voltage and light load, leading leg MOSFETs achieves partial ZVS or loses ZVS totally. Partial ZVS operation affects lifetime and reliability of MOSFETs switching at high frequencies. Hence, a new modulation technique is desired which achieves true ZVS of all four switches at light load conditions, thereby guaranteeing high light load efficiency by significantly reducing required range of switching frequency and MOSFET turn-off losses.

3.2 Concept of Proposed Adjustable Duty Cycle-Switching Frequency Hybrid Modulation Scheme

The basic idea for using hybrid control can be understood easily by using the voltage gain equation for LLC converter obtained using FHA under the following assumptions:

1. All MOSFET switches are ideal, ignoring the effect of the intrinsic resistors.
2. All the resonant variables can be regarded as sinewaves, ignoring the harmonics.
3. Dead time between switches is neglected.

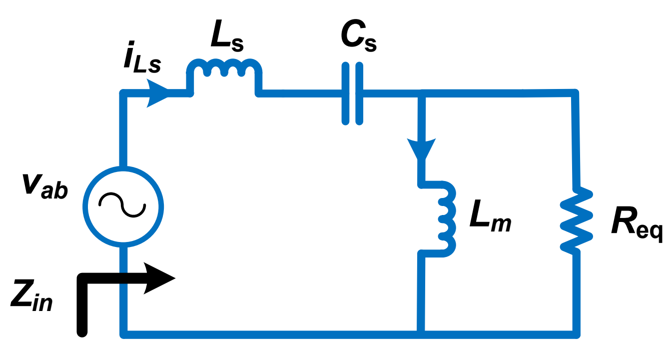


Figure 3-1: FHA based equivalent circuit diagram of LLC converter

$$G_{FHA} = \frac{1}{\sqrt{\left(1 + K - \frac{K}{\omega^2}\right)^2 + Q^2\left(\omega - \frac{1}{\omega}\right)^2}} \tag{3.1}$$

where

$$Q = \frac{\sqrt{\frac{L_s}{C_s}}}{R_{eq}}; \qquad R_{eq} = \frac{8n^2 R_l}{\pi^2}; \qquad n = \frac{N_p}{N_s}$$

$$\omega_r = \frac{1}{\sqrt{L_s C_s}}; \qquad \omega = \frac{\omega_s}{\omega_r} \tag{3.2}$$

As shown in Figure 3-1, the output gain equation can be characterized by dividing the equivalent resistance R_{eq} by total impedance of resonant network, Z_{in}. Z_{in} increases with the increase in ω above resonant frequency, ω_r. Variable frequency control with duty cycle, $D=0.5$ implies that the RMS value of the input square wave voltage applied to the LLC resonant tank is constant. Hence, Z_{in} is increased with corresponding reduction in load to maintain the gain relationship constant. It can be inferred that the input impedance of LLC resonant tank and the RMS value of square wave input voltage applied to the LLC resonant tank should be adjusted depending on load variations such that the output voltage is held constant.

The proposed modulation technique uses the same concept. RMS value of the square- wave input voltage can be reduced by varying the duty cycle. Also, LLC resonant tank impedance can be decreased by reducing the switching frequency. These two features allow the converter to be operated at lower switching frequencies while simultaneously varying the duty cycle.

3.3 Operational Principle

Figure 3-2 shows the circuit diagram of full bridge *LLC* resonant converter with the proposed adjustable duty cycle-switching frequency hybrid modulation scheme. It is composed of primary MOSFET switches Q_1-Q_4, resonant inductor L_s, resonant capacitor C_s, magnetizing inductance L_m, transformer T_1 with turns ratio $1: n$, diode rectifier Do_1-Do_4, filter output capacitor C_o and output load R_l. Snubber capacitors, C_{sn1}-C_{sn4} are connected across each MOSFET to reduce turn-off switching losses. The control logic implemented depends on the sensed PV voltage. The control logic can be implemented on any digital signal processor (DSP) microcontroller.

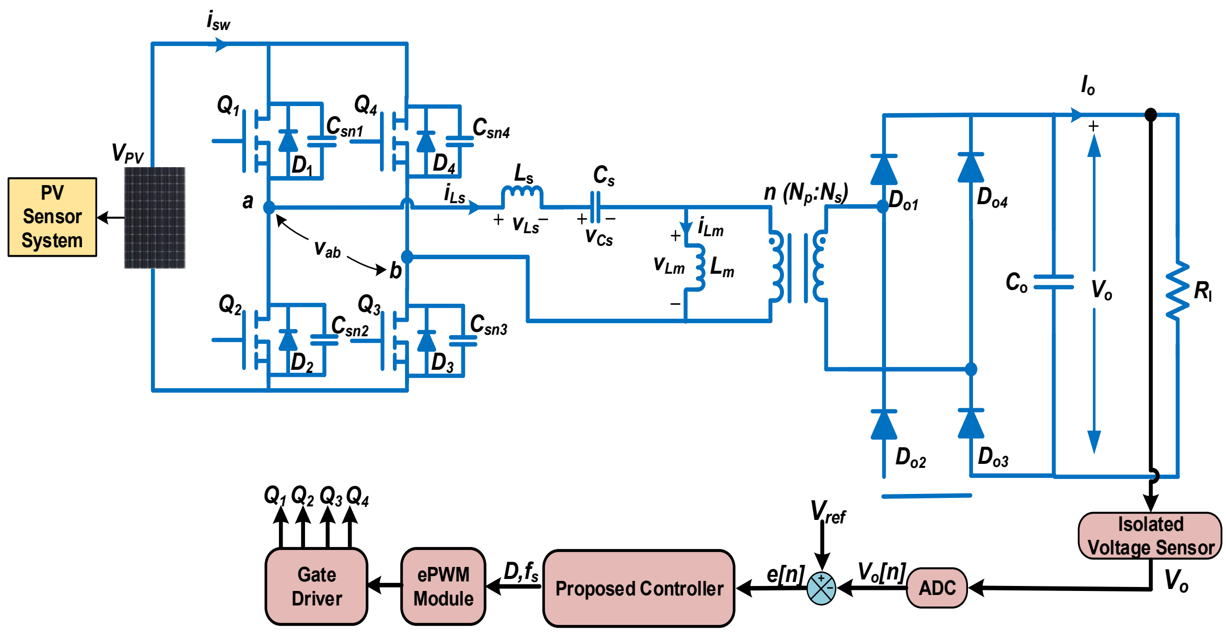


Figure 3-2: Full bridge LLC resonant converter with control structure

3.4 Assumptions

The following assumption are made in analysis of steady-state behaviour of the converter.

1) The semiconductor MOSFET switches along with the rectifier diodes and high frequency transformer are ideal.
2) MOSFET capacitances are negligible.
3) The output filter capacitor is large enough to keep the output voltage constant.
4) Dead time between switches is neglected.

Key ideal waveforms during light load conditions for the proposed modulation technique are shown in Figure 3-3. The rising and falling edge of Q_2 gate pulse is symmetrically placed from rising and falling edge of Q_1 gate pulse such that ZVS is achieved while regulating output voltage. The resulting bipolar square wave, V_s is symmetrical in nature which would reduce peak stresses on circuit components compared to an asymmetrical modulation waveform as observed in the previous chapter. Different stages of operation as evaluated as given below:

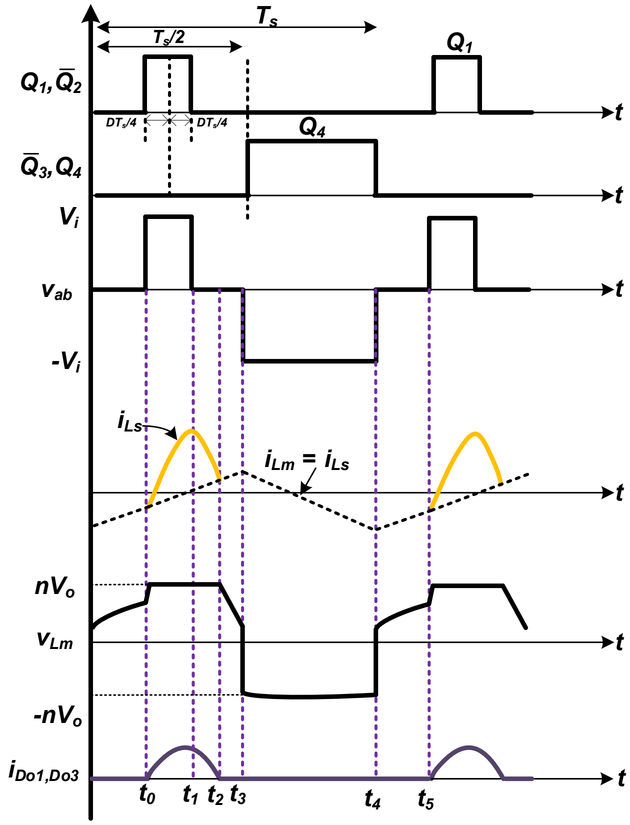


Figure 3-3: Key waveforms at light-load conditions

Stage 1 [t_0-t_1]

At t_0, Q_1 switch in the leading leg is turned on under ZVS while Q_3 was already conducting. Tank voltage, v_{ab} becomes equal to the input voltage. Resonant tank current, i_{Ls} starts flowing through LLC resonant tank during this period. Magnetizing inductor, L_m is clamped to the reflected output voltage $+nV_o$. Output diode rectifier D_{o1} and D_{o4} are turned on and transfer power to the load. Figure 3-4 shows the LLC circuit during this stage of operation.

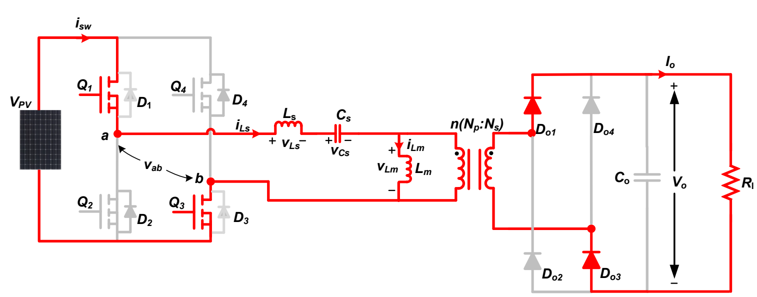


Figure 3-4: LLC circuit during Stage 1

$$i_{Ls}(t)=i_{Ls}(t_0)cos(\omega_r t)+\left[\frac{V_i-nV_o-v_{Cs}(t_0)}{Z_0}\right]sin(\omega_r t) \tag{3.3}$$

$$i_{Lm}(t)=\frac{nV_o}{L_m}t+i_{Lm}(t_0) \tag{3.4}$$

$$v_{Cs}(t)=Z_0 i_{Ls}(t_0)sin(\omega_r t)+v_{Cs}(t_0)cos(\omega_r t)+\left[V_i-nV_o\right]\left[1-cos(\omega_r t)\right] \tag{3.5}$$

This stage ends when Q_1 is turned off at $t=t_1$, which eventually depends on the duty cycle.

Stage 2 [t_1-t_2]:

At time instant t_1, Q_1 is turned off, whereas Q_2 is turned on. Since the turn-off current of Q_1 was positive, low side switch Q_2 will turn on with ZVS. The equivalent tank voltage becomes zero and magnetizing inductance L_m is clamped with the reflected output voltage, nV_o. until resonant tank current, i_{Ls} becomes equal to i_{Lm} at $t=t_2$. Figure 3-5 shows the equivalent LLC circuit during stage 2.

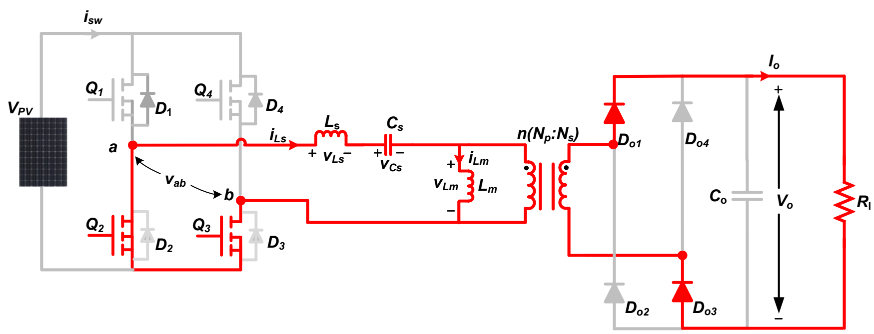


Figure 3-5: LLC circuit during Stage 2

$$i_{Ls}(t)=i_{Ls}(t_1)cos(\omega_r(t-t_1))-\left[\frac{nV_o+v_{Cs}(t_1)}{Z_0}\right]sin(\omega_r(t-t_1)) \tag{3.6}$$

$$i_{Lm}(t)=\frac{nV_o}{L_m}t+i_{Lm}(t_1) \tag{3.7}$$

$$v_{Cs}(t)=Z_0 i_{Ls}(t_1)sin(\omega_r(t-t_1))+v_{Cs}(t_1)cos(\omega_r(t-t_1))-nV_o\left[1-cos(\omega_r(t-t_1))\right] \tag{3.8}$$

Stage 3 [t_2-t_3]:

At $t=t_2$, L_m starts resonating with L_s and C_s as there is no clamping on L_m by reflected voltage. The resulting dynamics can be expressed by the following tank current, i_{Ls} and capacitor voltage, v_{Cs} equations solved using the LLC circuit shown in Figure 3-6.

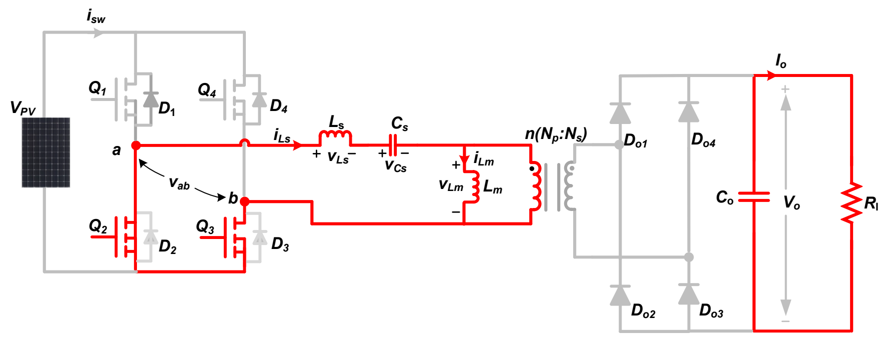


Figure 3-6: LLC circuit during Stage 3

$$i_{Ls}(t) = i_{Ls}(t_2)\cos(\omega_{r_1}(t-t_2)) - \frac{v_{Cs}(t_2)}{Z_1}\sin(\omega_{r_1}(t-t_2)) \tag{3.9}$$

$$v_{Cs}(t) = Z_1 i_{Ls}(t_2)\sin(\omega_{r_1}(t-t_2)) + v_{Cs}(t_2)\cos(\omega_{r_1}(t-t_2)) \tag{3.10}$$

This stage ends when switch Q_3 of the lagging leg is turned off at $t=t_3$.

Stage 4 [t_3-t_4]:

Q_3 is turned off while Q_4 is turned on with ZVS. It starts conducting with Q_2 at time t_3. L_m is still resonating with series L_s and C_s and no energy transfer to the output takes place. This stage ends when Q_4 is turned off. The resultant LLC circuit during this stage of operation is shown in Figure 3-7.

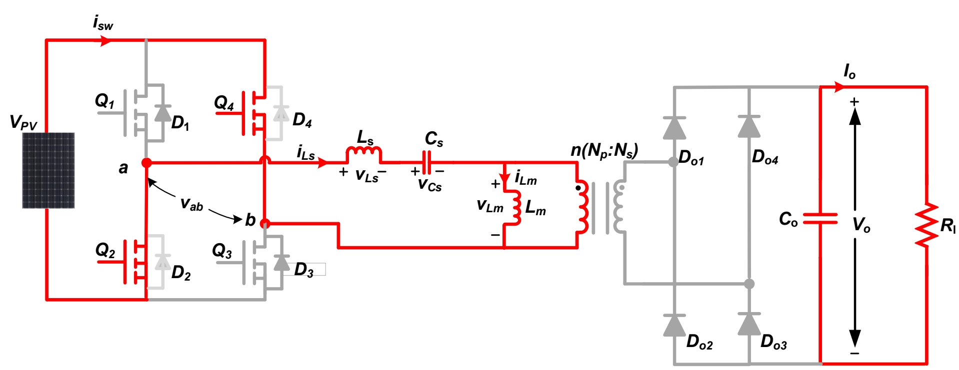


Figure 3-7: LLC circuit during Stage 4

$$i_{Ls}(t) = i_{Ls}(t_3)\cos(\omega_{r_1}(t-t_3)) - \left[\frac{V_i + v_{Cs}(t_3)}{Z_1}\right]\sin(\omega_{r_1}(t-t_3)) \tag{3.11}$$

$$v_{Cs}(t) = Z_1 i_{Ls}(t_3)\sin(\omega_{r_1}(t-t_3)) + v_{Cs}(t_3)\cos(\omega_{r_1}(t-t_3)) - V_i\left[1-\cos(\omega_{r_1}(t-t_3))\right] \tag{3.12}$$

Stage 5 [t_4-t_5]:

This stage leads to same equivalent circuit as the one discussed in Stage 3.

3.5 Solution of Proposed Modulation Scheme using Newton-Raphson Method

The resulting transcendental equations can be solved by using any iterative numerical technique. Due to its simplicity and reliability, Newton Raphson technique was selected. The switching instants t_1, t_3, t_4 and t_5 are known quantities given as:

$$\begin{aligned} t_1 &= {DT_s}/{2} & t_3 &= {(1-D)T_s}/{4} - t_2 \\ t_4 &= {T_s}/{2} & t_5 &= {(1-D)T_s}/{4} \end{aligned} \tag{3.13}$$

Time instant t_1 is the ON time of the switch Q_1. Time instant t_2 is the only unknown quantity which depends on the operating state of the LLC resonant converter.

In steady state operating conditions, the following conditions are valid for the proposed light load modulation technique

$$\begin{aligned} i_{Ls}(t_0) &= i_{Lm}(t_0) = i_{Ls}(T_s) \\ v_{Cs}(t_0) &= v_{Cs}(T_s) \end{aligned} \tag{3.14}$$

Solving (3.14), the initial values of resonant capacitor voltage, $v_{Cs}(t_0)$ and resonant tank current $i_{Ls}(t_0)$ are calculated as follows:

$$v_{Cs}(t_0) = V_i - nV_o - \left[\alpha_1\left(1-\cos\left(\omega_r\left(t_1+t_2\right)\right)\right)/\beta_1\right] \tag{3.15}$$

$$i_{Ls}(t_0) = \frac{V_i - nV_o - \left[\dfrac{v_{Cs}(t_0)}{\omega_r L_s}\right]\sin\left(\omega_r\left(t_1+t_2\right)\right) - \left[\dfrac{V_i}{\omega_r L_s}\right]\sin(\omega_r t_2) - \dfrac{nV_o\left(t_1+t_2\right)}{L_m}}{\left(1-\cos\left(\omega_r\left(t_1+t_2\right)\right)\right)} \tag{3.16}$$

$$P_o = \left[\frac{nV_o}{T_s} \right] * \left[\begin{array}{l} \left(\frac{i_{Ls}(t_0)}{\omega_r} \right) \left(sin\left(\omega_r \left(t_1 + t_2 \right) \right) - \left(\omega_r \left(t_1 + t_2 \right) \right) \right) + \left(V_i - nV_o - \frac{v_{Cs}(t_0)}{\omega_r^2 L_s} \right) \left(1 - cos\left(\omega_r \left(t_1 + t_2 \right) \right) \right) \\ - \left(V_i - \frac{v_{Cs}(t_0)}{\omega_r^2 L_s} \right) \left(1 - cos\left(\omega_r t_2 \right) \right) - \left(\frac{nV_o}{L_m} \right) \left(\frac{t_1^2 + t_2^2}{2} + t_1 t_2 \right) \end{array} \right] \tag{3.17}$$

It will be shown that α_1 and β_1 depend on unknown time value, t_2.

In order to solve the resulting set of equations expressed in (3.15) -(3.17) for unknown time instant t_2, we formulate the function, $f_{fixed\_gain} = f\,(t_1 + t_2)$ where

$$f(t_1 + t_2) = \alpha_1 \beta_2 - \alpha_2 \beta_1 \tag{3.18}$$

is valid for constant output voltage, variable output power. α_1, β_1, α_2 and β_2 are defined in Appendix B.

In the case of constant output power, variable output voltage, the following function, $f_{fixed\_power} = f(t_1 + t_2)$ is derived:

$$f(t_1 + t_2) = P_o - \frac{V_{o\_calc}}{nT_s} \left[\begin{array}{l} \left[\frac{\alpha_{1\_V_{in}}}{\beta_1 \omega_r^2 L_s} \right] \left[2\left(1 - cos\left(\omega_r \left(t_1 + t_2 \right) \right) \right) - \omega_r \left(t_1 + t_2 \right) sin\left(\omega_r \left(t_1 + t_2 \right) \right) \right] \\ \quad - \left[\frac{V_{in}}{\omega_r^2 L_s \left(1 - cos\left(\omega_r \left(t_1 + t_2 \right) \right) \right)} \right] \left[1 + cos\left(\omega_r t_1 \right) - cos\left(\omega_r t_2 \right) - cos\left(\omega_r \left(t_1 + t_2 \right) \right) - \omega_r \left(t_1 + t_2 \right) sin\left(\omega_r t_2 \right) \right] \\ \quad - \left[\frac{V_{o\_calc}}{n \omega_r L_m} \right] \left[\frac{\left(t_1 + t_2 \right) sin\left(\omega_r \left(t_1 + t_2 \right) - \omega_r \left(t_1 + t_2 \right) \right)}{\left(1 - cos\left(\omega_r \left(t_1 + t_2 \right) \right) \right) + \omega_r \left(\frac{t_1^2}{2} + \frac{t_2^2}{2} + t_1 t_2 \right)} \right] \end{array} \right] \tag{3.19}$$

where,

$$V_{o\_calc} = \frac{\alpha_{2\_V_{in}} \beta_1 - \alpha_{1\_V_{in}} \beta_2}{\alpha_{1\_V_o} \beta_2 + \alpha_{2\_V_o} \beta_1} \tag{3.20}$$

Variables occurring in (3.20) are also defined in Appendix B.

As per desired application, (3.18) or (3.19) can be solved by using the standard Newton Raphson iterative method for t_2 using

$$t_2 = t_2 - {f(t_1 + t_2)} \big/ {df(t_1 + t_2)} \tag{3.21}$$

3.6 Design Example

Section 2.5 demonstrated operation of LLC resonant converter for micro-inverter applications below resonant frequency. Experimental waveforms were compared with the analytical waveforms and proved the proposed analysis to be highly accurate. ZVS was obtained for the worst-case operating condition of minimum input voltage, rated load condition for the given design specifications. Operation under variable frequency control above resonant frequency for selected value of Q_{rated}=0.34 doesn't achieve regulation at light loads within a narrow switching frequency range. Hence, converter performance of different conventional modulation schemes will be compared with the proposed modulation scheme at light loading conditions in this section.

For the same design specifications as given in Section 2.5.1, the second worst-case operating condition, which is at the given maximum input voltage (V_{in_max}=40V) and light load condition (P_o=30W) will be evaluated. Light load condition has been taken as 10% of rated load for analytical and experimental purposes. Upper bound on the switching frequency for operation between 30V-40V is 200kHz., i.e., ω=1.33 based on core loss calculations. Modulation scheme switches from FM to PSM, APWM or the proposed technique when voltage regulation is no longer possible using FM only. It is expected from design analysis conducted in this Chapter 4, that due to the feature of simultaneously changing both switching frequency and duty cycle of the proposed technique, upper bound on the switching frequency can be reduced from ω=1.33 to ω=1.2. Lossless snubber capacitor, C_{sn}=1nF was connected across each primary MOSFET to reduce turn-off switching losses. TMS320F28335 DSP microcontroller was used to implement the various modulation techniques. Chroma 6314 DC Electronic Load was used to implement various loading scenarios for experimental prototype.

3.6.1 Analytical Results

Figure 3-8. demonstrates the ideal analytical steady state response of LLC converter under proposed modulation technique using MATLAB. The proposed input modulated voltage

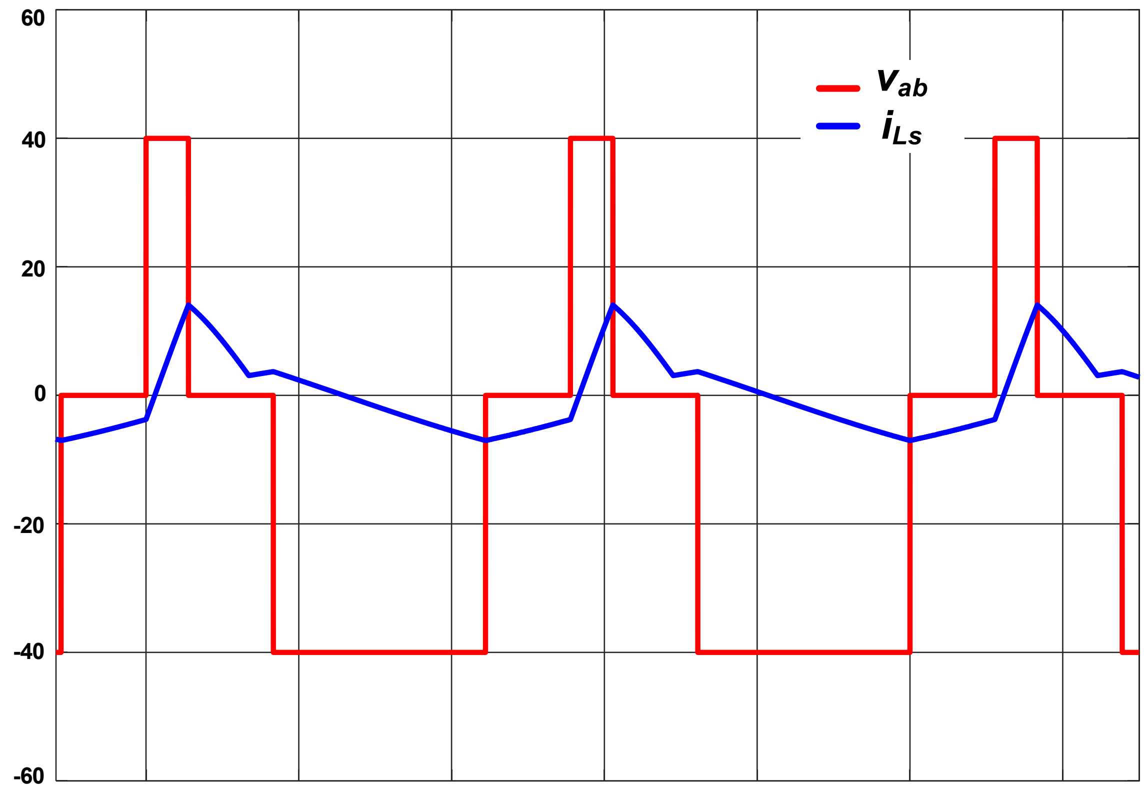


Figure 3-8: MATLAB generated steady-state waveforms at V_{in}=40V, 10% of rated Load=30W

waveform, v_{ab} is generated at a switching frequency of f_{sw}=180kHz with duty cycle, D=0.15. Resonant current, i_{Ls} lags the modulated voltage waveform to achieve ZVS of the primary MOSFETs of leading leg at 10% loading condition and ensures voltage regulation as well. Analytically calculated current and voltage values are a close match with the values obtained using simulation studies.

3.6.2 Experimental Results

3.6.2.1 Experimental Observations at Maximum Input Voltage, Light Load Condition Above Resonant Frequency

From experimental observations, it is noted that converter operation with frequency modulation at V_{in}=35V and V_{in_max}=40V, rated load condition fails to regulate output voltage at 380V at maximum allowable f_{sw}=200kHz. Hence, it is necessary to switch from variable frequency modulation to duty cycle control for achieving required voltage gain within the frequency range. Different modulation techniques are tested for their ZVS performance in the next sub-section.

3.6.2.1.1 Phase Shift Modulation

Modulation scheme is changed to conventional fixed frequency PSM at f_{sw_max} on the evaluation prototype at V_{in_max}=40V, rated load condition. The duty cycle of all four switches remains constant at D=0.5 while the Lagging Leg B (Q_3, Q_4) is phase shifted with respect to Leg A (Q_1, Q_2), thereby changing the effective duty cycle value. PSM demonstrates true ZVS of all four-primary side MOSFETs from rated load condition to part load condition at V_{in_max}=40V. However, at 30% loading condition, leading leg MOSFETs of the full bridge switching network achieves partial ZVS only as shown in Figure. 3-9. Hence, turn-on switching losses are not zero.

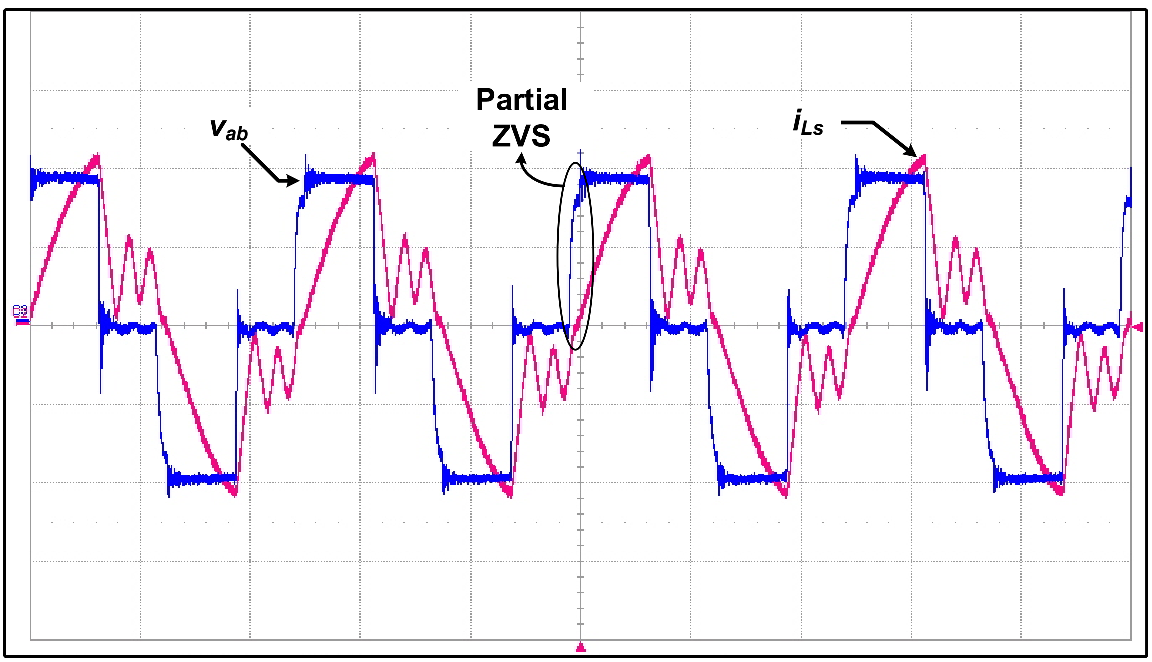


Figure 3-9: Experimental waveforms of phase shift modulated input voltage and resonant current at f_{sw}=200kHz (ω=1.33) at V_{in_max}=40V, 30% load. [v_{ab}: 20V/div., i_{Ls}: 5A/div., Time: 2μs/div]

Further, at 10% loading condition, operation at V_{in}=35V and V_{in}=40V is tested under phase shift modulation. ZVS of all four MOSFETs is lost under both input voltages as shown in Figure 3-10 and Figure 3-11. Apart from inability to turn on leading leg MOSFETs at zero voltages, ZVS of

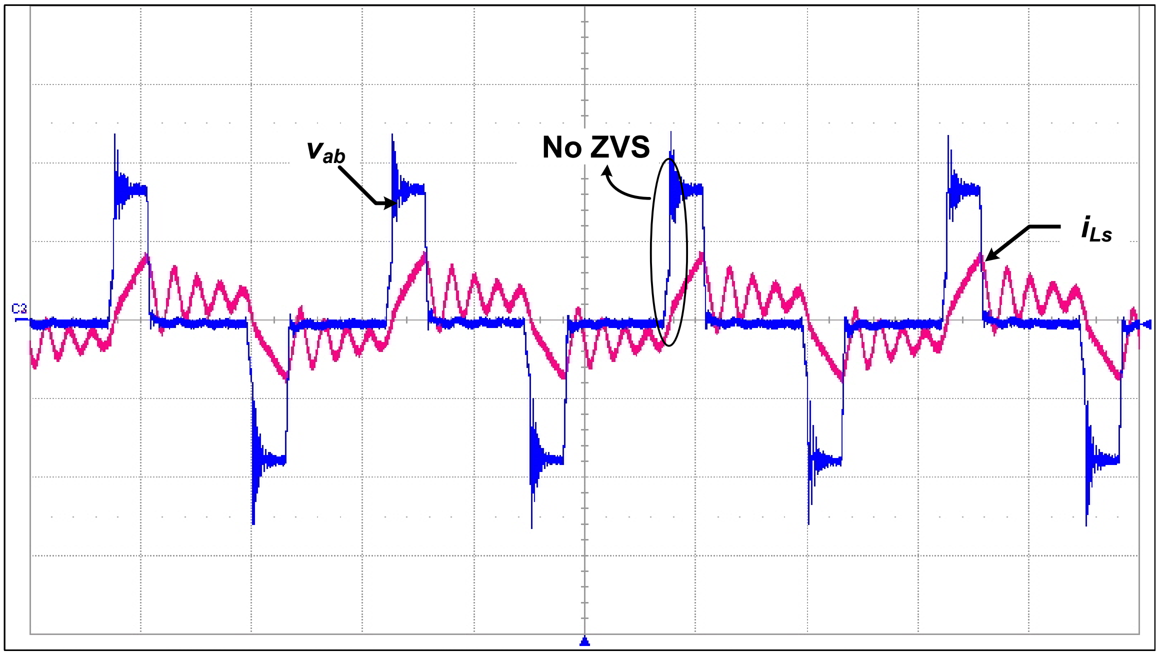


Figure 3-10: Experimental waveforms of phase shift modulated input voltage and resonant current at f_{sw}=200kHz (ω=1.33) at V_{in_max}=35V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 5A/div., Time: 2μs/div]

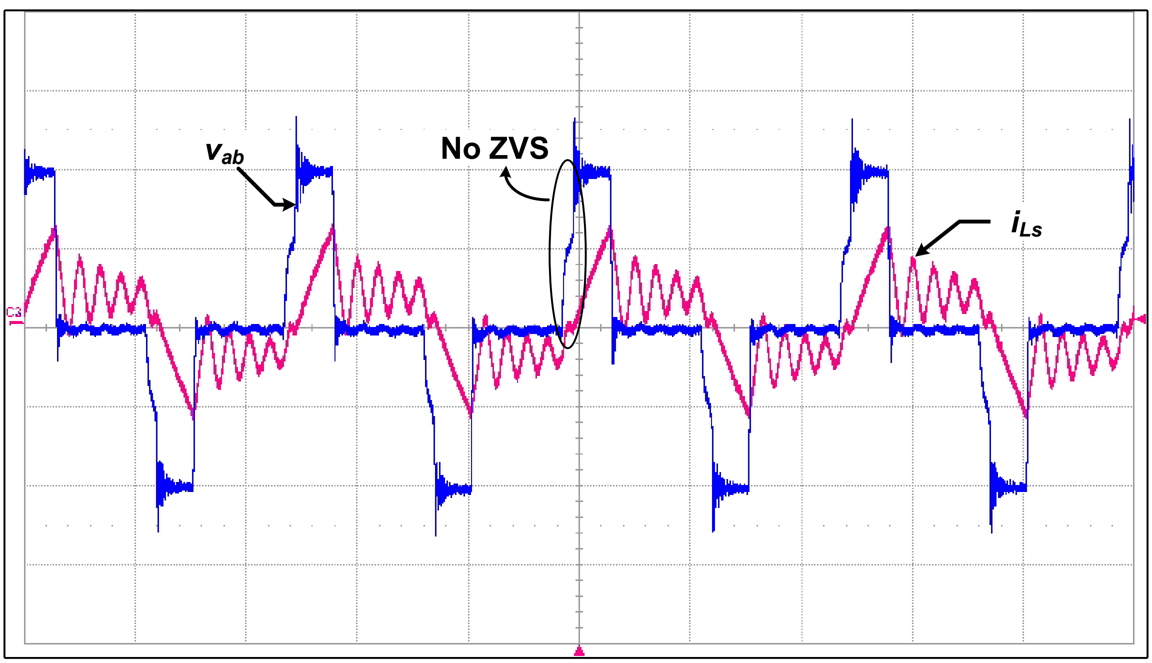


Figure 3-11: Experimental waveforms of phase shift modulated input voltage and resonant current at f_{sw}=200kHz (ω=1.33) at V_{in_max}=40V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 5A/div., Time: 2μs/div]

lagging leg MOSFETs cannot be guaranteed due to multiple zero crossings of series resonant current during interval when v_{ab}=0. Due to multiple zero crossings, MOSFETs anti-parallel diode conduction may or may not happen. Hence, PSM isn't suitable for achieving ZVS of a low Q LLC resonant converter for 2:1 input range application within the selected switching frequency range.

Such pronounced ringing in resonant current can be contributed to long intervals of zero voltage tank excitation, i.e., v_{ab} =0. This leads to large ripple in resonant current due to interaction of LLC resonant tank with distributed capacitance of high frequency low-profile transformer and primary reflected junction capacitance of rectifier diodes. Hence, in order to reduce the probability of losing ZVS due to multiple zero crossings of resonant current, intervals for which v_{ab} stays at zero should be reduced.

3.6.2.1.2 Asymmetrical Pulse Width Modulation

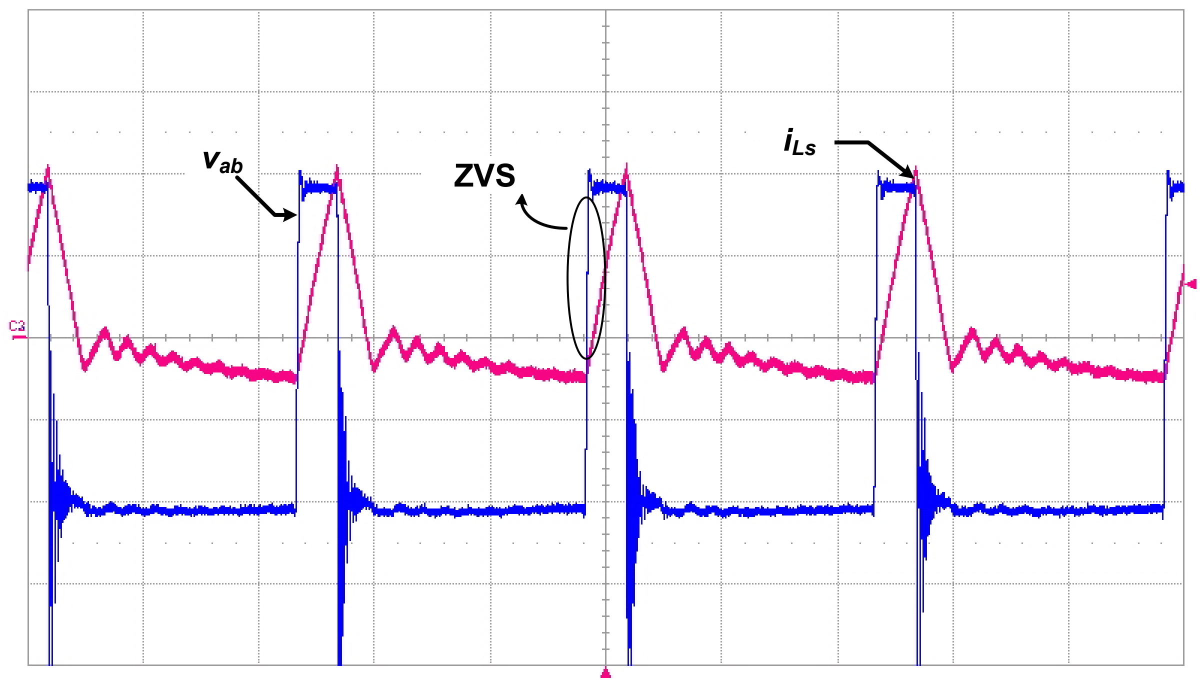


Figure 3-12: Experimental waveforms of APWM based input voltage and resonant current at f_{sw}=200kHz (ω=1.33), D=0.16 at V_{in_max}=40V, 30% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2µs/div]

APWM ensures a continuous bipolar dc excitation of the LLC resonant tank during its operation. It can be observed that the input waveform is a bipolar wave with no interval when v_{ab} goes to zero. It achieves ZVS of all primary MOSFETs from rated load to part load condition at V_{in}=35V and V_{in_max}=40V within the upper switching frequency limit of f_{sw}=200 kHz. Unlike PSM, APWM

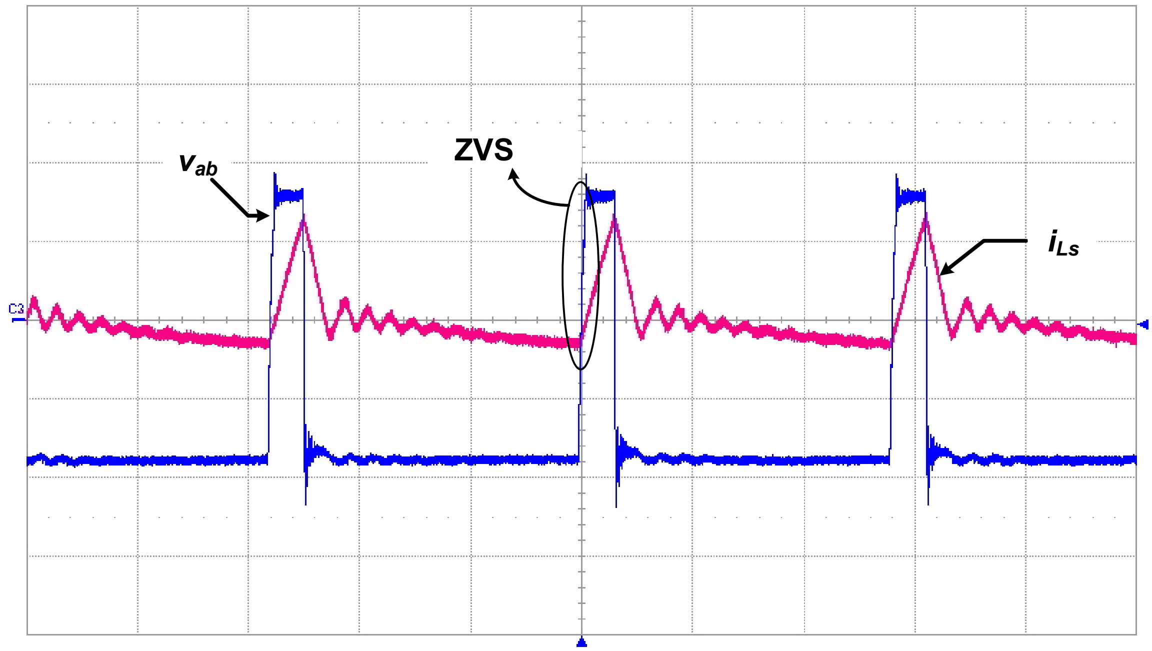


Figure 3-13: Experimental waveforms of APWM based input voltage and resonant current at f_{sw}=180kHz (ω=1.2), D=0.12 at V_{in_max}=35V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2μs/div]

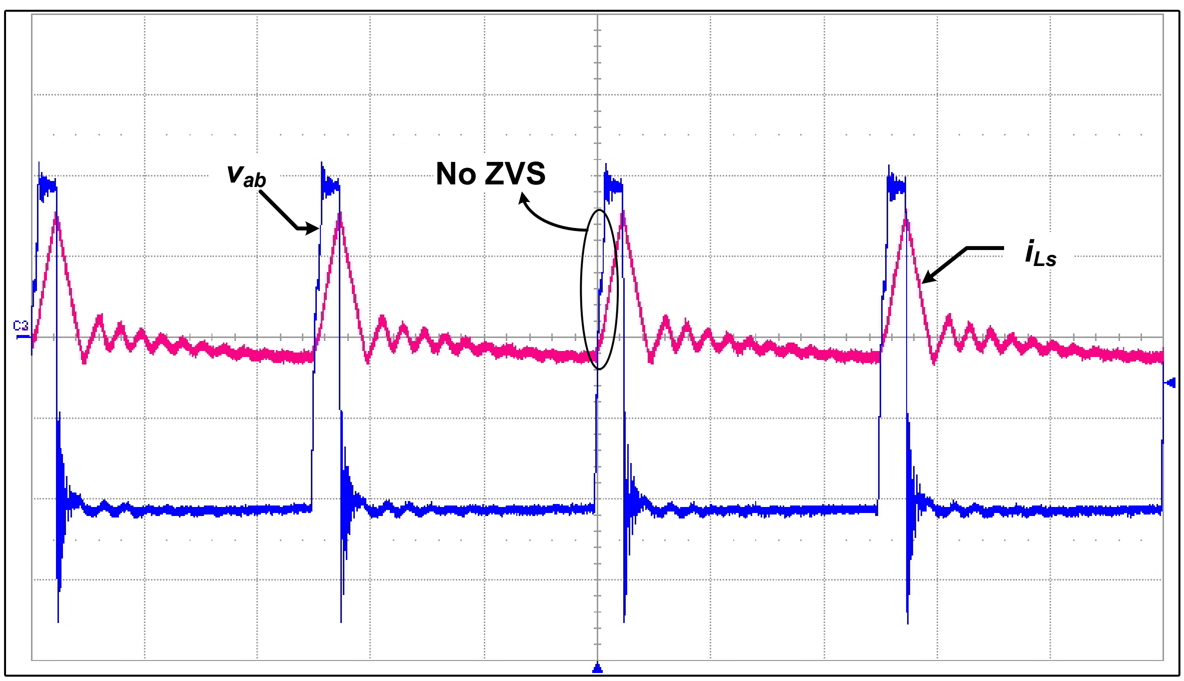


Figure 3-14: Experimental waveforms of APWM based input voltage and resonant current at f_{sw}=200kHz (ω=1.33), D=0.08 at V_{in_max}=40V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2μs/div]

guarantees ZVS of two switches operating with duty cycle D when operating at V_{in_max}=40V, 30% loading condition and V_{in}=35V, 10% loading condition as shown in Figure 3-12 and Figure 3-13 respectively. It can be observed that the current oscillations are significantly reduced compared to phase shift modulation technique. However, switches operating with duty ratio 1-D still may or may not attain ZVS due to multiple zero crossings of the resonant current. Ringing in the resonant current is due to circulating energy caused by the discharging of distributed capacitance from nV_o to -nV_o after DT_s interval ends. This circulating current resonates with transformer leakage inductance leading to ringing. Due to low-Q nature of resonant tank, it takes time for the ringing to be damped out which leads to multiple zero crossings. Therefore, operation at V_{in_max}=40V, 10% loading condition with D=0.08 at f_{sw}=200kHz (ω=1.33) may lead to true ZVS of only two switches (Q_2, Q_4) operating with duty cycle 1-D as shown in Figure 3-14. High stress due to large peak resonant current causes saturation of selected RM-6 core and degraded efficiency despite achieving true ZVS of two MOSFETs. High di/dt at turn-off causes drain-source voltage to start ringing due to stray inductances of PCB traces. High turn-off losses are another major concern with APWM based operation of low-Q LLC resonant converter at light load conditions.

3.6.2.1.3 Proposed Modulation Scheme

The proposed hybrid modulation technique was tested at 10% light load condition at operating input voltage V_{in}=35V and V_{in_max}=40V. Unlike PSM and APWM, it exhibits true ZVS of all four switches at D_{eff}=0.23 and D_{eff}=0.15 at a lower switching frequency, f_{sw}=180kHz (ω=1.2) when operating at V_{in}=35V in Figure 3-15 and worst-case condition of V_{in_max}=40V in Figure 3-16 at 10% load respectively. In order to validate the developed mathematical model for the proposed hybrid modulation technique, testing was done at extremely light load of 5%, V_{in_max}=40V. It was observed that true ZVS was observed even at this condition as shown in Figure 3-17. Values of D and ω were selected based on the required gain of 0.67 at V_{in_max}=40V and 10% loading condition. The proposed technique's waveform shape is a crossover between phase shift modulation and

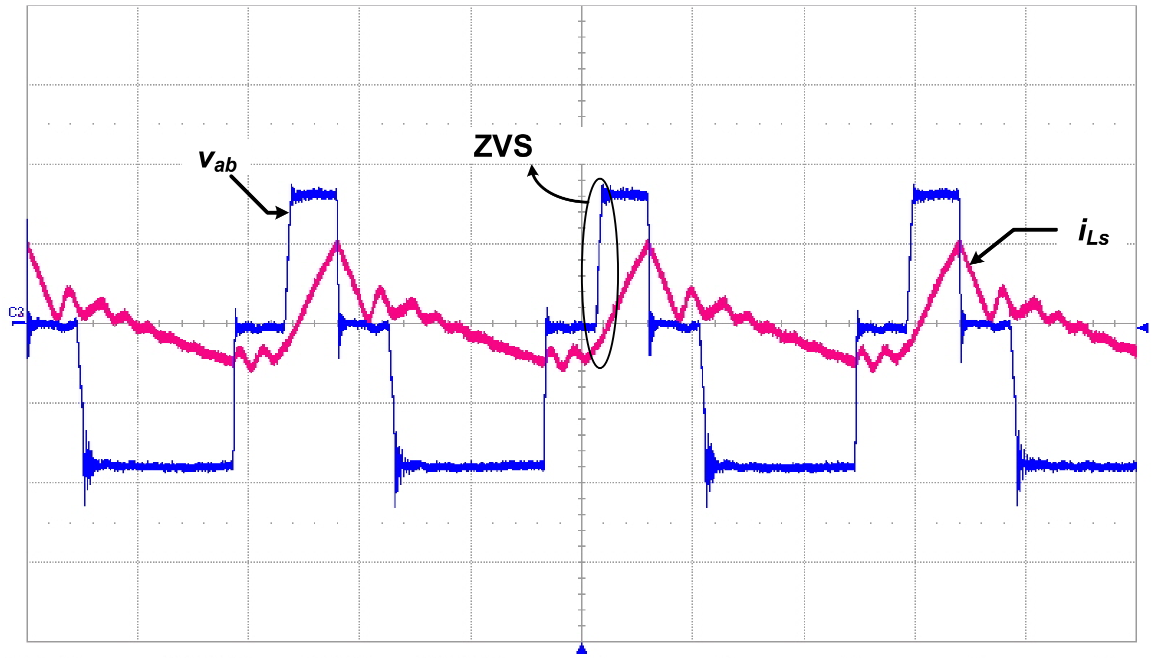


Figure 3-15: Experimental ZVS waveforms of proposed modulation technique-based input voltage and resonant current at f_{sw}=180kHz (ω=1.2), D_{eff}=0.23 at V_{in_max}=35V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2µs/div]

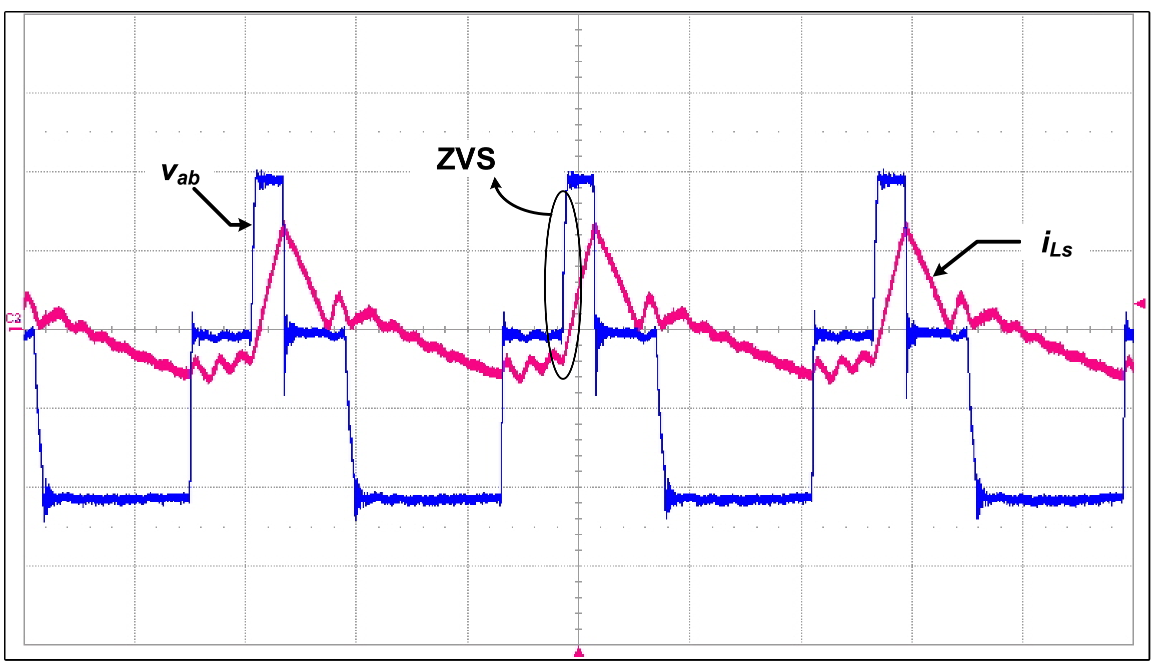


Figure 3-16: Experimental ZVS waveforms of proposed modulation technique-based input voltage and resonant current at f_{sw}=180kHz (ω=1.2), D_{eff}=0.15 at V_{in_max}=40V, 10% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2µs/div]

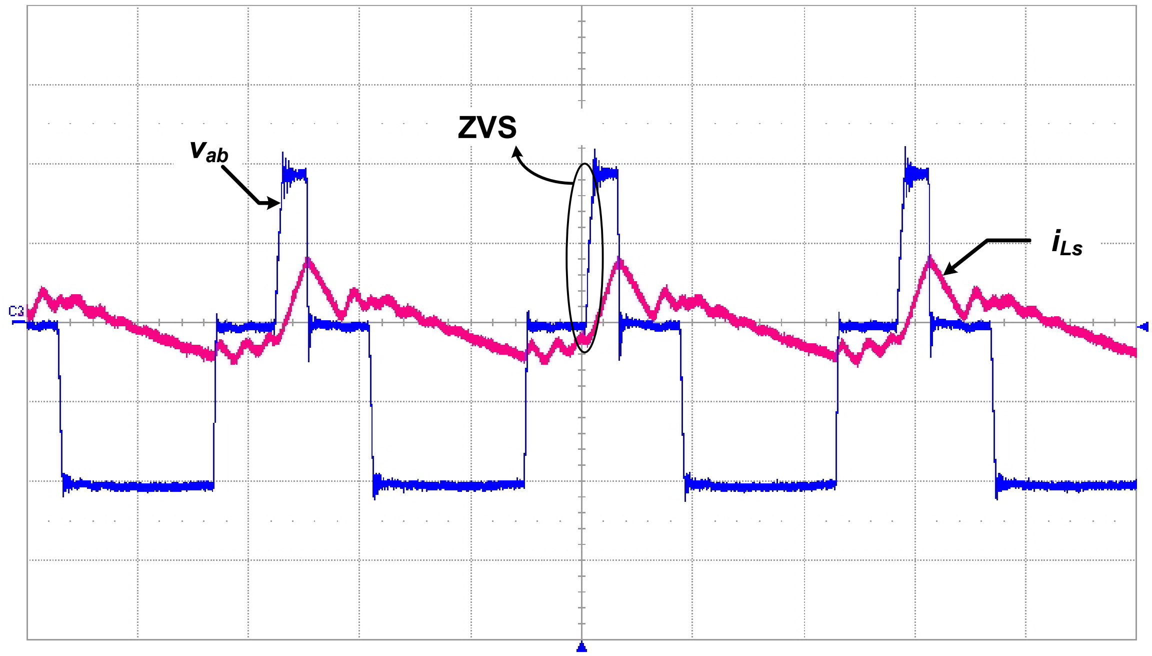


Figure 3-17: Experimental ZVS waveforms of proposed modulation technique-based input voltage and resonant current at f_{sw}=180kHz (ω=1.2), D_{eff}=0.1 at V_{in_max}=40V, 5% load. [v_{ab}: 20V/div., i_{Ls}: 10A/div., Time: 2μs/div]

asymmetrical pulse width modulation. It allows for a small interval when v_{ab} stays at 0 but due to the large negative pulse, the oscillations are damped out. Consequently, the distributed capacitance is not suddenly discharged from $+nV_o$ to $-nV_o$ due to the small v_{ab}=0 interval. It eliminates the occurrence of multiple zero crossings of resonant current evident in phase shift control and APWM at light load conditions. Further analysis has been conducted in Chapter 4 to determine combination of K and Q value for a fixed switching frequency at which the resonant current might cross zero when Q_1 is switched off. The proposed technique exhibits higher peak currents than PSM but guarantees soft switching of all four primary MOSFETs at light loading conditions for designed LLC resonant converter unlike phase shift modulation in which soft switching depends on the current oscillations due to component parasitics for the selected optimal values of K and Q. It exhibits lower peak resonant current compared to APWM thereby reducing magnetic losses and preventing inductor core saturation. Calculated turn-off current for leading leg switches are a close match with the experimental values. Partial ZVS was achieved when the converter was operated at

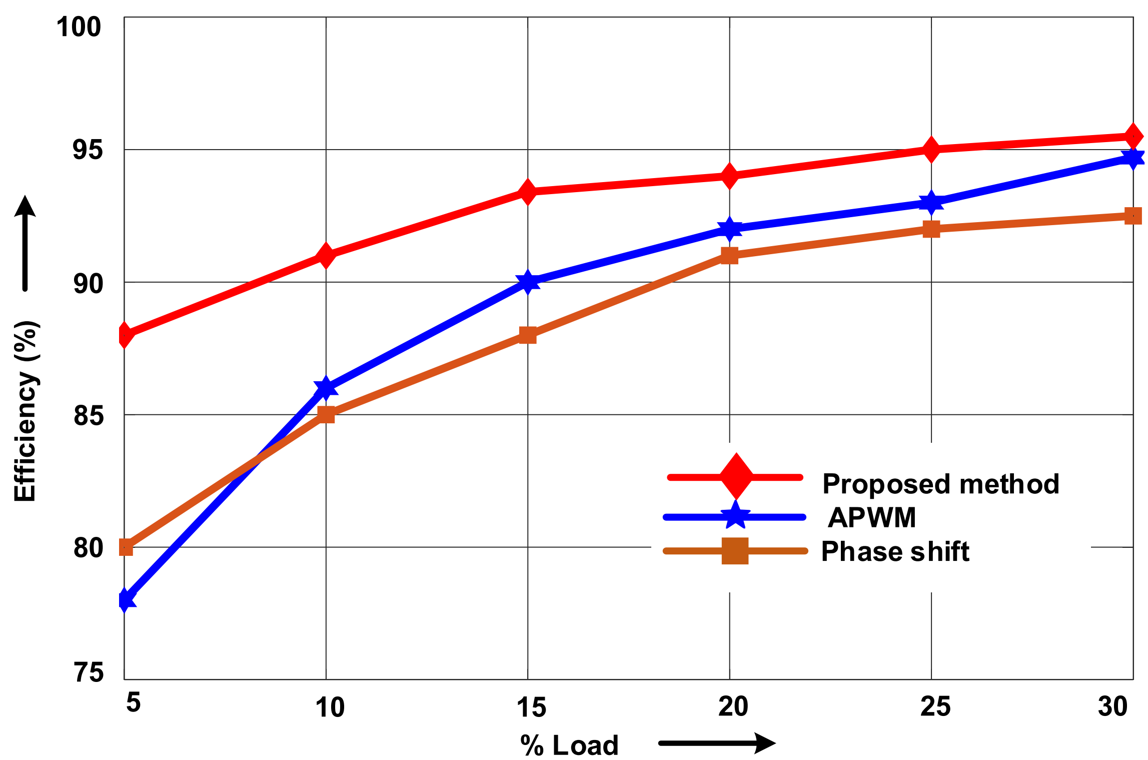


Figure 3-18: Measured efficiency curve for experimentally tested modulation techniques at V_{in_max}=40V

1% loading condition due to limitations on the gate driver ICs minimum input pulse width requirement. Therefore, it is experimentally verified that the proposed modulation technique is suitable for achieving ZVS of all four primary MOSFETs from part load to very light load conditions for wide- input range LLC converter. Experimental efficiency was measured using Chroma 6630 power analyzer. The light load efficiency curve for LLC converter operation at V_{in_max}=40V for PSM, APWM and the proposed modulation technique is given in Figure 3-17. The proposed method showed efficiency improvements of 6% and 8% at 10% and 5% load respectively compared to PSM. APWM showed a slight increment of 1% at 10% loading condition compared to PSM. The marginal improvement in efficiency of APWM based LLC converter despite achieving ZVS of two MOSFET switches at 10% load is primarily attributed to high magnetic losses due to higher peak currents than PSM. Efficiency curve for the whole load range using a combination of FM and proposed modulation technique for different input voltages is shown in

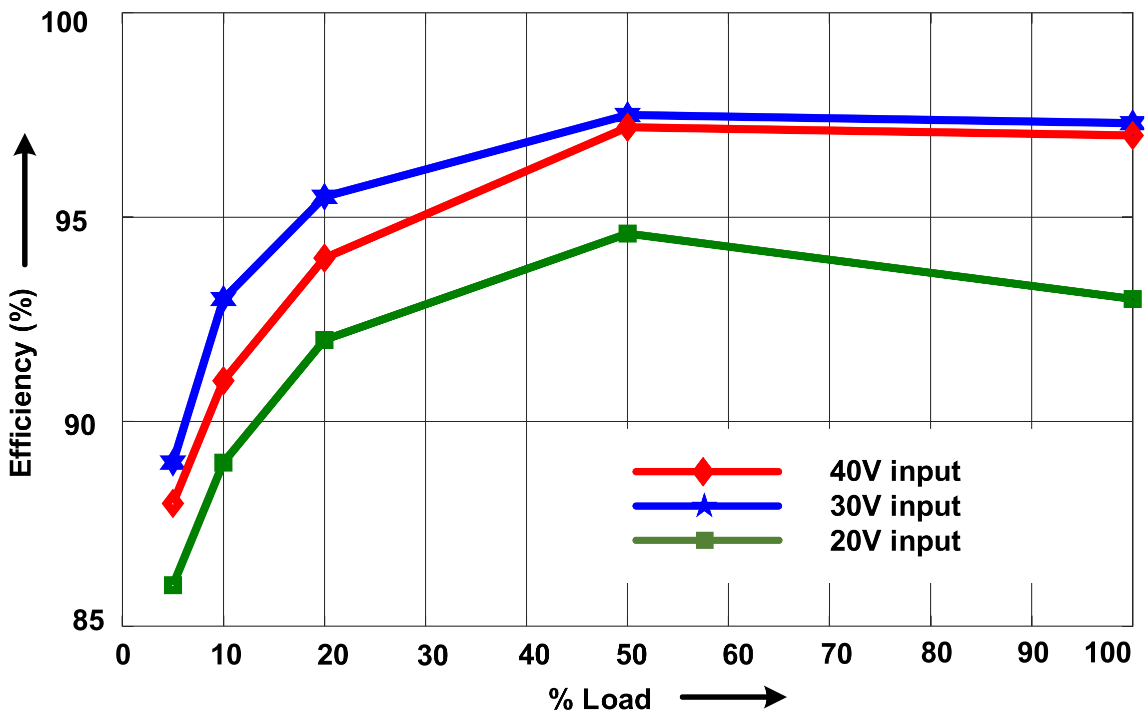


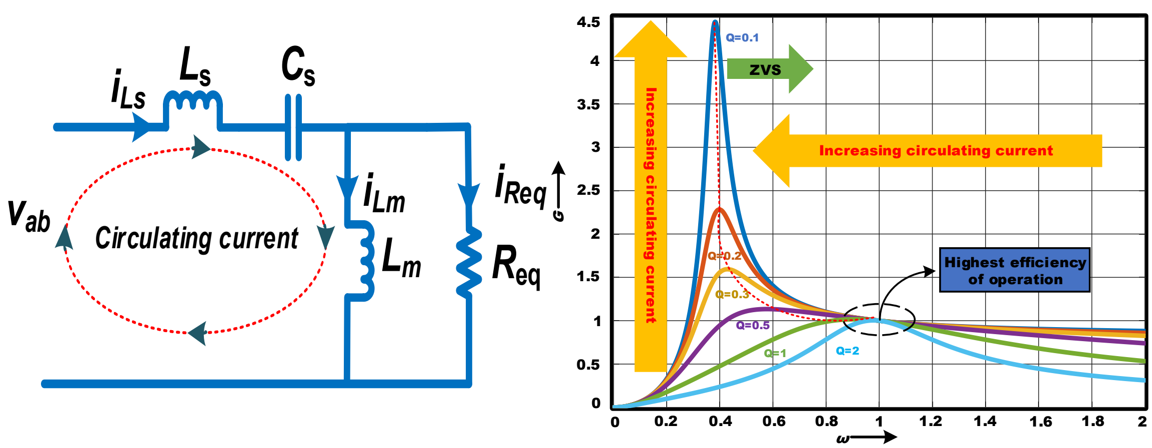
Figure 3-19: Measured efficiency curve for different input voltages

Figure 3-18. A peak efficiency of 97.5% was observed at nominal operating conditions. Hence, the proposed design and modulation strategy was successful in achieving optimized efficiency throughout the entire designed operating range.

Chapter 4

Design of Low-*Q* Full Bridge LLC Converter for Wide Input Applications

The time domain based mathematical analysis presented for evaluating resonant tank gain, currents and voltages for PO and NP modes was discussed in Chapter 2. The proposed hybrid modulation technique for realizing ZVS of primary side MOSFETs during operation at light load conditions was analyzed using a numerical technique-based time domain model in Chapter 3. Mathematical analysis done so far in this thesis will be used to obtain the design curves for LLC converter in the present chapter. This chapter also deals with the design methodology utilized to develop a low Q LLC converter for wide input solar PV applications. The ultimate objective is efficiency optimization from full load to extremely light load for the given input voltage range within a narrow switching frequency range.



(a) (b)

Figure 4-1: (a). Fundamental equivalent circuit of LLC converter; (b). DC voltage gain of LLC converter using FHA.

FHA based equivalent circuit of LLC converter and the resulting dc voltage gain curve is given in Figure 4-1. Choice of inductor ratio K is crucial in deciding whether the converter can operate at very light load conditions. If chosen value of K is too small, the magnetizing current relative to the primary side referred load current increases. This leads to a smaller switching frequency range and the converter starts showing characteristics like a PRC. However, since the magnetizing current represents the circulating current in the circuit, it generates high conduction losses in primary side MOSFETs and high frequency isolation transformer. If chosen value of K is too large, then the required peak gain cannot be achieved for a narrow switching frequency range. Low rated Q value leads to higher circulating current as well. Hence, K and rated Q should be chosen such that an optimal tradeoff between circulating current and switching frequency range is achieved.

Existing design methodologies impose peak gain design requirements and certain secondary constraints, such as light load operation [49], [57], [61], dead time duration [49], [50], [57] and switching frequency range [58] amongst many others. However, presuming these constraints in the initial design stage may exclude potential designs. For example, choosing a short dead-time might result in a lower magnetizing inductance, sacrificing efficiency. If the dead-time selected is large, the turn-off current might not be enough for the dead-time to be completed. Hence, an all-inclusive design approach is required which evaluates all possible designs with the aim of achieving full and part-load efficiency for the desired input voltage range.

The proposed approach is based on selecting designs which fulfills additional criterion of low Q and low current form factor, while achieving ZVS and required output voltage gain. An intuitive relationship between the current form factor and efficiency was derived in [87] which can be described as:

$$\eta^{-1} = 1 + \frac{R_{loss}}{R_l}\rho_i^2 \tag{4.1}$$

where η is the power efficiency, R_{loss} is the ohmic loss of converter, R_l is load resistance and ρ_i is current form factor ($\rho_i = I_{rms}/I_o$).

4.1 Proposed Design Methodology

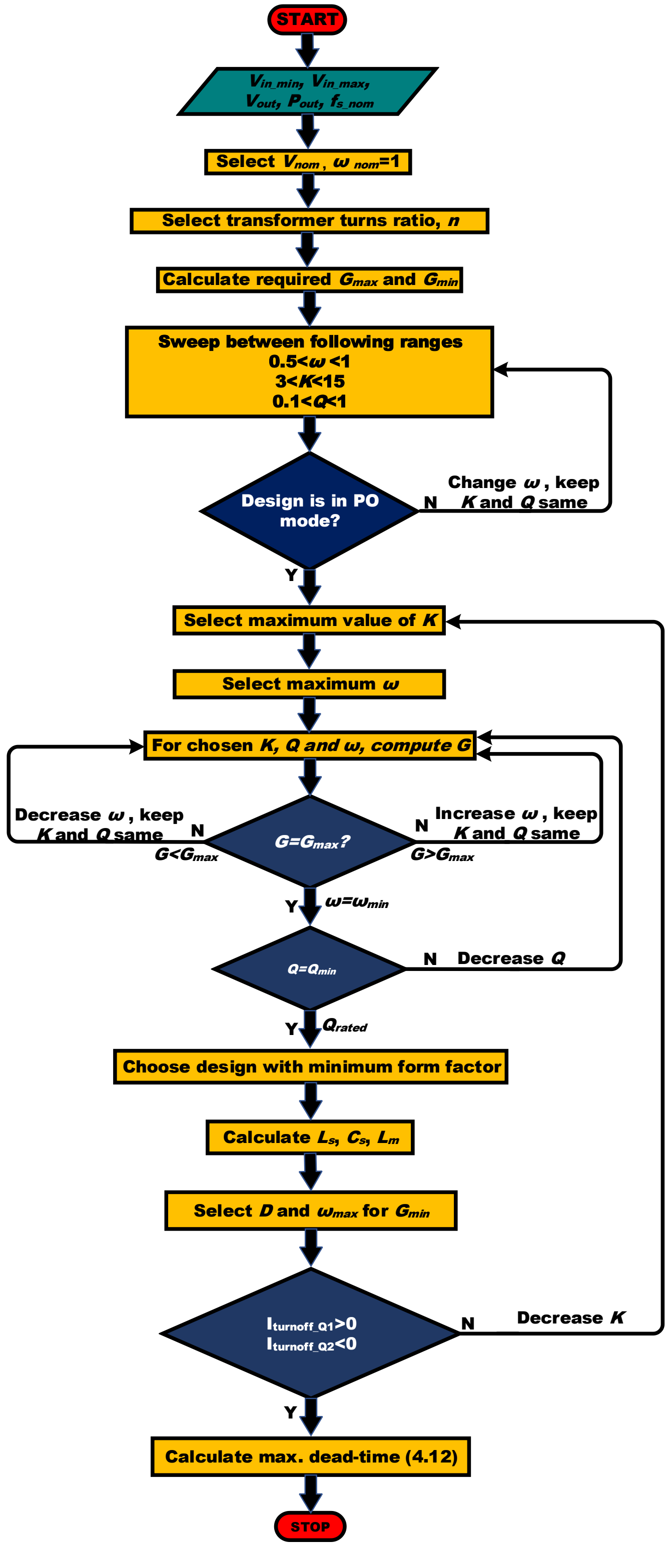


Figure 4-2: Proposed LLC Converter design flowchart

4.2 Design Example

Figure 4-2 illustrates the design process of low Q LLC resonant converter in the form of a flowchart. The design stresses on achieving high efficiencies at rated load and light load conditions without compromising on the voltage regulation capability. The design flowchart is implemented by a design example of an experimental converter having the following specifications.

1) Input Voltage Range:20V-40V (V_{in_nom}=30V)
2) Output Voltage (V_{out}): 380V
3) Output Power (P_{out}):300W
4) Switching Frequency (f_{sw})=150kHz

In order to generalize the design, the normalized circuit variables are defined as:

$$P_{base} = P_{out} \tag{4.2}$$

$$I_{base} = \frac{P_{base}}{V_{in\_nom}} \tag{4.3}$$

$$\omega_{base} = \omega_r \tag{4.4}$$

the normalized switching frequency can be defined as:

$$\omega = \frac{\omega_s}{\omega_{base}} \tag{4.5}$$

4.2.1 Procedure

For ease of understanding, the design procedure has been divided into two sub-sections, each one of which deals with analysis conducted in Chapter 2 and Chapter 3, respectively. The converter should be designed for the worst-case operating conditions, i.e., minimum input voltage at rated load and maximum input voltage at light load. Hence, the LLC resonant tank design chosen at the end of sub-section 4.2.1 keeping the minimum input voltage and rated load operating condition in mind is further investigated for performance under proposed modulation technique at maximum input voltage and light load conditions in sub-section 4.2.2. Sufficient ZVS margin at these worst-case operating conditions would guarantee optimized efficiency for the entire line/load range.

4.2.1.1 Design Inspection under Minimum Input Voltage and Rated Load Conditions below Resonance (ω<1)

1. For maximum efficiency at nominal conditions, operation at resonant frequency is preferred. Hence, the nominal switching frequency is set equal to the designed resonant frequency. Therefore, the proposed designed has ω_{nom}=1.

2. Calculate required transformer turns ratio, n. At switching frequency, ω=1, voltage gain of LLC converter is equal to 1. Turns ratio of the transformer is given by the relationship of nominal input voltage and output voltage as:

$$n = \frac{N_p}{N_s} = \frac{V_{in\_nom}}{V_{out}} = \frac{30}{380} = 1:12.67 \tag{4.6}$$

   Turns ratio, n was approximated to 1:14 to account for turns loss during transformer winding and forward voltage drop of output rectifier diodes.

3. Calculate maximum and minimum required output gain, G_{max} and G_{min} respectively.

$$G_{max} = \frac{nV_{out}}{V_{in\_min}} = 1.35 \tag{4.7}$$

$$G_{min} = \frac{nV_{out}}{V_{in\_max}} = 0.67 \tag{4.8}$$

   G_{max} was set equal to 1.4 to provide some margin due to loss of transformer turns ratio.

4. Start design process to find inductor ratio K, rated quality factor, Q_{rated} and ω_{min} such that the resultant output voltage gain is equal to required G_{max} in (4.7) while converter is operating in PO mode. Based on practical design experience and gain curves obtained using simulation tools, the following ranges were chosen for K, Q and ω_{min}

$$0.5 < \omega < 1$$
$$3 < K < 15 \tag{4.9}$$
$$0.1 < Q < 1$$

5. From selected values of K, plot voltage gain ratio for different Q values at selected ω, for which ensures that converter operates in PO mode.

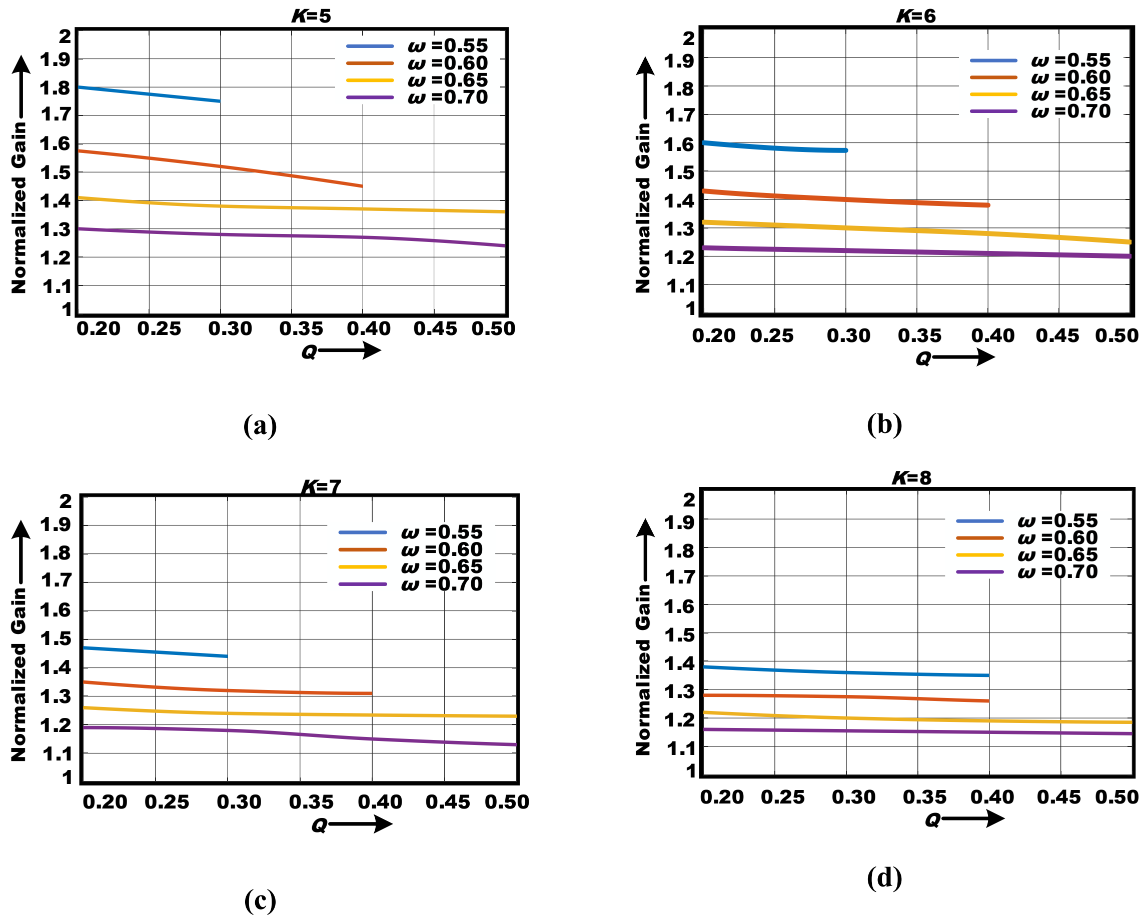


Figure 4-3: Design curve for normalized output voltage gain versus quality factor for inductor ratio, (a). *K*=5, (b). *K*=6, (c). *K*=7, (d). *K*=8

6. For same values of K, Q and ω, plot variation in form factor.

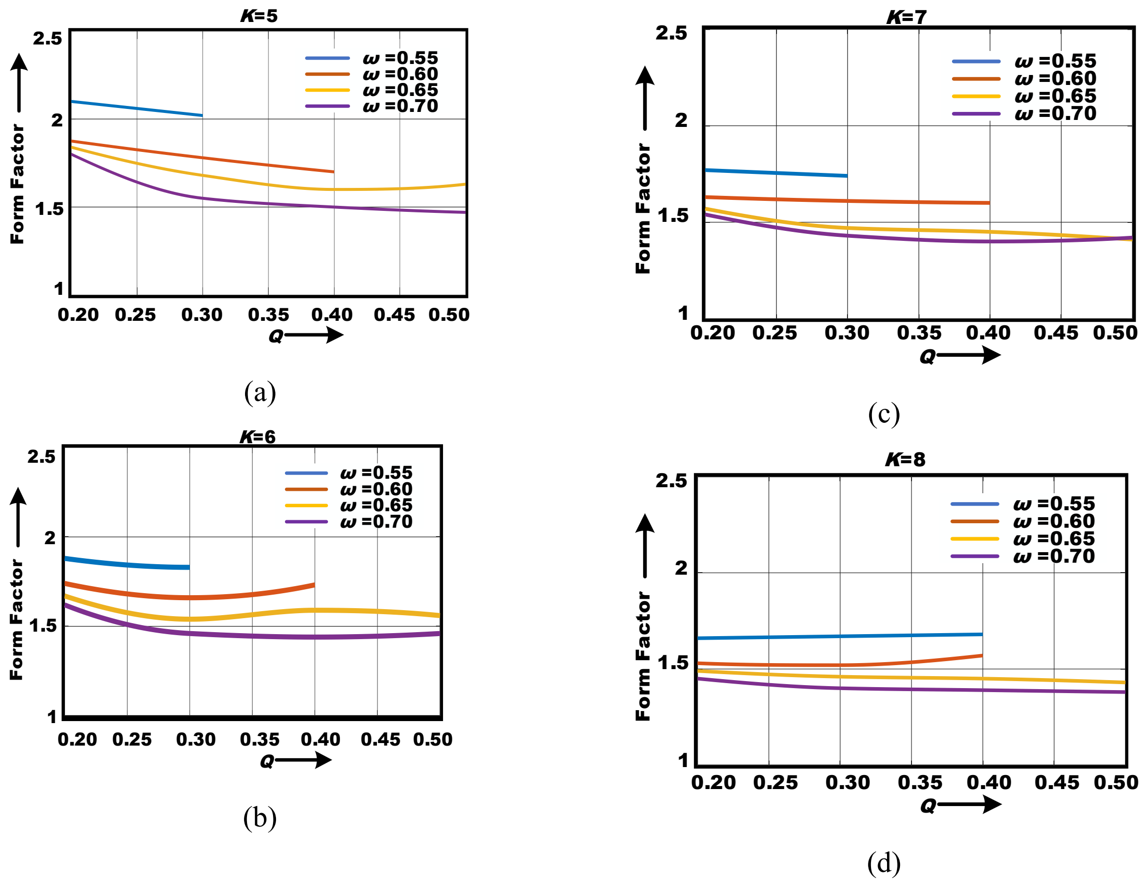


Figure 4-4: Design curve for resonant current form factor versus quality factor for inductor ratio, (a). *K*=5, (b). *K*=6, (c). *K*=7, (d). *K*=8

4.2.1.1.1 Selection of *K* and *Q* for Wide Input Range

Based on the analysis showed above, Q_{rated} was chosen equal to 0.34, ω_{min}=0.6 and inductor ratio, $K=6$. Final design values of L_s and C_s are solved by the following two equations:

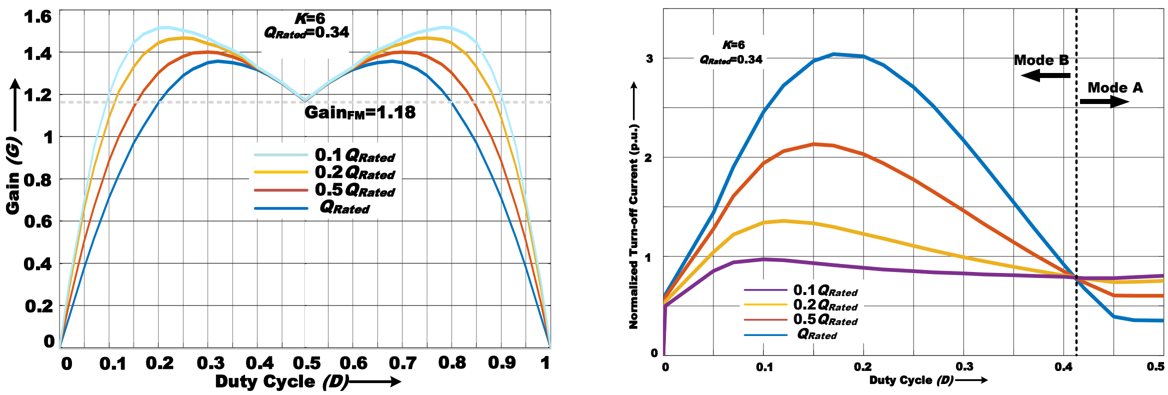
$$\sqrt{\frac{L_s}{C_s}} = Q_{rated} \times R_l \\ = 0.34 \times 550\Omega \tag{4.10}$$

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{4.11}$$

Solving (4.10) and (4.11), we obtain L_s=1µH and C_s=1.1µF. Since K (L_m/L_s) is chosen equal to 6, L_m is set equal to 6µH.

4.2.1.1.2 Narrow Switching Frequency Variation using APWM below resonant frequency

The switching frequency variation below resonant frequency can be further reduced by using APWM. ω_{min}=0.6 is required for variable frequency control. However, using APWM, ω_{min} can be chosen as 0.75. Normalized voltage gain and turn-off current under APWM is shown in Figure. 4-5. It is evident that once ω=0.75, duty cycle can be varied to get additional gain at the same frequency. However, the non-monotonous nature of gain curve requires means that a simple linear PI controller cannot be implemented for closed-loop control of converter. Mode boundary based



(a) (b)

Figure 4-5: APWM design curves of (a). Voltage gain and (b). Q_1, Q_3 Normalized turn-off current at fixed switching frequency ω=0.75.

on variation of duty cycle at selected K and Q value for different switching frequencies is shown in Figure 4-6.

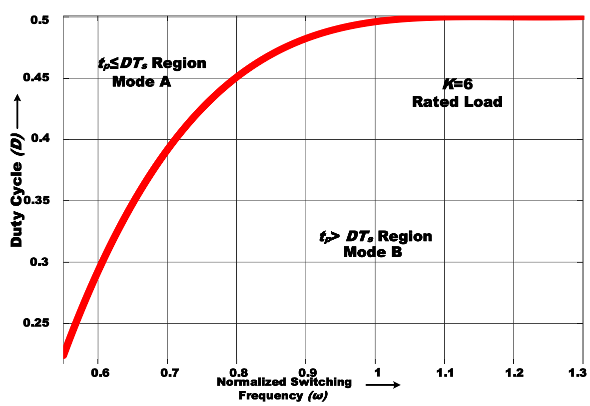
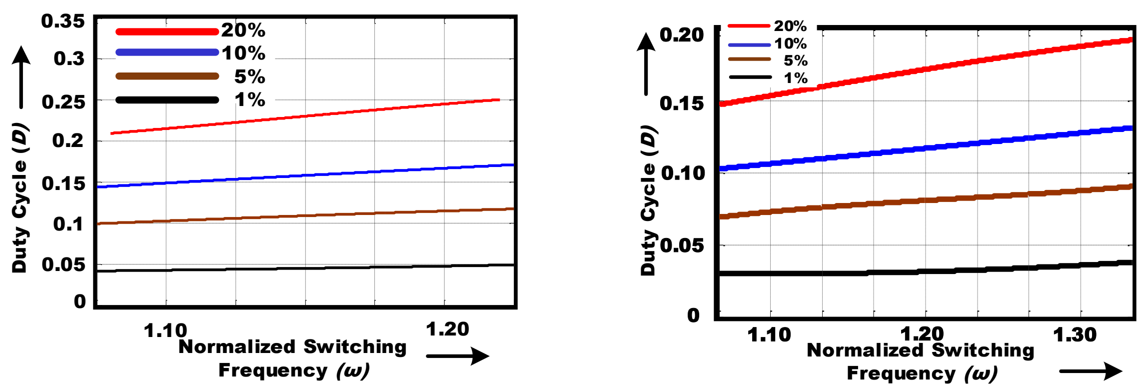


Figure 4-6: Time-domain boundary for mode operation at V_{in_min}=20V

4.2.1.2 Design Inspection under Maximum Input Voltage and Light Load Conditions above Resonance (ω>1)

For the designed values of L_s, C_s and L_m chosen through the proposed design methodology in Section 4.2.1 to suffice ZVS requirements at minimum input voltage and rated load conditions, further analysis for inspecting the same design for ZVS performance at maximum input voltage and light load conditions is performed in this section. Hence, the following inspection will be conducted at input voltages higher than the nominal value for this design, i.e. at V_{in}=35V and V_{in_max}=40V.

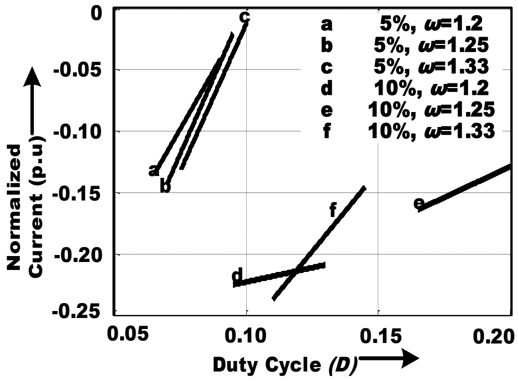
1. Based on analysis of the proposed light load modulation technique done in Chapter 3, the first step is to choose different combinations of $\omega=\omega_{max}$ and duty cycle at various light loading conditions which satisfy the gain requirement, G_{min} as defined in (4.8). A plot of duty cycle versus normalized switching frequency plot at V_{in}= 35V in Figure 4-7 (a) and V_{in_max}= 40V in Figure 4-7 (b) for a fixed output voltage of 380V.



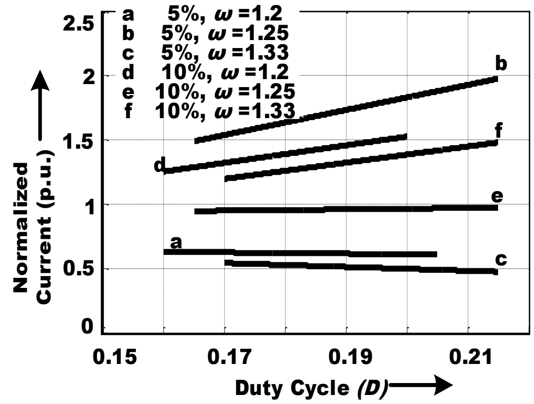
(a) (b)

Figure 4-7: Duty cycle vs normalized switching frequency curve for V_o=380V at light loading conditions at (a). V_{in}=35V and (b). V_{in_max}=40V

2. For selected duty cycle range of Q_1, plot the normalized turn-off current for MOSFET switches of leading leg of full bridge inverter i.e., Q_1 and Q_2 at different light loading



(a)

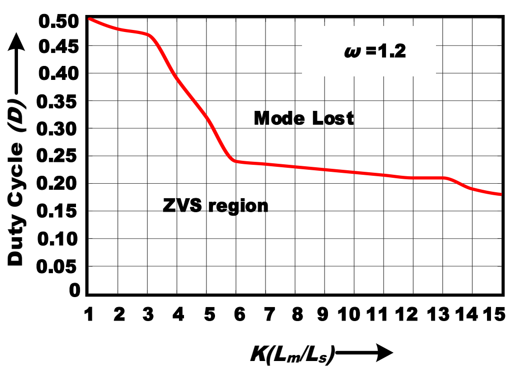


(b)

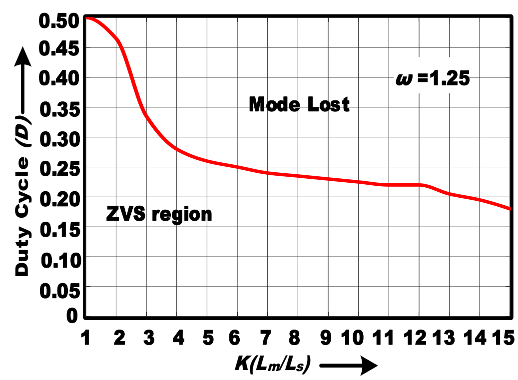
Figure 4-8: Normalized turn-off current for (a) switch Q_2 and (b) switch Q_1

conditions when operating at maximum input voltage, V_{in}=40V. Choose the switching frequency and duty cycle which corresponds to the minimum turn-off current of low-side switch Q_2, minimizing turn-off losses. At maximum input voltage and 10% load, D=0.12 and ω=1.2 were selected.

3. After selecting duty cycle and switching frequency for various light load conditions and input voltage, check whether the converter operates in the proposed mode.



(a)



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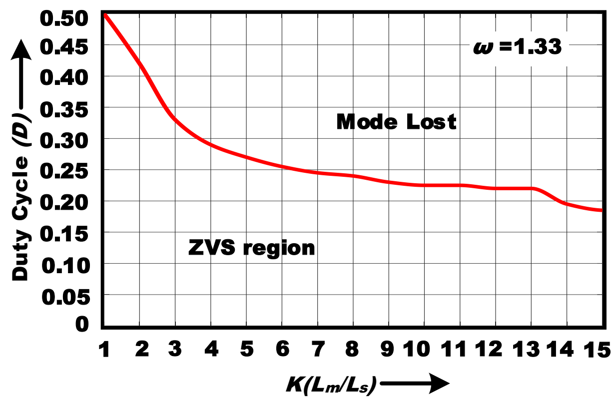


(c)

Figure 4-9: Boundary modes for ZVS operation at (a) ω=1.2, (b) ω=1.25, (c) ω=1.33

4) Calculate maximum required dead-time such that the resonant current is large enough to discharge the primary MOSFETs junction capacitance, C_{oss} and transformer distributed capacitance, C_d without changing direction. The minimum dead time required to discharge the capacitances is:

$$T_d \geq 4\,C_{oss}\frac{V_i}{I_{min}} + 2C_d\frac{nV_o}{I_{min}} \tag{4.12}$$

Figure 4-8 (a) shows normalized turn-off current for low-side switch Q_2 with respect to duty cycle, D of switch Q_1. A negative turn-off current for required duty cycle variation implies true ZVS for high side switch Q_1. Figure 4-8 (b) shows normalized turn-off current for high-side switch Q_1 with respect to duty cycle, D of switch Q_1. A positive turn-off current ensures that low-side MOSFET Q_2 achieves ZVS. Since, the lagging leg is soft switched, the proposed method achieves ZVS for all four switches for an input range of 2:1 for loading conditions as low as 5%.

4.3 Resonant Capacitor Bank Design

Film capacitors are preferred for resonant capacitor bank design as they possess high pulse strength and demonstrate stability with respect to temperature change which allows usage at large currents at high voltages. Since the proposed modulation scheme requires a dc blocking capacitor, with ability to withstand high ac voltages, it is necessary to select a capacitor based on AC voltage vs frequency curve given in Figure 4-10. Metallized polypropylene (MKP) film capacitor exhibit least capacitance variation by frequency upto 1 MHz. Dissipation factor variation over temperature, voltage and humidity is least affected for MKP type capacitors.

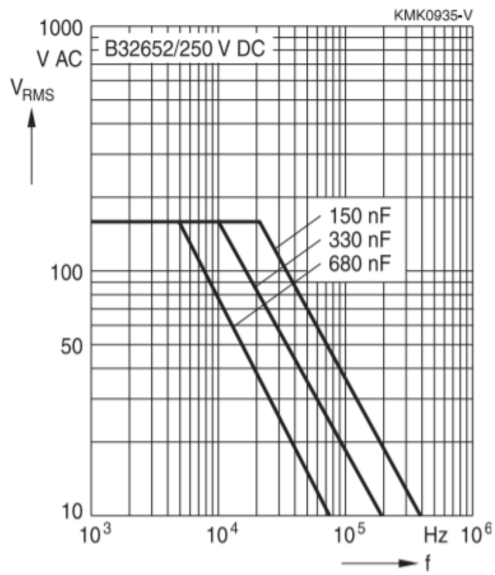


Figure 4-10: AC voltage vs frequency curve for film capacitor [89].

4.4 High Frequency LLC Transformer Design

As mentioned in Chapter 3, transformer core losses make up a significant part of the total losses at light loads. It can be expressed mathematically using the general Steinmetz equation as given below:

$$P_{core} = c\left(\Delta B\right)^{a} f_{sw}^{b} V_c \tag{4.13}$$

where *a, b, c* depends on the core material, ΔB is bipolar flux density, f_{sw} is switching frequency and V_c is volume of the transformer core. Improved Generalized Steinmetz equation (iGSE) can be utilized to give better prediction of magnetic core losses and parasitic elements incurred during operation of LLC converter. It can be expressed as:

$$P_{core} = \frac{V_c}{T_s}\int_0^{T_s} k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} \left(\Delta B\right)^{\beta-\alpha} dt \tag{4.14}$$

where, T_s is switching time period and k_i is integration constant which primarily depends on magnetic material of core. LLC resonant converter allows integration of magnetics during transformer design due to its resonant tank structure. Leakage inductance of designed transformer, L_{lkg} can be used as the resonant inductance, whereas the magnetizing current for soft switching can be provided by the magnetizing inductance of transformer due to air gap.

Hence, the primary objective is to select the smallest core shape with enough window area to satisfy the turns ratio required and provide the desired magnetizing inductance without transitioning the core into saturation.

4.4.1 Core Shape Selection

Primary consideration for transformer design includes determination of ferrite material, which depends upon operating frequency and temperature. As mentioned before, the nominal switching frequency is 150kHz. Since the present application for this transformer is PV microinverter, it must withstand temperatures as high as 90 C. Based on power loss density curves at varying temperatures [90], 3C95 core material was chosen for this design.

Selection of core shape and size for LLC converter depends primarily upon the LLC power circuit design. The transformer should provide the required magnetizing inductance, L_m and part or whole of resonant inductance, L_s. The magnetizing inductance can be related to the core shape as:

$$L_m = \frac{\mu_{eff} n^2}{C_1} \tag{4.15}$$

where C_1 represents the core factor which depends upon the core geometry and is defined as:

$$C_1 = \frac{L_e}{A_e} \tag{4.16}$$

L_e represents the effective magnetic loop length and A_e is the effective core area. Thus, for a selected core shape, desired magnetizing inductance can be achieved by introducing an air gap which changes the effective permeability of the transformer.

An easy thumb of rule in selecting core shape for high frequency transformer is to choose a geometry which offers lowest core factor and maximum window area for required number of winding turns. A low core factor ensures minimum energy loss for same flux density. Also, from (4.14), it is evident that a smaller air gap would be required for the same magnetizing inductance for a low core factor geometry. With the above required characteristics in mind, a low-profile version of RM-14 known as RM-14/ILP was chosen. Table 4-1 lists the characteristic material parameters.

Table 4-1: RM-14/ILP core parameters

Parameters	**Value**
Core Factor, C_1	0.25 mm^{-1}
Effective Volume, V_e	10230 mm^{-3}
Effective Area, A_e	201 mm^2
Effective Length, L_e	50.9 mm
Saturation flux density [B_{sat}]	530 mT

Litz wire is generally used to reduce proximity effect losses which are substantial at high operating frequencies. Litz wire is made up of number of strands of specific size twisted in a helical fashion such that each strand carries the same current. Number of strands depends upon the required RMS current carrying capability and the individual strand size depends on the frequency of the current flowing through each strand. Switching frequencies below 500kHz usually employ litz wire with individual strand size equal to #42. A # 44 strand gauge was chosen to allow for some design margin.

Due to unavailability of mathematically estimating leakage inductance for a given core shape and turns ratio, the leakage inductance must be measured using a power impedance analyzer. Leakage inductance was measured to be 0.21µH using Agilent 4294A Precision Impedance Analyzer.

Increasing transformer leakage inductance degrades power efficiency due to poor coupling of magnetic field between primary and secondary windings and causes ringing in the rising edge of square wave waveforms applied across the transformer. However, decreasing the leakage inductance in turn, increases the transformer's distributed capacitance, C_d which leads to different voltage gradients in the converter. Winding capacitance further increases with increase in number of winding turns which decreases inter-winding distances, leading to more storage of charge. Increase in C_d value will lead to higher dead-time for the initially designed magnetizing current or higher magnetizing current for the initially designed dead-time value as mentioned in (4.12), thereby affecting ZVS performance of the proposed modulation technique. Hence, it is necessary to design a transformer with as high a self-resonant frequency as possible. Figure 4-11 shows the self-resonant frequency of designed high-frequency isolation transformer core. It is equal to 1.18MHz. This would ensure that ringing caused due to transformer parasitic are kept to a minimum.

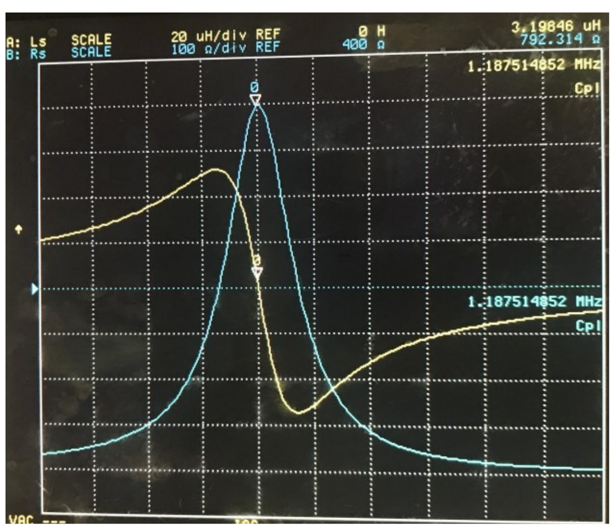


Figure 4-11: Self resonant frequency measurement of designed LLC transformer core

The final transformer parameters are given in Table 4-2.

Table 4-2: LLC transformer parameters

Parameter	Value
Core Shape	RM-14/ILP
Primary Wire	Litz #44/14
Secondary Wire	Litz 175*#46
Primary Winding Turns	3
Secondary Winding Turns	42
Leakage Inductance	0.21 μH
SRF	1.18 MHz

4.4.2 External Inductor Design

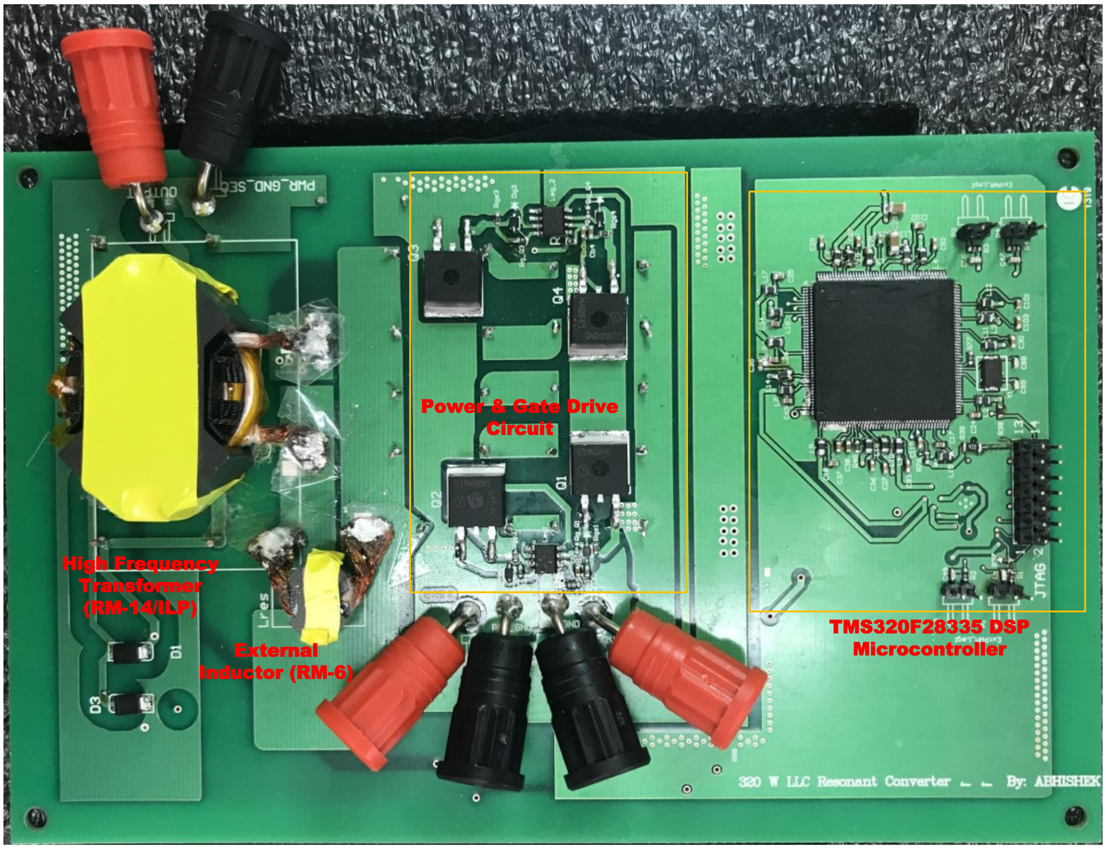
Since the leakage inductance obtained from the designed transformer isn't enough to fulfill the resonant inductance requirements, an external inductor is required. The core selected is RM-6, based on LI^2 vs nominal inductance (A_L) graphs given for different core shapes.

Table 4-3: LLC resonant inductor parameters

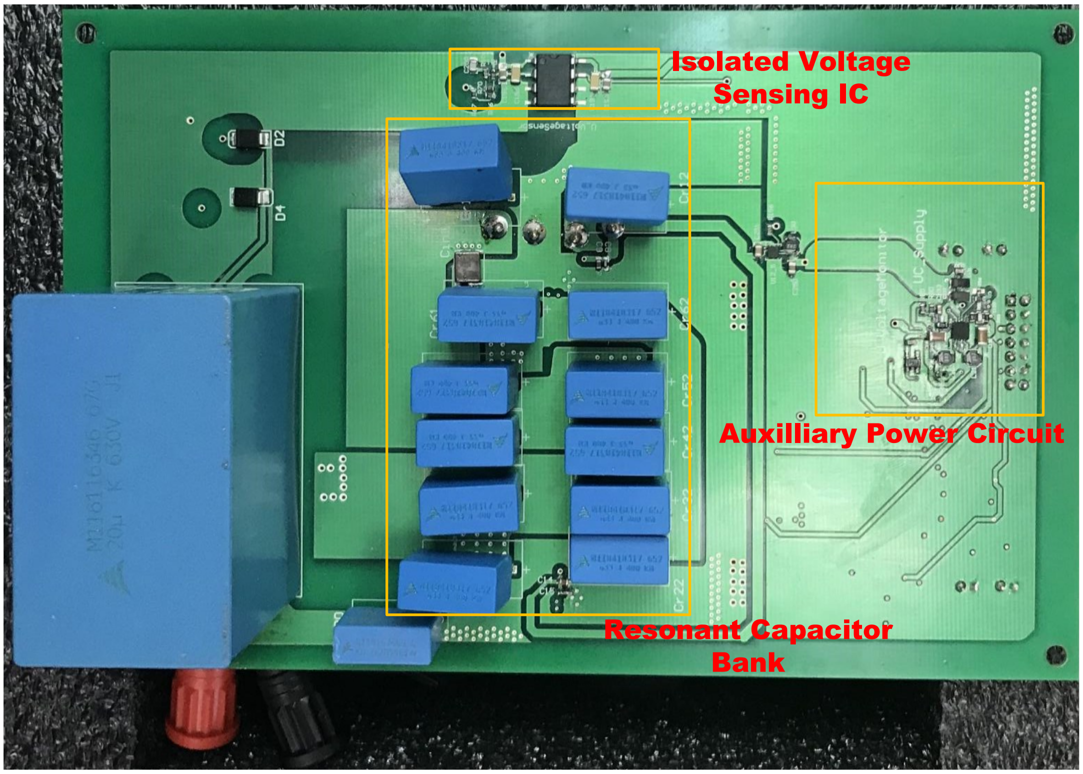
Parameter	Value
Core Shape	RM-6/I
Core Material	3C95
Wire Size	Litz #44/14
Inductance	0.89μH

4.5 Experimental Prototype

Based on the discussion above, an experimental prototype was developed as shown in Figure 4-12. PWM gating signals for various modulation techniques were generated using TMS320F28335 fixed-point DSP populated on the PCB.



(a)



(b)

Figure 4-12: Photo of developed LLC prototype (a). Top side and (b). Bottom side

Table 4-4 lists some of the major components used in experimental prototype.

Table 4-4: Component description of LLC converter prototype

Components	Part Description
Primary MOSFETs (Q_1-Q_4)	IPB031N08N5 (Infineon), 80V, 3.1mΩ, 82nC OptiMOS
Secondary Diodes (D_{o1}-D_{o4})	USB260HM3/52TGICT-ND (Vishay)
Primary Driver	UCC272712A-Q1 (TI) High and Low Side
Resonant Capacitor (C_s)	330 nF/ 400V (EPCOS B32652A4334)
Transformer Core	RM-14/ILP (3:42)
DC Bus Capacitor	20µF/ 630V (EPCOS-B32678G6206K)
DSP	TMS320F28335

4.6 Summary

This chapter provided a new design procedure for wide input low-Q LLC resonant converter. Performance characteristics of LLC resonant converter were discussed with emphasis on K and Q value of resonant tank. The proposed design methodology was summarized in a flowchart followed by elaborate discussion on a design example, typical of PV applications. Design curves were presented based on analysis performed in Chapter 2 and Chapter 3. LLC resonant tank was designed such that it minimizes circulating current flow. The design procedure stressed on optimizing efficiency throughout the whole operating range without sacrificing voltage regulation capability of converter. Selection criterion of high frequency resonant capacitor bank, isolation step-up transformer and external inductor was discussed in detail for development of experimental prototype.

Chapter 5

Conclusions and Future Work

5.1 Summary of Contributions

In this thesis, the primary focus was to propose a novel method of analysis, design and control of low-Q LLC dc-dc resonant converter for wide input range applications with a primary focus on improving light load efficiency. This section will list the major contributions of this thesis and highlight the improvements over existing work.

5.1.1 Adjustable Duty Cycle- Switching Frequency Hybrid Modulation Control

The first major contribution of this work is a new modulation method for wide input range LLC resonant converter that boasts many advantages while overcoming the limitations of existing conventional modulation strategies. The main contributions are:

- Time-domain analysis and solution of proposed strategy using Newton Raphson iterative method.
- True ZVS of all four-primary side MOSFETs from part load to extremely light load conditions.
- Stable voltage regulation at light loading conditions for low-Q LLC resonant circuit design.
- ZVS operation for narrower switching frequency range compared to conventional modulation techniques such as PSM and APWM, above resonant frequency for 2:1 input voltage range.
- Lower turn-off switching losses incurred compared to conventional modulation techniques.
- The advantages are achieved without sacrificing the natural benefits of full bridge LLC resonant converter topology, i.e.,
    - Primary MOSFET voltage stress is equal to the input voltage.
    - Rectifier diode voltage stress is equal to the output voltage.

    - For a different transformer design, the resonant inductor can be completely integrated with the transformer to achieve higher power density.

Measured efficiency of a 20-40V input, 380V/300W output LLC resonant converter improved by 6% and 8% at 10% and 5% loading condition compared to conventional PSM technique.

5.1.2 Time Domain Analysis and Design of Low-*Q* LLC Resonant Converter

The second contribution is the analysis of LLC resonant converter valid at any operating frequency and *Q* value is presented. The main contributions of this analysis method are:

- Unlike frequency domain methods, no restriction on range of designed *Q* values for which the analysis is applicable.
- Expressions for peak gain, current/ voltage stress, ZVS angle and RMS current were evaluated.
- The proposed method of analysis can be applied to any operational mode of LLC converter.
- The proposed method is valid for any possible 3 or 4 element resonant converter.

Using the proposed time domain analysis, performance characteristic curves were generated to select *K* and *Q* value of the resonant tank such that the primary current form factor is kept to a minimum value.

5.2 Conclusions

This thesis dealt with examining performance of a LLC resonant converter for wide input range applications. Time domain approach was used since the analysis based on frequency domain cannot predict peak gain and tank voltages/ current accurately for low values of *Q*. Various resonant stages were explained with their equivalent circuit and modeled using the proposed technique. Important modes of operation occurring under variable frequency control and asymmetrical duty cycle control were analyzed and resulting expressions of voltage gain, RMS current and ZVS angle were derived. A novel modulation technique which can adjust duty cycle and switching frequency simultaneously was proposed for improving light load performance of low-*Q* based LLC resonant converter. The proposed scheme modulated the input square wave by changing the duty cycle and switching frequency simultaneously of full bridge switching network such that the RMS value of input voltage waveform applied to the LLC tank is changed. This allows for reducing switching frequencies to achieve ZVS of all four primary MOSFETs at light load conditions while maintaining the output voltage constant. Time domain model was solved using Newton Raphson method for optimal selection of duty cycle and switching frequency based on calculated voltage gain and minimum turn-off current which can achieve ZVS of the leading leg for selected LLC design. A design example of 20-40V input, 380V/300W output LLC resonant converter was demonstrated using design curves generated from the proposed design procedure. Optimal design values of L_s, C_s and L_m were chosen for a specified switching frequency range which would guarantee ZVS at worst case conditions of minimum input voltage, rated load and maximum input voltage and light load. Mode boundary conditions for ZVS operation were defined as a function of inductor ratio, K and duty cycle at specific switching frequencies. Since, optimized magnetic design ensures efficiency optimization at light load conditions, an easy and effective criterion for selecting high frequency isolation transformer and external resonant inductor was utilized.

Finally, steady-state analytical waveforms have been generated on MATLAB based on proposed analysis. An experimental prototype of 380V/300W LLC converter operating between input voltage 20-40V, typical of PV applications, has been developed for validating ZVS performance of proposed LLC converter design and modulation technique.

5.3 Future Work

The significant impact of transformer parasitics on ZVS performance of LLC converter was evident in this work. Inclusion of parasitics and dead-time and further analysis of their impact on ZVS performance for low-Q LLC resonant converter is required as the existing ZVS criterion depends on using static charge balance equations to calculate the dead time required for discharging MOSFET capacitances.

Novel methods of including inductor and transformer core geometry into the design considerations would have a positive impact on LLC design optimization process. Detailed loss analysis using ferrite loss models valid for custom waveforms would further help in optimal selection of duty cycle and switching frequency for the proposed modulation technique. Finite element analysis would lead to highly accurate results.

Design and operation of extremely low-Q micro-inverters (Q_{rated}<0.1) for MOSFET switching frequencies above 500kHz and its cost/performance comparison with wide-bandgap devices such as GaN is another possible future area of research. Mitigating EMI issues at high switching frequencies through optimized PCB layout and component selection would be a challenge for future research work.

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Appendix A
Variable definition for APWM

Following variables occurred in expressions derived for ZVS angle and voltage gain in Section II which are valid for Mode A operation

$$\alpha_1 = \frac{\left[sin(x)cos(y+z) - 2\,sin(y)cos(y)\right]}{Z_0} + \frac{\left[cos(x)sin(y+z) - 2\,cos(x)sin(y) - 2\,sin(z)\right]}{Z_1} \tag{A.1}$$

$$\beta_1 = \frac{sin(x)}{Z_0}\left[cos(y+z) - 1\right] + \frac{sin(y+z)}{Z_1}\left[cos(x) - 1\right] \tag{A.2}$$

$$\alpha_2 = \frac{sin(x)\left[Z_1^2\,sin(y+z) + 2Z_0^2\,sin(y)\right]}{Z_1 Z_0} - cos(x)\left[cos(y) + cos(y+z)\right] + 2\,cos(z) + 1 \tag{A.3}$$

$$\beta_2 = \frac{Z_1}{Z_0} sin(x)sin(y+z) + \left[1 + cos(y+z)\right]\left[1 - cos(x)\right] \tag{A.4}$$

$$L = 2 + \frac{\left[Z_0^2 - Z_1^2\right] sin(x)sin(y+z)}{Z_1 Z_0} \tag{A.5}$$

where,

$$x = \frac{\omega_r}{\omega_{sw}} 2\pi t_p\ ;\ y = \frac{\omega_{r1}}{\omega_{sw}} 2\pi(D - t_1)\ ;\ z = \frac{\omega_{r1}}{\omega_{sw}} 2\pi(1 - D) \tag{A.6}$$

Following variable definition is valid for Mode B:

$$\alpha_1 = \frac{2\left[sin(x)cos(y) - sin(x-z)cos(y) - sin(z)\right]}{Z_0} + \frac{2\left[cos(x)sin(y) - cos(x-z)sin(y)\right]}{Z_1} \tag{A.7}$$

$$\beta_1 = \frac{sin(x)\left[cos(y) - 1\right]}{Z_0} + \frac{sin(y)\left[cos(x) - 1\right]}{Z_1} \tag{A.8}$$

$$\alpha_2 = sin(x)sin(y)\left[\frac{Z_1^2 - Z_0^2}{Z_1 Z_0}\right] + cos(y)\left[2\,cos(x-z) - cos(x)\right] \tag{A.9}$$

$$\beta_2 = \frac{Z_1}{Z_0} sin(x)sin(y) + \left[1 + cos(y)\right]\left[1 - cos(x)\right] \tag{A.10}$$

$$L = 2\left[1 - cos(x)cos(y)\right] + sin(x)sin(y)\left[\frac{Z_1^2 + Z_0^2}{Z_1 Z_0}\right] \tag{A.11}$$

where,

$$x = \frac{\omega_r}{\omega_{sw}} 2\pi t_p \ ; y = \frac{\omega_{r_l}}{\omega_{sw}} 2\pi(1 - t_p) \ ; z = \frac{\omega_{r_l}}{\omega_{sw}} 2\pi D \tag{A.12}$$

Appendix B
Variable definition for proposed light load modulation technique

Constant Output Voltage, Variable Output Power

$$\alpha_1 = \left[\frac{V_i \sin(\omega_r t_2)}{\omega_r L_s} + \frac{V_o / nL_m}{(1-\cos(\omega_r(t_1+t_2)))}(t_1+t_2) \right][1-\cos(\omega_r(t_1+t_2))*\cos(\omega_{r1}(T_s-t_1-t_2))$$
$$+\left(\frac{\omega_1}{\omega}\right)\sin(\omega_r(t_1+t_2))*\sin(\omega_{r1}(T_s-t_1-t_2))+\frac{V_o\omega_{r1}C_s\sin(\omega_{r1}(T_s-t_1-t_2)}{n} \tag{B.1}$$
$$-V_i[\frac{\sin(\omega_r t_2)\cos(\omega_{r1}(T_s-t_1-t_2))}{\omega_r L_s}+\omega_{r1}C_s[\cos(\omega t_2)\sin(\omega_{r1}(T_s-t_1-t_2))+\sin(\omega_{r1}(t_4+t_5))-\sin(\omega_{r1}t_5)]$$

$$\alpha_{21} = V_i\left[1+\cos(\omega_{r1}t_5))-\cos(\omega_{r1}(t_4+t_5))-\cos(\omega_r t_2)\cos(\omega_{r1}(T_s-t_1-t_2))+\left(\frac{\omega_r}{\omega_{r1}}\right)\sin(\omega_r t_2)\sin(\omega_{r1}(T_s-t_1-t_2))\right] \tag{B.2}$$

$$\alpha_{22} = [V_i\sin(\omega_r t_2)/(1-\cos(\omega_r(t_1+t_2)))]$$
$$*\left(\sin(\omega_r(t_1+t_2))*\cos(\omega_{r1}(T_s-t_1-t_2))+(\omega_r/\omega_{r1})*\cos(\omega_r(t_1+t_2))*\sin(\omega_{r1}(T_s-t_1-t_2))\right) \tag{B.3}$$

$$\alpha_{23} = -\left[\left(\frac{V_o}{n}\right)\left(1-\cos(\omega_{r1}(T_s-t_1-t_2))\right)\right]-\left[V_o\omega_r L_s*(t_1+t_2)/(nL_m(1-\cos(\omega_r(t_1+t_2))))\right]$$
$$*\left[\sin(\omega_r(t_1+t_2))*\cos(\omega_{r1}(T_s-t_1-t_2))+\left(\frac{\omega_r}{\omega_{r1}}\right)*\cos(\omega_r(t_1+t_2))*\sin(\omega_{r1}(T_s-t_1-t_2))\right] \tag{B.4}$$

$$\alpha_2 = \alpha_{21}+\alpha_{22}+\alpha_{23} \tag{B.5}$$

$$\beta_1 = \left(\frac{1}{\omega_r L_s}\right)\left[\left(\frac{\omega_{r1}}{\omega_r}\right)\sin(\omega_{r1}(T_s-t_1-t_2))(1-\cos(\omega_r(t_1+t_2)))+\sin(\omega_r(t_1+t_2))*(1-\cos(\omega_{r1}(T_s-t_1-t_2)))\right] \tag{B.6}$$

$$\beta_2 = (1-\cos(\omega_r(t_1+t_2)))*(1+\cos(\omega_{r1}(T_s-t_1-t_2)))+\left(\frac{\omega_r}{\omega_{r1}}\right)\sin(\omega_r(t_1+t_2))\sin(\omega_{r1}(T_s-t_1-t_2)) \tag{B.7}$$

Constant Output Power, Variable Output Voltage

$$\alpha_{1\_V_{in}} = \frac{V_{in}\sin(\omega_r t_2)}{\omega_r L_s\left(1-\cos\left[\omega_r(t_1+t_2)\right]\right)}\left[\begin{array}{l}\left[1-\cos\left[\omega_{r1}(T_s-t_1-t_2)\right]+\frac{\omega_{r1}}{\omega_r}\sin\left[\omega_r(t_1+t_2)\right]\sin\left[\omega_{r1}(T_s-t_1-t_2)\right]\right]\\ -\left[V_{in}\omega_{r1}C_s\left[\cos(\omega_r t_2)\sin\left[\omega_{r1}(T_s-t_1-t_2)\right]+\sin\left[\omega_{r1}(t_4+t_5)\right]-\sin\left(\omega_{r1}t_5\right)\right]\right]\end{array}\right] \tag{B.8}$$

$$\alpha_{1\_V_o} = \frac{t_1+t_2}{nL_m\left(1-cos\left[\omega_r\left(t_1+t_2\right)\right]\right)}\begin{bmatrix} 1-cos\left[\omega_r\left(t_1+t_2\right)\right]cos\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right]+\dfrac{\omega_{r_1}}{\omega_r}sin\left[\omega_r\left(t_1+t_2\right)\right]sin\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right] \\ +\dfrac{\omega_{r_1}C_sL_m}{t_1+t_2}sin\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right]\left[1-cos\left[\omega_r\left(t_1+t_2\right)\right]\right] \end{bmatrix} \quad \text{(B.9)}$$

$$\alpha_{2\_V_{in}} = V_{in}\begin{bmatrix} \left(1+cos\left(\omega_{r_1}t_5\right)\right)-cos\left(\omega_{r_1}\left(t_4+t_5\right)\right)-cos\left(\omega_r t_2\right)cos\left(\omega_{r_1}\left(T_s-t_1-t_2\right)\right)+\dfrac{\omega_r}{\omega_{r_1}}sin\left(\omega_r t_2\right)sin\left(\omega_{r_1}\left(T_s-t_1-t_2\right)\right) \\ +\dfrac{V_{in}\,sin\left(\omega_r t_2\right)}{\left(1-cos\left(\omega_r\left(t_1+t_2\right)\right)\right)}sin\left(\omega_r\left(t_1+t_2\right)\right)cos\left(\omega_{r_1}\left(T_s-t_1-t_2\right)\right)+\dfrac{\omega_r}{\omega_{r_1}}cos\left(\omega_r\left(t_1+t_2\right)\right)sin\left(\omega_{r_1}\left(T_s-t_1-t_2\right)\right) \end{bmatrix} \quad \text{(B.10)}$$

$$\alpha_{2\_V_o} = \left[\frac{1-cos\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right]}{n}-\frac{\omega_r L_s\left(t_1+t_2\right)}{nL_m\left[1-cos\left(\omega_r\left(t_1+t_2\right)\right)\right]}\begin{bmatrix} sin\left[\omega_r\left(t_1+t_2\right)\right]cos\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right] \\ +\dfrac{\omega_r}{\omega_{r_1}}cos\left[\omega_r\left(t_1+t_2\right)\right]sin\left[\omega_{r_1}\left(T_s-t_1-t_2\right)\right] \end{bmatrix}\right] \quad \text{(B.11)}$$